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Volatile Memristor in Leaky Integrate-and-Fire Neurons: Circuit Simulation and Experimental Study

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Abstract: In this paper, circuit implementation of a leaky integrate-and-fire neuron model with a volatile memristor was proposed and simulated in the SPICE simulation environment. We demonstrate that simple leaky integrate-and-fire (LIF) neuron models composed of: volatile memristor, membrane capacitance and neuron resistance can mimic spatial and temporal integration, firing function and signal decay. The existing leaky term originates from the recovery of the initial resistive state in the memristor in the spontaneous reset cycle, which is essential for emulating the forgetting process in all-memristive neural networks (MNNs). Furthermore, a diffusive perovskite memristor was used to validate the model where intrinsic memristors' capacitance acts as neuron membrane capacitance. Good agreement with experimental and simulation results was observed. Volatility, as an inherent property of specific memristors, eliminates the need for usage of an additional peripheral circuit which will reinitialize device state, thus allowing the development of energy-efficient, large scale complex memristive neural networks. The presented circuit level model of LIF neurons can facilitate the design of MNNs.

Keywords: memristor; volatility; leaky integrate-and-fire; SPICE model

1. Introduction

The application of memristors as part of artificial neural networks (ANN), especially spiking neural networks (SNN) has been extensively studied in recent years [1–4] due to their unique performances such as: adjustable conductance, multilevel resistance states, fast operation speed, low dissipation, and prominent scaling potential [2,5]. Memristive synapse, for instance, allows implementation of Spike Time Dependent Plasticity (STDP) learning rule [6] as a result of existing ability to memorize state and process information. Furthermore, memristors can be implemented in neural networks in the form of various memristive synapse circuits: single memristor (1M), two memristors (2M), one memristor-one transistor (1M-1T), four memristor synapse circuit (4M), etc. [1,2]. Nowadays, various memristive neuron models are available in the literature: Hodgkin–Huxley [7], FitzHugh–Nagumo [8], Hindmarsh–Rose [9], integrate-and-fire model [6], and leaky integrate-and-fire model [10]. Although the well-known Hodgkin–Huxley model [11] presents the most accurate biologically plausible neuron model, the memristive interpretation of this model requires the existence of rare local-activity behaviour reported only in a few physically realized devices [12,13].

On the other hand, the leaky integrate-and-fire model (LIF), is the most commonly used neuron model in spiking neural networks, [4,14], due to its simple realization, with the ability to perform the following essential neuron functionalities: signal integration, firing function and decay of local gradient potential (LGP). Memristive LIF neurons may require additional peripheral circuits: Schmitt trigger-based amplifier-STBA [15], comparator, and pulse generator [16] depending on the properties of memristor itself, which should discharge the capacitor, the element that mimics neural membrane capacitance, and reset the memristor state.

Recently, an all-memristive neural network was presented with a simple memristive LIF neuron circuit and additional membrane capacitance and axon resistance, where leaky functionality was realized using volatility in diffusive memristor, while drift memristor was used in a synaptic circuit composed of one memristor and one transistor (1M-1T) [17].

Although the volatile characteristics of memristors' response were considered originally as unwanted, they have become more interesting recently due to the valuable feature, specifically useful in advanced neuromorphic architectures [17–19], selectors [20], in security applications as random generators [21], etc. Volatile memristors can be included either as part of a neuron cell circuit of a memristive neural network [17] or in combination with a non-volatile drift memristor for emulation of synaptic activity [18].

Aiming to standardize the characterization techniques, novel experimental protocols have been proposed recently [22], revealing some of the following effects: number of programming pulses, programming amplitude, polarity, overall input energy on resistive RAM (ReRAM) relaxation response. Available literature reports on the existence of both metastable-volatile and stable-non-volatile states within the same memristive device, dependent on the electrical potential gradient and device history [22,23].

Furthermore, a modelling methodology that accounts for bidirectional volatility was presented in [24], predicting a transient change of memristance through the data-driven analytical approach. In a recent study [25], physical models of the filamentary type of volatile resistive switching devices were presented accounting for Ag nanoparticles motion, which defines disruption and formation of the filament. This model is numerical and based on Monte Carlo simulations and molecular dynamics, whereas the same group of authors presented the analytical model [26], also for volatile memristors confirmed through measurement of ac characteristics and filament disruption dynamics. Application of this physical-based model as ReRAM synapse is demonstrated consisting of a single volatile and non-volatile memristor, mimicking short-term memory effect. Other physical models of volatile/diffusive memristors are also available and based on: electrical, mechanical, thermal effects and electrochemical reaction on filament dynamics [17,18].

Starting from the circuit-level SPICE model, which incorporates both non-volatile and volatile effects in memristor [23], in this paper we included our new window function [27,28] in the memristor's model. The memristor's model was then used in the SPICE simulation of a simple LIF artificial neuron circuit for all-memristive neural networks. Numerical results show that the model can mimic spatial-temporal integration, firing function and leaky functionality of a biological neuron. Results of conducted simulations were verified through carried out experiment on perovskite $Pt/BaTiO_3/Pt$ diffusive thin film memristor due to the fact that perovskite materials have already proven as good candidates for an active material in diffusive memristors [16]. For the realization of the LIF circuit, internal capacitance of memristor was used to mimic membrane capacitance in a biological neuron and shunt resistor was used as neuron resistance. A good agreement between numerical and experimental findings was observed. As far as our knowledge, this is the first circuit-based SPICE model of simple LIF neuron with volatile memristor which can be used in all-memristive neural networks. Validation of the proposed model was performed by comparison of simulated and experimental results obtained as a response of perovskite volatile memristor in the LIF neuron circuit. This circuit model of LIF neuron allows decoupling of memristive and capacitive influence of neuron response, without the usage of additional optimization tools, such as genetic algorithm [15], and can be potentially used for simulation of complex large memristive neural networks.

2. Materials and Methods

Simulations of volatile memristor and leaky integrate-and-fire artificial neuron circuits were performed in the SPICE simulating environment (LTspice version). $Pt/BaTiO_3/Pt$ (BTO) diffusive/volatile memristors were fabricated by spin-coating deposition technique of stable precursor solutions [29], on silicon substrate coated with platinum Pt(~150 nm)/ TiO_2(~40 nm)/SiO_2(500 nm) (Vin Karola Instruments, Norcross, GA, USA). Top Pt electrode

(~100 nm) was deposited by sputtering (LeyboldHeraeusL560Q) on BTO (~100 nm) film. The dynamical response of the LIF circuit was experimentally studied with a measurement setup consisting of NI USB 6351 data acquisition card (National instruments, Austin, TX, USA) and SDG1025 arbitrary waveform generator (Siglent Technologies). SDG1025 is used to supply predefined waveforms to the LIF circuit, while NI USB 6351 is used for the measurement of memristor current and voltage. Memristor current was calculated based on the voltage drop measured across the series resistor (resistor is utilized as a shunt or current sensing resistor). The LabVIEW virtual instrument is designed for simultaneous control of the waveform generator and data acquisition card. Timing characteristic and relaxation time were estimated using Keithley 2410 High-Voltage Source Meter (Tektronix) also controlled with LabVIEW, while frequency analysis of capacitance was performed using Hioki IM3590 impedance analysed (HiokiE.E. Corporation, Nagano, Japan) in frequency range from 1 Hz–100 Hz using the equivalent circuit of parallel connection between capacitor and resistor. Electrical measurements were performed at room temperature in laboratory conditions.

3. Simulation of LIF Neuron with Volatile Memristor

Starting from the reported SPICE model which can incorporate memristor volatility [23], we included our new window function

$$f_N(x) = \frac{1 - (2x - 1)^2}{1 - (2x - 1)^2 + (2x - 1)^{2N}},$$ (1)

where parameter N corresponds to parameter p of original Joglekar [30] and Prodromakis [31] window functions. The properties of novel window functions compared to other window functions most often used in literature are listed in Table 1.

Table 1. Comparison between different window functions.

Different Window Functions	Joglekar [30]	Prodromakis [31]	Biolek [32]	Kvatinsky [33]	Singh [34]	This Paper
Symmetric	Yes	Yes	Yes	Not necessarily	Yes	Yes
Resolve boundary conditions	No	Practically Yes	Yes	Practically Yes	Yes	Practically Yes
Accounts for non-linear effects	Partially	Partially	Partially	Yes	Partially	Partially
Scalability $0 \leq f_{max}$ (x) ≤ 1	No	Yes	No	No	Yes	Partially *
Fits memristive device model	L/N/TEAM	L/N/TEAM	L/N/TEAM	TEAM	L/N/TEAM	L/N/TEAM

Note: L—Linear ion drift, N—Non-linear ion drift, TEAM—Threshold adaptive memristor. * Easily extended to Yes using multiplicative constant.

In addition to the properties listed in Table 1, the novel window function $f_N(x)$ has the first $2N - 1$ consecutive derivatives equal to zero at $x = 1/2$. Since $f_N(1/2) = 1$ and $f_N(x) \leq 1$, it follows that $f_N(x)$ has flattened maximum at $x = 1/2$. The function $f_N(x)$ is shown in Figure 1a for $N = 1 \sim 10$. Based on the results from [27], the specific advantage of the proposed novel window function is the possibility to determine exact closed-form analytical solutions, expressing the dependence of the charge q (flux φ) on the state variable x, in the case of the used model of memristor:

$$q(x) = \frac{1}{4k} \left[\ln \frac{x}{1 - x} - 2 \sum_{n=1}^{N-1} \frac{(2x - 1)^{2n+1}}{2n + 1} \right],$$ (2)

$$\varphi(x) = \frac{1}{4k} \left[R_{off} \ln(2x) - R_{on} \ln(2 - 2x) + R_{off} \sum_{n=3}^{2N} \frac{(1 - 2x)^n}{n} - R_{on} \sum_{n=3}^{2N} \frac{(2x - 1)^n}{n} \right].$$ (3)
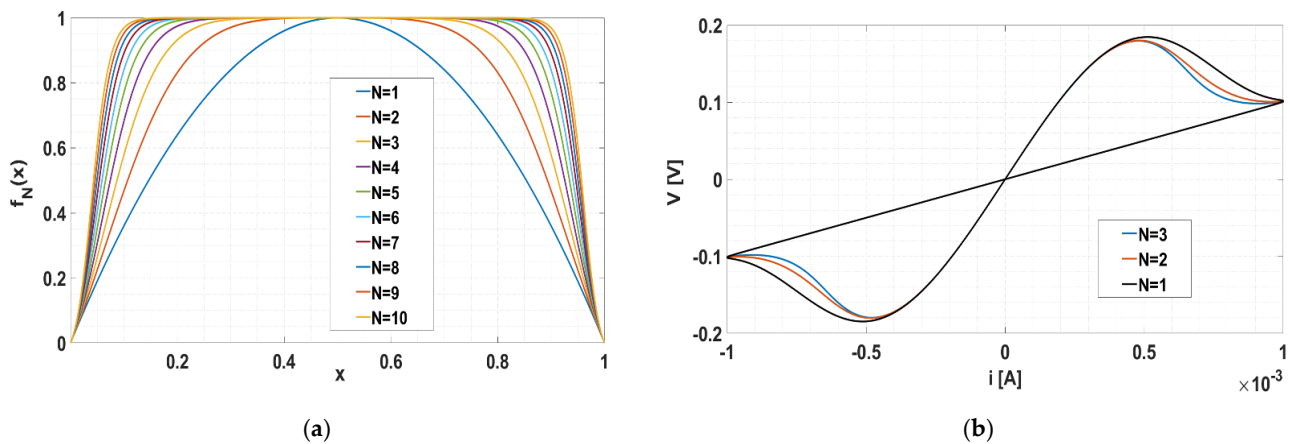
(a)

(b)

Figure 1. (**a**) Proposed novel window function in the used model of memristor; (**b**) Current–voltage characteristics of model with novel window function for N = 1, 2 and 3. Simulation parameters: $i(t) = Im\cos(\omega t)$, Im = 1 mA, $\omega = 2\pi$ rad/s, R_{OFF} = 1 kΩ, R_{ON} = 100 Ω, $k = 10^4$ C^{-1}.

In this way, when our model is used in numerical simulations, we do not have to numerically solve the state equation $dx/dt = kf(x)i$. Instead, for current-controlled (voltage-controlled) memristor, from $i(t)$ ($u(t)$) we obtain $q(t)$ ($\varphi(t)$), and for each value of the charge q (flux φ) we can numerically solve nonlinear algebraic equation $q(x)$ ($\varphi(x)$) by x, and substitute this x in the state-dependent Ohm's law of memristor $v_M(t) = R_M(x)i_M(t)$ ($i_M(t) = G_M(x)v_M(t)$). With respect to the monotonicity of the functions $q(x)$ and $\varphi(x)$, there exists only one solution $x \in (0, 1)$ in both cases. The influence of the window function on current–voltage characteristics is presented in Figure 1b.

The model of the volatile memristor is composed of four cells: terminal cell, x-module, y-module and z-module, which realize coupled differential equations [23]. Terminal cell of the model as originally proposed by Biolek [32], brings the well-known current–voltage relation of memristors:

$$v_M(t) = R_M(x)i_M(t), \tag{4}$$

where $v_M(t)$ and $i_M(t)$ represent memristor voltage and current, respectively. Resistance $R_M(x)$ depends on state variable x and values of High Resistance State, HRS, R_{OFF} and Low Resistance State R_{ON}:

$$R_M(x) = R_{ON}x + R_{OFF}(1 - x) \tag{5}$$

Additional module cells: x, y and z are composed of controlled current and voltage sources, used to implement coupling between differential equations, resistors and capacitors (R_x, C_x, C_y, R_z, C_z), which determine the rate of volatile and non-volatile switching, time constant and leaky function. For more details see [23]. It is important to note that parameters of module cell x, y and z as well as the cell circuit itself, do not have physical interpretation and are only used to implement corresponding differential equations [23,35]. In this paper, we modified the equation for the current of controlled sources using a new window function $f_N(x)$, therefore obtaining the following form for the x-cell controlled current source:

$$I_C(x) = \frac{i_M \mu_V R_{ON}}{D^2} \frac{1 - (2x - 1)^2}{1 - (2x - 1)^2 + (2x - 1)^{2N}}, \tag{6}$$

where μ_V stands for dopant mobility, and D represents the thickness of the active layer. The controlled current source in y-cell is obtained by analogy.

As recently demonstrated, volatile memristors are suitable candidates for realizing Leaky integrate-and-fire artificial neuron circuit [16,17], as besides integration they could implement the "leaky" function of biological neurons after the actuation signal (input stimulus) is turned off. Here, we incorporated the volatile memristor SPICE model of

a memristive artificial neuron, proposed in the recent paper presenting neurons in an all-memristive neural network [17]. The LIF neuron circuit, see Figure 2, is composed of neuron resistance R, neuron capacitance C and memristor M. Voltage source, V_S, as stimulus generator, generates input signals (pulses) on voltage divider circuit formed of a neuron resistance and parallelly connected memristor and capacitor. Memristor models the variable ion channel conductivity, while the capacitor is used to implement cell membrane capacitance [17]. For a large on-to-off resistance ratio of memristor, a capacitor is charged through input resistance R, and the capacitor voltage value is increased. Eventually, capacitor voltage reaches the memristors threshold voltage value, switching it to LRS (on-state), which presents the onset of a capacitor discharging through the memristor. Abrupt changes of memristance are detected as the "firing" event in the artificial neuron. After the pulse train voltage is turned off, the volatile memristor turns to HRS (off-state), which eliminates the need for additional reset circuits.
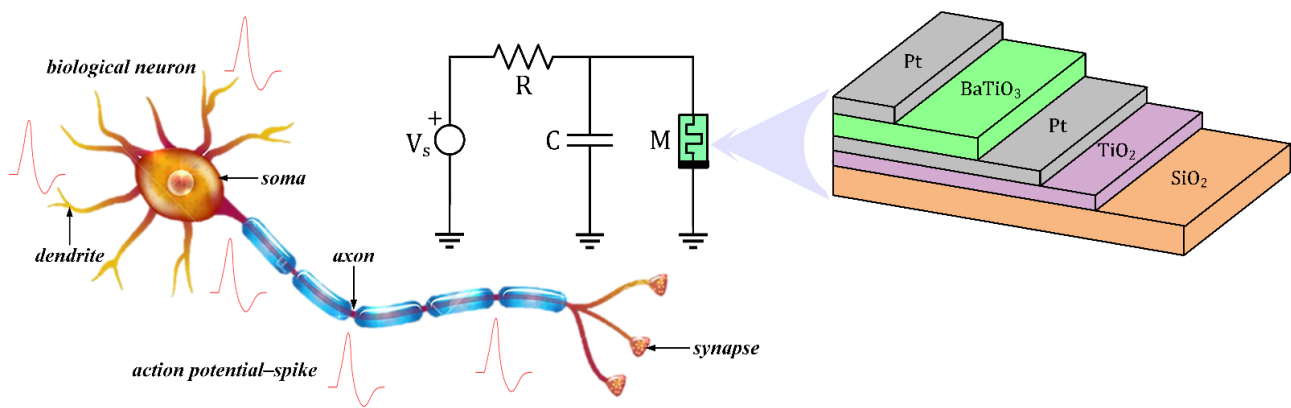

Figure 2. Memristive leaky integrate–and–fire artificial neuron and biological neuron counterpart.

Results of the SPICE simulations of LIF neuron with volatile memristor are given in Figure 3, parameters values were implemented from [23], while external components equal to: neuron resistance is $R = 10\ \Omega$k and membrane capacitance is initially set to $C = 50$ nF and later variated demonstrating their influence on neuron dynamics. SPICE code (LTspice version) used for simulation of the volatile memristor is included in Appendix A. Values of memristor's subcircuit model parameters are given in Table 2, while independent and controlled source values follow from the model's equation [23].

The neuron circuit is stimulated with multiple subsequent voltage pulses of the following characteristics: pulse duration 1 ms, pulse period 2 ms and amplitude 0.5·V (subthreshold value). Results, given in Figure 3 are shown for two pulse trains with five consecutive pulses and a resting period of 180 ms. Firing occurs at the $t_f \sim 5$ ms detected as memristor's current increase, Figure 3 (middle graph, Ix-memristor current in referent direction) and discharging of the capacitor (bottom graph), i.e., decay of voltage across parallel circuit formed from memristor and capacitor (v_M). This behaviour is classified as memristors' threshold switching initiated by the pulse input stimulus, where the required time to reach the threshold corresponds to integration time in neuron dynamics [17]. Resting period t_r between the pulses is chosen to demonstrate the volatility effect in the LIF neuron circuit. Namely, following the increase rate of memristance R_M after the switching, Figure 3 (top graph), turns back to the initial resistive state value during the resting period t_r, simulating decay of local graded potential (LGP), i.e., "leaky" or forgetting function in the biological neuron. This initial value of memristance is a biological counterpart to the resting state of LGP. Relaxation or decay time allows the implementation of STM in artificial neural networks [17]. Following, second pulse train in the simulations, starting from t_r, induces same effect: charging of membrane capacitance, and transition of memristor's state.
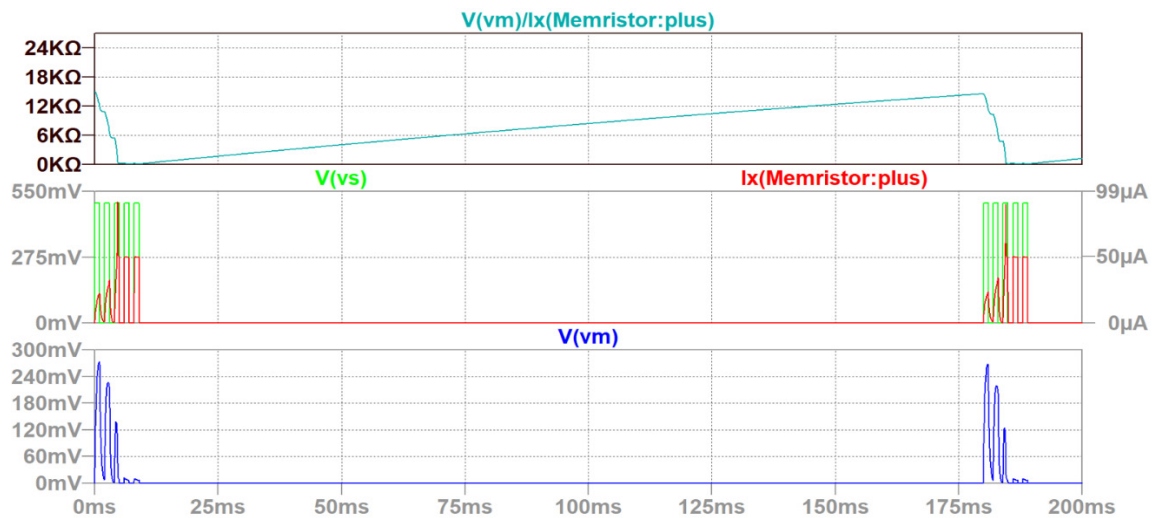
Figure 3. Simulated response of LIF circuit with volatile memristor on voltage pulse actuation: Memristance R_M (**upper graph**), memristor's current i_M (**middle graph**) and the voltage across memristor v_M (**bottom graph**).

Table 2. Memristor's subcircuit model parameters.

R_x	C_x	C_y	R_z	C_z
1 Ω	0.5 F	1 F	0.1 Ω	1 F

It is worth noticing that memristance transient response highly depends on input stimulus energy, device history, switching threshold values [22] and on-to-off ratio. Respectively, volatile phenomenon, yet not entirely revealed can be considered as spontaneous reset process and returning the device in an initial state.

It is known in the literature [16], that the spatial integration function of an artificial neuron can be validated as a circuit response under external stimulation with different amplitudes, presenting summed spatial stimulus signals. Namely, biological action potential has uniform amplitude, thus the sum of multiple input signals arriving at the same cell can be modelled with the alteration of signal amplitudes. LIF model of a neuron implemented in SPICE environment can also demonstrate spatial integration functionality, e.g., after increasing amplitude of pulse train input signals from 0.5 V to 1 V (see Figure 4a), a rise of spike current is observed, from ~90 μA (Figure 3) to ~320 μA (Figure 4a), respectively. For larger stimulus amplitude, firing event occurs faster as fewer pulses are required for memristor to reach the threshold value.

The temporal integration function of a biological neuron allows summation of signals with different frequencies, which will consequently generate a different spike response [16]. This process is also possible to emulate using the proposed LIF model in the SPICE environment, as higher values of input frequencies induce larger response current, i.e., increased stimulus frequency from 500 Hz to 2 kHz, see Figure 4b,c for comparison, induces 60% current response increase. This behaviour is recognized as temporal signal high pass filtering and originates from diffusion processes in volatile memristor, as dynamical modulation of memristance [16].
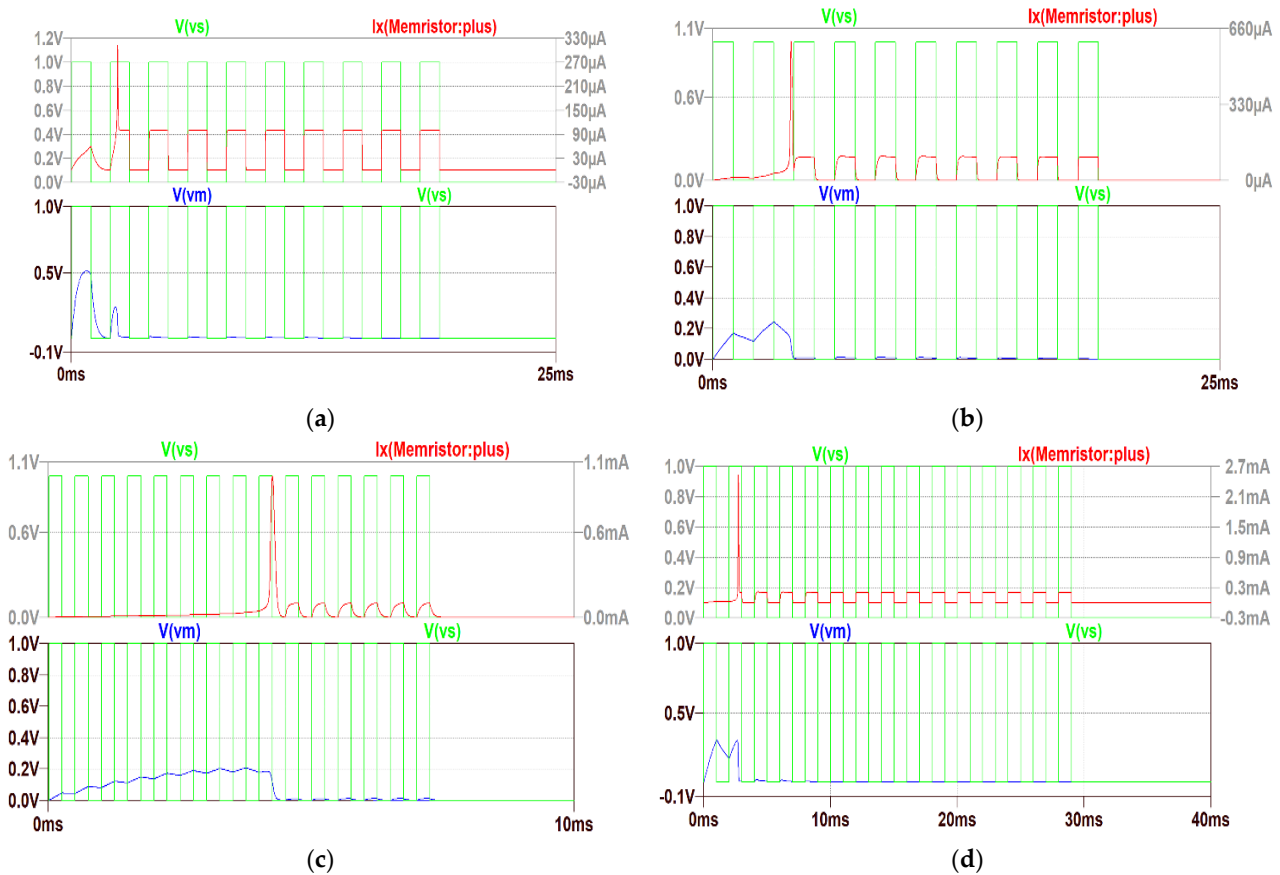
Figure 4. Simulation of firing dynamics of memristive LIF artificial neuron under different stimulus and variable membrane capacitance and neuron resistance. (**a**) $V_a = 1$ V, $T_{on} = 1$ ms, $T_p = 2$ ms, $C = 50$ nF, $R = 10$ kΩ, $I_{max} = 320$ μA; (**b**) $V_a = 1$ V, $T_{on} = 1$ ms, $T_p = 2$ ms, $C = 500$ nF, $R = 10$ kΩ, $I_{max} = 600$ μA; (**c**) $V_a = 1$ V, $T_{on} = 0.25$ ms, $T_p = 0.5$ ms, $C = 500$ nF, $R = 10$ kΩ, $I_{max} = 1$ mA; (**d**) $V_a = 1$ V, $T_{on} = 1$ ms, $T_p = 2$ ms, $C = 500$ nF, $R = 5$ kΩ, $I_{max} = 2.68$ mA.

Neuron resistance and membrane capacitance values also have an immense impact on firing dynamics [17], which could be observable using the proposed SPICE model.

Starting from membrane capacitance, larger values result in extra pulses required to generate the spike, see Figure 4a,b for comparison for the same stimulus signal due to higher time constant of capacitance charging. Spike current is increased due to the larger amount of stored charge in the capacitor. On the other hand, neuron resistance value in the model influences on the time constant of the capacitor charging (required time to turn on the memristor), i.e., spike time occurrence (integration time) and spike amplitude (Figure 4b vs. Figure 4d). Neuron resistance can be used to model synaptic weight, larger values correspond to lower weight and vice versa [17].

4. Experimental Results and Discussion

In the following section, we report experimental results performed on perovskite BTO thin film memristor, by analysing device response on consecutive multiple reading pulses, and single writing pulse in order to test volatility behaviour. We also examined the dynamic response of LIF artificial neurons composed of physical memristor with intrinsic capacitance value and external shunt resistance. Experimental results are compared with numerical results from LIF memristive SPICE model.

Firstly, a typical volatility test [17,18], was performed on a BTO memristor composed of a train of reading pulses and a single writing pulse, as is shown in Figure 5, where red circles correspond to measured resistance values. Initial resistance R_0 of this device is ~1.43 kΩ

estimated by application of low-voltage reading pulses of 0.1 V, prior to writing event. BTO memristor was further stimulated using a single above-threshold pulse with the amplitude of 5 V, which switches the memristors in LRS state (~1.2 kΩ). Afterwards, a sequence of low-voltage reading pulses was applied, revealing finite characteristic relaxation time τ_r ~60 s. After this time, the device returns to the initial state R_0. This behaviour is typical for volatile memristors, indicating that after the stimulus is turned off, the device returns to the HRS state in a finite time period. In realized Pt/BTO/Pt device, diffusion of oxygen vacancies could lead to changes of electrical properties within the material [36], which resembles the ionic diffusion process controlling neuron channel conductance [37]. Both analogue-type switching [16] and threshold switching [38,39] was observed in volatile memristors [40]. Due to the low off-to-on resistance ratio (~1.5) and moderately steep transition between the resistance states (Figure 5 inset), realized device could be classified as an analogue switching volatile device [40].
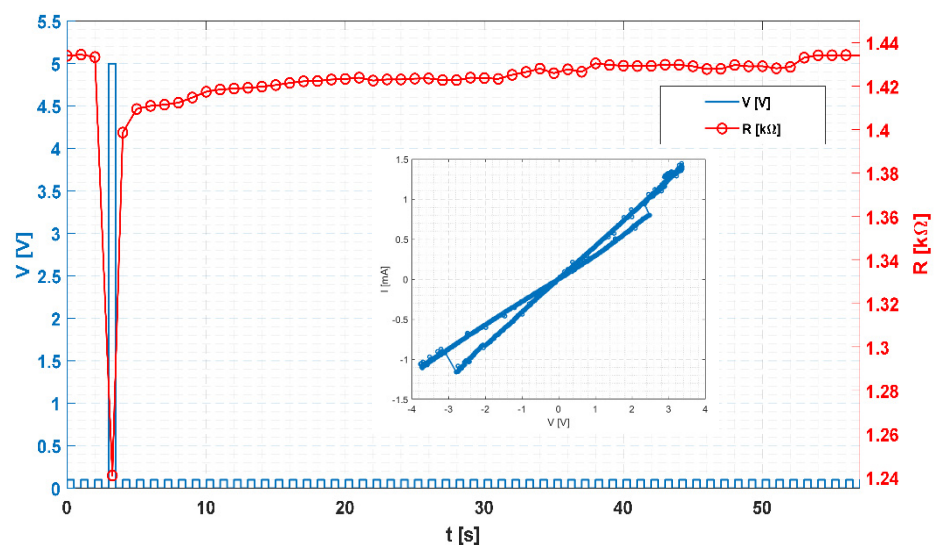

Figure 5. Volatility test of BTO memristor: reading pulses with low amplitude combined with single writing pulse. Inset- current-voltage characteristics of perovskite memristor.

In Figure 6 we included both simulated and experimental values of normalized resistance response upon the previously explained shown pulse train cycles. Simulation was performed in LTspice simulator on volatile memristor model, presented in Section 3, with the following parameters: R_{ON} = 1.5 kΩ, R_{OFF} = 2 kΩ, u_V = 10^{-10} cm^2/Vs, D = 100 nm corresponding to sample properties. As fitting parameters, we used electrical parameters of x-module Cx, Rx, i.e., components of the volatile cell, which determines the amount of volatile switching and relaxing period [23], respectively. Results, illustrated in Figure 6, show good agreement between experimental and simulated data. Existing discrepancies in the decay rate may originate from intrinsic device capacitance as well as the parasitic capacitance induced through measurement setup.

For a simple LIF circuit, an additional capacitor and resistor are included in the neuron model. Recent studies show that external capacitance can lead to a prominent delay in integration time [17], thus we use the intrinsic memristor's capacitance, whose value is estimated to ~1 nF, using an impedance analyzer for the frequency range of interest. The extracted simulation parameters and frequency-dependent capacitance value were used as input parameters for SPICE simulation of LIF neuron, Figure 7.
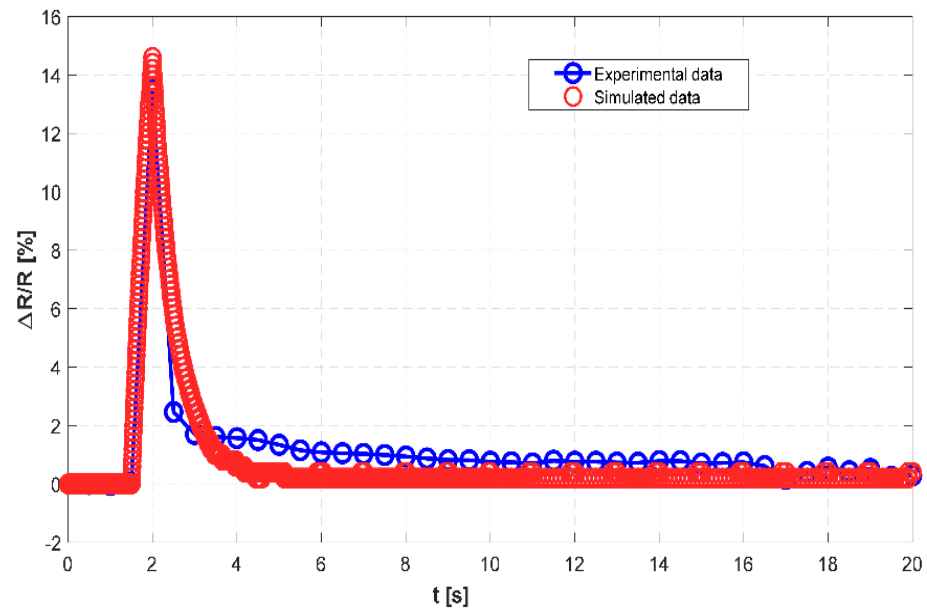
Figure 6. Simulated and experimental data of normalized resistance change upon a single writing pulse.
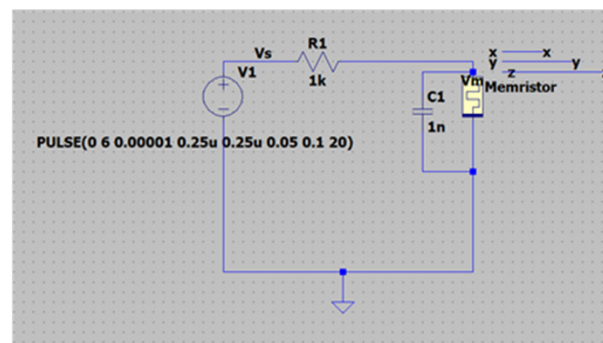

Figure 7. LIF neuron simulation circuit with volatile memristor.

The firing dynamic of the artificial neuron circuit could be analyzed using pulse train stimulation as proposed in [16,17]. In this experimental study, we applied multi-pulse voltage stimulation, *Vs* (frequency 10 Hz, amplitude 6 V, pulse duration 50 ms), Figure 8. Actuation voltage is divided between shunt resistor R and memristor-capacitor parallel connection. In the experimental setup as described in the materials and method section, current response is estimated according to values of voltage across constant resistor *R*, *Vr*, see Figure 8b. During the fourth pulse (see Figure 8a), the voltage across the memristor (including intrinsic capacitance), *Vm* drops down from ~3.8 V to ~3.5 V which occurs as a consequence of memristor switching to LRS state ($R_{ON} \approx 1.5$ kΩ). Namely, pulse actuation induces conduction modulation within diffusive memristor, which will eventually turn the device to on state and change the *Vm* value. At the same time, ~0.33 s, the current through the circuit increases starting from 2 mA to 2.36 mA, which is determined according to values of voltage *Vr* across constant resistor od 1 kΩ (see Figure 8b). An increase in current during pulse stimulation is interpreted as a firing event [16,17], yet due to the limited performance of BTO physical devices, specifically low off-to-on resistance ratio, this is not a very pronounced effect. It is worth noting that the amplitude of actuation voltage in our experimental studies was chosen in order to more easily reveal switching time, as for lower voltage values, the off-to-on resistance ratio of the diffusive memristor is decreased.
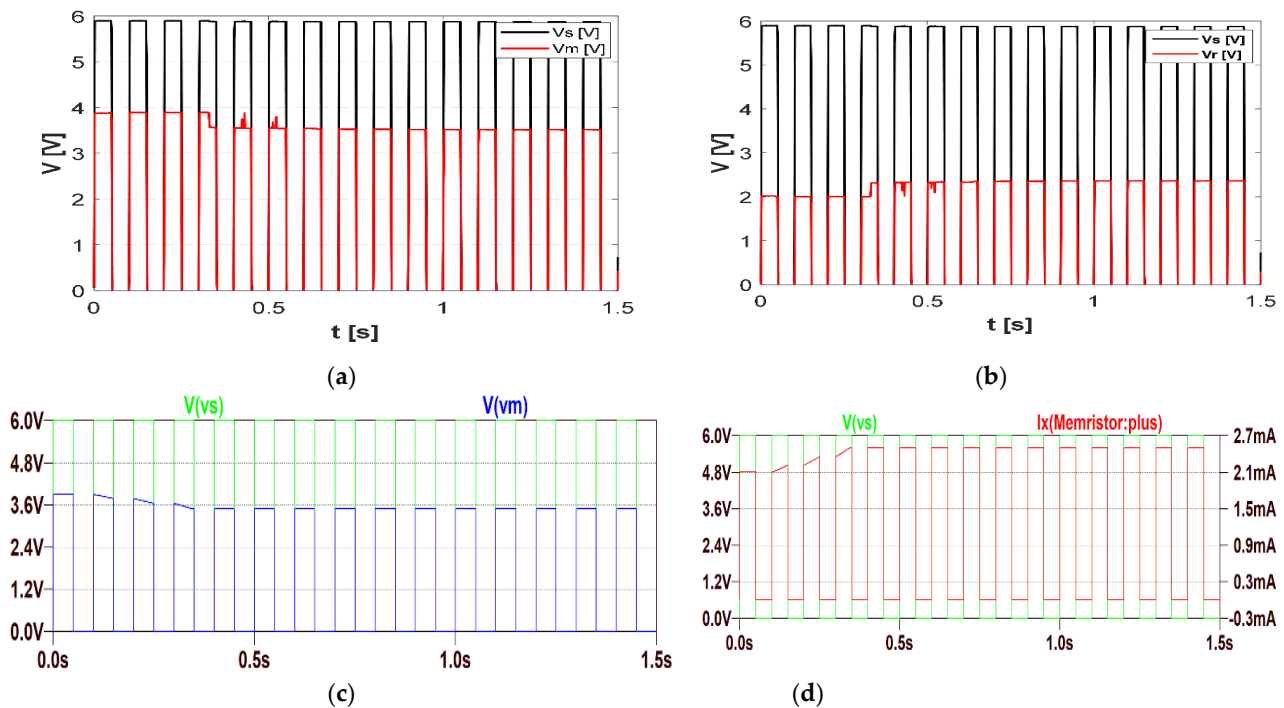
Figure 8. Experimental (**a**,**b**) and simulated response of LIF neuron circuit with volatile memristor under multiple pulses voltage actuation. (**a**) Voltage across memristor-experimental analysis; (**b**) voltage across constant resistor-experimental analysis; (**c**) voltage across memristor–simulation analysis; (**d**) memristor current–simulation analysis.

The additional peripheral circuit could be placed after the artificial neuron, in order to distinguish a spike event from an integration period. Solutions using comparator and pulse generator [16] or Schmitt trigger-based amplifier [15], already presented in literature, allow spike events to occur only when the input signal reaches the predefined threshold value. Certainly, improved performances of volatile memristor eliminate the need for a peripheral circuit in LIF neuron as presented in [17].

In Figure 8c,d SPICE simulation results of the LIF circuit are illustrated with the parameters extracted from normalized resistance timing characteristics (Figure 6) and properties of the BTO memristor. Regarding memristor voltage value transition, the initial voltage value is 3.69 V, while the final state amounts to 3.49 V, reached at 0.32 s (Figure 8c). Moreover, SPICE simulation results allow extraction of memristor current, without the need for usage of optimization tools for separation of memristive and capacitive effect which is required in the circuit design process [15]. Figure 8d illustrates memristors' current (Ix(Memristor:plus)) increases at ~0.32 s from 2.11 mA to 2.49 mA, which is in good agreement with the experimental analysis (see Figure 8b for comparison). Gradual changes of simulated memristors voltage and current values (Figure 8c,d) before reaching the stable state can not be detected through experimental results due to limitations of measuring equipment. After the pulse train is turned off the device returns to its initial state in finite relaxation time.

5. Conclusions

In summary, we have implemented our new window function in the existing model of the volatile memristor in the SPICE simulation environment and included it in a simple leaky integrate-and-fire neuron circuit applicable in all-memristive neural networks. Simple LIF circuit uses inherent volatility of resistive switching element to provide decay of local gradient potential, as a leaky term in short term memory, therefore no additional blocks are required. Performed simulations demonstrate that the model can capture biological neuron

dynamic: spatiotemporal integration task, firing function and leakage, i.e., forgetting functionality. The neuron model can also illustrate the influence of neuron resistance (synaptic weight) and membrane capacitance on firing behaviour and integration time. Verification was performed through comparison with an experimental study using $Pt/BaTiO_3/Pt$ diffusive/volatile memristor. In a physical LIF circuit, the intrinsic capacitance of the diffusive memristor is utilized as an integration element. Results show good agreement between model and experimental study for both resistance decay rate of volatile memristor itself and firing behaviour of LIF circuit. Demonstrated SPICE simulation of LIF allows decoupling of individual component influence of spiking behaviour and contributes to the enhancement of design of complex memristive neuromorphic architectures.

Appendix A

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SPICE CODE for volatile memristor
*Volatile Memristor Model
*Copyright 2021 FTS UNS MEMR Research Group
.param Ron=1 Roff=100k uv=1e-10 D=10n qp=300e-9 qn=-300e-9 Rint=15k
+ k={uv*Ron/D**2} deltaR={Roff-Ron} p=10
.param x0={(Roff-Rint)/(Roff-Ron)} y0={(Roff-Rint)/(Roff-Ron)} z0=0
*New window functions
.func fours(x)={(1-(2*x-1)**2)/(1-(2*x-1)**2+(2*x-1)**(2*p))}
.func
iy(y,v,z)={if(v>0,if(z>qp,I(Emem)*uv*Ron*fours(y)/D**2,0),if(z<qn,I(Emem)*uv*Ron*fours(y)/D**2,0))}
.subckt memristor_vol 1 2 x y z
*terminal cell
Roff 1 aux {Roff}
Emem aux 2 value={-deltaR*v(x)*I(Emem)}
*end of terminal cell
*x-module
Gx 0 x value={I(Emem)*uv*Ron*fours(v(x))/D**2}
```

```
Cx x 0 0.5 IC={x0}
Rx x 3 1
Enov 3 0 value={v(y)}
*end of x-module
*y-module
Gy 0 y value={iy(v(y),v(x),v(z))}
Cy y 0 1 IC={y0}
*end of y-module
*z-module
Gch 0 z value={I(Emem)}
Cz z 0 1 IC={0}
Rz z 0 0.1
*end of z-module
.ends memristor_vol
```

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