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Review

An Overview on Fault Management for Electric Vehicle Onboard Chargers

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Abstract: Onboard charging systems (OBCs) convert AC power from an external charging source into a DC voltage used to charge the battery pack of an electric vehicle (EV). OBCs are versatile since they can convert energy from almost every AC source, including standard household electrical receptacles, without needing wall chargers or charging stations. Since the same motor-drive electronics are reconfigured for onboard charging, weight and cost barely increase. However, the power quality and reliability of the OBCs are essential elements for proper grid interconnection. This article reviews the failures of power electronic converters that can be used for onboard charging and their most prominent fault-tolerance techniques. The various fault-tolerance methods are evaluated and compared in terms of complexity, cost, and performance to provide insights for future developments and research directions.

Keywords: fault tolerance; onboard chargers; electric vehicles

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1. Introduction

Power electronic converters (PECs) with high efficiency and power density play an increasingly important role not only in OBCs but in adjustable speed drives, renewable energy interfaces, flexible high-voltage direct current (HVDC) transmission systems, EVs, plugin hybrid electric vehicles (PHEV), and hybrid electric vehicles (HEVs) [1]. However, failures on PECs have been an important issue in various applications, such as vehicular OBCs and renewable energy generation, where a state of deviation from standard and usual conditions is shown.

Particular electronic configurations or topologies of PECs can be used in the OBCs for EVs, HEVs, and PHEVs. Those configurations include many electric and electronic components, but power semiconductors are considered the weakest and most fragile parts [2]. Power metal-oxide field-effect transistors (MOSFETs) are standard power semiconductors in various applications, including OBCs. Many methods that allow the diagnosis of both individual MOSFETs and the complete systems that comprise them can be found in the literature [3].

In the last decades, diverse research has been carried out on fault detection systems in PECs and their fault-tolerant methods. The first fault-tolerant studies focus on hardware redundancy [1]. Associated with increasing demands for system safety and reliability,

fault detection (FD) and fault-tolerant control (FTC) have attracted considerable attention lately in both research and application fields due to the continuous increase in automation, integration, and complexity of systems [4].

Although some years ago, some authors provided a basic review of fault-tolerance methods, many fault detection and tolerance techniques have emerged in the last decade, and a deep actualization becomes necessary [1]. Efficiency, reconfiguration, isolation, and other characteristics of the existing topologies and fault-tolerance techniques must be compared to show a general state-of-the-art perspective. Additionally, future research directions must be established so that the reader can have a comprehensible guide in a vast information world.

This paper presents an updated classification of the faults encountered in PECs for onboard charging and their associated tolerance techniques. A comparison of the most relevant fault-tolerance capabilities is developed to analyze the possibility of new techniques and future research directions. The fault-tolerance techniques in this paper were selected on an onboard charging capability basis of PECs, including AC and DC drive systems. Power quality in PECs is not the subject of this paper; however, some references combine its enhancement with fault-tolerance techniques in this review.

Note that every presented configuration/topology can operate as a bidirectional PEC and hence, an OBC; the three-phase sources can be replaced by an AC motor or grid sources, and the load or DC bus could be connected to the battery bank of the vehicle.

This paper is organized as follows. Section 2 presents the general classification of PEC/OBC faults and a brief description of the fault-tolerance techniques. Section 3 compares relevant characteristics of these techniques; power density, control type, control complexity, bidirectional capability, input voltage level, output voltage level, efficiency, hardware reconfiguration capability, isolation, and the number of additional devices are considered. Finally, Section 4 presents insights for future developments and research directions.

2. General Classification

Nowadays, different fault-tolerant solutions have been reported for power electronic converters focused on the robustness to specific failures. These faults can be classified into six categories: switch level, leg level, module level, system level, measurement level, and network level.

A switch-level fault refers to a short or open circuit in some power semiconductor such as a Diode, SCR, MOSFET, or BJT. A leg-level fault is a short/open circuit of one or more components that degrade/disable the power conversion of an AC phase. Module-level faults mean faults in some cascaded multilevel converter (CMC) or modular multilevel converter (MMC) sections (modules); if any module fails, other modules are reconfigured to maintain operation. Cascaded or paralleled configurations consist of several simpler PECs connected this way; a system-level failure refers to the damage of one of these converters. Series/parallel switches are regularly added to bridge/disable the faulty converter.

Measurement-level faults occur in current or voltage sensors that degrade the system performance and cause severe misfunctions in PECs. Grid or network-level faults are related to power quality issues, including phase unbalance, sags, and swells, damaging the PECs/OBCs.

Figure 1 categorizes the faults in power electronic converters for onboard charging. This classification is based on [1], but new categories are included due to recent research that does not fit previous ones.

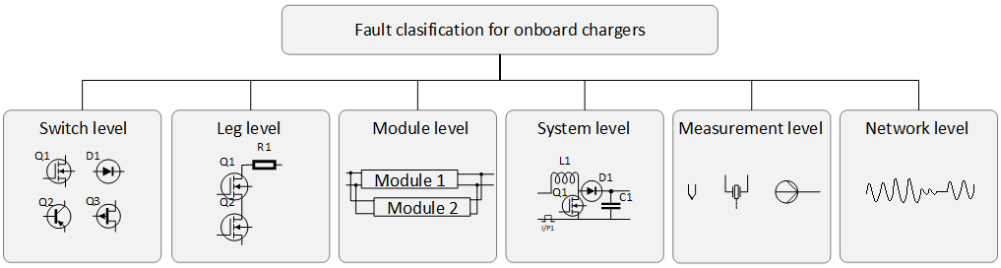


Figure 1. Fault classification for PECs/OBCs. Symbology shows common fault origins.

Many solutions have been proposed for switch-level faults that focus on control methods without reconfiguring or adding electronics to the PEC/OBC [1,5–22] and using backup devices [23–26].

Switch-level failures can be caused by a controller malfunction or an output short circuit, provoking their breakdown. Open-circuit failures of the power semiconductor probably do not lead to a catastrophic failure but do decrease OBC/PEC performance and efficiency. Therefore, the first answer for the problem has been a control method to isolate the defective open-circuit switch [5–13]. The second solution for switch level reconfiguration is to connect the faulty converter to a midpoint of the DC bus utilizing additional auxiliary switches [14–20].

For leg-level scenarios, a solution for the fault is to add supplementary legs in parallel with the main legs. Using the backup devices to replace the damaged ones can guarantee a regular operation of the converter after failure, including faults on other leg components and not only on semiconductors. Hence, the converter can be designed with an auxiliary leg connected to a DC midpoint like the switch level solution [21–44].

CMC and MMC are typical topologies with module-level redundancy. Module redundancy controllers are specific for this kind of power converter and operate by residual values obtained by calculating the difference between measured and observed variables. If some modules/stages fail, a supervisory control uses fault-tolerant reconfiguration to maintain continuous operation [45–58]. A particular scenario is presented with asymmetric converters. It has been proposed to use Clarke's transform to detect the fault by separating the positive and negative sequence current components. Additionally, there have been studied proportional-resonant current controllers in the ab frame [59]; still, at the moment, research on fault-tolerance techniques for asymmetric converters is scarce.

In a measurement failure or communication breakdown scenario, techniques such as DC voltage and AC frequency control are used to cope with a signal deficiency [60–66]. Network-level faults include three-phase systems and refer also to power quality issues, including phase unbalance. These faults can cause poor performance in three-phase loads, and regularly, higher than normal currents/voltages are manifested. Different fault-tolerant solutions to phase-unbalance have been proposed; one solution is to use a control method that can operate in both ideal and unbalanced modes. A fix to minimize the problem is to add hardware components to absorb the additional power ripple during phase unbalance [59,67–77].

System-level failures occur only in cascaded and parallel converters, and their mitigation includes significant hardware reconfigurations [78–82].

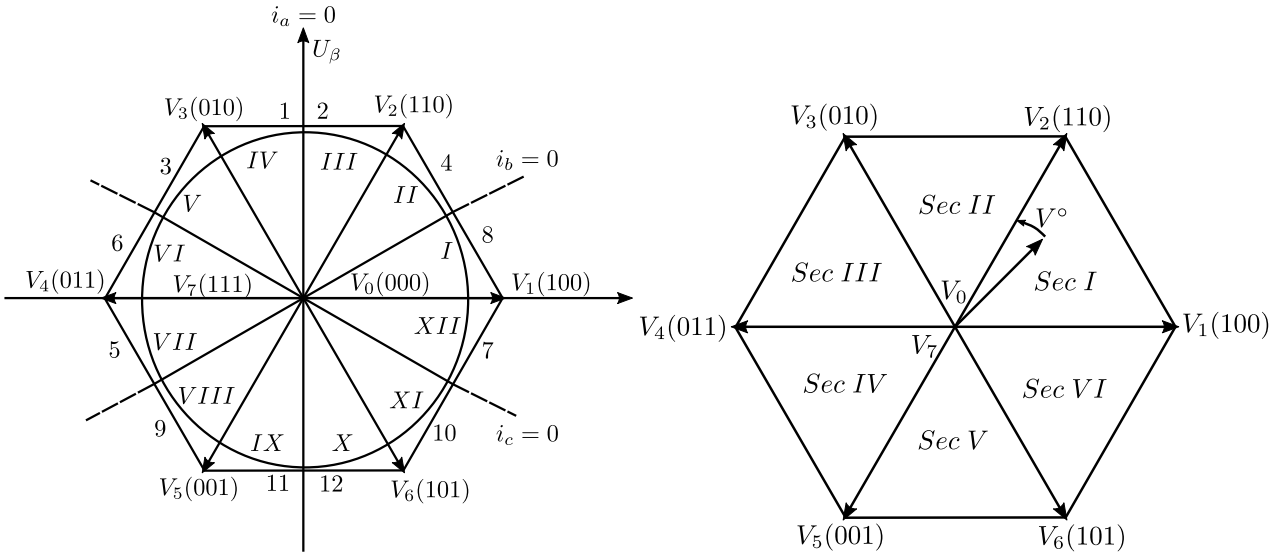
2.1. Switch-Level Fault Tolerance Techniques

When a single switch fails in a three-phase PEC, two possibilities to cope with it are compensation by the remaining circuitry or the addition of redundant hardware during the design stage. This section is dedicated to overview control techniques with and without hardware reconfiguration/redundancy at the switch level.

2.1.1. Control Strategies for Switch-Level Faults

Different fault-tolerant control methods for OBCs requiring no converter reconfiguration or additional devices have been proposed.

In Ref. [5], the deviation of voltage vectors and the affected voltage space sectors under fault conditions are analyzed for a three-phase two-level converter with DC output. A fault control approach based on twelve-sector splitting is proposed (Figure 2a).



(**a**) Twelve sectors. (**b**) Six sectors.

Figure 2. Fault partitioning schemes for a three-phase two-level converter with DC output.

The sectors indicate the combinations of the switches. Eight combined states are obtained since a three-phase converter has three bridge arms, and each one has two interrupters. They constitute eight active vectors, including six effective vectors: $V_1(100)$, $V_2(110)$, $V_3(010)$, $V_4(011)$, $V_5(001)$, $V_6(101)$, and two null vectors: $V_0(000)$, $V_7(111)$. In the one with 12 sectors, the three-phase currents $i_a = 0$, $i_b = 0$, and $i_c = 0$ are used to subdivide the 6 sectors into 12. This splitting scheme allows the sectors affected by faulty switches to be effectively separated from the unaffected. Space vector pulse width modulation (SVPWM) strategies are implemented to compensate for each sector's distorted reference voltage vector. In Refs. [6–8], a six-sector partitioning scheme (Figure 2b) is used for the fault detection system. The detection regions are independent because each switch has an assigned circuit region. Therefore, the superposition principle is used during multi-fault conditions; a DPWM (discontinuous PWM)-based control scheme is proposed to compensate for the faulted voltage vectors. A similar six-sector fault detection scheme is used in topologies as a Vienna-type rectifier [9] and a three-level T-type inverter [10]. The six-sector fault detection technique is also employed in matrix converters, using the current vector angle time-derivative to determine the faulty switch accurately [11].

In most fault-tolerant solutions, deficiency detection and isolation are the first steps, especially at the switch level. Different methods have been proposed for fault detection at the switch level; in Ref. [12], an analogic circuit-based fault detection system for IGBT transistors is proposed for open-circuit and short-circuit faults. This technique is based on gate signal monitoring, and an essential characteristic is a reduction in fault detection time. In Ref. [13], a method based on the calculation of the rectifier phase voltage errors is used; their values and signs are analyzed to locate the faulty transistors.

In Ref. [83], the authors present a digital optimal battery charger that has an inherent characteristic of detecting the fault within one switching cycle. The charger consists of a synchronous buck converter, and a novel carrier generation (synthetic ripple) digital feedback clamped hysteresis modulator. The proposed charger charges the battery with

the constant current for less battery state of charge (SOC) and charges it with the constant voltage when the battery SOC reaches near 100%.

2.1.2. Hardware Redundancy for Switch-Level Faults

When an open-circuit fault occurs in a switch, the deficiency can be initially identified and the faulty section of the converter can be isolated by eliminating the gate signal from the damaged device. Figure 3 shows a typical fault isolation scheme at the switch level [14,15]. This fault-tolerant scheme directly measures the currents i_a, i_b, and DC voltage. Each leg is directly connected to the midpoint N of the DC current link by the bidirectional switches TR_A, TR_B, and TR_C. If a S_1, ..., S_6 switch failure occurs, the diagnostic scheme identifies the fault, and the defective switch is isolated from the circuit by eliminating its gating signal. The corresponding TRIAC (TR_A, TR_B, TR_C) is gated to connect the phase with the midpoint of the DC link.

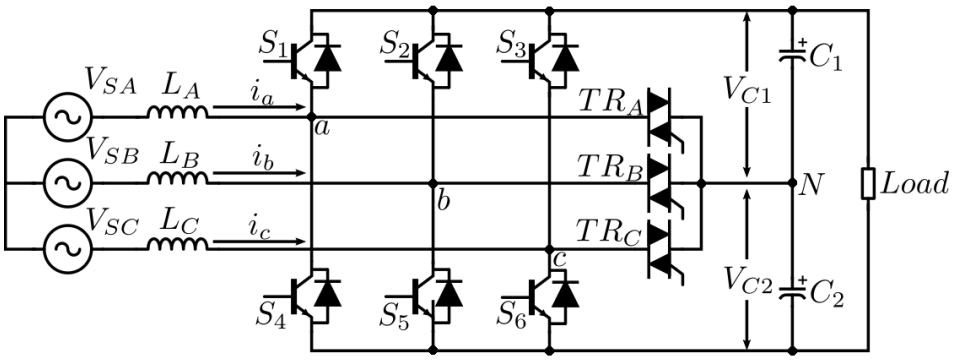


Figure 3. Fault-isolation scheme strategy at the switch level.The TRIAC (TR_A, TR_B, TR_C) of the faulty switch (S_1, ..., S_6) is gated to connect the phase to the midpoint of the DC link.

An enhanced strategy to achieve fault tolerance at the switch level is depicted in Figure 4; bidirectional switches connect a classic three-leg power converter topology to a redundant circuit consisting of two semiconductors (S_7 and S_8) [16]. When a fault occurs in one of the power switches (S_1, ..., S_6), a supervisor circuit detects the occurrence and isolates the faulty leg by eliminating the gate signal. In the case of a short circuit, the defective leg is supposed to be isolated by fast-acting fuses (f_1, ..., f_6); however, this might not work in practice, as the short-circuit protection of the transistor driver circuits should react in microseconds to avoid the propagation of the fault. In both cases, the reconfiguration scheme activates the appropriate bidirectional switch (T_1, T_2, or T_3) to connect the faulty phase to the midpoint (g) of the redundant circuit. The strategy allows the redirection of the control commands of the defective section to the redundant switch, restoring the complete operation of the PEC.

Figure 5 shows a third strategy for switch-level fault protection in a back-to-back power converter with three additional bidirectional switches T_a, T_b, and T_c [17]. These bi-directional switches are used for converter reconfiguration after fault isolation; i.e., these switches are all off before the fault occurs. The bidirectional switches T_a, T_b, or T_c are gated during a switch failure, replacing the faulty switch (S_1, ..., S_6, S'_1, ..., S'_6). Each side of the converter may be connected to a source, load, or machine, depending on its utilization.

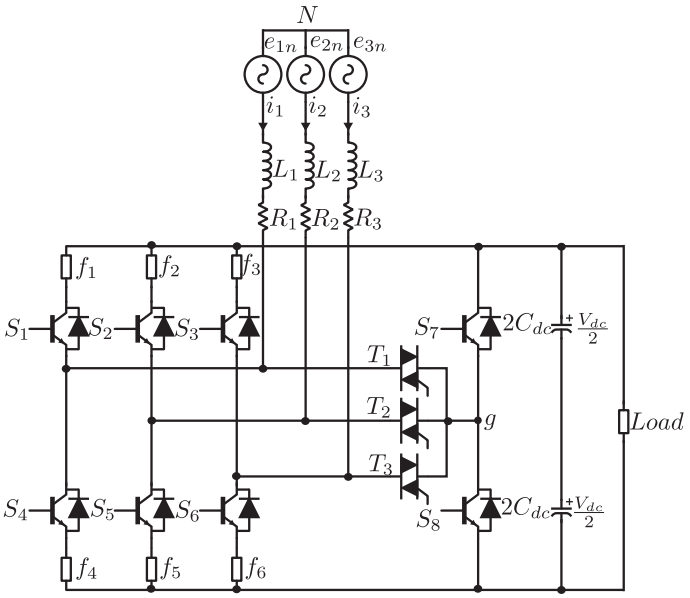


Figure 4. Fault-isolation at the switch level.The defective switch is isolated, and control commands are redirected to the redundant switch.

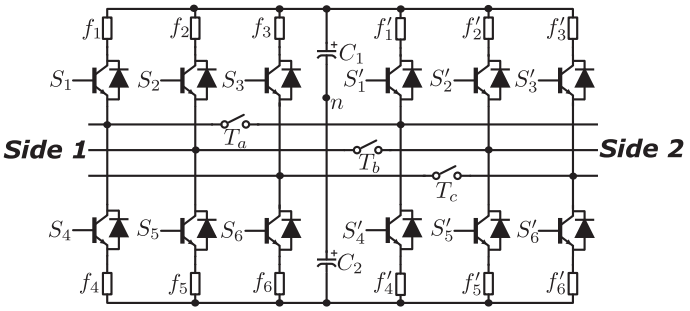


Figure 5. Switch-level fault protection in a back-to-back power converter.The bidirectional switches T_a, T_b or T_c are gated during a switch failure, replacing the faulty switch (S_1, ..., S_6, S'_1, ..., S'_6).

Some researchers have proposed detection solutions that identify the fault in a single switching device. In Ref. [18], such an IGBT open-circuit fault diagnosis strategy is based on error estimation of the three-phase two-level AC/DC voltage-controlled converter. The technique allows finding the faulty IGBT in rectification and regeneration modes faster than in an entire period of the AC.

Bridgeless rectifiers are widely used due to unity power factor, lower conduction loss, high efficiency, and absence of bidirectional power switches. However, failures in these converters threaten reliability in critical applications such as motor drives with OBCs; due to this, in Ref. [19], a method of fault detection, location, and tolerance using additional switches is proposed.

With the increase of renewable energy in smart grids and electric vehicles, fault-tolerant control techniques and artificial intelligence-based fault detection techniques have gained attention. For instance, in Ref. [20], a redundant topology consisting of three extra TRIACs (Figure 6) is combined with a fuzzy detection system. This strategy uses the average rotor current (load) values to detect the faulty switch briefly.

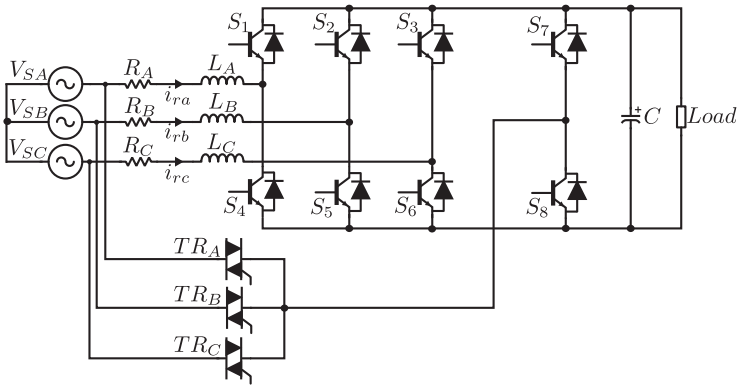


Figure 6. Redundant topology consisting of three extra TRIACs. If a switch fails (S_1, ..., S_6), the respective TRIAC (TR_A, TR_B, or TR_C) is triggered.

2.2. Leg-Level Fault Tolerance Techniques

Bidirectional AC/DC converters are widely used in uninterruptible power supplies, energy adapters, and OBCs. However, their susceptibility to failure due to many components is a significant disadvantage. Research has demonstrated that the six-switch AC-DC converter of Figure 3 can be reconfigured to a four-switch converter connected to a split capacitor upon leg failure.

In Ref. [34], the same bidirectional converter is controlled by a hybrid SVM (HBSVM) strategy; the authors include a vector plane distribution for reduced DC-link capacitor currents to achieve a reduced ripple voltage on the DC capacitors. Model predictive control (MPC) has been widely used in this converter to minimize power quality issues during leg failure (see [35–38], for instance) by analyzing disturbances that cause changes in the converter behavior or the control system itself. Additionally, by finite-state model predictive direct power control (MPDPC), an optimal voltage vector has been selected by a power prediction model, and a cost function to achieve flexible switching between inverter and rectifier modes [39–41]. The exciting scheme is that injecting bias during a phase current absence (leg) can achieve the DC-link splitting capacitor voltage balance control.

Several AC/DC converter fault detection systems that operate both single-switch and leg faults in the same phase for the converter of Figure 3 have been proposed. In Refs. [42,43], measurements between current links in a period are saved in a data list. A background analysis is used to describe the converter symmetry, divide the faults into three classes, and thus locate and isolate the broken leg or switch faults. In Ref. [44], the fault detection method is based on monitoring diagnostic signals. These signals include detecting sustained near-zero output current values by the ratio of the average phase current and the average magnitude thereof; this allows isolation of the faulty leg/switch.

Hardware Redundancy for Leg-Level Faults

Redundancy for leg-level faults is implemented by adding parallel or series legs. A solution based on a parallel leg is presented in Figure 7 [21]. In this configuration, on the AC side, three TRIACS (TR_A, TR_B, and TR_C) are connected as bidirectional switches between the phases and the center point of the split capacitance (C_2, C_3); when a fault occurs in the phase leg, the fuse f_1, f_2, or f_3 is disconnected, and the respective TRIAC (TR_A, TR_B, or TR_C) is triggered; however, this might not work in practice, as the short-circuit protection of the transistor driver circuits should react in microseconds to avoid the propagation of the fault. A similar approach is used in induction motor systems [22]; the strategy utilizes minimal devices and predictive torque control to achieve reconfiguration.

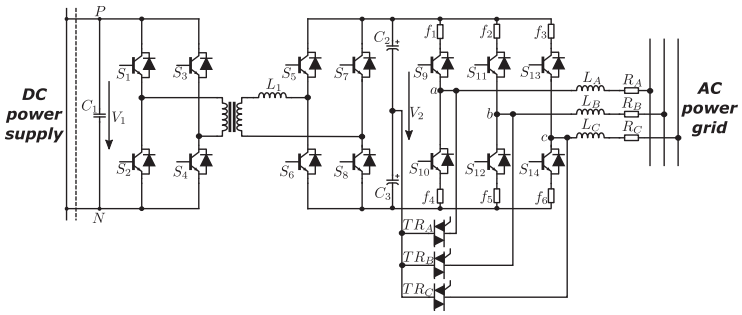


Figure 7. Topology of bidirectional AC/DC converter. On the AC side, three TRIACS are connected as bidirectional switches between the phases and the center point of the split capacitance; when a fault occurs in the phase leg, the fuse f_1, f_2 or f_3 is disconnected, and the respective TRIAC (TR_A, TR_B, or TR_C) is triggered.

Another approach for fault tolerance on permanent magnet sync motor (PMSM) control is proposed in Ref. [23]. A six-switch inverter with direct torque control is used (Figure 8); if the OBC faults a phase, the converter is reconfigured to a four-switch inverter by the respective TRIAC (TR_A, TR_B, or TR_C). In Ref. [24] two different fault-tolerant topologies (Figure 9) are proposed for a marine current turbine (MCT) built with a permanent magnet synchronous generator (PMSG). The first structure presents a four-leg converter capable of isolating the faulty leg using the fourth auxiliary leg. The second structure connects the TRIACs TR_a, TR_b, and TR_c to the DC split bus; this structure has several advantages: simplicity, good compatibility, low cost, and fault tolerance.

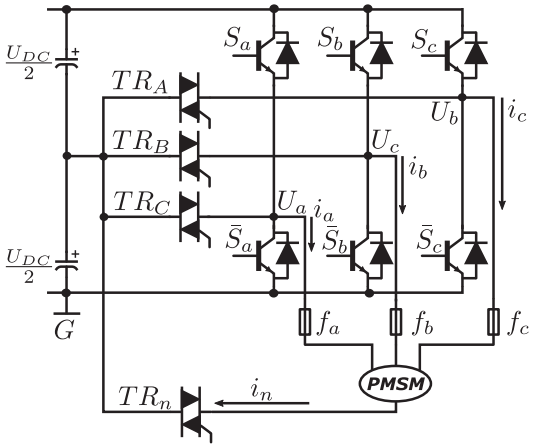
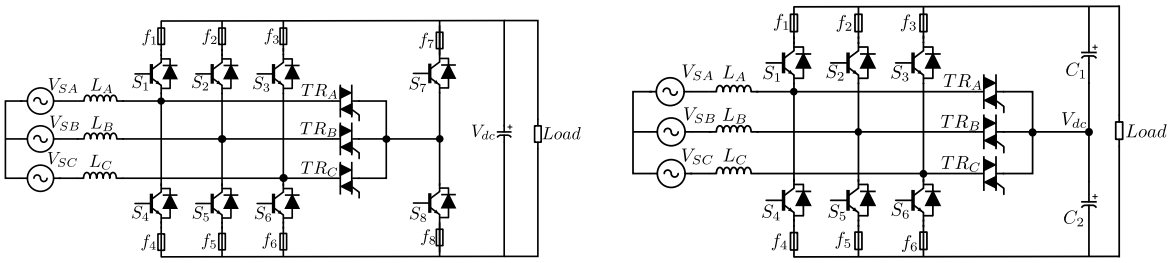


Figure 8. Six-switch inverter for PMSM direct torque control. If the OBC faults a phase, the converter is reconfigured to a four-switch inverter by the respective TRIAC (TR_A, TR_B, or TR_C).



(**a**) (**b**)

Figure 9. Fault-tolerant topologies. (**a**) PEC for PMSG turbine. The four-leg converter can isolate the faulty leg using the fourth auxiliary leg. (**b**) PEC for PMSG turbine. The respective faulty-phase TRIAC TR_A, TR_B, or TR_C is connected to the DC split bus to isolate the leg.

Substantial attention is attracted to the synchronous motor, fed by a dual inverter with a current bus in electric vehicle applications because of its simple structure, wide speed range, and fault tolerance. Different fault-tolerance control methods have been proposed for such scenarios. In Ref. [25], a technique based on winding reconnection is proposed (Figure 10). Such a proposal is based on the idea of leg sharing and can achieve regular operation by reconnecting the windings, providing fault-tolerant operation of up to three legs. In Ref. [26], a simplified PWM strategy for fault-tolerant control is proposed; as in the previous PEC, the converter comprises two three-phase six-switch inverters. When a fault happens, the circuit can be reconfigured to a four-switch inverter; unlike the earlier work, it has the disadvantage of working only for single-leg defects.

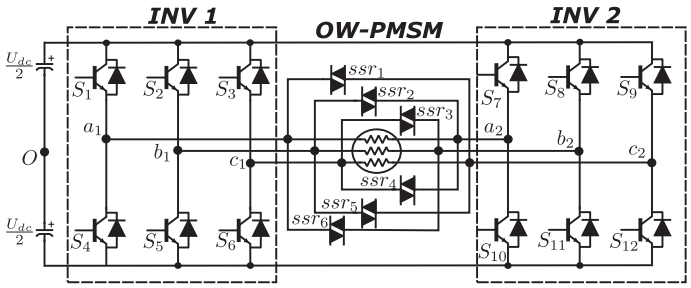


Figure 10. Fault-tolerant control of an open-end winding permanent magnet synchronous motor (OW-PMSM). The TRIACs allow reconnection of the winding with the faulty leg.

With the advantages of bidirectional power flow and adjustable dc-link tension, the back-to-back converter is widely used in many motor applications. In Ref. [27], this PEC feeds an induction motor, and the TRIACs can replace any inverter-side faulty leg. This six-leg PEC, shown in Figure 11, can be reconfigured into a four-leg converter by employing one motor phase connected to the midpoint of the capacitors (C_1, C_2). In Ref. [28], a fault-tolerant control method is based on a Luenberger observer for this PEC. This method uses input variables already available in the control system; hence no additional measuring is necessary. This method also avoids using other hardware that increases complexity and cost.

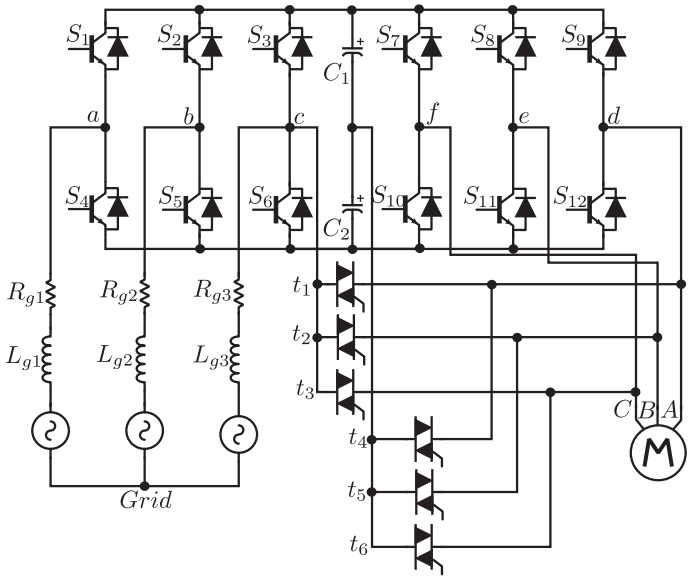


Figure 11. Fault-tolerant back-to-back converter. The t_1, t_2, or t_3 TRIACs can replace any inverter-side faulty leg and be reconfigured to a four-leg converter by connecting the midpoint of the capacitors (using t_4, t_5, or t_6).

The service continuity of wind power conversion systems and their reliability and performance are some of the main concerns in the electricity generation field, particularly on wind energy conversion systems (WECS) based on a doubly fed induction generator (DFIG). Because of this, six-legged fault-tolerant AC/DC/AC PECs have been suggested [29,30], and these can also be used for OBCs. The topology described in Figure 12 is based on a classical DC back-to-back converter with a redundant joint leg on both sides. The redundant portion consists of two switches (S_7 and S_8) and will replace the faulty leg in case of a failure on the primary or motor converter sides. On the other hand, since fast fault detection and reconfiguration of the converters are necessary to avoid losses and enable continuity of services, in Ref. [31], a similar topology based on five legs is proposed. After fault detection, it operates on four legs, and using an FPGA makes high-speed fault detection possible.

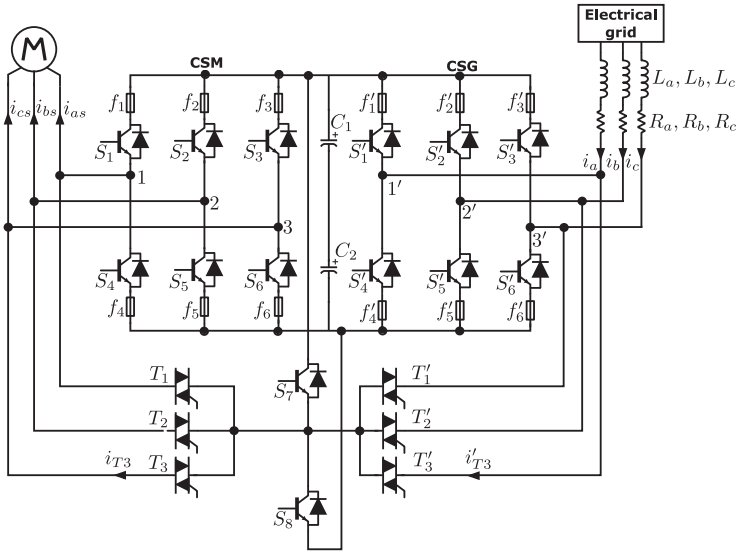


Figure 12. Fault-tolerant WECS topology with DFIG. The redundant switches S_7 and S_8, replace the faulty leg in case of a failure on the primary or motor converter side.

Isolated three-phase AC-DC PECs have become prevalent for industrial uses, and recently, more attention has been set to their reliability. In Ref. [32], a single-phase isolated AC/DC converter with fault-tolerant capability is proposed (Figure 13). The proposed three-phase fault-tolerant isolated AC-DC converter can be implemented with only six main switches and has the advantage of being simple to control. In Ref. [33], a single-stage isolated three or two-phase AC/DC converter with Y-Δ connected symmetrical transformers is presented (Figure 14); this topology is used for isolated buck conversion with a high power factor. The converter provides high power conversion in normal operation because the transformer operates in symmetry and shares the power equally. When there is a fault or at light load conditions the converter operates in dual transformer mode. For instance, during S_{c1} fault the switches S_{a1}, S_{b1}, and S_{c3} are switched on, and the current flows into the dotted terminal of a_p and out of the dotted terminal of c_p. Hence, the diodes D_{s1}, D_{s3}, and D_{s6} are on, providing uninterrupted output power.

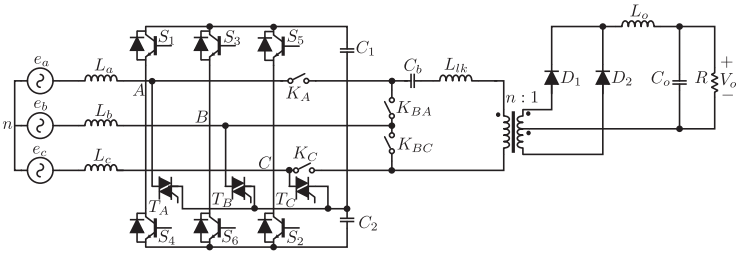


Figure 13. Fault-tolerant AC-DC single-stage isolated PEC. Combining T_A, T_B, T_C TRIACs, and K_A, K_C, K_{BA}, and K_{BC} bidirectional switches, a faulty leg can be replaced.

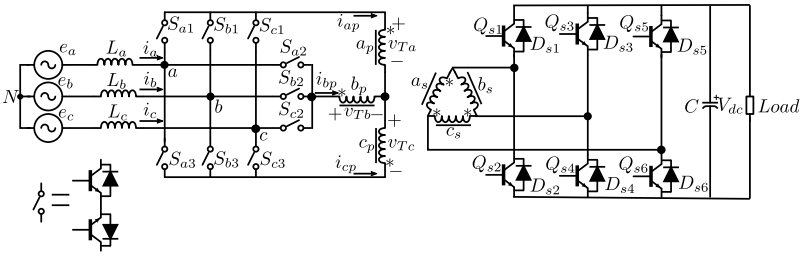


Figure 14. Single-stage isolated three or two-phase AC/DC converter with Y-Δ connected symmetrical transformers. When there is a fault or at light load conditions the converter operates in dual transformer mode. For instance, during S_{c1} fault the switches S_{a1}, S_{b1}, and S_{c3} are switched on, and the current flows into the dotted terminal of a_p and out of the dotted terminal of c_p. Hence, the diodes D_{s1}, D_{s3}, and D_{s6} are on, providing uninterrupted output power.

Variable speed drives for induction motors operating by voltage source inverter (VSI), and vector pulse width modulation (SVPWM), are used for various purposes requiring high reliability. The authors in Ref. [76] use a novel space vector modulation strategy for a fault-tolerant inverter supplying an induction motor (IM) (Figure 15). This system uses two space vector modulation strategies to switch from healthy to faulty operation. The modulation strategy proposed for flawed processes has the symmetry of a classical six-switch inverter. Under normal operating conditions, switch f_1 is closed, f_2 is open, and the motor is supplied from the typical inverter (S_1–S_6). Additionally, a model of the three-phase voltage converter is presented in Ref. [77]; this model can be used to simulate its operating modes in standard and fault states.

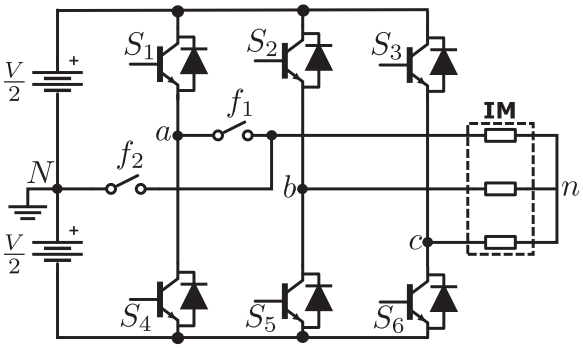


Figure 15. Schematic diagram of a typical fault-tolerant inverter. Under normal operating conditions, switch f_1 is closed, f_2 is open, and the motor is supplied from the typical inverter (S_1–S_6).

2.3. Module-Level Fault Tolerance Techniques

The matrix converter system is becoming an up-and-coming candidate to replace the conventional two-stage AC/DC/AC converter. However, the reliability of the system is still an open problem. In Ref. [45], output currents are used for fault detection since no additional devices or modifications are required by this technique, offering a very economical solution. In Ref. [46], a fault diagnosis method to identify a single switch failure is proposed; this method is based on finite set model predictive control (FCS-MPC), which employs a discrete-time model of the matrix converter topology. A short-circuit fault-tolerant system for conventional matrix converter (MC) is proposed in Ref. [47]. When a short-circuit fault occurs, it is detected quickly. The semiconductors are shut down smoothly to prevent the short-circuit fault from spreading to the healthy semiconductors. The authors in Ref. [48] propose a new matrix converter topology and modulation techniques for short-circuit and open-circuit fault tolerance (Figure 16). During normal operation, this PEC operates as a standard matrix converter (without TRIACS and fuses). When the system controller detects a fault (S_aA for instance), the two remaining switches in the faulty output leg (S_bA and S_cA) open to avoid the short circuit condition of the other power sources. The connecting device linked to the output leg with the short-faulted switch (CD_A) is then

triggered. As a result, the short-circuit condition is redirected through the input voltage V_a, the short-failed switch S_aA, the connecting device CD_A, and the fast-acting fuse F_A that is finally burned.

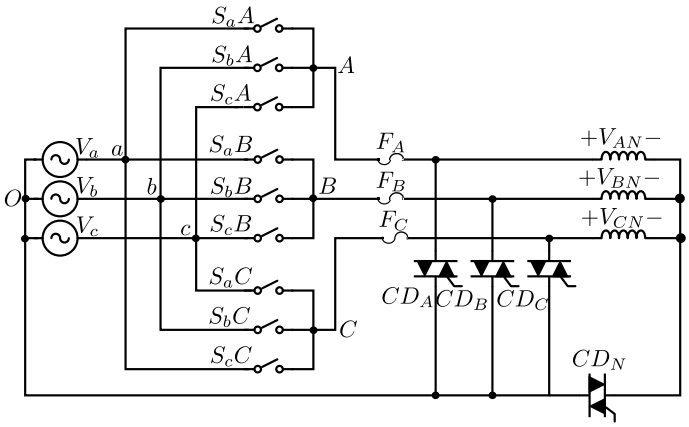


Figure 16. Matrix converter structure with short-circuit and open-circuit fault tolerance. When the system controller detects a fault (S_aA for instance), the two remaining switches in the faulty output leg (S_bA and S_cA) open to avoid the short circuit condition of the other power sources. The connecting device linked to the output leg with the short-faulted switch (CD_A) is then triggered. As a result, the short-circuit condition is redirected through the input voltage V_a, the short-failed switch S_aA, the connecting device CD_A , and the fast-acting fuse F_A that is finally burned.

In Ref. [49], a single-phase fault-tolerant matrix converter is proposed (Figure 17); fault compensation is achieved by reconfiguring the matrix topology with the help of a switching device (TR_N). Based on the redefined structure of the converter, a fault-tolerant modulation algorithm is developed to reshape the output currents of the two non-fault phases to obtain continuous operation. Similarly, in Ref. [50], a fault-tolerant four-legged matrix converter topology combined with space vector modulation is proposed. The four-leg-based fault-tolerant structure uses an additional redundant phase module.

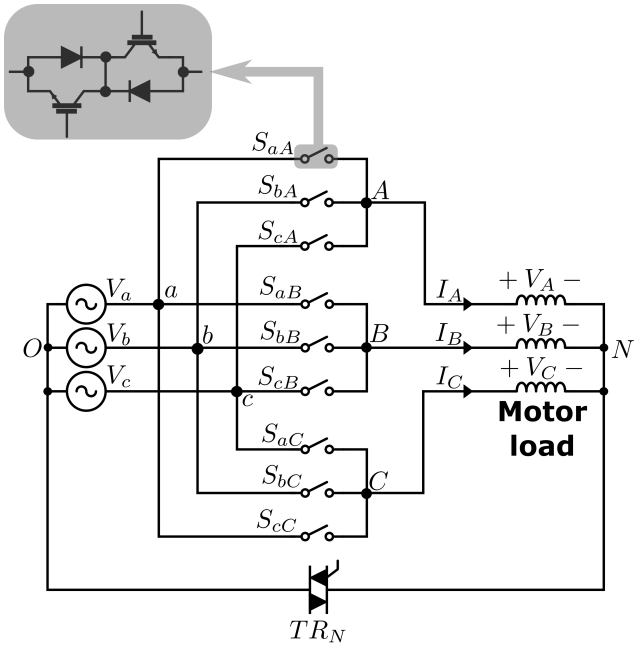


Figure 17. Fault-tolerant single-phase matrix PEC. Fault compensation is achieved by reconfiguring the matrix topology with the help of a switching device (TR_N). Based on the redefined structure of the converter, a fault-tolerant modulation algorithm is developed to reshape the output currents of the two non-fault phases to obtain continuous operation.

Multilevel converter topologies offer advantages in increased permissible DC-link voltage and improved input current harmonics compared to conventional two-level converters. Therefore, three-level topology systems with neutral point clamping (NPC) have been widely used. In Ref. [51], the DC link voltage and the phase angle of the input are used for the fault detection system; this method significantly minimizes the fault effect by compensating for the distorted reference voltage. In Ref. [52], open-switch and short-circuit fault detection strategies for a single device based on a reconfiguration of the NPC PEC are proposed (Figure 18).

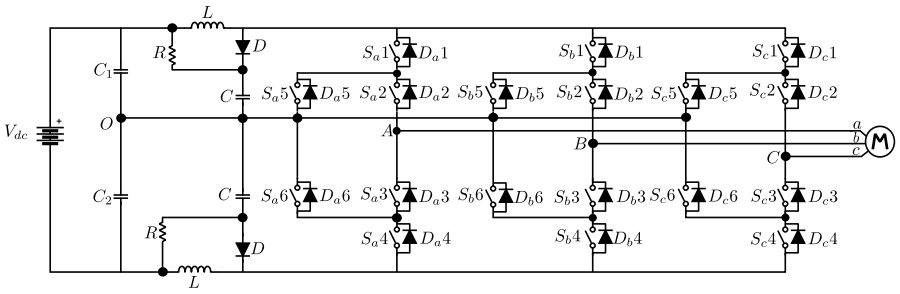


Figure 18. Active NPC. Open-switch and short-circuit faults are faced by proper bidirectional switches reconfiguration. For instance, when S_a1 open failure occurs at the positive stage, the AC phase output is connected to neutral-point (O) of DC link instead of positive DC bus by S_a2 and S_a5.

Similarly, in Ref. [53], an instantaneous-voltage error algorithm requires only signals already available in the control system, avoiding the use of additional hardware. The algorithm is independent of the load and the control strategy used and provides high-speed fault detection and identification, with diagnostic times as low as two sample periods. In Ref. [54], a phase disposition pulse width modulation (PDPWM) technique based on an adaptive carrier for MMCs using only one carrier for fault-tolerance capability is presented. Power-based control is also used in this study to regulate the balance of SMs during and after a fault.

Due to the increased reliability of the MMCs, the capacitors must guarantee the proper operation of the converter and voltage reduction of the submodules; due to the above, Ref. [55] presents an adaptive voltage balancing strategy based on capacitor voltage estimation using a hybrid ADALINE-RLS scheme. The proposed method eliminates the need to measure the capacitor voltages of the submodules and the associated communication link with the central controller. In addition, the estimated capacitor voltages are used to detect and locate different types of faults in the submodules. After isolating the faulty submodules, the proposed fault-tolerant control unit (FTCU) modifies the parameters of the voltage balancing strategy to overcome the derating of the active submodules. Similarly, a comparison of capacitor voltage ripple suppression methods under unbalanced conditions is presented in Ref. [56]. Three methods are explained and compared in simulation: the circulating current specific sequence elimination method (CCSSE), the instantaneous circulating current optimization method (ICCO), and the arm current control method (ACC).

DC line faults have a substantial impact on the converter power electronics. Fault-tolerant multilevel converters must limit and control these fault currents upon detection. Therefore, [57] presents a dynamic internal overcurrent control (DIOC) for full-bridge multilevel converters (FB-MMC). The control protects the converter power electronics against thermal overload without locking the converter. The DIOC does not rely on fault detection and effectively limits the arm currently in stable and transient situations.

Modular series-to-parallel DC-DC converters (MSPDDC) are good choices in high power and high voltage applications (Figure 19). The reliable operation should be a significant concern in critical situations. A general switching fault-tolerance method for MSPDDCs is proposed in Ref. [58] for open and short circuit faults (Figure 20). Fault diagnosis is achieved using a small winding (L_1) integrated into the inductor magnetic

core to measure the output inductor voltage in each module. A diagnostic circuit allows isolating the defective module by combining additional switches.

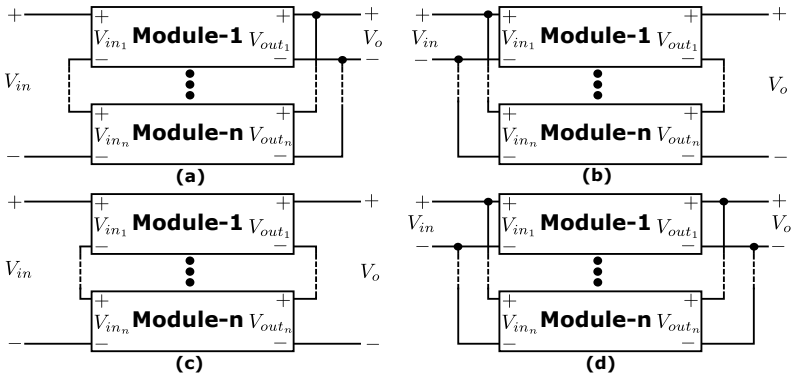


Figure 19. Four connections of series-parallel converter system. (**a**) Input-series–output-parallel. (**b**) Input-parallel–output-series. (**c**) Input-series–output-series. (**d**) Input-parallel–output-parallel.

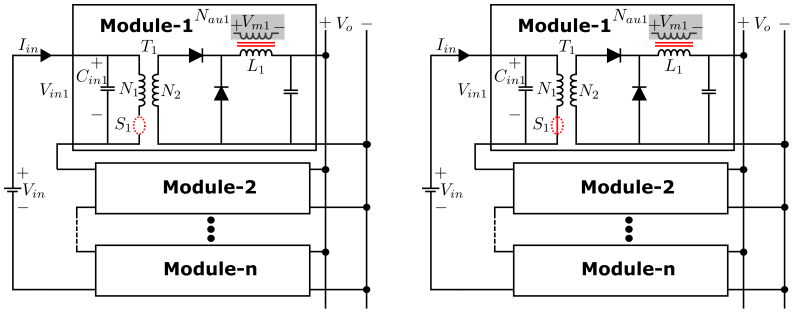


Figure 20. Circuit structure after switch fault for input-series–output-parallel PEC. (**a**) Open-circuit fault. (**b**) Short-circuit fault.

In Ref. [84], the authors propose connecting a six-phase machine and three-phase AC source by a symmetrical six-phase open-end winding machine, a twelve-leg inverter, and a DC–DC converter. The charger circuit is constructed by directly connecting the three-phase grid to the middle point of the machine phase winding. The grid currents split into equal portions and flow in opposite directions without adding an extra mechanical switch (or relay). From this concept, the proposed system has the advantages of obtaining high-power density with a significant inductance value for grid-side filter during charging and avoiding an electromagnetic torque, and providing a high fault-tolerant capability. Moreover, the proposed system can operate under the unity power factor (UPF) with a total harmonic distortion (THD) below 5%.

2.4. System-Level Fault Tolerance Techniques

The parallel hybrid multilevel converter (PHMC) (Figure 21) is gaining popularity for HVDC applications due to its modular structure and independent active and reactive power control. However, this PEC requires twice as many semiconductor switches (S_1–S_{12}) and many DC capacitors; it significantly increases its volume compared to the two-level voltage source converter [78]. The PHMC circuit has gained much interest due to its two main advantages. It requires fewer components than the typical MMC and has lower conduction losses because the daisy-chain-link HBSMs are not in the primary conduction path [79]. Due to this, in Ref. [80], a modified parallel hybrid converter (MPHC) for HVDC applications with a wide operating range and DC fault-tolerance capabilities is presented. A new control technique for capacitor voltage balancing is also proposed; performance evaluations are carried out using PSCAD/EMTDC for the under modulation index and overmodulation range.

In Ref. [81], the authors propose an open-switch fault-tolerant control method for a single IGBT in two parallel-connected three-phase AC/DC converters. The paper presents a new fault-tolerant control method using the combined control of the two converters to compensate for the distorted current of the fault-side converter. Similarly, in Ref. [82], the fault operation mechanism of a parallel wind converter is analyzed in detail. A fault-tolerant control strategy based on negative sequence current compensation is proposed, and a non-faulty converter module is used to compensate for the negative sequence current of the faulty converter module. When the system power is less than or equal to 0.5 percentual units (pu), the maximum output power of the converter is achieved under the condition of ensuring the current balance of the grid-connected side. When the system power is more significant than 0.5 pu, the grid-side negative sequence is controlled to the minimum under the condition of producing the maximum capacity.

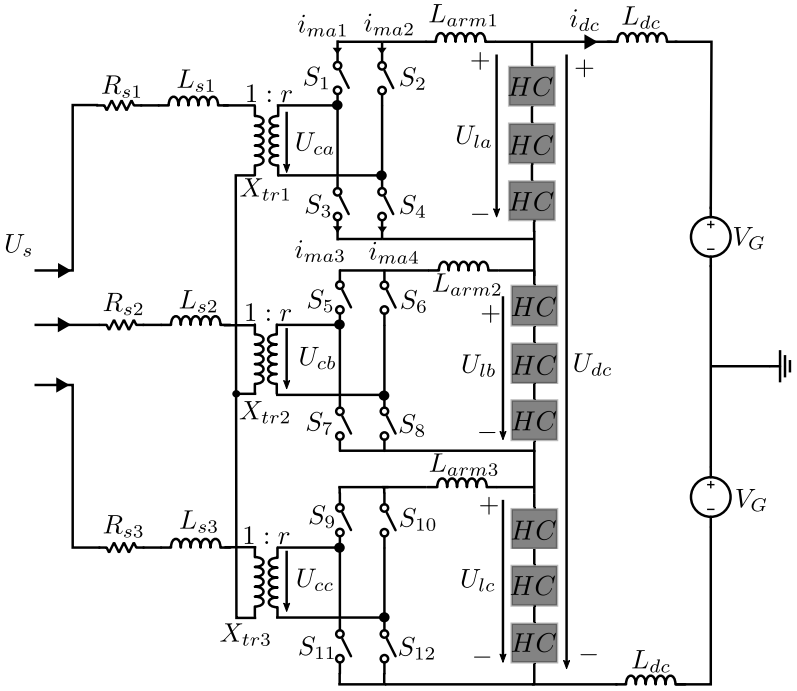


Figure 21. PHMC topology. HC are half-bridge (HB) cell stacks. The cell stack is used to produce the absolute value of a sinusoidal wave, and then its polarity will be rotated to produce the required AC by the IGBT H-bridge.

The authors in Ref. [85] propose a fully integrated onboard DC fast charger, which is compatible with permanent magnet synchronous machines (PMSMs), DC excited synchronous machines, and induction motors as well as single or dual inverter drive systems. The sum of the energy storage sources' voltages must be higher than the input voltage. Therefore, the proposed OBC offers fault blocking possibility in cases where the energy storage sources' voltages drop below the input voltage.

2.5. Measurement-Level Fault Tolerance Techniques

Due to aging devices, human errors, environmental disturbances, and mechanical vibrations, the sensors of the PEC/OBC system may malfunction. As a result, the feedback value of the control system deviates, which directly affects the system performance and even causes permanent damage to the electrical devices. In Ref. [60], the authors propose replacing an erroneous measured value with the output of a state observer for the rectifier stage of a basic single-phase to three-phase PEC. The exciting item is the design of the observer to be digitally implemented, preventing its output from chattering because of the discretization procedure of the PEC model. An intelligently coupled filtering scheme achieves the above.

The authors in Ref. [61] propose a fault-tolerant algorithm consisting of the following steps using the circuit exposed in Figure 22. Firstly, measurement of line voltages (V_{ab}, V_{bc}, and V_{ca}) and summation of voltages ($V_{sum} = 0$) are performed. Significant V_{sum} values are compared with a failure threshold. If a fault is advised, resolution of the faulty sensor is achieved, and it is determined if the measured value of the faulty sensor can be replaced by the value of the other two sensors.

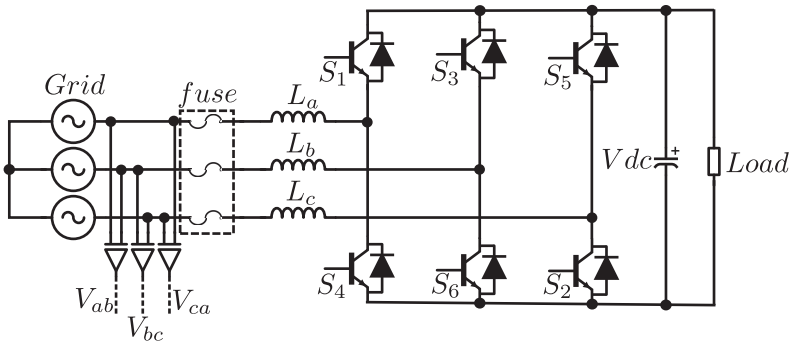


Figure 22. Three-phase AC/DC PWM PEC. Comparison of V_{ab}, V_{bc}, and V_{ca} with a threshold is performed, and the value of the other sensors replaces a faulty sensor signal.

In Ref. [62], the authors use a Luenberger observer built from a nonlinear model of the PEC. The algorithm improves reliability, preventing the system from tripping when sensor faults occur. The authors in Ref. [63] proposed a control strategy for coping with lacking AC voltage signal. This fault condition may be caused by a measurement fault or a communication malfunction.

A fault-tolerant supervisory controller for a hybrid AC/DC microgrid is proposed in Ref. [64]. In a hybrid microgrid, DC sources, energy storage, and loads are connected to the main bus, while AC sources and sinks are coupled to an AC main bus. The authors in Ref. [65] use a fault sensor detection method for single-phase PWM rectifiers in railway electric traction applications; this method is based on observers and residuals generation. The algorithm enables the detection and isolation of the faulty sensor.

In Ref. [86], the authors propose online estimation of the battery model parameters such as battery state of charge, voltage, and temperature. The charging response information of the model is compared with the actual to determine whether the charging process is normal. This method can identify more than ten types of faults, including the failure of the battery management system function.

2.6. Network-Level Fault Tolerance Techniques

Unbalanced three-phase grid voltages and loads can cause unexpected power ripples. These power ripples can result in current and voltage ripples in the output, possibly creating instability in the whole system, reducing its efficiency, or shortening the lifetime of DC sources (e.g., batteries). Once the three-phase unbalance problem occurs in the power supply and distribution system, it could cause damage to lines, transformers, and power equipment. Due to the above, several control solutions have been proposed. In Ref. [67], a control method for a line-side connected AC/DC converter operating under generalized unbalance conditions is presented. By nullifying the oscillating components of the instantaneous active power at the poles of the converter instead of the front-end, the output harmonics can be more effectively eliminated even under generalized unbalanced operating conditions (e_a–e_c). In Ref. [68], an active power filter is used to compensate for the unbalanced load of a three-phase system. This filter dramatically improves three-phase imbalance, compensates reactive power, and opposes harmonics.

The authors in Ref. [69] propose three methods to handle the unbalance, synchronous detection, power equality, and similar-current approaches. Their merit is the ability to operate in three-phase unbalanced systems by phase-wise calculation avoiding conversion errors. However, this method has several disadvantages as it requires additional hardware

to implement the algorithms, increasing its monetary cost. Recently, other proposals to control three-phase boost type converters with PWM rectifiers under unbalanced input voltage conditions have been proposed. In Ref. [70], the instantaneous power of the PWM rectifier in a two-phase steady-state converter is analyzed; three control methods, input power, input-output, and output power controllers, are proposed. Compared with the existing techniques, simplicity may be the most significant advantage of the method.

Control methods operating under balanced and unbalanced network conditions have become widely used. In Ref. [71], a simple control method based on direct power control (DPC) using space vector modulation (SVM) is proposed; the controller uses an extension of the original instantaneous power theory. After deriving the power slopes of both active and reactive power, the appropriate PEC voltage reference is analytically derived from canceling the dynamic energy and reactive power errors, which are subsequently synthesized by SVM. To improve the steady-state performance of rectifiers under non-ideal grid voltage conditions, the authors in Ref. [72] propose a multi-vector predictive power control (MV-MPPC) scheme. The proposed method features constant switching frequency and better steady-state control performance without increasing sampling frequency. The optimal vector range for active and reactive power regulation can be extended for arbitrary phase and magnitude by selecting active and zero vectors.

Power quality can be defined as measuring, analyzing, and improving the bus voltage to maintain a sinusoidal waveform at rated voltage and frequency and is elementary in a disturbance-free electrical network. An essential characteristic of power quality is the absence or treatment of undesirable harmonic components in the AC signals. In Ref. [73], a new stationary frame control scheme for three-phase rectifiers is proposed (Figure 23); the proposed control scheme regulates the instantaneous active power at the input (e_{abc}) and output (V_{dc}) of the converter to minimize such harmonics. The novelty of this research is the development of a new current-reference generator implemented directly in the stationary reference frame.

For the case of network peak voltage variations, the authors in Ref. [59] use Clarke's transform to separate positive and negative voltage sequences, and the model is also extended to harmonics; in the case of harmonic disturbances, an optimized regulation is presented. Together with identifying the network parameters, this line current compensation loop method offers an excellent solution to stabilize the PWM rectifier in an unbalanced network.

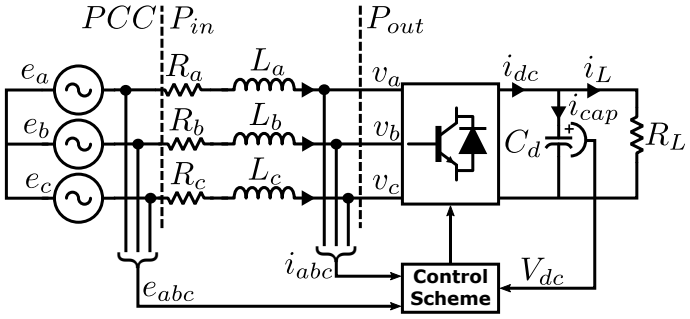


Figure 23. Schematic diagram of the power quality improvement scheme. The proposed control scheme regulates the instantaneous active power at the input (e_{abc}) and output (V_{dc}) of the converter to minimize the harmonics.

In Ref. [74], a control method that uses a virtual network flux and a fundamental voltage harmonic is presented; the method calculates the instantaneous reference power oscillations to maintain the sinusoidal current. Due to the number of devices connected to the power grid through power electronic converters, the stability of the power grid can be decrescent. Hence, a three-phase converter is proposed for grid recovery as a virtual synchronous generator (VSG). In Ref. [75], an MPC strategy for a virtual synchronous generator (MPC-VSG) is proposed. The MPC can automatically control the output power

of the converter despite grid frequency and voltage changes, providing fault-tolerant capabilities without a proportional-integral (PI) controller.

In Ref. [87], the authors investigate the winding design and configuration effect on the current quality of a six-phase-based non-isolated OBC. First, the relation between the winding design and the induced low order harmonics in the charging current is clarified. The proposed current controller structure ensures balanced grid line currents with high power quality under either healthy or one-phase fault conditions.

3. Comparison of Fault Tolerance Techniques

Tables 1–6 compare the techniques focusing on OBCs for electric vehicles from the above-presented research on fault tolerance. Power density, control complexity (computational burden), bidirectional capability, input voltage, output voltage, efficiency, required hardware reconfiguration, type of isolation, and additional devices are compared. This is to show the reader an updated and general perspective of the type of research that can encounter for the fault tolerance for OBCs and PECs.

Table 1 shows a comparison of the different switch-level fault-tolerance methods; values for power density and efficiency are also provided. The presented references demonstrate good performance for diverse uses, including OBCs; an advantage of some of these PECs is that they do not require hardware reconfiguration for fault tolerance, which improves the PEC efficiency, power density, and cost. However, in general, the control method becomes complex, causing the fault to take longer to be detected. Most importantly, fault tolerance by the control method is limited to three-phase AC-DC converters, and the power quality detriment by phase unbalance is considerable. Comparatively, hardware reconfiguration at the switch level is faster but has higher cost and volume; also, dynamics during switching at failure conditions must be analyzed since these shortcomings are not easy to reproduce. Even more, the increase in the number of devices causes the efficiency and power density of the PEC/OBC to decrease. For OBCs, the fault has to be detected and isolated quickly; although [14–17] are a good starting point to catch and handle faults efficiently, hardware quality and good algorithms are crucial. It is important to note that only three proposals use a three-phase bidirectional converter that can be used in OBCs, but OBCs should operate in one, two, or three phases to be versatile. Hence, switch-level fault tolerance for isolated, reconfigurable single, dual, or three-phase feeding is an open problem. Note that a possible advantage of switch-level against leg-level hardware fault tolerance could be a reduced number of additional devices since only some must be redundant instead of all legs.

Table 2 compares the fault-tolerant at leg level techniques. It is observed that most of the references also propose additional devices to operate, thus decreasing the power density. Despite the above, using a redundant leg in parallel is one of the most useful fault-tolerant solutions at a hardware level, instead of coping with only a switch failure (maybe at the same cost). Combining the faulty leg to the midpoint of the DC bus and two-phase control, widely used in motor drives, optimizes the design and reduces the cost. Still, bidirectional PECs that can charge with single, dual, and three-phase sources are an open problem. Attention is caught by the fact that few authors consider galvanic isolation, and for a Level 1 or Level 2 charge it seems a little-studied promising safety alternative for domestic users. Note that most leg-level fault-tolerance techniques involve a high computational burden; many of these can be synthesized in FPGA implementations to improve response and dynamical switching behavior.

Table 1. Comparison of the different fault-tolerant switch-level techniques.

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[5]	300	High	Speed/current control	No	200–280 VAC (3ϕ)	101 VDC	85–90%	No	No	0	3ϕ AC-DC
[6]	150	High	Current control	No	220 VAC (3ϕ)	400 VDC	80–85%	No	No	0	3ϕ AC-DC
[7]	180	High	Voltage control	No	220 VAC (3ϕ)	400 VDC	80–85%	No	No	0	3ϕ AC-DC
[8]	50	Medium	Current control	No	60 VAC (3ϕ)		86%	No	No	0	3ϕ AC-DC
[9]	150	Medium	PI	No	100 VAC (3ϕ)	200 VDC	85%	No	No	0	Vienna Rectifier
[10]	60	High	Neutral point control	No	100 VDC	200–250 VAC (3ϕ)	85–90%	No	No	0	T-Type 3-Level Inverter
[11]	20	Medium	PI	Yes	50 VAC (3ϕ)	60 VAC (3ϕ)	82%	Yes	No	6	Reverse Matrix
[12]	25	Low	PI	No	300 VDC	380 VAC (3ϕ)	86%	Yes	No	1	3ϕ inverter
[13]	150	Medium	Voltage oriented control	No	200-250 VAC (3ϕ)	600 VDC	80–85%	No	No	0	3ϕ AC-DC
[14]	50	High	Predictive control	No	50 VAC (3ϕ)	200 VDC	80–85%	Yes	No	3	3ϕ AC-DC
[15]	25	High	Predictive control	Yes	50 VAC (3ϕ)	200 VDC	80–85%	Yes	No	3	3ϕ AC-DC
[16]	500	High	Current control	Yes	690 VAC (3ϕ)	1200 VDC	85%	Yes	No	5	3ϕ AC-DC
[17]	30	High	Voltage oriented control	Yes	50 VAC (3ϕ)	300 VDC	90%	Yes	No	3	Back-to-Back
[18]	10	Medium	PI	No	30 VAC (3ϕ)	200 VDC	85–90%	No	No	0	3ϕ AC-DC
[19]	108	Medium	Voltage/current control	No	220 VAC (3ϕ)	380 VDC	80–85%	Yes	No	2	3ϕ Bridgeless Rectifier
[20]	250	Low	Fuzzy	No	11 kVAC (3ϕ)	20 kVDC	90–95%	Yes	No	5	3ϕ AC-DC
[83]	60	Low	Lead-lag compensator	No	10 VDC	5 VDC	90–95%	No	No	0	Buck

Table 2. Comparison of the different fault-tolerant leg-level techniques.

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[21]	60	High	FSMPPC	Yes	110 VAC (3ϕ)	400 VDC	80–85%	Yes	Galvanic	3	2-stage AC-DC
[22]	32	Medium	Predictive torque control	No	280 VAC (3ϕ)	540 VAC (3ϕ)	85%	Yes	No	3	Nonredundant inverter
[23]	250	High	Direct torque control	No	300 VDC		86%	Yes	No	4	3ϕ Inverter
[24]	222	Low	PI, BC, and SMC	Yes	230–440 VAC (3ϕ)	600 VDC	85–90%	Yes	No	3–5	3ϕ AC-DC
[25]	30	High	PI	Yes	150 VDC	100 VAC (3ϕ)	80–85%	Yes	No	6	Dual Inverter
[26]	22	High	DQ control	Yes	300 VDC	250 VDC	80–85%	Yes	No	3	Hybrid Inverter
[27]	30	High	Model Predictive Control	Yes	50 VAC (3ϕ)	540 VDC	80–90%	Yes	No	6	Back-to-Back
[28]	60	Medium	Voltage oriented control	Yes	250 VAC (3ϕ)	150 VDC	80%	No	No	0	3ϕ Back-to-Back
[29]	500	High	Voltage oriented control	Yes	200 VAC (3ϕ)	400 VDC	85%	Yes	No	8	6-Leg AC-DC-AC
[30]	100	Medium	PI	No	30 VAC (3ϕ)	500 VAC (3ϕ)	80%	Yes	No	8	PWM AC-DC-AC
[31]	120	High	Voltage oriented control	No	60 VAC (3ϕ)	50 VAC (3ϕ)	80–90%	Yes	No	9	5-Leg Converter
[32]	60	Medium	PI	No	120 VAC (3ϕ)	48 VDC	80%	Yes	Galvanic	5	3ϕ Isolated AC-DC
[33]	20	High	Voltage control	Yes	400 VAC (3ϕ)	196 VDC	80%	Yes	Galvanic	3	3ϕ Bidirectional AC-DC
[34]	300	High	HSVM	No	110 VAC (3ϕ)	600 VDC	80–85%	Yes	No	3	3ϕ Rectifier
[35]	70	High	MPC	Yes	400 VDC	110 VAC (3ϕ)	80–85%	Yes	No	3	Bidirectional AC-DC
[36]	50	High	FSMPPC	Yes	50 VAC (3ϕ)	300 VDC	80%	Yes	No	3	3ϕ Bidirectional AC-DC
[37]	85	High	MPC	Yes	400 VDC	70 VAC (3ϕ)	80%	Yes	No	3	3ϕ Four-Switch

Table 2. *Cont.*

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[38]	120	Medium	MPDPC	No	250 VAC (3ϕ)	350 VDC	85%	Yes	No	3	2-Level Back-to-Back
[39]	80	Medium	MPDPC	Yes	190 VAC (3ϕ)	400 VDC	80–85%	Yes	No	3	3ϕ Bidirectional AC-DC
[40]	100	Medium	MPDPC	Yes	190 VAC (3ϕ)	400 VDC	85%	Yes	No	3	Bidirectional AC/DC
[41]	50	High	FSMPPC	Yes	50 VAC (3ϕ)	300 VDC	85%	Yes	No	3	Bidirectional AC/DC
[42]	40	Medium	Current control	No	140 VAC (3ϕ)	230-280 VDC	80–85%	No	No	0	3ϕ 2-Level
[43]	40	Medium	Current control	No	140 VAC (3ϕ)	230-280 VDC	80–85%	No	No	0	3ϕ 2-Level
[44]	230	Medium	Current control	No	300 VDC	277 VAC (3ϕ)	80%	No	No	0	DC-AC

Table 3. Comparison of the different fault-tolerant module-level techniques.

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[45]		High	Current control	No	110 VAC (3ϕ)	220 VAC (3ϕ)	85%	No	No	0	Matrix
[46]	50	High	FCS-MPC	No	60 VAC (3ϕ)	60 VAC (3ϕ)	70-80%	No	No	0	Matrix
[47]	60	Medium	Voltage oriented control	No	220 VAC (3ϕ)	110 VAC (3ϕ)	80–85%	No	No	0	Matrix
[48]	70	Low	Voltage control	No	300 VAC (3ϕ)	500 VAC (3ϕ)	80–90%	Yes	No	3	Matrix
[49]	70	Low	Current control	No	300 VAC (3ϕ)	500 VAC (3ϕ)	85–90%	Yes	No	1	3ϕ Matrix

Table 3. *Cont.*

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[50]	125	High	Voltage/current control	No	300 VAC (3ϕ)	100 VAC (3ϕ)	85%	No	No	0	Matrix
[51]	86	High	Voltage control	No	60 VAC (3ϕ)	400 VDC	80%	No	No	0	3ϕ 3-Level Rectifier
[52]	67	Medium	PI	No	200 VDC	100 VAC (3ϕ)	85–90%	No	No	0	3-Level Inverter
[53]	100	Medium	Phase control	No	50 VAC (3ϕ)	150 VDC	85%	No	No	0	3-Level Rectifier
[54]	20	Medium	Voltage control	No	200 VDC	70 VAC (3ϕ)	85%	No	No	0	Multilevel converter
[55]	300	Medium	PI	No	9 kVDC	5 kVAC (3ϕ)	86%	No	No	0	Modular Multi-Level
[56]	400	Medium	CCSSE, ICCO ACC	No	200 kVDC	100 kVAC (3ϕ)	85–90%	No	No	0	Modular Multi-Level
[57]	500	Medium	DIOC	No	400 kVAC (3ϕ)	400 kVAC (3ϕ)	75–80%	No	No	0	Modular Multi-Level
[58]	100	Medium	Voltage control	No	60–250 VDC	12–18 VDC	80–90%	No	Galvanic	0	Modular
[84]	700	High	Voltage oriented	Yes	300 VAC (3ϕ)	200 VDC	85–90%	No	No	0	Twelve-Leg Inverter
[88]	300	Medium	PI	Yes	120 VAC (1ϕ)	250 VDC	85–90%	No	No	0	1ϕ Rectifier

Table 4. Comparison of the different fault-tolerant system level techniques.

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[78]	600	High	DC voltage compensation	No	220 kVDC (3ϕ)	300 kVDC	80–90%	No	Galvanic	0	Parallel Hybrid Multilevel
[79]	80	Low	PI	No	50 VAC (3ϕ)	180 VDC	80–90%	No	Galvanic	0	Parallel Hybrid Modular Multilevel
[80]	600	Medium	PI	Yes	128 kVAC (3ϕ)	200 kVDC	75–80%	No	Galvanic	0	Parallel Hybrid
[81]	250	High	Current control	No	80 VAC (3ϕ)	130 VDC	80%	No	No	0	3ϕ 2-Parallel AC-DC
[82]	700	Medium	DPC-SVM	No	35 kVAC (3ϕ)	1200 VDC	86%	No	No	0	2-Parallel DC-AC
[85]	500	Medium	DQ Control	Yes	375 VDC (3ϕ)	800 VDC	90–95%	No	No	0	Buck-Boost

Table 5. Comparison of the different fault-tolerant measurement-level techniques.

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[60]	300	Low	Transient current control	No	1550 VAC (1 ϕ)	2700-3600 VDC	80–85%	No	No	0	PWM Rectifier
[61]	100	Low	PI	No	200 VAC (3ϕ)	400 VDC	80–85%	No	No	0	3ϕ AC-DC
[62]	110	Low	PI	No	220 VAC (3ϕ)	360 VDC	80–90%	No	No	0	3ϕ AC-DC-AC
[63]	800	Medium	MTDC	No	110 kVAC	400 kVDC	88%	No	No	0	Multi-Terminal High-Voltage
[64]	150	Low	Sliding modes controller	No	600 VAC (3ϕ)	380 VDC	80–90%	No	No	0	Hybrid AC-DC
[65]	180	Low	PI control	No	220 VAC (3ϕ)	400 VDC	70-80%	No	No	0	1-Phase PWM Rectifier
[66]	140	Low	Adaptive control	No	100 VDC	220 VDC	80–90%	No	No	0	PWM Inverter
[86]				No		350 VDC	80–90%	No	No	0	3ϕ AC-DC

Table 6. Comparison of the different fault-tolerant network-level techniques.

Refs.	Power Density, W/in^3	Control Complexity	Control	Bidi.	Input Voltage	Output Voltage	Efficiency	Hardware Reconfig.	Iso.	Addl. Devs.	Topology
[67]	100	High	PI	No	140 VAC (3ϕ)	400 VDC	85%	No	No	0	PWM AC/DC
[68]	140	Medium	Active power filter (APF)	No	380 VAC (3ϕ)	720 VDC	80–90%	No	No	0	3ϕ AC-DC
[69]	100	Medium	Current compensation	No	110-80 VAC (3ϕ)		90-95%	No	No	0	3ϕ AC-DC
[70]	100	Medium	Input power control, input-output power control, and output power control.	No	160 VAC (3ϕ)	300 VDC	75–80%	No	No	0	3ϕ AC-DC
[71]	100	Medium	Direct power control	No	150 VAC (3ϕ)	300 VDC	80%	No	No	0	2-Level PWM Rectifier
[72]	130	High	MV-MPPC	No	110 VAC (3ϕ)	300 VDC	85%	No	No	0	3ϕ Rectifiers
[73]	250	Medium	SFCS	No	300 VAC (3ϕ)	700 VDC	80–90%	No	No	0	3ϕ Rectifiers
[59]	100	Medium	Voltage/current control	No	50 VAC (3ϕ)	150 VDC	80%	No	No	0	PWM Rectifiers
[74]	190	Medium	Direct power control	No	230 VAC (3ϕ)	390 VDC	86%	No	No	0	3ϕ AC-DC
[75]	160	High	Model predictive control	No	110 VAC (3ϕ)	400 VDC	85–90%	No	No	0	3ϕ AC-DC
[76]	150	High	PI	No	200 VDC	230–400 VAC (3ϕ)	85–90%	Yes	No	2	3ϕ Inverter
[77]	130	Low	PI	No	100 VAC (3ϕ)	200 VDC	80%	No	No	0	3ϕ AC-DC
[87]	1500	High	Current control	No	110 VAC (3ϕ)	270 VAC (3ϕ)	80–90%	No	No	0	3ϕ Inverter

In Tables 3 and 4, module and system-level converters are good options for managing an entire module fail and switch and leg level faults. Advantages of these are that control methods are uncomplicated and easy to implement [52–58]. These are ideal characteristics for critical or industrial applications with very high power transfer. However, due to the high number of additional devices in the MMC/CMC, one can discard them for OBCs due to the weight and higher mass production cost. Despite the above, one can note that bidirectionality is absent at modular PECs (and very scarce for system-level configurations) and could be attractive research for other MIMO uses.

Fault-tolerant methods based on the measurement level are compared in Table 5. It is worth noting that few literary works on the topic could be found, and these techniques could be easily combined with any other fault-tolerant approach. Their complexity is low, and none were designed for bidirectional/isolated PECs. Even more, advanced deep learning models can be designed to predict and classify failure with minimal error.

Power quality issues are quite common, especially in domestic AC systems. Although is not the objective of this review to deepening on power quality enhancement on PECs, some relevant references are compared in Table 6. These compared references are good choices for OBCs in combination with other fault-tolerant techniques at the switch, leg, or module level; they do not require hardware reconfiguration or additional devices and are compatible with OBC controllers. Note that there are scarce single or dual-phase PEC fault-tolerant network-level techniques; smart grids and microgrids generally include those subsystems.

4. Discussion

As mentioned in the introduction, diverse PECs with fault-tolerant capabilities have been proposed in the literature. These strategies can be classified into six categories, switch, leg, module, system, measurement, and network levels. While hardware redundancy is relatively standard at almost all levels, fault tolerance at a network level has been widely addressed, from prediction to automated interconnection with smart and microgrids. Diverse systems allow coping with power quality issues, from ripple and harmonic minimization to uninterruptible power systems. Indeed, updated classifications and reviews on network-level issues are nowadays open problems. Additionally, studies on the diverse causes of PEC faults could be a call for designing robust production devices.

Most PEC/OBC topologies are characterized by using additional devices for operation such as switches and, in some cases, passive components such as capacitors. Indeed, there is a tendency to develop switched-capacitor inductor-less PECs. However, research on fault detection and reconfiguration for passive devices is insufficient; especially, electrolytic capacitors are prone to die back from diverse causes, damaging active components such as MOSFETs, IGBTs, and TRIACs in PECs.

A particular scenario is presented for asymmetric converters in which series or parallel stages have different energy transfer capabilities. In such systems, hardware redundancy must consider that duplicative stages (switch, level, or module) may be incompatible with some asymmetric circuits. One can also note that bidirectionality is absent at modular PECs (and very scarce for system-level configurations) and could be attractive research for other MIMO uses with fault tolerance.

On the other hand, fault tolerance for OBCs operating in single, dual, or three-phase systems must be further analyzed since they are increasing due to their versatility. Power quality, automated reconfiguration, hardware redundancy, and measurement fault tolerance are possible research directions for smart grid scenarios. It is worth noting that isolation is a safety premise. Most of the PECs/OBCs presented here do not prevent unwanted current from flowing between two units sharing a ground conductor.

Another little-researched phenomenon is the dynamics during the switching to redundant hardware at failure conditions. It is well known that switched systems can be unstable even if their subsystems are globally stable because of the commutation state jump. This represents an exciting challenge since some shortcomings producing failures in PECs/OBCs are not easy to be experimentally reproduced.

FPGA implementations must be studied to handle fault-tolerance techniques. This could allow the central controller or supervisor to decentralize fault-tolerance tasks in cooperative/distributed systems.

Some fault-tolerant methods could be unified in a single system to increase the fault-tolerance capability in an OBC. For instance, the proposals [5,40,75] can be combined since the fault detection and tolerance methods are compatible with a predictive control method in a bidirectional converter topology tolerant to leg-level faults. As another example, the strategies in Refs. [40,75] can be used altogether since the same control method is used. In the same way, Refs. [6,76] can be combined for both switch level faults and leg level faults and phase unbalance conditions preserving the number of devices and hence efficiency. Refs. [7,23,72] can also perform together since [7,23] use similar control methods, and the technique presented in Ref. [72] uses model predictive control, making it a good choice for network-level faults. The works presented in Refs. [8,32,77] are also excellent options to combine in a single fault-tolerant converter. All measurement-level techniques can be combined with the rest of the methods. Finally, one can exchange control strategies for fault tolerance to compare and gain in performance, production cost, PEC efficiency, et cetera.

5. Conclusions

This paper presents a review of the different fault-tolerant techniques in power electronic converters that could be used for OBcs. Fault-tolerant solutions are always associated with hardware redundancy and control strategies, but other types can also occur. Therefore, the different fault-tolerant techniques are classified into switch level, leg level, measurement level, network level, module level, and system level. Several representative approaches are presented, and different fault-tolerant methods are discussed. For OBCs, many fault-tolerant converters are good choices since they demonstrate effective operation for various faults. Much research can be directed for fault tolerance from single electronic devices to the entire system; new OBCs and fault-tolerant techniques for them are emerging, so there is a vast work field, and here are presented only some of the most obvious.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
ACC	Arm Current Control
BJT	Bipolar Junction Transistor
BC	Backstepping
CMC	Cascaded Multilevel Converters
CCSSE	Circulant Current Specific Sequence Elimination Method
DC	Direct Current
DPWM	Discontinuous Pulse Width Modulation
DIOC	Dynamic Interval Overcurrent Control
DFIG	Doubly Fed Induction Generator
DPC	Direct Power Control
DSP	Digital Signal Processing

DPCSVM	Direct Power Control-Space Vector Modulation
EV	Electric Vehicle
EMTDC	Electromagnetic Transients including DC
FD	Fault Detection
FTC	Fault-Tolerant Control
FCS-MPC	Finite Control Set-Model Predictive Control
FPGA	Field Programmable Gate Arrays
FSMPPC	Finite State Model Predictive Power Control
FTCU	Fault-Tolerant Control Unit
FB-MMC	Full-Bridge Modular Multilevel Converters
HVDC	High-Voltage Direct Current
HEV	Hybrid Electric Vehicle
HBSVM	Hybrid Space Vector Modulation
HBSM	Half-Bridge Submodules
IGBT	Insulated Gate Bipolar Transistor
IM	Induction Motor
ICCO	Instantaneous Circulating Overcurrent Control
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MMC	Modular Multilevel Converters
MPC	Model Predictive Control
MPDPC	Model Predictive Direct Power Control
MCT	Marine Current Turbine
MC	Matrix Converters
MSPDDC	Modular Series-to-Parallel DC-DC Converters
MPHC	Modified Parallel Hybrid Converter
MV-MPPC	Multi-Vector Model Predictive Power Control
MPC	Model Predictive Control
MPC-VSG	Model Predictive Control-Virtual Synchronous Generator
MPDPC	Model Predictive Direct Power Control
MIMO	Multi-Input-Multi-Output
MTDC	Multi-Terminal High-Voltage Direct Current
NPC	Neural Point Clamping
OBCs	Onboard Charging systems
OW-PMSM	Open-end Winding Permanent Magnet Sync Motor
PEC	Power Electronic Converters
PHEV	Plugin Hybrid Electric Vehicles
PHMC	Parallel hybrid multilevel converter
PWM	Pulse Width Modulation
PMSM	Permanent Magnet Sync Motor
PDPWM	Phase Disposition Pulse Width Modulation
PHMC	Parallel Hybrid Multilevel Converter
PSCAD	Power System Computer-Aided Design
pu	Percent Unit
PI	Proportional-Integral
PLL	Phase-Locked Loop
PMSG	Permanent Magnet Synchronous Generator
SCR	Silicon Controlled Rectifier
SFCS	Stationary Frame Control Scheme
SMC	Sliding Mode Control
SOC	State of Charge
SPWM	Sinusoidal Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
SVM	Space Vector Modulation
TRIAC	Triode for Alternating Current
VSG	Virtual Synchronous Generator
VSI	Voltage Source Inverter
WECS	Wind Energy Conversion Systems

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