electronics

MDPI

Article

Modeling and Analysis of Voltage Ripple-Controlled SIDO Buck Converter in Pseudo-Continuous Conduction Mode with Limited Cross-Regulation and Fast Load Transient Performance

Haoyu Jiao, Mingzhi He *, Pan Feng and Shuhan Zhou

College of Electrical Engineering, Sichuan University, Chengdu 610044, China; jiaohaoyu@stu.scu.edu.cn (H.J.); 2019141440045@stu.scu.edu.cn (P.F.); shuhanzhou92@gmail.com (S.Z.)
* Correspondence: darmyhe@vip.126.com

Abstract: Typical voltage mode-controlled DC–DC converters with single-inductor dual-output (SIDO) in pseudo-continuous conduction mode (PCCM) have slow load transient performance, and cross-regulation still exists between their two outputs. For the purposes of suppressing the cross-regulation and improving the load transient performance, a voltage ripple control technique for a PCCM SIDO buck converter is proposed in this study. A description of the PCCM SIDO buck converter and the voltage ripple control technique is provided in detail. In addition, the small-signal model was established, and the cross-regulation was further compared by Bode plots, as well as the load range and the power losses being analyzed. The cross-regulation and load transient performance of the voltage ripple-controlled PCCM SIDO buck converter was studied and compared with the conventional voltage mode-controlled. Using the proposed voltage ripple control for PCCM SIDO buck converters, we found no cross-regulation or rapid load transient behavior, which was validated by experimental results.

Keywords: single-inductor dual-output converter; pseudo-continuous conduction mode; voltage ripple control; cross-regulation; load range; efficiency

Citation: Jiao, H.; He, M.; Feng, P.; Zhou, S. Modeling and Analysis of Voltage Ripple-Controlled SIDO Buck Converter in Pseudo-Continuous Conduction Mode with Limited Cross-Regulation and Fast Load Transient Performance. *Electronics* **2022**, *11*, 1731. https://doi.org/10.3390/electronics11111731

Received: 2 May 2022
Accepted: 27 May 2022
Published: 30 May 2022

1. Introduction

For portable electrical devices, single-inductor multiple-output (SIMO) DC–DC converters can offer a cost-effective, high-reliability, and high-integrity solution [1–4] that can provide different supply voltage levels for different function modules. However, since all the outputs share one inductor, they are affected by a mutual cross-regulation when the system operates in continuous conduction mode (CCM) [2–9]. This has a drastic impact on the stability and performance of the system, both in the steady state and transient operations [4–7]. In addition, compared with the traditional single-input single-output (SISO) DC–DC converter, the system becomes more complex to operate, control, and design since all outputs are coupled through one single power switch.

Many studies focus on new control schemes that address the cross-regulation issue of a CCM SIMO DC–DC converter. For example, Wang et al. [6] proposed a deadbeat-based control that solved the cross-regulation problem and was capable of regulating both the input current and the output voltage at the same time. In [7,8], the capacitor current control was applied to a CCM single-inductor dual-output (SIDO) buck converter, and the cross-regulation was effectively suppressed under the influence of its fast transient response. Dong et al. [9] proposed a DC–DC converter topology based on the current-source mode SIMO for a light-emitting diode driver, which realized the decoupling of all individual dimming controls. Despite the benefits of suppressing the cross-regulation for a CCM SIDO DC–DC converter, it could not be eliminated completely.

To cancel cross-regulation, the single-inductor dual-output (SIDO) DC–DC converter in discontinuous conduction mode (DCM) was introduced in [10–12]. After discharging

into the appropriate output, the inductor current became zero, which ensured each output was isolated from the load changes in other outputs. This enabled each output to be controlled independently, thereby overcoming the effects of cross-regulation. However, under heavy loads, the SIDO DC–DC converter suffered a large ripple in the inductor current and a output voltage ripple when operating in DCM, which severely impaired the switching noise and dynamic response performance of the converter.

A pseudo-continuous conduction mode (PCCM) for a SIDO DC–DC converter was proposed in [13]. The circuit diagram and operating waveforms of the PCCM SIDO buck converter are illustrated in Figure 1. After the current was charged and discharged in the inductor, the converter entered a freewheeling interval. Since the starting and ending inductor current were both equal to the freewheeling current I_{dc}, the load change in one output did not affect the other output. It only changed the freewheeling interval. The cross-regulation can be absolutely suppressed in theory.

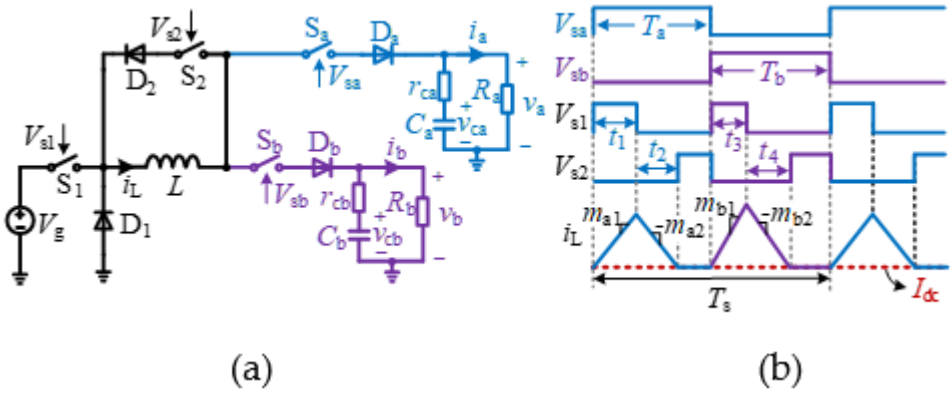

Figure 1. Power stage (**a**) and operation waveforms (**b**) of PCCM SIDO buck converter.

However, in the presence of a DC offset current, the additional freewheeling switch will cause unnecessary power loss during the freewheeling period. There are a lot of researchers investigating techniques for an adaptive freewheeling current control to overcome this problem [14–16]. Woo et al. [14] proposed a new control technique for a freewheeling current control, that is, to adjust the output voltage through the operation of the comparator and control the average feedback of the freewheeling current to a reference level. A SIMO converter with a linear regulator based on error control was introduced in [15]. Using this scheme, the switching frequency and switching sequence of the output power switches were controlled arbitrarily according to each error, and high efficiency and regulation stability under a light load were achieved at the same time. A hybrid-mode control method of a single freewheel phase was proposed, which could achieve the reduction of switching loss and the minimization of cross-regulation [16]. In the above-referenced literature, the simulation and experimental results indicated that the cross-regulation still exists in PCCM SIDO DC–DC converters. In the literature, the common way to control the main switch is conventional voltage mode control, which leads to a slow load transient performance, impeding the cross-regulation suppression. Thus, it is necessary to investigate an effective control technique for a PCCM SIDO DC–DC converter to absolutely restrain the cross-regulation.

The voltage ripple control technique is widely used in conventional single-inductor single-output (SISO) DC–DC converters, owing to its fast load transient response and simple design [17,18]. However, it is not used in SIDO DC–DC converters. Although the circuit topology of a SIDO DC–DC converter does not seem complex, when compared with the traditional SISO DC–DC converter, the functional interdependencies and the circuit operation among basic converter parameters, such as output voltage, power switches, duty cycle, and load current magnitude, are much more complex. Moreover, the small-signal model, transient analysis, and efficiency analysis of SIDO DC–DC converter are more complex. In this study, a voltage ripple control technique of suppressing the cross-regulation is

proposed to improve the transient performance of a PCCM SIDO buck converter, which is significant for the application of the converter.

The rest of this paper is organized as follows. Section 2 illustrates the operation principle of the PCCM SIDO buck converter and its state equations. The voltage ripple control technique for the PCCM SIDO buck converter is proposed, and its control constraint equations are performed. In Section 3, the small-signal model is established, and its cross-regulation is analyzed using Bode plots. The load range and efficiency are analyzed in detail in Section 4. Experimental results are given to verify the theoretical analysis in Section 5, where the load transient performance of the proposed voltage ripple-controlled and conventional voltage mode-controlled PCCM SIDO buck converters are compared. In addition, the load range and the efficiency are presented. Section 6 summarizes the conclusion of this paper.

2. Proposed Voltage Ripple Control for PCCM SIDO Buck Converter

2.1. Operation Principle of PCCM SIDO Buck Converter

As shown in Figure 1a, one main switch S_1, one freewheeling switch S_2, two output switches S_a and S_b, four diodes D_1, D_2, D_a, and D_b, one inductor L, and two output capacitors C_a and C_b with their ESRs r_{ca} and r_{cb} form the PCCM SIDO buck converter together. The voltages of C_a and C_b are v_{ca} and v_{cb}, respectively. The output currents of output A and output B are i_a and i_b, respectively. Figure 1b shows its operating waveforms, where I_{dc} is a freewheeling current; i_L is the inductor current; m_{ai} and m_{bi} (i = 1, 2) are the increasing and decreasing slopes of the inductor current for outputs A and B, respectively; T_s is the switching period; T_a and T_b are the working times of outputs A and B, respectively; and V_{s1}, V_{s2}, V_{sa}, and V_{sb} are the driver pulse signals corresponding to S_1, S_2, S_a, and S_b, respectively. S_a and S_b are complementary conducted.

In one switching cycle, there are six operation modes for PCCM SIDO buck converter. Its corresponding equivalent circuits are shown in Figure 2. When V_{sa} = 1, S_a turns on and S_b turns off, the inductor works in output A. There are three operation modes. Otherwise, the inductor works in output B, and there are three operation modes too.

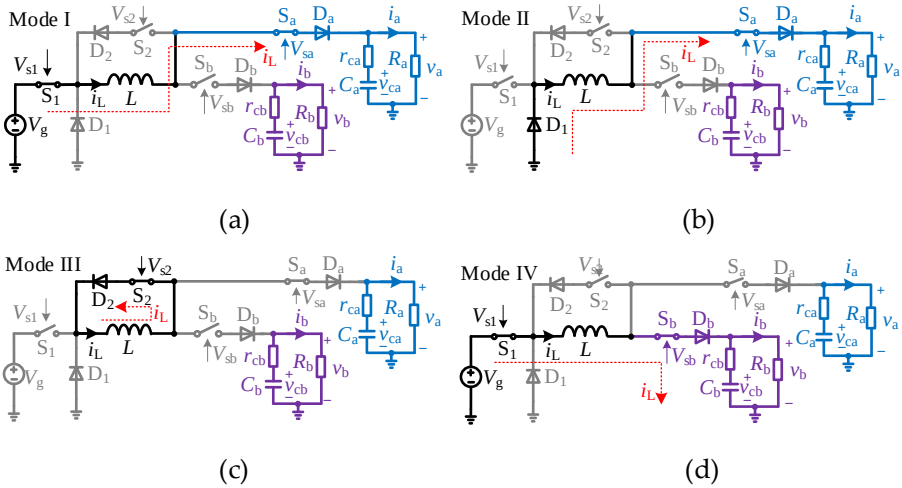

Figure 2. *Cont.*

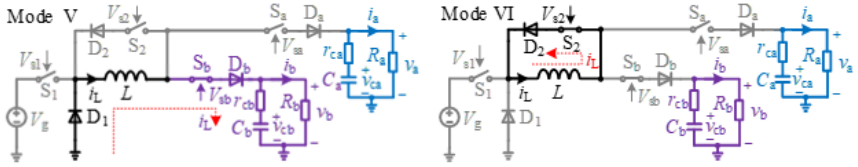

Figure 2. Equivalent circuits for PCCM SIDO buck converter: (**a**) Mode I: Charging interval of output A; (**b**) Mode II: Discharging interval of output A; (**c**) Mode III: Freewheeling interval of output A; (**d**) Mode IV: Charging interval of output B; (**e**) Mode V: Discharging interval of output B; (**f**) Mode VI: Freewheeling interval of output B.

(1) Mode I: Charging interval t_1. In this mode, S_a and S_1 are turned on, and S_2 is off. i_L increases with slope $m_{a1} = (V_g - V_a)/L$. D_1 is reverse biased, and D_a is forward conducted. C_a is charged, while C_b is discharged to provide power for the output B. At the end of this interval, the inductor current i_{n1} and capacitor voltages v_{can1} and v_{cbn1} are derived as:

$$\begin{cases} i_{n1} = i_n + m_{a1}t_1 \\ v_{can1} = v_{can} + (i_n - i_a)t_1/C_a + m_{a1}t_1^2/(2C_a) \\ v_{cbn1} = v_{cbn} - i_b t_1/C_b \end{cases} \tag{1}$$

(2) Mode II: Discharging interval t_2. S_1 is turned off, and both D_1 and D_a are forward biased. i_L decreases with slope $m_{a2} = V_a/L$. C_a and C_b are discharged to provide power for the appropriate outputs. Similarly, at the end of this operation mode, the inductor current i_{n2} and capacitor voltages v_{can2} and v_{cbn2} are:

$$\begin{cases} i_{n2} = i_{n1} - m_{a2}t_2 \\ v_{can2} = v_{can1} + (i_{n1} - i_a)t_2/C_a - m_{a2}t_2^2/(2C_a) \\ v_{cbn2} = v_{cbn1} - i_b t_2/C_b \end{cases} \tag{2}$$

(3) Mode III: Freewheeling interval. The freewheeling switch S_2 is switched on to short out the inductor. D_1 and D_a are reverse biased. i_L stays constant at I_{dc}. This freewheel interval could be used to isolate two outputs. The inductor current i_{n3} and capacitor voltages v_{can3} and v_{cbn3} are obtained as:

$$\begin{cases} i_{n3} = i_{n2} = I_{dc} \\ v_{can3} = v_{can2} - (T_a - t_1 - t_2)i_a/C_a \\ v_{cbn3} = v_{cbn2} - (T_a - t_1 - t_2)i_b/C_b \end{cases} \tag{3}$$

When $V_{sb} = 1$, S_a is switched off, while S_b is switched on. The inductor works in output B. There are also three operation modes, which are similar to output A. The inductor current and capacitor voltages are deduced as follows:

$$\text{Mode IV}: \begin{cases} i_{n4} = i_{n3} + m_{b1}t_3 \\ v_{can4} = v_{can3} - i_a t_3/C_a \\ v_{cbn4} = v_{cbn3} + (i_{n3} - i_b)t_3/C_b + m_{b1}t_3^2/(2C_b) \end{cases} \tag{4}$$

$$\text{Mode V}: \begin{cases} i_{n5} = i_{n4} - m_{b2}t_4 \\ v_{can5} = v_{can4} - i_a t_4/C_a \\ v_{cbn5} = v_{can4} + (i_{n4} - i_b)t_4/C_b - m_{b2}t_4^2/(2C_b) \end{cases} \tag{5}$$

$$\text{Mode VI}: \begin{cases} i_{n+1} = i_{n5} = I_{dc} \\ v_{ca(n+1)} = v_{can5} - (T_b - t_3 - t_4)i_a/C_a \\ v_{cb(n+1)} = v_{cbn5} - (T_b - t_3 - t_4)i_b/C_b \end{cases} \tag{6}$$

where $m_{b1} = (V_g - V_b)/L$, $m_{b2} = V_b/L$, t_3 is the charging interval for output B, and t_4 is the discharging interval for output B.

When referencing Equations (1)–(6), the expressions of i_L, v_{ca} and v_{cb} at the beginning of the $(n + 1)$-th switching cycle for the PCCM SIDO buck converter are easily obtained.

2.2. Operation Principle of the Proposed Voltage Ripple-Controlled PCCM SIDO Buck Converter

Figure 3a shows the control loop of the proposed voltage ripple-controlled PCCM SIDO buck converter, from which we can see that the main switch S_1 is managed by voltage ripple control, and the freewheeling switch S_2 is managed by constant reference current control. The output switches S_a and S_b are complementary controls. This converter has a stable switching frequency using pulse-width modulation. The control circuit of S_1 consists of two error amplifiers EA_1 and EA_2, two comparators CMP_1 and CMP_2, two RS triggers RS_1 and RS_2, and one selector S. The controller of S_2 is composed of one comparator CMP_3 and one RS trigger RS_3. The S_a and S_b are controlled by a D trigger and clock signal named clk.

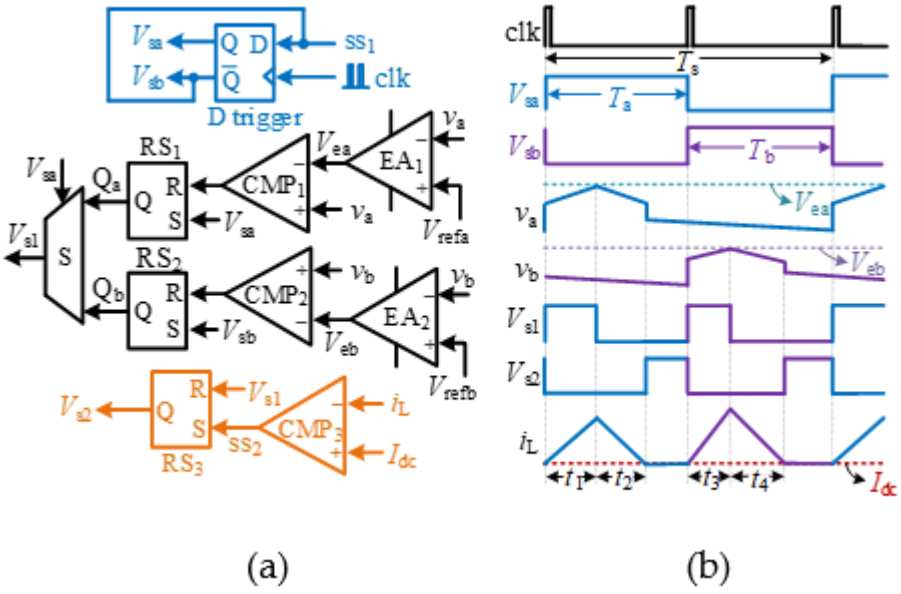

Figure 3. Voltage ripple-controlled PCCM SIDO buck converter: (**a**) control block diagram; (**b**) operation waveforms.

Upon the initial moment of each output operation, S_1 is turned on first. The $CMP_{i(i=1,2)}$ compares $V_{ei(i=a,b)}$ with $v_{i(i=a,b)}$ to generate reset signals for RS_1 and RS_2, respectively, where V_{ea} and V_{eb} are the compensated error voltages between each output $v_{i(i=a,b)}$ and reference voltage $V_{refi(i=a,b)}$, respectively. Q_a and Q_b are the output signals of RS_2 and RS_3. When $V_{sa} = 1$, Q_a is selected by S (i.e., $V_{s1} = Q_a$), and V_a is regulated to V_{refa}. When V_a increases to V_{ea}, the output of CMP_1 resets RS_1, and S_1 is turned off. Similarly, when $V_{sa} = 0$, Q_b is selected (i.e., $V_{s1} = Q_b$), V_b is regulated to V_{refb}. When v_b increases to V_{eb}, the output of CMP_2 resets RS_2, and then S_1 is turned off.

The above descriptions show that $v_{i(i=a,b)}$ is equal to $V_{ei(i=a,b)}$ when S_1 turns off. This is a much slower variable than $v_{i(i=a,b)}$ and is considered a constant in each switching cycle. Therefore, the expressions of the control constraint are as follows:

$$v_{can+da} + (i_{n+da} - i_a)r_{ca} = V_{refa};\ v_{cbn+db} + (i_{n+db} - i_b)r_{cb} = V_{refb} \tag{7}$$

When i_L reduces to I_{dc}, S_2 is turned on to short-circuit the inductor and force the inductor current to circulate through L. Therefore, the S_2 freewheeling interval is activated until the corresponding output switch is off. Based on Figure 3b, there is

$$i_{n+fa} = i_{n+da} - m_2 t_2 = I_{dc};\ i_{n+fb} = i_{n+db} - m_4 t_4 = I_{dc} \tag{8}$$

Based on Equations (7) and (8), we can calculate the charging, discharging, and freewheeling intervals for outputs A and B.

2.3. Operation Principle of the Conventional Voltage Mode-Controlled PCCM SIDO Buck Converter

Figure 4 shows the controller and operation waveforms for a conventional voltage mode-controlled PCCM SIDO buck converter.

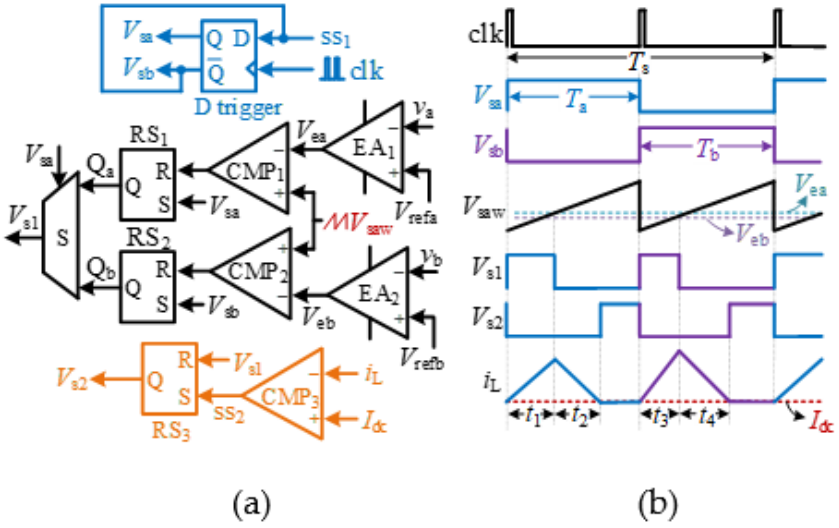

Figure 4. Conventional voltage mode-controlled PCCM SIDO buck converter: (**a**) control block diagram; (**b**) operation waveforms.

Compared with Figure 3, the controller is similar, and the inner control loop of the main switch S_1 is slightly different with a sawtooth waveform V_{saw} instead of the output voltages v_a and v_b. The other control logics are the same as on the voltage ripple-controlled PCCM SIDO buck converter.

The block diagram of the voltage mode control is presented in Figure 4. It shows that when the input voltage or output current changes, the voltage mode control can only detect the change and feedback for correction after the corresponding change of the output voltage, making the reaction speed relatively slow. However, the voltage ripple controller shown in Figure 3 controls the converter by detecting the ripple voltage on the equivalent series resistance of the capacitor. When the load voltage and current change, the inductance current cannot change suddenly; thus, the change of load current is reflected in the change of ripple voltage on the equivalent series resistance, that is, the change of v_a and v_b. Therefore, the voltage ripple controller has a faster response than the voltage mode controller.

3. Small-Signal Model and Frequency Performance Analysis

In Section 3, the small-signal model of the proposed voltage ripple-controlled PCCM SIDO buck converter is established. The frequency performance of cross-regulation is analyzed and compared in detail.

3.1. Small-Signal Modeling of PCCM SIDO Buck Converter

According to Equations (1)–(6), the state-space average equations of the PCCM SIDO buck converter are given as Equation (9).

After introducing the small-signal perturbations in Equation (9) and then removing the direct-current and higher-order parts of the perturbations, the small-signal model for the PCCM SIDO buck converter is written as Equation (10).

$$\begin{cases} L\frac{di_L}{dt} = V_g(d_{a1}+d_{b1}) - \frac{R_a v_{ca}(r_{ca}i_L+v_{ca})}{R_a+r_{ca}}(d_{a1}+d_{a2}) - \frac{R_b(r_{cb}i_L+v_{cb})}{R_b+r_{cb}}(d_{b1}+d_{b2}) \\ C_a\frac{dv_{ca}}{dt} = \frac{R_a i_L(d_{a1}+d_{a2})}{R_a+r_{ca}} - \frac{v_{ca}}{(R_a+r_{ca})} \\ C_b\frac{dv_{cb}}{dt} = \frac{R_b i_L(d_{b1}+d_{b2})}{R_b+r_{cb}} - \frac{v_{cb}}{(R_b+r_{cb})} \end{cases} \tag{9}$$

$$\begin{cases} L\frac{d\hat{i}_L}{dt} = -\frac{R_a}{R_a+r_{ca}}\left((r_{ca}(\hat{v}_{ca}I_L+V_{ca}\hat{i}_L)+2\hat{v}_{ca})(D_{a1}+D_{a2}) + (r_{ca}V_{ca}I_L+{V_{ca}}^2)\left(\hat{d}_{a1}+\hat{d}_{a2}\right)\right) \\ -\frac{R_b}{R_b+r_{cb}}\left((D_{b1}+D_{b2})(r_{cb}\hat{i}_L+\hat{v}_{cb}) + (r_{cb}I_L+V_{cb})\left(\hat{d}_{b1}+\hat{d}_{b2}\right)\right) + \hat{v}_{in}(D_{a1}+D_{b1}) + V_{in}\left(\hat{d}_{a1}+\hat{d}_{b1}\right) \\ C_a\frac{d\hat{v}_{ca}}{dt} = \frac{1}{R_a+r_{ca}}\left(R_a\left(\hat{i}_L(D_{a1}+D_{a2})+I_L\left(\hat{d}_{a1}+\hat{d}_{a2}\right)\right)-\hat{v}_{ca}\right) \\ C_b\frac{d\hat{v}_{cb}}{dt} = \frac{1}{R_b+r_{cb}}\left(R_b\left(\hat{i}_L(D_{b1}+D_{b2})+I_L\left(\hat{d}_{b1}+\hat{d}_{b2}\right)\right)-\hat{v}_{cb}\right) \end{cases} \tag{10}$$

where V_{ca}, V_{cb}, I_L, D_{a1}, D_{a2}, D_{b1}, and D_{b2} are the average of the output capacitors' voltage v_{ca} and v_{cb}, the inductor current I_L, and duty ratios d_{a1}, d_{a2}, d_{b1}, and d_{b2}, respectively.

Based on the above small-signal model, the matrix operation in MATLAB can calculate the self-regulation transfer functions, cross-regulation transfer functions, the duty ratios–output transfer functions, and cross-coupled transfer functions of the PCCM SIDO buck converter.

3.2. Small-Signal Modeling of Voltage Ripple-Controlled PCCM SIDO Buck Converter

For the voltage ripple-controlled PCCM SIDO buck converter, Figure 5 shows the geometric relationship between the output voltage v_a and corresponding inner loop control signal V_{ea} and the output voltage v_b and corresponding inner loop control signal V_{eb}.

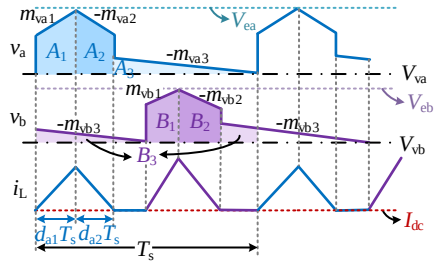

Figure 5. Geometric relationship between output voltage and control signal.

According to the geometric relationship shown in Figure 5, the average of the output voltage v_a during one switching cycle is derived as

$$V_a = V_{va} + (A_1 + A_2 + A_3)/T_s \tag{11}$$

where V_{va} is the valley value of v_a. A_1, A_2, and A_3 denote the areas between v_a and V_{va} shown in Figure 5, which is expressed as

$$V_{va} = V_{ea} - m_{va1}d_{a1}T_s - I_{dc}r_{ca} \tag{12}$$

$$A_1 = 0.5(2I_{dc}r_{ca} + m_{va1}d_{a1}T)d_{a1}T_s \tag{13}$$

$$A_2 = 0.5(2I_{dc}r_{ca} + 2m_{va1}d_{a1}T_s - m_{av2}d_{a2}T_s)d_{a2}T_s \tag{14}$$

$$A_3 = 0.5m_{va3}(d_{a3}+0.5)^2{T_s}^2 \tag{15}$$

In Equations (11)–(15), $m_{vai(i=1,2,3)}$ is the absolute value of the increase and decrease slopes for output voltage v_a, and its corresponding expressions are $m_{va1} = (V_g - V_a)r_{ca}/L$, $m_{va2} = V_a r_{ca}/L$, $m_{va3} = V_a/(R_a C_a)$.

By adding a small disturbance into Equation (11) and ignoring the direct-current and higher-order perturbations, the small-signal expression of the duty ratio d_{a1} can be obtained as

$$\hat{d}_{a1} = G_{a1}\hat{i}_{dc} + G_{a2}\hat{d}_{a2} + G_{a3}\hat{v}_a + G_{a4}\hat{v}_g + G_{a5}\hat{v}_{ea} \tag{16}$$

where the expressions for G_{a1}–G_{a5} are given in Appendix A.

Similarly, based on the waveform of inductor current i_L, the small-signal expression of the duty ratio d_{a2} is given as follows.

$$\hat{d}_{a2} = G_{a6}\hat{i}_L + G_{a7}\hat{i}_{dc} + G_{a8}\hat{d}_{a1} + G_{a9}\hat{v}_a + G_{a10}\hat{v}_g \tag{17}$$

where the expressions for G_{a6}–G_{a10} are given in Appendix A.

The small-signal expressions of the duty ratios d_{b1} and d_{b2} are determined in the same way; moreover, the forms are similar. Thus, the process will not be repeated here.

Based on Equations (16) and (17), the small-signal block diagram of the voltage ripple-controlled PCCM SIDO buck converter can be obtained, as shown in Figure 6. It includes the power circuit, the control circuit of the main switch, and the freewheeling switch. In Figure 6, $H_{v1}(s)$ is the sampling coefficient of the output voltage v_a, and $G_{c1}(s)$ is the transfer function of the error amplifier EA_1. The small-signal model of output B resembles output A.

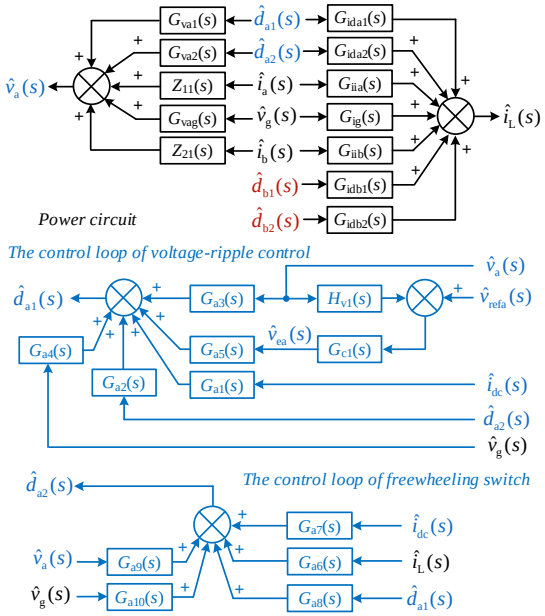

Figure 6. Small-signal model of voltage ripple-controlled PCCM SIDO buck converter.

3.3. Cross-Regulation Analysis in Frequency

There are disturbances propagating from a load current to the cross-output voltage, and the closed-loop cross-regulation transfer functions $\hat{v}_b/\hat{i}_a$ and $\hat{v}_a/\hat{i}_b$ can be used to represent the capacity to attenuate these disturbances. When the low-frequency gain is relatively low, it signifies that the cross-regulation is also relatively small [7,8,19]. When considering the small-signal model presented in Figure 6, the cross-regulation of the proposed voltage ripple-controlled PCCM SIDO buck converter can be researched by means of Bode plots. With the parameters in Table 1, the Bode plots of $\hat{v}_b/\hat{i}_a$ and $\hat{v}_a/\hat{i}_b$ under both a conventional voltage mode-controlled and a voltage ripple-controlled PCCM SIDO buck converter are depicted in Figure 7.

Table 1. Parameters of voltage ripple-controlled PCCM SIDO buck converter.

Symbol	Quantity	Value
V_g	Input voltage	20 V
I_{dc}	Reference current	2 A
L	Inductor	100 μH
T_a, T_b	Operation time	20 μs
C_a, C_b	Output capacitor	550 μF
V_{refa}	Reference voltage	12 V
V_{refb}	Reference voltage	5 V
r_{ca}, r_{cb}	Output capacitor ESR	50 mΩ
I_a, I_b	Load current	0.5 A

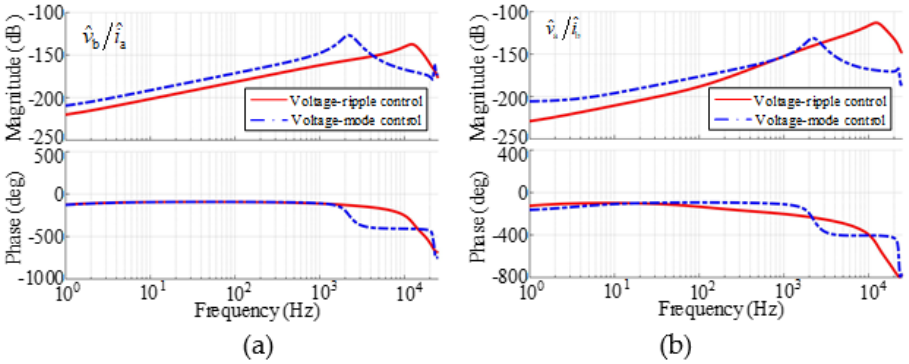

Figure 7. Bode plots of cross-regulation transfer functions under voltage mode-controlled and voltage ripple-controlled PCCM SIDO buck converters: (**a**) $\hat{v}_b/\hat{i}_a$; (**b**) $\hat{v}_a/\hat{i}_b$.

Comparing the low-frequency gains of these two controls in Figure 7 shows that the low-frequency gains (−210 dB) of the voltage mode-controlled PCCM SIDO buck converter are a very negative value. According to the definition of amplitude in the Bode plot and the logarithmic algorithm, it can be considered that there may be only a little cross-regulation between different outputs. Moreover, the low-frequency gains of the voltage ripple-controlled PCCM SIDO buck converter are smaller than those of the voltage mode-controlled PCCM SIDO buck converter. These results show that the cross-regulation of the voltage ripple-controlled PCCM SIDO buck converter is so much smaller than those of the voltage mode-controlled that it can be regarded as no cross-regulation entirely.

3.4. Load-Transient Response Analysis in Frequency Domain

Figure 8a manifests the Bode plots of output impedance transfer function for output A $\hat{v}_a/\hat{i}_a$ of the PCCM SIDO buck converters under voltage mode control and voltage ripple control, respectively. The low frequency magnitude of $\hat{v}_a/\hat{i}_a$ for the voltage ripple-controlled is clearly lower than the voltage mode-controlled, which means that the load transient response of the voltage ripple-controlled PCCM SIDO buck converter is faster than that of the voltage mode-controlled when load variation of output A occurs. Figure 8b shows the Bode plot of the output impedance transfer function $\hat{v}_b/\hat{i}_b$ for output B under voltage mode control and voltage ripple control, which can prove that the low frequency amplitude of $\hat{v}_b/\hat{i}_b$ for voltage ripple control is lower than that of the voltage mode control. These results indicate that the load transient response of the voltage ripple-controlled PCCM SIDO buck converter is faster than that of the voltage mode-controlled.

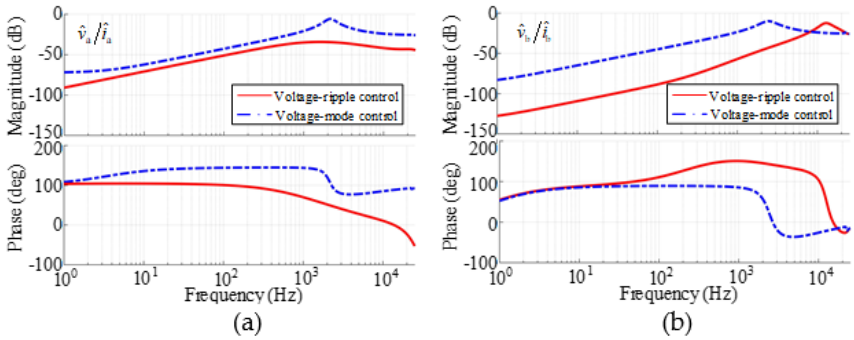

Figure 8. Bode plots of output impedance transfer functions under voltage mode-controlled and voltage ripple-controlled PCCM SIDO buck converters: (**a**) $\hat{v}_a/\hat{i}_a$; (**b**) $\hat{v}_b/\hat{i}_b$.

4. The Load Range and Efficiency Analysis

In the voltage ripple-controlled PCCM SIDO buck converter mentioned above, the constant reference current control is used to manage the freewheeling switch S_2. Therefore, a power limitation is imposed on the converter by this control scheme. In other words, the converter's performance is closely related to the value of the freewheeling current. In this section, the load range and efficiency are investigated in detail, which can supply design guidance for future studies.

4.1. Load Range

Analyzing the load range is beneficial for the optimization of parameters, which can ensure both the output A and output B of a SIDO buck converter operate in PCCM. If the output currents i_a and i_b surpass the maximum output currents $i_{a(max)}$ and $i_{b(max)}$, the converter will transfer from PCCM to CCM mode; therefore, the different outputs are coupled, and the cross-regulation occurs.

Analyzing the volt-second balance on the inductor L, we can find that

$$m_{a1}d_{a1} = m_{a2}d_{a2}, m_{b1}d_{b1} = m_{b2}d_{b2} \tag{18}$$

where $m_{ai(i=1,2)}$ and $m_{bi(i=1,2)}$ represent the charging and discharging slopes of the inductor current, respectively, and $d_{ai(i=1,2)}$ and $d_{bi(i=1,2)}$ represent the charging and discharging times of output A and output B, respectively.

Since the inductor current is equivalent to the output current, the output currents can be shown based on Equation (18).

$$i_a = (1 + m_{a1}/m_{a2})(I_{dc} + m_{1a}d_{a1}T_s/2)d_{a1} \tag{19}$$

$$i_b = (1 + m_{b1}/m_{b2})(I_{dc} + m_{b1}d_{b1}T_s/2)d_{b1} \tag{20}$$

From Equations (18)–(20), the maximum output current occurs when $d_{a1} + d_{a2} = T_a/T_s$ and $d_{b1} + d_{b2} = T_b/T_s$. Therefore, the maximum output currents of the PCCM SIDO buck converter are

$$i_{a(max)} = \left(I_{dc} + (V_g - V_a)V_aT_a/2LV_g\right)T_a/T_s \tag{21}$$

$$i_{b(max)} = \left(I_{dc} + (V_g - V_b)V_bT_b/2LV_g\right)T_b/T_s \tag{22}$$

Note that $i_{a(max)}$ and $i_{b(max)}$ are positively correlated to I_{dc}. The larger I_{dc} can extend the load range for PCCM operation.

4.2. Efficiency

Generally, power losses on a semiconductor are the main source of power losses that influence the efficiency of a PCCM SIDO buck converter. As mentioned in [20,21], the losses caused by semiconductor losses mainly consist of two parts: (1) conduction losses P_{con}; (2) switching losses P_{sw}, including turn-on losses $P_{sw(on)}$ and turn-off losses $P_{sw(off)}$.

The conduction losses of switching device are equal to the product of the square of the transistor rms current and the ON-state resistance, while for the diode, the product of the forward conduction voltage and the average value of rms current can represent its conduction losses [22]. The turn-on resistance of power switches S_1, S_2, S_a, and S_b are defined as r_{on1}, r_{on2}, r_{ona}, and r_{onb}, respectively; and the forward voltage of diodes D_1, D_2, D_a, and D_b are defined as V_{F1}, V_{F2}, V_{Fa}, and V_{Fb}, respectively, while the conduction loss P_{con} can be calculated by Equation (23).

$$\begin{aligned} P_{con} &= {I_L}^2 D_{a1}(r_{ona} + r_{on1}) + {I_L}^2 D_{a2} r_{ona} + I_L V_{F1} D_{a2} \\ &+ {I_L}^2 D_{a3} r_{on2} + I_L V_{F2} D_{a3} + {I_L}^2 D_{b1}(r_{onb} + r_{on1}) \\ &+ {I_L}^2 D_{b2}(r_{onb} + r_{on1}) + {I_L}^2 D_{b3} r_{on2} + I_L V_{F2} D_{b3} \end{aligned} \tag{23}$$

Switching on and off will lead to the switching loss, which is mainly affected by the switching frequency f_s, the drain-source parallel capacitor C_{ds}, and the diode forward voltage V_{SD}. The power switch diode forward voltages S_1, S_2, S_a, and S_b are defined as V_{SD1}, V_{SD2}, V_{SDa}, and V_{SDb}, respectively; while the parallel capacitors of the power switches S_1, S_2, S_a, and S_b are defined as C_{ds1}, C_{ds2}, C_{dsa}, and C_{dsb}, respectively. Therefore, the switching losses can be calculated by Equation (24).

$$\begin{aligned} P_{SW} &= P_{SW(on)} + P_{SW(off)} \\ &= C_{ds1}\left(V_g - V_{SD1}\right)^2 f_s + 0.5 C_{dsa}(V_b - V_a)^2 f_s \\ &+ 0.5 C_{dsb}(V_a - V_b)^2 f_s \end{aligned} \tag{24}$$

The output power of a PCCM SIDO buck converter is $P_{out} = V_a I_a + V_b I_b$; thus, the efficiency η can be calculated by the relative losses:

$$\eta = P_{out}/(P_{out} + P_{con} + P_{SW}) \tag{25}$$

Using the MOSFET BSC010N04LS, its parasitic parameters are r_{on} = 1 m, C_{oss} = 1900 pF, C_{rss} = 160 pF, $C_{ds} = C_{oss} - C_{rss}$, and V_{SD} = 0.8 V; and the diode MBRA320 is V_F = 0.5 V. The efficiency curves with variation of load current are shown in Figure 9.

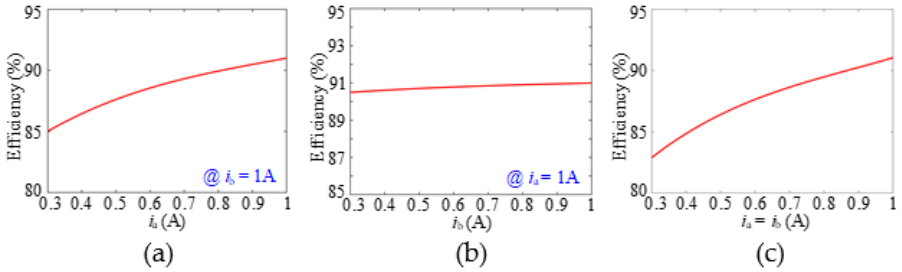

Figure 9. Efficiency curves with variation of load current under voltage ripple-controlled PCCM SIDO buck converters: (**a**) i_a = 0.3–1 A, i_b = 1 A; (**b**) i_a = 1 A, i_b = 0.3–1 A; (**c**) $i_a = i_b$.

Figure 9a shows that when the load current i_b keeps 1 A, the load current i_a varies from 1 A to 0.3 A, and the efficiency significantly decreases. As Figure 9b shows, when i_a = 1 A, the i_b changes from 1 A to 0.3 A, and the efficiency decreases slowly. When the load current i_a is equal to i_b and both of them vary into light load, the efficiency decreases rapidly, as shown in Figure 9c.

According to the above analysis, it is reasonable to conclude that, when the load is in a light load, the efficiency of the voltage ripple-controlled PCCM SIDO buck converter is low. The reason can be easily identified that, the freewheeling switch of PCCM SIDO buck converter using constant-reference-current control, so the freewheeling time will increase under light load, which increases the loss and reduces the efficiency.

5. Experimental Waveforms

To verify the effectiveness of the proposed voltage ripple-controlled PCCM SIDO buck converter in cross-regulation suppression, load transient improvement, and the theoretical analysis of load range and efficiency, the experimental studies were carried out using the circuit parameters shown in Table 1.

5.1. Experimental Environment of Proposed Circuit

The experimental prototype is shown in Figure 10. The prototype in the figure includes a power converter, a control circuit, and three sampling circuits: the sampling circuit of A output voltage, the sampling circuit of B output voltage, and the sampling circuit of the inductor current. Based on the experimental prototype, the experimental results of the proposed PCCM SIDO buck converter are given. The advantages of the proposed converter are shown from the aspects of efficiency, cross-regulation, load range, and load transient, in comparison with the existing methods.

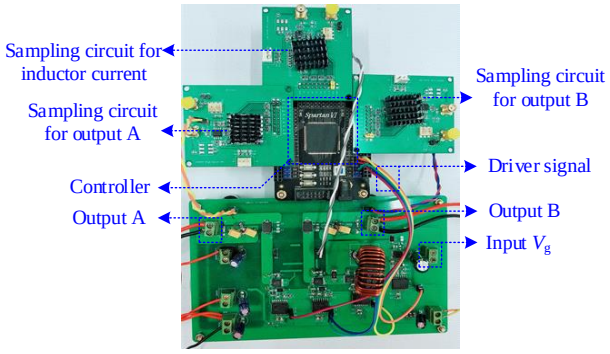

Figure 10. Photograph of experimental prototype.

5.2. Cross-Regulation and Load Transient Analysis

Figure 11 shows the experimental waveforms of the PCCM SIDO buck converter when the load step-up variation of output happened. Under voltage mode control, experimental waveforms of the converter are shown in Figure 11a when only i_a was changed and shown in Figure 11b when only i_b was changed. Similarly, Figure 11c,d show the experimental waveforms of the voltage ripple-controlled PCCM SIDO buck converter with i_a and i_b changed, respectively. The description of Figure 12 is similar to that of Figure 11; the only difference is that Figure 11 describes the experimental waveforms when the load step-up variation happened, while Figure 12 describes them when the load step-down variation happened. The following is the specific analysis:

For the purpose of investigating the cross-regulation performance, the load step-up experimental results of voltage mode control and voltage ripple control for the PCCM SIDO buck converter are shown in Figure 11. In Figure 11a, i_a stepped from 0.5 A to 1 A, while i_b was fixed at 1 A. About 0.64 ms (about sixteen switching periods) were required to regulate v_a, and the overshoot was 0.13 V. The experimental results when i_b stepped from 0.5 A to 1 A are shown in Figure 11b. About 0.4 ms (about ten switching periods) were required to regulate v_a. The undershoot of v_a was 0.08 V. Figure 11a clearly shows that for the voltage mode-controlled PCCM SIDO buck converter, there existed cross-regulation between different outputs.

For the voltage ripple-controlled PCCM SIDO buck converter, the corresponding load step experimental waveforms are shown in Figure 11b. When a load step change was implemented in i_a as shown in Figure 11c, the regulation time of v_a was about two switching periods. There was a little voltage ripple variation in v_a and no variation in v_b. Likewise, the regulation of output B took just one switching period, as shown in Figure 11d. The v_a did not have any variation. This illustrated that no cross-regulation existed for the voltage ripple-controlled PCCM SIDO buck converter.

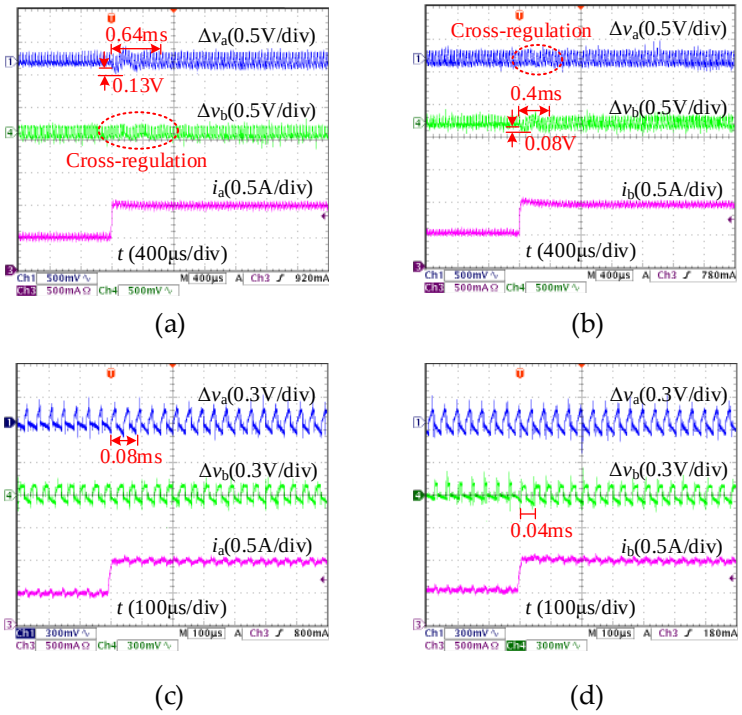

Figure 11. Experimental waveforms of PCCM SIDO buck converter with output load step-up variation: (**a**) change i_a under voltage mode control; (**b**) change i_b under voltage mode control; (**c**) change i_a under voltage ripple control; (**d**) change i_b under voltage ripple control.

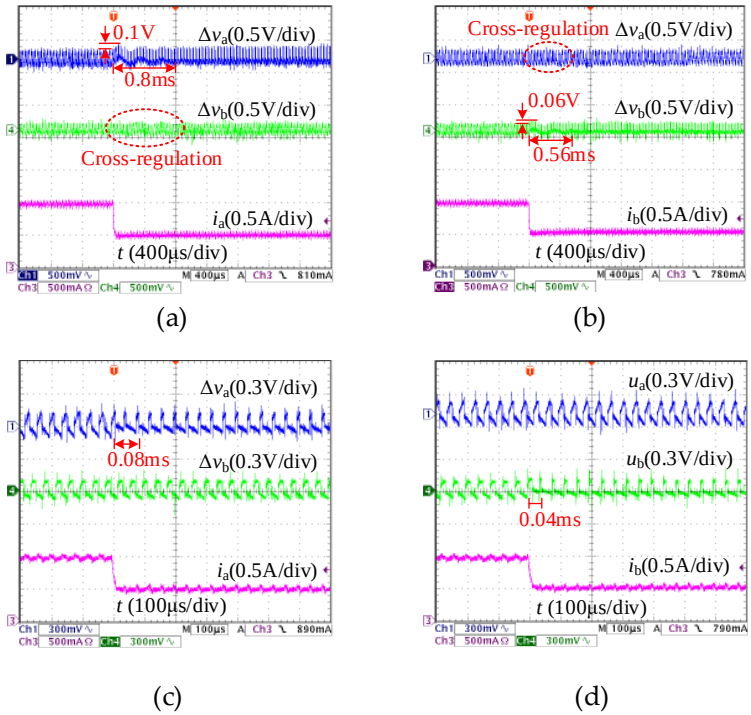

Figure 12. Experimental waveforms of PCCM SIDO buck converter with output load step-down variation: (**a**) change i_a under voltage mode control; (**b**) change i_b under voltage mode control; (**c**) change i_a under voltage ripple control; (**d**) change i_b under voltage ripple control.

Similarly, the experimental waveforms of the PCCM SIDO buck converter with output load step-down variation under voltage mode control and voltage ripple control are presented in Figure 12. It can be observed that, under voltage mode control, i_a and i_b

varied from 1 A to 0.5 A, and the regulation of v_a and v_b took about 0.8 ms and 0.56 ms, respectively. The cross-regulation existed. However, it took only about 0.08 ms and 0.04 ms for voltage ripple control. Moreover, there is no obviously cross-regulation.

The above experimental results illustrate that there still existed cross-regulation for the voltage mode-controlled PCCM SIDO buck converter. On the contrary, the voltage ripple-controlled PCCM SIDO buck converter realized the absolute suppression of its cross-regulation. In addition, the load step had excellent transient performance.

5.3. Load Range Analysis

For verification purposes, the correctness of the theoretical analysis of the load range given earlier and the steady-state experimental waveforms of the voltage ripple-controlled PCCM SIDO buck converter were investigated with the same parameters, as shown in Table 1.

Putting these circuit parameters into Equations (21) and (22), the maximum load currents $I_{a(max)}$ = 1.24 A and $I_{b(max)}$ = 1.19 A were calculated. When $I_a = I_{a(max)}$ = 1.24 A and I_b = 1 A, the freewheeling time of output A was zero, indicating that the output A operated in CCM. The corresponding steady-state experimental waveforms of the inductor current i_L, output voltage v_a and v_b, and the driver signal of freewheeling switch V_{S2} are shown in Figure 13a. Similarly, when $I_b = I_{b(max)}$ = 1.19 A and I_a = 1 A, the output B operates in CCM, and the corresponding experimental waveforms are presented in Figure 13b. The experimental results reveal the correctness of Equations (21) and (22).

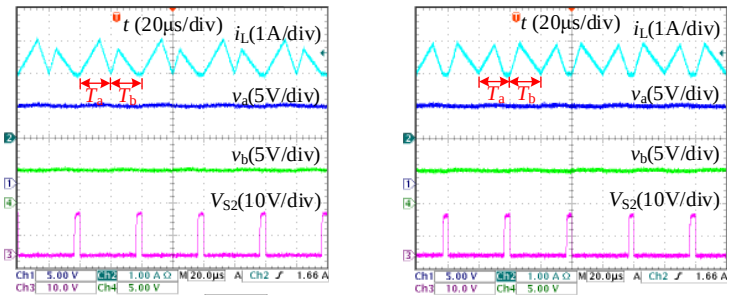

Figure 13. Steady-state experimental waveforms of PCCM SIDO buck converter: (**a**) the maximum load current of output A; (**b**) the maximum load current of output B.

5.4. Efficiency Analysis

The measured experimental efficiency of the conventional voltage mode-controlled and the proposed voltage ripple-controlled PCCM SIDO buck converter is illustrated in Figure 14, with the efficiency versus the load resistor R_a when i_b = 1 A. Figure 14 shows the peak efficiency was 90.6% when the load current was i_a = 1 A and i_b = 1 A. The efficiency significantly degraded at the low load current due to the conduction loss of the freewheeling switch S_f being dominant at the low load current, which verified the efficiency theoretical analysis shown in Figure 9. Comparing the efficiency curves of the conventional voltage mode-controlled and the proposed voltage ripple-controlled PCCM SIDO buck converter proved that while the control of the freewheeling switch followed the same control scheme such as the constant reference current control, the control scheme of the main switch did not affect efficiency significantly.

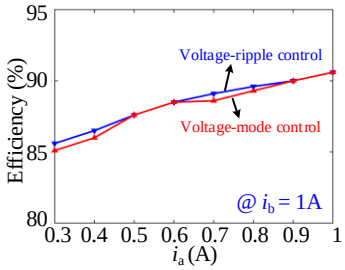

Figure 14. Measured efficiency of the conventional voltage mode-controlled converter and the proposed voltage ripple-controlled PCCM SIDO buck converter against i_a when i_b = 1 A.

5.5. Comparison Analysis

The comparison among the existing literature for the PCCM SIDO DC–DC converter is presented in Table 2. In contrast to the existing studies [8,19] that solved the cross-regulation problem of the CCM SIDO DC–DC converter, the peak efficiency of this study was 90.6%, which is better than [8]. Although [19] was superior in efficiency, the proposed voltage ripple control technique had the advantage in both the load-regulation response and cross-regulation suppression. In addition, given the incomplete operation state and single inductor-current trend of the current mode-controlled CCM SIDO DC–DC converter, the stability in [19] was limited, which means the stability was affected by the input and output voltage. In this study, because of the utilization of the output-voltage ripple control, the input and output voltage did not affect the stability. Compared with the previous PCCM SIMO DC–DC converter studies, this study had a higher peak efficiency than that of [1], which showed the proposed converter could improve the efficiency successfully. Due to the superior performance in relative efficiency, load transient response, and cross-regulation, the proposed voltage ripple-controlled PCCM SIDO DC–DC converter is more advantageous in the application of SIDO power supply.

Table 2. Survey of the existing literature on PCCM SIDO DC–DC converters.

References	This Study	Ref. [1]	Ref. [8]	Ref. [19]
Process	Discrete components	Discrete components	Discrete components	Discrete components
Conduction mode	PCCM	PCCM	CCM	CCM
Input voltage	20 V	24 V	10 V	12 V
Inductor	100 µH	3.4 µH	100 µH	100 µH
Frequency	20 kHz	100 kHz	50 kHz	50 kHz
Capacitors	550 µF	33 uF	470 µF	100 µF
Output voltages	12, 5 V	10, 10 V	3.3, 5 V	15, 24 V
Cross-regulation	0	0	0.4 mV/mA	0.0067 mV/mA
Load transient	1–2 T_s	\	6–8 T_s	7–8 T_s
Efficiency	90.6%	87.8%	\	94.3%

6. Conclusions

The voltage ripple-controlled PCCM SIDO buck converter with no cross-regulation and fast load transient response was proposed in this study. By establishing the small-signal model and portraying the Bode plots, this study theoretically investigated the cross-regulation. Based on its state equations, the load range expression of a PCCM SIDO buck converter was derived. In addition, the power losses were analyzed in detail. The efficiency curves were presented for different load conditions, which showed that the efficiency was significantly decreased under a light load. Compared with a conventional voltage mode-controlled PCCM SIDO buck converter, the proposed voltage ripple-controlled PCCM SIDO buck converter improved cross-regulation and the transient response significantly. The experimental results were fully demonstrated in order to confirm the theoretical analysis results and prove the superiority of the proposed converter.

Author Contributions: Conceptualization, H.J. and S.Z.; formal analysis, S.Z., H.J., M.H. and P.F.; methodology, S.Z., H.J., M.H. and P.F.; validation, M.H., P.F. and S.Z.; writing—original draft preparation, H.J.; writing—review and editing, H.J., M.H., P.F. and S.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Natural Science Foundation of China under Grant No. 62101361.

Acknowledgments: The authors want to thank all who supported them in completing this paper.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

The expressions of G_{a1}–G_{a5} in Equation (16) are as follows:

$$G_{a1} = \frac{1}{1 - \frac{T\left(1-2(D_{a1}+D_{a2})+(D_{a1}+D_{a2})^2\right)}{2R_aC_a} + \frac{r_{ca}T\left((D_{a1}+D_{a2})^2-2D_{a1}\right)}{2L}}$$

$$G_{a2} = \frac{r_{ca}I_{dc} + \frac{r_{ca}T\left(V_g-V_a\right)(1+D_{a1}+D_{a2})}{L} - \frac{V_aT(1-D_{a1}-D_{a2})}{R_aC_a}}{G_{a1}}$$

$$G_{a3} = \frac{r_{ca}I_{dc} + \frac{r_{ca}T\left(D_{a1}\left(V_g-V_a\right)-D_{a2}V_a\right)}{L} - \frac{2V_aT(1-D_{a1}-D_{a2})}{R_aC_a}}{G_{a1}}$$

$$G_{a4} = \frac{r_{ca}D_{a1}T(D_{a1}+2D_{a2}-2)}{2LG_{a1}};\ G_{a5} = \frac{r_{ca}(D_{a1}+D_{a2}-1)}{G_{a1}}$$

The expressions of G_{a6}–G_{a9} in Equation (17) are as follows:

$$G_{a6} = \frac{2L}{(V_g-V_a)D_{a1}T} = -G_{a7}; G_{a8} = \frac{-(2D_{a1}+D_{a2})}{D_1}; G_{a9} = \frac{D_{a1}+D_{a2}}{V_g-V_a} = -G_{a10}$$

References

1. Lee, T.L.; Jin, W.; Tan, S.; Hui, S.Y. Single-inductor multiple-output (SIMO) buck hybrid converter for simultaneous wireless and wired power transfer. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *10*, 2163–2177. [CrossRef]
2. Chen, H.; Huang, C.; Kuo, C.; Lin, L.; Ma, Y.; Yang, W.; Chen, K. A single-inductor dual-output converter with the stacked mosfet driving technique for quiescent current and cross regulation. *IEEE Trans. Power Electron.* **2019**, *34*, 2758–2770. [CrossRef]
3. Jiang, Y.; Asar, S.; Ahmed, M.; Zhang, H.; Fayed, A. Output control techniques for dual-frequency SIMO buck converters. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 4055–4067. [CrossRef]
4. Dong, Z.; Tse, C.K.; Ron, H.S.Y. Current-source-mode single-inductor multiple-output LED driver with single closed-loop control achieving independent dimming function. *IEEE J. Emerg. Sel. Topics Power Electron.* **2018**, *6*, 1198–1209. [CrossRef]
5. Chen, G.; Liu, Y.; Qing, X.; Ma, M.; Lin, Z. Principle and topology derivation of single-inductor multi-input multi-output dc-dc converters. *IEEE Trans. Ind. Electron.* **2021**, *68*, 25–36. [CrossRef]
6. Wang, B.; Zhang, X.; Ye, J.; Gooi, H.B. Deadbeat control for a single-inductor multiple-input multiple-output dc-dc converter. *IEEE Trans. Power Electron.* **2019**, *34*, 1914–1924. [CrossRef]
7. Wang, Y.; Xu, J.; Yan, G. Cross regulation suppression and stability analysis of capacitor current ripple controlled SIDO CCM buck converter. *IEEE Trans. Ind. Electron.* **2019**, *66*, 1770–1780. [CrossRef]
8. Wang, Y.; Xu, J.; Qin, F.; Mou, D. A capacitor current and capacitor voltage ripple controlled SIDO CCM buck converter with wide load range and reduced cross regulation. *IEEE Trans. Ind. Electron.* **2020**, *69*, 270–281. [CrossRef]
9. Dong, Z.; Li, Z.; Li, X.L.; Chi, K.T.; Zhang, Z. Single-inductor multiple-input multiple-output converter with common ground, high scalability, and no cross-regulation. *IEEE Trans. Power Electron.* **2021**, *36*, 6750–6760. [CrossRef]
10. Ma, D.; Ki, W.H.; Tsui, C.Y.; Mok, P.K.T. A 1.8 V single-inductor dual-output switching converter for power reduction techniques. In Proceedings of the 2001 Symposium on VLSI Circuits. Digest of Technical Papers, Kyoto, Japan, 14–16 June 2001; pp. 137–140.
11. Ma, D.; Ki, W.H.; Tsui, C.Y.; Mok, P.K.T. Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode. *IEEE J. Solid-State Circuits* **2003**, *38*, 89–100.
12. Jing, X.; Mok, P.K.T.; Lee, M.C. A wide-load-range constant charge-auto-hopping control single-inductor dual-output boost regulator with minimized cross-regulation. *IEEE J. Solid-State Circuits* **2011**, *46*, 2350–2362. [CrossRef]
13. Ma, D.; Ki, W.H.; Tsui, C.Y. A pseudo-CCM/DCM SIMO switching converter with freewheel switching. *IEEE J. Solid-State Circuits* **2003**, *38*, 1007–1014.

14. Woo, Y.J.; Le, H.P.; Cho, G.H.; Cho, G.H.; Kim, S.I. Load-independent control of switching dc-dc converters with freewheeling current feedback. *IEEE J. Solid-State Circuits* **2008**, *43*, 2798–2808. [CrossRef]
15. Jung, M.Y.; Park, S.H.; Bang, J.S.; Cho, G.H. An error-based controlled single-inductor 10-output dc-dc buck converter with high efficiency under light load using adaptive pulse modulation. *IEEE J. Solid-State Circuits* **2015**, *50*, 2825–2838. [CrossRef]
16. Xu, J.; Weng, Z.; Jiang, H.; Zhang, C.; Wang, Z.; Lin, Q. A high efficiency single-inductor dual-output buck converter with adaptive freewheel current and hybrid mode control. In Proceedings of the 2016 IEEE International Symposium on Circuits and Systems, Montreal, QC, Canada, 22–25 May 2016; pp. 1614–1617.
17. Tian, S.; Lee, F.C.; Li, Q.; Yan, Y. Unified equivalent circuit model and optimal design of V2 controlled buck converters. *IEEE Trans. Power Electron.* **2016**, *31*, 1734–1744. [CrossRef]
18. Zhou, G.; Mao, G.; Zhou, S.; Li, Z.; Leng, M. Digital valley V^2 control for boost converter with fast load-transient performance. *IEEE Trans. Circuits Syst. II Express Briefs* **2020**, *67*, 2089–2093. [CrossRef]
19. Zhou, S.; Zhou, G.; Liu, G.; Mao, G. Small-signal modeling and cross-regulation suppressing for current-mode controlled single-inductor dual-output dc-dc converters. *IEEE Trans. Ind. Electron.* **2021**, *68*, 5744–5755. [CrossRef]
20. Sadigh, A.K.; Dargahi, V.; Corzine, K.A. Analytical determination of conduction and switching power losses in flying-capacitor-based active neutral-point-clamped multilevel converter. *IEEE Trans. Power Electron.* **2016**, *31*, 5473–5494. [CrossRef]
21. Xu, Q.; Ma, F.; He, Z.; Chen, Y.; Guerrero, J.M.; Luo, A.; Li, Y.; Yue, Y. Analysis and comparison of modular railway power conditioner for high-speed railway traction system. *IEEE Trans. Power Electron.* **2017**, *32*, 6031–6048. [CrossRef]
22. Friedli, T.; Hartmann, M.; Kolar, J.W. The essence of three-phase PFC rectifier systems—Part II. *IEEE Trans. Power Electron.* **2014**, *29*, 543–560. [CrossRef]