A 12-Bit 50 MS/s Split-CDAC-Based SAR ADC Integrating Input Programmable Gain Amplifier and Reference Voltage Buffer

Zhuofan Xu 1,2, Biao Hu 1,2, Tianxiang Wu 1,2, Yuting Yao 1,2, Yong Chen 3, Junyan Ren 1 and Shunli Ma 1,2,*

Abstract: This article describes an asynchronous split-CDAC-based SAR ADC with integrated input PGA and an RV-Buffer. The split CDAC structure not only reduces the area of the ADC, but also relieves the driving pressure of the input PGA and RV-Buffer. Using the input PGA instead of the traditional input buffer as the driving circuit of the ADC increases the dynamic input range of the ADC. The proposed on-chip RV-Buffer can provide 1.1 V positive and 0.1 V negative voltage, avoiding the disturbance caused by off-chip reference. This prototype is implemented in a 65 nm CMOS process and occupies an active area of 0.088 mm$^2$. The input PGA can provide 0–18 dB programmable gain with a step of 3 dB. Measurement results show that as the provided gain changes, the ADC’s SNR is best, reaching 50.9 dB, and the SFDR is beat, reaching 62.35 dB at 50 MS/s.

Keywords: split CDAC; asynchronous SAR ADC; input PGA; RV-Buffer

1. Introduction

Successive approximation register (SAR) analog-to-digital converters (ADCs) are considered as appropriate candidates for use in wireless communication for their power efficiency [1–3]. Many techniques have been put forward to improve the performance of the ADC core, but there has not been much research on ADC driving circuits. The ADC driving circuit, especially the input programmable amplifier (PGA), may become the bottleneck of the entire ADC design. The sampling capacitance could be very large in high-speed and high-resolution ADCs. It is difficult to drive such a large sampling capacitor with high accuracy in a short sampling window. One method to reduce the total number of capacitors is to use a split capacitor digital-to-analog converter (CDAC) structure, but the total number of capacitors after the reduction still reaches the pF level. Plus, SAR ADCs have a large (rail-to-rail) input range, and thus, the driving circuit is required to be able to output low noise, is highly linear, and as a nearly full-swing signal near the Nyquist input frequency [4]. However, a simple input buffer is not enough in many cases since the output signal amplitude of the front stage is too small to be processed by the ADCs. Thus, an analog front-end (AFE) with a large gain range is necessary for adjusting the signal amplitude to match the full swing of the SAR ADC. References [5,6] focused on enhancing the drivability and reducing the power consumption of the input driving circuit for a high-resolution SAR ADC, but these driving circuits cannot provide enough variable gain, which limits their applications. Furthermore, the tested results in [6] were measured when the PGA was not functioning, and the dynamic performance of the whole link was not measured. Reference [7] provided a highly linear third-stage input variable gain amplifier...
(VGA) for CCD image sensor applications, but two stages of this were off-chip. The off-chip VGA consumed a large amount of power and could hardly reduce the voltage ringing.

The high sampling frequency and precision put forward stringent requirements on the ADC reference voltage. When the sampling frequency is low, using an off-chip reference source to provide the reference voltage not only has better temperature characteristics, but also facilitates a flexible configuration on the PCB. However, when the sampling frequency goes higher, the parasitic inductance introduced by the bonding wire and PCB trace may produce damping oscillation [8], deteriorating the performance of the ADC. Taking the inductance of 4 nH to simulate bonding wire and PCB trace as an example, the simulation of a 12-bit SAR ADC showed that the voltage fluctuation of the reference voltage node is more than 70 mV at 100 MS/s due to mutual inductance effects. Therefore, it is critical to design a reference voltage buffer (RV-Buffer) to generate reference voltages on-chip.

This paper presents a split CDAC structure-SAR ADC with an integrated input PGA and RV-Buffer. The rest of this paper is organized as follows. Section 2 introduces the top architecture of the proposed SAR ADC and describes its working principle. Section 3 details the circuit implementation consideration, including the split CDAC structure, input PGA, and RV-Buffer. Section 4 shows the measurement results, and Section 5 provides the conclusion.

2. Overall Architecture

The overall ADC architecture is illustrated in Figure 1, which consists of an input PGA, sampling switches, capacitor array, SAR logic, comparator, and RV-Buffer. The supply voltages of the input PGA and SAR ADC core are both 1.2 V. The positive and negative reference voltages of the capacitor array are 1.1 V and 0.1 V, respectively, which are generated by the RV-Buffer with a 2.5 V supply voltage. The input PGA can provide a 0–18 dB programmable gain with a 3 dB step. The working process of the proposed ADC is divided into two parts, sampling and conversion. The sampling period accounts for 1/4 of one clock period, and the remaining time is allocated to conversion. During the sampling period, the input signal of the SAR ADC is amplified to 1.8 Vpp,diff by controlling the gain of the PGA according to the different amplitudes of the input signal. The output common-mode voltage of the PGA and the input common-mode voltage of the SAR ADC are both 0.6 V. The input PGA drives the capacitor array through bootstrapped switches.

![Figure 1. Overall ADC architecture.](image)

This SAR ADC employs a top plate sampling topology in which the sampling front-end is connected to the comparator input, so the comparator starts to perform the first-bit decision step after the sampling phase is finished. Therefore, an (N-1) bit CDAC can meet the quantization requirements for an N bit SAR ADC, which can save half of the capacitors [9,10]. During the data conversion phase, the comparison result of the
comparator is used to control the flip direction of the bottom plate of the capacitor array. This SAR ADC adopts asynchronous logic control [11], shown in Figure 2, that is the clock of the comparator is generated by the comparison result at the previous moment. There are two critical signal paths in the circuit. One is the path from the output of the comparator to the next time the CKC goes high, which is path 1. The second path is from the output of the comparator to the flipping of the bottom plate of the CDAC, which is path 2. It is critical to ensure the signal of the top plate of the CDAC has been established before the succeeding comparison period, so a delay block is inserted into path 1. The capacitor array employs a 4 bit (least-significant bits (LSB)) + 7 bit (most-significant bits (MSB)) split structure, and one redundant bit [12,13] is added to high and low bits, respectively, to form a 14 bit (D13-D0) digital output code. After this arrangement, the total capacitance of a single end is 129 Cu, while Cu is the unit capacitance. A custom-designed unit capacitor is implemented to improve the matching property, and its capacitance is about 6.5 fF, resulting in total single-ended capacitance of about 0.84 pF.

Figure 2. The asynchronous logic.

3. Circuit Implementation
3.1. Split CDAC

Taking 12 bits as an example, the total number of single-ended capacitors reaches 2048 (211) Cu. The increase in the number of capacitors undoubtedly increases the chip area and the design pressure of the input PGA and RV-Buffer. On the other hand, it will also increase the sampling setup time and the CDAC setup time during the conversion phase, resulting in deteriorating the speed of the ADC. The split CDAC can effectively reduce the total number of capacitors. The bridge capacitor CB divides the capacitor array into high M bits and low L bits. The total number of capacitors is reduced from 2N−1 to 2L + 2M. The capacitor array used in this design is shown in Figure 3, in which L is 4 and M is 7, and CB equals 2Cu to avoid fractional capacitance [14]. The split CDAC is very sensitive to parasite capacitance. To make the split CDAC meet the requirements of high linearity, the low-bit dummy capacitor CD is set to be adjustable [14].
The high-bit capacitors adopt a hybrid arrangement [15] in which each capacitor is equally divided into two sub-capacitors \( C_u \) and \( C_b \). The advantage of this structure is that the input common-mode voltage of the comparator remains unchanged during the conversion phase. The low-bit capacitors use a monotonic arrangement [16]. Although this structure will change the input common-mode voltage of the comparator during the conversion phase, this variation can be tolerable since the weight of low-bit capacitors is relatively small.

3.2. Input PGA

The structure of the proposed PGA is shown in Figure 5; the closed-loop negative feedback structure is necessary to ensure high linearity [17]. To further improve the linearity of the sampling signal, the sampling switch adopts the boot-strapped switch structure. The
gain of the PGA equals \( R_f/R_s \), while the resistance of \( R_f \) is adjustable and controlled by a 3–8 decoder. This input PGA can provide a 0–18 dB adjustable gain with a gain step of 3 dB. Assuming that the amplifier used here is a single-pole amplifier, the transfer function of this PGA can be written as

\[
H(s) = \frac{V_{out}}{V_{in}} = -\frac{R_f A_0}{R_s + R_f + R_s A_0}, \quad 1 + \frac{1}{1 + \frac{R_s}{R_f + R_s A_0}} = \frac{1}{1 + \frac{R_s}{R_f + R_s A_0}}\omega_0
\]

where \( A_0, \omega_0 \) is the DC gain and the 3dB bandwidth of the operational amplifier (OPA) used in the PGA. The total error of the input PGA consists of two parts: static error \( \varepsilon_{sta} \) and dynamic error \( \varepsilon_{dyn} \) [18]. \( \varepsilon_{sta} \) is determined by the gain error and can be calculated as

\[
\varepsilon_{sta} = \frac{R_f}{K_c} - \frac{R_f A_0}{R_f + R_f + R_s A_0} = 1 - \frac{R_s A_0}{R_s + R_f + R_s A_0}
\]

\[ (3) \]

Figure 5. The proposed PGA.

If \( \varepsilon_{sta} \) is required to be less than \( (1/4) \text{ LSB} / V_{FS} \), then we can obtain

\[
A_0 > \frac{(2^{N+2} - 1)(R_s + R_f)}{R_s} = \left(2^{N+2} - 1\right)(\text{Gain} + 1) \quad (4)
\]

The dynamic error \( \varepsilon_{dyn} \) is mainly caused by the incomplete establishment of the PGA. The time-domain expression of the output signal is demonstrated as Equation (5).

\[
V_{out}(t) = -\frac{R_f}{R_s}V_{in}(t)\left(1 - e^{-\frac{t}{\tau}}\right)
\]

\[ (5) \]

\[
\frac{1}{\tau} = \left(1 + \frac{R_s}{R_s + R_f} A_0\right)\omega_0 \approx \frac{1}{\text{Gain}} \cdot GBW_{open-loop}
\]

where \( GBW_{open-loop} \) is the unity-gain bandwidth of the OPA used in the PGA, respectively.

As shown in Figure 6, it is assumed that within a signal period, 1/4 is allocated for sampling, and the remaining 3/4 is allocated for signal rebuilding. It is required that
the output signal of the PGA should be established to a precision of $1/4\, LSB$ after each sampling period. Then, we can obtain

$$GBW_{open-loop} > Gain \cdot 4(N + 2) \cdot ln2 \cdot \frac{f_s}{2\pi}$$

(7)

Figure 6. Signal establishment during the sampling phase.

The schematic of the proposed fully differential OPA is shown in Figure 7. It is a modified version of a rail-to-rail input, class AB output, and two-stage amplifier introduced in [19]. The transistors M1-M4 form the rail-to-rail input stage, while M17 and M18 form the class AB output stage. The gate voltage of M5c and M5d $V_{cmfb}$ comes from the output of the common-mode feedback (CMFB) amplifier. It should be noted that the quiescent biasing current of the output stage is set to a relatively high value (1 mA in this design) to ensure that the P and N transistors are turned on at any time for obtaining the good linearity of the output signal.

Table 1 lists the main performance of the designed OPA by the simulation results.

<table>
<thead>
<tr>
<th>Performance</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>1.2 V</td>
</tr>
<tr>
<td>Common mode Output Voltage</td>
<td>0.6 V</td>
</tr>
<tr>
<td>DC Current</td>
<td>6.78 mA</td>
</tr>
<tr>
<td>DC Gain</td>
<td>77 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>1.95 GHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>50°</td>
</tr>
<tr>
<td>IRN</td>
<td>1.52 nV/√Hz</td>
</tr>
<tr>
<td>DC Gain</td>
<td>77 dB</td>
</tr>
<tr>
<td>GBW</td>
<td>1.95 GHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>50°</td>
</tr>
<tr>
<td>IRN</td>
<td>1.52 nV/√Hz</td>
</tr>
</tbody>
</table>
3.3. RV-Buffer

During the conversion phase, the switching action of the bottom plate of the split CDAC causes the equivalent load capacitance of the RV-Buffer to change. Consequently, the load capacitance will extract from or release a certain amount of charge to the reference voltage node in a very short time, causing the disturbance of the reference voltage, as shown in Figure 8. The RV-Buffer needs to restore the output voltage to the required accuracy (0.5 LSB) before the next bit cycling.

![Diagram of RV-Buffer](image)

Figure 8. Sinking and overshoot of reference voltage during sampling.

The main circuit structure of the RV-Buffer can be divided into two categories: closed-loop and open-loop. The fast transient response requires the OPA in the closed-loop RV-Buffer to have a large GBW with a large capacitance load, which will inevitably lead to high power consumption. To avoid this, this paper adopts the open-loop RV-Buffer with replica technique shown in Figure 9a. The size ratio of the replica branch to the original branch is N:1. The positive (1.1 V) and negative (0.1 V) reference voltage, respectively, come from the source voltage of transistors M1b and M2b. The voltage transfer circuit depicted in Figure 9b generates the positive and negative input voltage of the RV-Buffer and provides a 0.6 V common-mode reference voltage for the input PGA at the same time. Since the proposed RV-Buffer eliminates the charge pump [20,21], the gate voltage of M1b is higher than the positive reference voltage by the Vth of NMOS, and it is the output of the voltage transfer circuit at the same time, resulting in the power supply voltage of the RV-Buffer of 2.5 V. Thanks to the split CDAC and open-loop replica structure, 1 mA is sufficient for the output branch to restore the disturbance by simulation results.

![Diagram of Voltage Transfer Circuit](image)

Figure 9. (a) The structure of the proposed RV-Buffer; (b) the structure of the voltage transfer circuit.
In order to verify the necessity of an on-chip RV-Buffer, the designed 12 bit SAR ADC is connected to the load of the RV-Buffer for transient simulation. At the same time, another two simulations are performed on the SAR ADC: One is a connecting series inductance of 4 nH simulating the bonding wire at the positive and negative reference voltage nodes. The other is an ideal situation without any parasitic inductance. The sampling frequency and input frequency are respectively set to 100 MS/s and 10 MHz during the simulation, with transient noise of 10 GHz. Note that this simulation is mainly to prove the necessity; thus, Figure 10 shows the previous simulation’s results. From left to right, Figure 10a–c, respectively, show the transient spectrum under ideal conditions, with parasitic inductance and without the RV-Buffer, and with parasitic inductance and the RV-Buffer. It can be seen from the figure that after considering the parasitic inductance of the bonding wire, the ENOB after adding the RV-Buffer is 2.4 bits higher than without adding it, which is only 0.5 bits less than the ideal situation.

![Figure 10](image_url)

**Figure 10.** The simulated spectrum: (a) under the ideal situation; (b) with parasitic inductance and without RV-Buffer; (c) with parasitic inductance and with RV-Buffer.

### 4. Measurement Results

The prototype of the proposed 12 bit SAR ADC with the input PGA and RV-Buffer was implemented in 65 nm CMOS technology. Figure 11a shows the chip photograph and its zoomed-in view of the core layout occupying an active area of 440 µm × 200 µm. The SAR ADC core and input PGA use a 1.2 V supply, while the RV-Buffer uses a 2.5 V supply. The total power consumption is 17.7 mW, of which the input PGA occupies 8.1 mW, the RV-Buffer occupies 8.8 mW, and the SAR ADC occupies 0.8 mW, as shown in Figure 11b. Combining the bias circuit and reducing the quiescent current of the operational amplifier can reduce the power consumption of the RV-Buffer. However, the reduction of the static current of the operational amplifier will worsen the buffer setup time, which can be compensated by the large off-chip capacitor connected between the reference voltage and the reference ground.

The measurement results of this proposed chip have not adopted any calibration technology. Figure 12 shows the measured spectrum for a low input frequency when the gain provided by the input PGA is 9 dB at 20 MS/s and 50 MS/s, respectively. Fin1 is 10% of Fs1 in Figure 12a, while Fin2 is 3% in Figure 12b. Comparing Figure 12a,b, Fin1 is closer to the corresponding Nyquist frequency than Fin2. When the input signal frequency is close to the Nyquist frequency, it will be charged and discharged more frequently in capacitor array sampling. At this time, poor sampling quality may occur. Therefore, the ENOB in Figure 12b is a little better than that in Figure 12a.
The measurement results of this proposed chip have not adopted any calibration, thus the ENOB in Figure 12b is a little better than that in Figure 12a.

When the input signal frequency is close to the Nyquist frequency, it will be charged and discharged more frequently in capacitor array sampling. At this time, poor sampling quality may occur. Therefore, the ENOB in Figure 12b is a little better than that in Figure 12a. Fin1 is closer to the corresponding Nyquist frequency than Fin2. When the input signal frequency is close to the Nyquist frequency, the dynamic performance of the chip decreases on the whole, which may be because the incomplete establishment caused by the PGA becomes more serious within a shorter sampling window.

In order to keep the input swing of the SAR ADC as constant as possible, the input swing of the chip decreases as the gain provided by the input PGA increases. The measured dynamic performance of the whole chip versus different gain modes at 20 MS/s and 50 MS/s is shown in Figure 13a,b, respectively. With the increase of the sampling frequency, the dynamic performance of the chip decreases on the whole, which may be because the incomplete establishment caused by the PGA becomes more serious within a shorter sampling window.

![Figure 11. (a) The chip photograph with detailed layout; (b) power breakdown.](image1)

![Figure 12. Measured spectrum for low-frequency input at 9 dB gain at: (a) 20 MS/s; (b) 50 MS/s.](image2)

![Figure 13. Measured dynamic performance versus different gain modes for low-frequency input at: (a) 20 MS/s; (b) 50 MS/s.](image3)
Table 2 summarizes the measured performance of the prototype and compares it with other reported works. All the testing data of this design were measured under the condition of the PGA, ADC, and RV-Buffer functioning together. Compared with other SAR ADCs, the ENOB of the work is not good. The main reason is that the amplitude of the analog input signal provided by the test board to the chip is seriously limited, resulting in the SAR ADC not showing the performance it should have. The equivalent resistance of the two differential inputs of the PGA to the ground has a serious deviation, resulting in serious DC offset at the output of the balun device (used to convert the single-ended signal to the differential signal) on the test board. In order to ensure that the output stream of the SAR ADC does not overflow 12 bit, the chip can only be tested at a small analog input amplitude. The data for [6] were measured only when the ADC was working, and the PGA functionality was not used. Reference [7] did not account for the off-chip two-stage PGA when calculating the power consumption. The measured data of [22] and [23] do not suffer from the PGA’s influence. The work described here is the only one that integrated the PGA and RV-Buffer with the ADC, and all three were included when measured. On the other hand, the adjustable gain range provided by this design is relatively large.

<table>
<thead>
<tr>
<th>Architecture</th>
<th>This Work</th>
<th>[6]</th>
<th>[7]</th>
<th>[22]</th>
<th>[23]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>PGA + ADC + RV-Buffer</td>
<td>PGA + ADC</td>
<td>PGA + ADC</td>
<td>ADC</td>
<td>ADC</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>65 nm</td>
<td>65 nm</td>
<td>0.18 µm</td>
<td>0.18 µm</td>
<td>0.18 µm</td>
</tr>
<tr>
<td>Power_{ADC} (mW)</td>
<td>0.8</td>
<td>0.26</td>
<td>22.2</td>
<td>0.736</td>
<td>4.734</td>
</tr>
<tr>
<td>Power_{PGA} (mW)</td>
<td>8.1</td>
<td>0.16</td>
<td>5.9</td>
<td>/</td>
<td>/</td>
</tr>
<tr>
<td>Gain Range (dB)</td>
<td>0−18</td>
<td>−6, 0, 6</td>
<td>−3−0</td>
<td>/</td>
<td>/</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>12</td>
<td>10</td>
<td>12</td>
<td>10</td>
<td>12</td>
</tr>
<tr>
<td>Sampling Frequency (MS/s)</td>
<td>50</td>
<td>40</td>
<td>50</td>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>Input Range for ADC (V_{pp})</td>
<td>1.8</td>
<td>0.88</td>
<td>1.5</td>
<td>1</td>
<td>1.4</td>
</tr>
<tr>
<td>ENOB_{peak}</td>
<td>8.16</td>
<td>9</td>
<td>10</td>
<td>9.13</td>
<td>10.4</td>
</tr>
<tr>
<td>SNR_{peak}</td>
<td>50.9</td>
<td>/</td>
<td>/</td>
<td>56.7</td>
<td>64.3</td>
</tr>
<tr>
<td>SFDR_{peak}</td>
<td>62.35</td>
<td>72</td>
<td>73.1</td>
<td>65.8</td>
<td>74.7</td>
</tr>
<tr>
<td>FoM_{ADC} (fJ/conv.-step)**</td>
<td>55.9</td>
<td>21.7***</td>
<td>433.6</td>
<td>32.84***</td>
<td>70.6***</td>
</tr>
</tbody>
</table>

* The 2.5 V supply is only used by RV-Buffer. ** FoM_{ADC} = Power_{ADC}/(Sampling Frequency × 2^{ENOB}). *** These FoMs did not include the PGA’s influence.

5. Conclusions

This brief presented a split CDAC asynchronous SAR ADC with an integrated input PGA and RV-Buffer in 65 nm CMOS technology for wireless communication applications. The split CDAC structure reduces the total number of capacitors, thereby alleviating the driving pressure of the input PGA and RV-Buffer. The input PGA can improve the dynamic input range of the SAR ADC. The positive and negative reference voltages are provided by the RV-Buffer on-chip, thus avoiding the disturbance caused by the off-chip reference.

Author Contributions: Conceptualization, Z.X., Y.Y. and S.M.; methodology, Y.Y., T.W. and S.M.; validation, Y.Y. and B.H.; data analysis, Y.Y. and Z.X.; writing—original draft preparation, Y.Y.; writing—review and editing, S.M., J.R. and Y.C.; supervision, J.R.; project administration, J.R. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Natural Science Foundation of China (NSFC) under Grants 62104039 and 61934008, the Natural Science Foundation of Shanghai (Grant No.
21ZIR1405700), and the Young Scientist Project of the MOE innovation platform and the Independent Project of State Key Laboratory of ASIC and System under Grant 2021MS012.

Conflicts of Interest: The authors declare that they have no conflict of interest.

References
2. Liu, C.; Kuo, C.; Lin, Y. A 10 bit 320 MS/s Low-Cost SAR ADC for IEEE 802.11ac Applications in 20 nm CMOS. IEEE J. Solid-State Circuits 2015, 50, 2645–2654. [CrossRef]
7. Choi, M.; Ahn, G.; Lee, S. 12b 50MS/s 0.18 µm CMOS SAR ADC with highly linear input variable gain amplifier. Electron. Lett. 2010, 46, 1254–1256. [CrossRef]
15. Gimbv, B.P.; Chandrakasan, A.P. 500-MS/s 5-bit ADC in 65 nm CMOS with split capacitor array DAC. IEEE J. Solid-State Circuits 2007, 42, 739–747. [CrossRef]