Total Ionizing Dose Effects of $^{60}$Co $\gamma$-Ray Radiation on Split-Gate SiC MOSFETs

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Abstract: SiC power devices require resistance to both single-event effects (SEEs) and total ionizing dose effects (TIDs) in a space radiation environment. The split-gate-enhanced VDMOSFET (SGE-VDMOSFET) process can effectively enhance the radiation resistance of SiC VDMOS, but it has a certain impact on the gate oxide reliability of SiC VDMOS. This paper investigates the impact mechanism and regularity of using the SGE process to determine the radiation resistance and long-term reliability of SiC VDMOS under other identical processes and radiation conditions. Our experimental results show that after $^{60}$Co $\gamma$-ray irradiation, the degradation degrees of the static parameters of SGE-VDMOSFET and planar gate VDMOSFET (PG-VDMOSFET) are similar. The use of the new process leads to more defects in the oxide layer, reducing the long-term reliability of the device, but its stability can recover after high-temperature (HT) accelerated annealing. This research indicates that enhancing the resistance of SEEs using an SGE-VDMOSFET structure requires simultaneously considering the demand for TIDs and long-term reliability.

Keywords: split-gate-enhanced VDMOSFET; planar gate VDMOSFET; total ionizing dose effect; long-term reliability

1. Introduction

As the aerospace industry rapidly develops towards deep space exploration, electronic devices are facing increasingly diverse working environments, making it particularly important to ensure the stability of device operation in complex space environments. A space radiation environment is filled with a large number of high-energy particles such as electrons, protons, gamma-rays, and heavy ions, which pose a threat to semiconductor components in spacecrafts [1,2]. Silicon carbide power field effect transistors (SiC VDMOS) have significant advantages, including high temperature, high power, high efficiency, and reduced volume, meeting the requirements of the new generation of spacecraft power semiconductor devices. Therefore, SiC-based power semiconductor devices have great potential for application in space radiation environments [3,4].

Currently, the radiation effects of SiC metal-oxide semiconductor field-effect transistors (SiC MOSFETs) have gained attention [5–8]. In 2012, Akturk et al. conducted a TID experiment on 1200 V SiC MOSFET power devices using $^{60}$Co $\gamma$-radiation. The results showed that the device still had good performance when the accumulated dose exceeded 100 krad (Si). When the accumulated dose exceeded 300 krad (Si), the capacitance between the gate and drain changed, which significantly affected the device’s switching...
In 2014, Alexandru et al. examined the influence of proton and electron irradiation on the electrical parameters of 4H-SiC nMOSFETs \[10\]. The results showed that the threshold voltage decreased after proton irradiation and tended to stabilize over time. With an increase in proton dose, the threshold voltage showed a decreasing trend. Similar changes were observed before and after electron irradiation. Meanwhile, the gate leakage current remained almost unchanged under the highest flux proton irradiation and the maximum dose of electron irradiation \[11\]. In 2019, TID radiation experiments were conducted on different SiC power devices by Hazdra and Popelka. The results showed that SiC devices with an oxide layer were more susceptible to TIDs after radiation \[12\].

In recent years, the radiation damage effects and radiation hardening techniques of SiC VDMOS devices have gradually become a research hotspot due to their sensitivity to radiation-induced damage in the oxide layer. Among them, the function disablement characteristic of SEE radiation damage has received extensive attention both domestically and abroad \[13-16\]. Increasing the thickness of the VDMOS oxide layer is a commonly employed measure to strengthen resistance against SEEs. This method can effectively enhance the device’s resistance to single-Event gate rupture (SEGR) and has already been extensively studied in silicon-based VDMOS. As early as 1986, A. E. Waskiewicz et al. first proposed the SEB effect of power VDMOS devices \[17\]. In 1987, T. Fischer proposed the SEGR effect of power VDMOS devices \[18\]. Cascio, A et al. proposed a method of thickening the gate dielectric, where they reinforced the device by separately depositing a thick oxide layer in the gate oxide region of the JFET region. The purpose of this structure is to increase the breakdown voltage of the gate dielectric layer by increasing the thickness of the oxide dielectric layer, thereby improving the device’s resistance to SEEs \[19\]. The LOCOS (Local Oxidation of Silicon) structure adopted by Tang Zhaohuan and colleagues is also a reinforcement measure based on the principle of thickening the gate oxide layer. However, unlike the method of depositing a thick gate oxide layer alone, this structure consumes some of the silicon thickness in the JFET region \[20\]. Currently, conventional reinforcement technology improves the SEE resistance in power MOSFET, which can result in performance loss to factors such as conductivity and reliability. Therefore, determining how to improve SEE resistance while meeting the basic operating characteristics of the device has long been a focus of research for experts in radiation hardening.

Specific on-resistance ($R_{onsp}$) is an important indicator for evaluating the performance of unipolar power devices. Its physical meaning is the product of the on-resistance of the device and the active conducting area of the chip. A smaller value indicates a higher technical level, meaning that products with the same on-resistance value require smaller chip areas. In 1993, J.W. Palmour proposed a vertical UMOSFET structure based on an immature ion implantation process in a silicon carbide material. As a result, this structure eliminated lattice loss caused by ion implantation through epitaxy, enabling the device to withstand voltages up to 330 V with a $R_{onsp}$ of 33 m$\Omega$cm$^2$. Due to various issues in the UMOS structure process, more researchers have focused on research on VDMOS devices in recent years. However, VDMOS devices have a large gate-drain capacitance, which greatly reduces their frequency response and performance when the device operates under a high-frequency state, leading to performance losses \[21,22\]. To optimize the working performance of VDMOS devices under high-frequency conditions, the split-gate structure (split gate) emerged as a solution, dividing the gate structure in two. This structure significantly reduced gate leakage capacitance and improved the performance of trench-gate VDMOS devices.

Modifying the oxide layer structure of VDMOS can effectively enhance the radiation tolerance of SiC VDMOS, but this complex process could potentially affect the reliability of the gate oxide. With the use of a new split-gate structure oxide process, defects of different types and spatial distributions will occur inside the gate oxide layer, which will affect the TID sensitivity of SiC VDMOS. Therefore, investigating the quality of the oxide layer of the split-gate structure and studying the changes in TID radiation damage are crucial.
This paper presents a comparative study on the TID sensitivity and long-term reliability of the traditional PG-VDMOSFET structure and the SG-VDMOSFET structure. The transfer characteristics curves ($I_{DS}-V_{GS}$), threshold voltage drift ($\Delta V_{TH}$), on-resistance ($R_{DS(on)}$), leakage current ($I_{GSS}$), interface state density ($N_{it}$), and current density–electric field strength characteristic curves (J-E characteristic curves) were analyzed before and after radiation exposure. This research is based on the improvement of electrical parameters and reliability degradation of SiC VDMOS, providing experimental data to optimize the gate oxide process and mitigate TID damage for SiC VDMOS.

2. Samples and Experimental Setup

This experiment utilized two domestically produced 1200 V N-channel SiC VDMOS devices with a planar gate structure, both packaged in TO-247-3 packages and processed using the same process flow. P-type wells and N+ source regions were doped via ion implantation on a 10 um epitaxial layer to form the MOSFET channel region. The gate oxide layer was then grown via thermal oxidation and annealed in a NO atmosphere after a HT treatment to activate the carriers. The two devices featured the same cell structure and had a tox of 50 nm. Specifically, the split-gate structure SiC VDMOS has two symmetrical gate electrodes placed at an interval on top of the gate insulation layer, with a single gate length of 1.2–1.25 um and a distance of 1.3 um between the two gates. Figure 1 shows the schematic of two different structures of VDMOSFETs: (a) SGE-VDMOSFET; (b) PG-VDMOSFET.

![Figure 1. Typical-size VDMOSFET structure diagram: (a) PG-VDMOSFET; (b) SGE-VDMOSFET.](image)

The experiment was carried out at the Xinjiang Institute of Physics and Chemistry, Chinese Academy of Sciences. The irradiation source was $^{60}$Co, and the dose rate was 100 rad (Si)/s. The samples were irradiated to 300 krad (Si) with a positive gate bias ($V_{GS} = 20$ V, drain and source grounded) at room temperature (RT).

An Agilent B1500 A semiconductor device analyzer was used to measure the $I_{DS}-V_{GS}$ curve before irradiation. Linear extrapolation was performed on the $I_{DS}-V_{GS}$ curve to obtain the threshold voltage ($V_{TH}$) of the device. The $R_{DS(on)}$ was tested using a semiconductor isolation device testing system (BC3193) based on the device datasheet, and $I_{GSS}$ was tested at $V_{GS} = 20$ V and $V_{DS} = 0$ V. Some devices were subjected to TID irradiation followed by 168 h annealing at 100 °C, with the same bias as the radiation process maintained on all pins. The device characteristics were then retested after annealing.
3. Results and Analyses

3.1. The Influence of TID Radiation on the Static Characteristics of SGE-VDMOSFET and PG-VDMOSFET

Figure 2 shows the relationship between the $I_D$–$V_{GS}$ curves and cumulative dose for the two types of SiC VDMOS transistor. For the $I_D$–$V_{GS}$ curve, we mainly focus on its sub-threshold region, so the size of $V_D$ does not affect the area we need to observe. At the same time, when testing the $I_D$–$V_{GS}$ curve using the Agilent B1500 A semiconductor device analyzer, if $V_D$ is greater than 0.1 V and the device is conducting, the equipment will cause current limiting and cannot be tested. Therefore, to obtain the complete $I_D$–$V_{GS}$ curve of the device, $V_D$ needs to be set to less than or equal to 0.1 V. As the same process and cell size were used, the investigation of TIDs was mainly focused on the oxide thickness (tox) of the devices. In terms of radiation damage, the SGE-VDMOSFET exhibited less severe damage than the PG-VDMOSFET. Figure 3 shows the threshold voltage degradation curves of the two devices, with good consistency observed among multiple tested devices in terms of threshold voltage performance. As the cumulative dose increased, the threshold voltage decreased uniformly for both devices. The threshold voltage of the PG-VDMOSFET had a negative drift of 1.62 V at a cumulative dose of 300 krad (Si), while the SGE-VDMOSFET already exhibited a threshold voltage drift of 1.36 V at the same cumulative dose.

![Figure 2: Transfer characteristic curve: (a) PG-VDMOSFET; (b) SGE-VDMOSFET.](image)

![Figure 3: Threshold voltage shifts $\Delta V_{TH}$ as a function of TIDs for PG-VDMOSFET and SGE-VDMOSFET.](image)

Radiation causes ionization in the gate oxide, resulting in the generation of a large number of electron–hole pairs. Although there are a small number of electron traps formed by carbon residues during the thermal oxidation growth process in the gate oxide, their...
density is extremely low, and the electrons with high mobility will be quickly swept out of the gate oxide layer under the influence of an electric field. The holes with lower mobility are more likely to be captured by hole traps in the oxide layer, becoming positively charged oxide traps. Oxide traps (mainly hole traps generated during the thermal oxidation process) will capture more positively charged holes after irradiation, leading to an increased inversion degree of the NMOS channel and a negative shift in the transfer characteristic curve towards the negative x-axis. The oxide trap charges that affect the threshold voltage of the device are mainly located above the channel, with a smaller influence on the gate oxide layer in the JFET region. Therefore, theoretically, under the same gate oxide thickness for both devices, the degradation of the threshold voltage should be almost the same. However, it can be clearly seen from the data of multiple devices that the threshold voltage degradation of the SGE-VDMOSFET is weaker. This phenomenon often occurs due to defects in the interface between the gate oxide layer and the silicon carbide substrate caused by changes in the gate oxide layer fabrication process. Therefore, in Section 3.2 of this article, this inference is validated.

Subthreshold Swing (SS) refers to the change in $I_{DS}$ with a one-decade increase in $V_{GS}$. It represents the change in gate voltage required for the $I_{DS}$ to vary by a factor of 10 and is also known as the S factor. A smaller S value indicates a faster ON/OFF switching speed.

$$\text{SS} = kT \eta \ln 10 = kT \frac{C_{ox} + C_{dep} + C_{it}}{C_{ox}} \ln 10$$

In this equation, $\frac{kT}{q}$ represents the thermal voltage, $\eta$ is referred to as the body factor, and $\psi_s$ is the surface potential. $C_{ox}$ is the capacitance of the top-gate oxide layer, $C_{dep}$ is the depletion capacitance, $C_{it}$ is the interface trap capacitance, $k$ is the Boltzmann constant, $T$ is the temperature, and $q$ is the electronic charge.

The factors affecting subthreshold swing are as follows: (1) An increase in temperature leads to an increase in subthreshold swing. (2) An increase in gate oxide capacitance leads to a decrease in subthreshold swing; the use of high-k dielectric materials or a reduction in the gate oxide thickness can result in a decrease in subthreshold swing. (3) A decrease in Si depletion layer capacitance results in a decrease in subthreshold swing; factors that may increase the depletion layer width, such as a decrease in substrate concentration Na or an increase in substrate bias voltage, lower the subthreshold swing. (4) Interface defects between the gate oxide layer and the substrate silicon can store charge and can effectively increase the capacitance, leading to an increase in the subthreshold swing. (5) A shorter channel length weakens the gate control capability, and hence, leads to an increase in subthreshold swing. (6) An increase in gate voltage results in stronger surface inversion, leading to weaker gate control of the channel and an increase in subthreshold swing.

Figure 4 shows the relationship between the S and the total irradiation dose for the two SiC VDMOS transistors. After TID radiation, the S value of the SGE-VDMOSFET changes slightly from 282 to 301, while the S of the PG-VDMOSFET remains almost unchanged.
with weaker degradation in the $\Delta V$ (2) from the process and weaker degradation in the $\Delta V_{TH}$ of SGE-VDMOSFET, leading to weaker degradation in the $\Delta V$ (3) of PG-VDMOSFET decreased by 1.9 V, and the $\Delta V_{TH}$ of SGE-VDMOSFET decreased by 1.8 V, with weaker degradation in the $\Delta V_{TH}$ of SGE-VDMOSFET. The $\Delta V_{TH}$ of PG-VDMOSFET decreased by 1.6 V, and the $\Delta V_{TH}$ of SGE-VDMOSFET decreased by 1.4 V, with weaker degradation in the $\Delta V_{TH}$ of SGE-VDMOSFET. The $\Delta V_{TH}$ of PG-VDMOSFET decreased by 1.9 V, and the $\Delta V_{TH}$ of SGE-VDMOSFET decreased by 1.8 V, with weaker degradation in the $\Delta V_{TH}$ of SGE-VDMOSFET. Our analysis indicates that there are two reasons for the weaker degradation in the $\Delta V_{TH}$ of SGE-VDMOSFET: (1) from the $\Delta V_{IT}$ perspective, the SGE-VDMOSFET utilizing the new process has fewer oxide defect potential hole traps in the oxide layer produced during the thermal oxidation process compared to PG-VDMOSFET, leading to weaker degradation in the $\Delta V_{IT}$ of SGE-VDMOSFET; (2) from the $\Delta V_{IT}$ perspective, PG-VDMOSFET has fewer interface states at the gate oxide interface due to less etching, resulting in fewer captured electrons during the radiation process and weaker degradation in the $\Delta V_{IT}$. Overall, reason 2 is the main reason for the weaker degradation in the $\Delta V_{TH}$ of SGE-VDMOSFET.
When designing a switching power supply or driving circuit using MOSFET, it is generally necessary to consider the on-resistance of the MOSFET. Because energy is consumed on this resistance when current flows through the drain and source, this energy consumption is called conduction loss. Choosing a MOSFET with a lower on-resistance can reduce conduction loss to a certain extent. If a higher breakdown voltage is required, the internal structure needs to be made thicker, so the on-resistance of a MOSFET with a higher breakdown voltage will be larger.

Meanwhile, gate leakage current is also a very important parameter in semiconductor devices. It describes the insulation effect of the transistor and has an important impact on the service life and stability of the device. The gate leakage current refers to the leakage current between the gate and drain of a transistor when it is in the off state. By measuring the leakage current value of the device, we can evaluate the insulation quality. As an important component of semiconductor devices, the gate leakage current of a transistor has a significant impact on its performance.

There are three factors that affect gate leakage current: 1. Temperature is an important factor that affects gate leakage current. As the temperature increases, the leakage current between the gate and drain of the transistor gradually increases. Therefore, when conducting temperature tests, it is necessary to ensure that the operating temperature of the transistor does not exceed its allowable maximum temperature. At the same time, it is also necessary to compare different devices under the same temperature conditions to determine the magnitude of their gate leakage current. 2. Voltage is also one of the factors that affect the magnitude of the transistor’s gate leakage current. At a certain operating temperature, as the acceleration voltage increases, the gate leakage current of the transistor also shows an increasing trend. Therefore, when conducting gate leakage current tests, attention should be paid to the selection of the test voltage and the duration of the test. 3. The quality of insulation materials also affects the magnitude of the gate leakage current. Higher-quality insulation materials can effectively suppress the gate leakage current of the transistor. Therefore, when designing semiconductor devices, it is necessary to select high-quality insulation materials to ensure the stability and reliability of the device.

Figure 6 shows the changes in the electrical parameters of two SiC VDMOS transistors as a function of accumulated radiation dose. After irradiation, the gate oxide of the two devices accumulated positive charges in oxide traps to varying degrees. Defects that carry a positive charge attract electrons onto the semiconductor surface, increasing the surface electron concentration, and hence, reducing the device RDS (on). When the accumulated dose reaches 300 krad (Si), the IGSS of SGE-VDMOSFET increases slightly but remains at the nA level. TIDs do not significantly affect the IGSS of either device. The examination of gate leakage current is often carried out by observing whether it undergoes a sudden change from the nA level to the µA level. The variation in Figure 6 is very small, which is highly likely to be due to measurement errors caused by the equipment.
An energy band diagram of P-type substrate silicon carbide under positive gate bias.

3.3. The Influence of TID Radiation on Electron Tunneling in Gate Oxide

It is generally accepted that Fowler–Nordheim (F-N) tunneling becomes one of the main reasons for charge transport through the oxide layer when the oxide layer is thick or the gate voltage is high. F-N tunneling is an electron tunneling phenomenon caused by an electric field. As shown in Figure 7, when a high voltage is applied to the polycrystalline silicon/oxide/carbon structure, the barrier in the oxide layer becomes very steep, and electrons in the SiC conduction band face a triangular barrier that depends on the external electric field. When the voltage is high enough, the barrier becomes extremely narrow, and electrons can tunnel through the barrier, entering the oxide conduction band from the SiC conduction band, thus inducing F-N tunneling. The tunneling current density can be expressed as follows using a self-consistent electron model and WKB approximation [27]:

\[ J_{FN} = \frac{q^3 E^2}{16\pi\hbar \phi_B} \exp\left(-\frac{4\sqrt{2m^* \phi_B}}{3\hbar E}\right) \]  

(5)

The expression can be adjusted using a correction factor that includes \( h \) as the reduced Planck constant, \( \phi_B \) as the barrier height, \( m^* \) as the effective mass of electrons in the oxide layer, and \( E \) as the electric field strength in the oxide layer. The correction factor can reflect the effect of the mirror potential as well as the influence of temperature on the tunneling process [28].

Figure 8 shows changes in the gate oxide J-E curves of two SiC VDMOS transistors as a function of accumulated total dose. For the PG-VDMOSFET device, the gate oxide current density increases uniformly when the accumulated dose reaches 300 krad (Si), but the characteristic gradually recovers after 168 h HT accelerated annealing. The J-E charac-
teristic of non-irradiated SGE-VDMOSFET exhibits hysteresis at an electric field strength of 4 MV/cm. When the accumulated dose for SGE-VDMOSFET reaches 300 krad (Si), the tunneling characteristic of the device tends to be stable, and the device has better gate oxide characteristics after subsequent 168 h HT accelerated annealing. Further investigation is required to ensure the long-term reliability of the device.

![Figure 8. Current density–electric field strength (J-E) characteristic curves for devices irradiated with $^{60}$Co $\gamma$-rays up to 300 krad (Si) at a dose rate of 100 rad(SiO$_2$)/s, and annealed for 168 h at 100 °C.](image)

4. Conclusions

With an increase in accumulated dose during $^{60}$Co $\gamma$-ray irradiation, both PG-VDMOSFET and SGE-VDMOSFET experience varying degrees of radiation damage. For $V_{TH}$, SGE-VDMOSFET experiences weaker degradation compared to PG-VDMOSFET. This is mainly due to the presence of more defects at the interface during the growth and etching of gate oxide in SGE-VDMOSFET, and an increase in interface states after irradiation. The electrical performance consistency of SGE-VDMOSFET devices is poor. At the same time, there are reliability problems with the gate oxide. The initial samples had more deep-level defects inside the gate oxide, which facilitated electron tunneling from the substrate through F-N tunneling under electric stress. The SGE process may lead to the generation of more deep-level defects in the gate oxide when solving the SEE problems of SiC VDMOS. J-E can be significantly improved after irradiation and 168 h high-temperature annealing. Improving the SEE resistance of SiC VDMOS via the SGE process requires consideration of the long-term reliability degradation of the devices.

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