Comparison of Gamma Irradiation Effects on Short Circuit Characteristics of SiC MOSFET Power Devices between Planar and Trench Structures

Lei Shu 1,2,3,*, Huai-Lin Liao 1, Zi-Yuan Wu 4, Yan-Yan Li 2, Xing-Yu Fang 2,3, Shi-Wei Liang 4, Tong-De Li 2,3, Liang Wang 2,3, Jun Wang 4 and Yuan-Fu Zhao 2,3,*

1 School of Integrated Circuit, Peking University, Beijing 100871, China; shulei@pku.edu.cn (L.S.); liaohl@pku.edu.cn (H.-L.L.)
2 Beijing Microelectronics Technology Institute, Beijing 100076, China; lyy007887@163.com (Y.-Y.L.)
3 Laboratory of Science and Technology on Radiation Hardened Integrated Circuits, China Aerospace Science and Technology Corporation (CASC) Fengtai, Beijing 100076, China
4 College of Electrical and Information Engineering, Hunan University, Changsha 410082, China; wzy123@hnu.edu.cn (Z.-Y.W.)
* Correspondence: zhaoyf@vip.163.com

Abstract: The short circuit withstand energy (SCWE) variations, and short circuit withstand time (SCWT) variations, of planar and trench silicon carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFET) power devices are studied after exposure to a total ionizing dose (TID). The results for ON bias are explored. The SCWE and SCWT are studied for planar and trench SiC MOSFET power devices tested for TID with gamma irradiation. A higher degradation phenomenon for the SCWE and SCWT are observed for the planar SiC MOSFET. The physical mechanisms for these variations are analyzed and confirmed by technology computer-aided design (TCAD) simulation.

Keywords: SiC MOSFET; TID; SCWE; SCWT; TCAD simulations

1. Introduction

For its superior material and device properties, SiC MOSFET power devices have higher efficiency and power density of power electronic systems than silicon IGBTs, making them one of the most promising power switches in space power systems [1–4]. However, radiation particles in the space environment generates trapped charges in the oxide, which, in turn, leads to device electrical characteristic variations [5]. When SiC MOSFET power devices operate in earth, the short circuit (SC) is already a very important issue [6]. In addition, the SC robustness of SiC MOSFET power devices is weaker than silicon devices in earth (before being exposed to a radiation environment) [7–11]. However, when SiC MOSFET power devices operate in space, radiation in space causes a TID effect on the devices. The TID produces defects on their gate oxide and, when the devices experience a SC, it can also cause damage to the gate oxide. Therefore, compared to the devices before irradiation, the SC problems that have been exposed to the radiation environment are more severe. Therefore, it is very important to study the TID effects on the SC characteristics of SiC MOSFET power devices for their application in space. Currently, most of the published literature focuses on the TID effect on the static characteristics of SiC MOSFET power devices, and no published papers have investigated the TID effects on the SC characteristics [12–14].

This paper investigates the TID effects on SC characteristics of 1200 V commercial planar and trench SiC MOSFET power devices. The mechanisms of the studied devices are simulated through experiment and technology computer-aided design (TCAD). The description of the SiC MOSFET power devices under test and experimental setups will be introduced in Section 2. The experimental results are given in Section 3. The analysis
and TCAD simulation of the physical mechanisms are given in Section 4, followed by the conclusions in Section 5.

2. Device Structure and Experimental Method

Figure 1 shows the cross-sectional views of the studied planar and trench SiC MOSFET power devices. Figure 1a–c are the planar, trench and double trench schematic cross-sectional view, respectively. The studied devices are commercial SiC MOSFETs from CREE (C3M0075120D), Infineon (IMW120R090M1H) and Rohm (SCT3080KR) Corporation, respectively. The rated voltage of these devices is 1200 V.

![Cross-sectional views of planar and trench SiC MOSFETs](image)

**Figure 1.** Schematic cross-sectional view of (a) planar structure, (b) trench structure and (c) double trench structure of SiC MOSFET power devices.

The TID experiment was performed at the National Institute of Metrology, China. Co-60 gamma rays were sourced at a dose rate of 50 rad (Si)/s. The device samples were irradiated under on-bias condition. The on-bias condition was $V_{GS} = 15$ V and $V_{DS} = 0$ V. The planar devices were irradiated to a total dose of 600 krad(Si) and the trench and double trench devices were irradiated to a total dose of 150 krad(Si).

The studied SC characteristics were needed for characterization by a SC test platform. The SC characteristics test platform is shown in Figure 2. Figure 2a shows the schematic of SC test circuit. Figure 2b is the picture of the SC test platform. Figure 2c is the theoretical waveforms of SC.

![SC test platform](image)

**Figure 2.** SC test platform. (a) The schematic of SC test circuit, (b) a picture of the SC test platform and (c) SC theoretical waveforms.
3. Experimental Results

3.1. Measured Threshold Voltage after Irradiation

The measured threshold voltages (VTH) for the planar and trench SiC MOSFET at different dose levels are shown in Figure 3. The VTH decreases with dose for the planar and trench SiC MOSFET but with different rates of degradation. For the planar SiC MOSFET, the VTH degraded only about −1 V as the dose accumulated to 600 krad(Si). However, for the trench SiC MOSFET, the VTH shifts of approximately −2.5 V and −4.5 V for cool trench and double trench with dose accumulated to 150 krad(Si), respectively.

![Figure 3](image1.png)

**Figure 3.** Measured VTH variations of planar and trench SiC MOSFET with different accumulated doses.

3.2. Measured SC Characteristics of Planar SiC MOSFET after Irradiation

Figure 4 shows the measured typical SC waveforms of the planar SiC MOSFET with a DC voltage as high as 600 V, which corresponds to 50% of the rated breakdown voltage. From Figure 4, it can be seen that, at the SC time reaches about 5.5 μs, the gate voltage drops rapidly to gate turn-off voltage. At this time, the drain current rapidly drops, but the device is not completely turned off, and the drain current slowly drops from about 28 A. However, as the SC time reaches about 8.2 μs, the gate voltage suddenly increases, and the device encounters a gate source failure. By testing the SC waveforms of the twelve planar SiC MOSFET samples, these devices’ SC failures before and after irradiation are all gate source failures, and the measured equivalent resistance of the gate source is several Ω to thousands of Ω.

![Figure 4](image2.png)

**Figure 4.** Measured SC waveforms of planar SiC MOSFET.

The SCWE and SCWT of the planar SiC MOSFET can be calculated by the SC waveforms of Figure 4, as shown in Figure 5. Figure 5 shows the SCWE and SCWT of the
planar SiC MOSFET before and after irradiation. From Figure 5, it can be seen that, as the dose is accumulated to 300 krad(Si), SCWE and SCWT decrease to about 462 mJ and 5.2 µs from rated SCWE 471 mJ and rated SCWT 5.6 µs for fresh devices, respectively. The reduction rates of SCWE and SCWT are 1.9% and 7.1%, respectively. However, as the dose accumulates to 600 krad(Si), SCWE and SCWT decrease sharply to about 406 mJ and 4.6 µs, respectively. Their reduction rates are 13.8% and 17.9%, respectively. By comparing the degradation rates of SCWE and SCWT at lower doses (TID = 300 krad(Si)) and higher doses (TID = 600 krad(Si)), we can know that the SC characteristics of planar SiC MOSFET are less affected by lower TID. For the abrupt reduction in SCWT at TID = 600 krad(Si), we guess that higher doses caused some defects inside the device.

![Figure 5](image.png)

**Figure 5.** Calculated SCWE and SCWT of planar SiC MOSFET before and after irradiation.

### 3.3. Measured SC Characteristics of Trench SiC MOSFET after Irradiation

Figures 6 and 7 are the typical SC waveforms of the cool trench and double trench SiC MOSFET with a DC voltage as high as 600 V, respectively. From Figures 6a and 7a, we can see that the drain current of the cool trench and double trench SiC MOSFET drops slowly, while the gate voltage is turned off and then suddenly increases, and the devices encounter gate source failure. Figures 6b and 7b show that the drain current of cool trench and double trench SiC MOSFET drops slowly, while the gate voltage is turned off and then the drain current and the gate voltage suddenly increase, and the devices encounter thermal runaway failure.

![Figure 6](image.png)

**Figure 6.** Measured SC waveforms of trench SiC MOSFET. (a) Gate-source failure and (b) thermal runaway failure.
The radiation-induced trapped charges will influence the robustness of the device, and then the trapped positive charge is the main cause of the threshold voltage shifting negatively.

By runaway thermal effect, the VTH variation of the planar SiC MOSFET is much smaller than that of the trench SiC MOSFET under the higher dose levels, the SCWE and SCWT variation of the planar SiC MOSFET is larger.

Figure 7. Measured SC waveforms of double trench SiC MOSFET. (a) Gate-source failure and (b) thermal failure.

The SCWE and SCWT of the cool and double trench SiC MOSFET can be calculated by the SC waveforms of Figures 6 and 7, as shown in Figure 8. Figure 8a,b shows the SCWE and SCWT of the cool and double trench SiC MOSFET before and after irradiation, respectively. From Figure 8a, it can be seen that, as the dose accumulated to 150 krad(Si), the SCWE and SCWT of the cool trench SiC MOSFET are improved, but these variations are very small. In addition, Figure 8b shows that, as the dose accumulated to 150 krad(Si), the SCWE and SCWT of the double trench SiC MOSFET did not change.

Figure 8. Calculated SCWE and SCWT of SiC MOSFET before and after irradiation. (a) Cool trench SiC MOSFET and (b) double trench SiC MOSFET.

4. Analysis and Simulations

TID caused oxide-trapped charges and interface charges in the gate oxide (GOX) [15]. In contrast to the interface charges, TID caused substantial oxide-trapped charges in GOX. The trapped positive charge is the main cause of the threshold voltage shifting negatively. The radiation-induced trapped charges will influence the robustness of the device, and then affect the SC withstand. For example, the SCWT of the device decreases after irradiation, and the lattice temperature of the device after irradiation is significantly higher than that of the device before irradiation under the same SCWT conditions. Based on the above analysis, the reason for the SCWE and SCWT rapidly decreasing during higher dose levels is perhaps that the device works in a radiation environment for a long time, and the radiation-induced trapped charges will produce serious defects inside the device. In this analysis, although the VTH variation of the planar SiC MOSFET is much smaller than that of the trench SiC MOSFET under the higher dose levels, the SCWE and SCWT variation of the planar SiC MOSFET is larger.
To further explore the mechanisms of the SCWE and SCWT variations before and after irradiation, 2D TCAD models are developed. We chose the SiC MOSFET of planar structure as an example for simulation studies. Standard SiC device physical models were used, including the Shockley–Read–Hall (SRH) recombination, mobility as a function of doping, and bandgap narrowing. The models were built based on the known structures (similar to those in Figure 1a) and parameters calibrated by fitting simulation results to measurement data for the fresh SiC MOSFET. Figure 9 shows the transfer characteristics (shown in Figure 9a) and breakdown characteristics (shown in Figure 9b) of the measured device and the simulation model. From Figure 9, it can be seen that the simulation results fit relatively well with the test results. To imitate the TID effect, charges are placed inside the GOX, 5 nm from the SiC-SiO2.

Figure 9. Simulation and measured non-irradiated (a) threshold characteristics and (b) breakdown characteristics curves for SiC MOSFET power devices with planar structure.

Figure 10a,b shows the simulation results of drain current and maximum lattice temperature for a fresh model and an irradiation model, respectively. From Figure 10a, we can see that the device failure at short-circuit time (tsc) is equal to about 7 µs after irradiation, while the device does not fail at tsc = 7 µs before irradiation. And, as the accumulated dose increases, the device failure is more serious. Figure 10b shows the lattice temperature of the device during SC states before and after irradiation. For the increase in the device lattice temperature, we speculate that this is due to the trapped charges in the GOX by the TID, which leads to the degradation of the VTH (as shown in Figure 3) of the device and generates damage inside the device. When the devices experience a SC, the damage caused by the TID inside the devices become more severe, resulting in an increase in the lattice temperature of the devices. The lattice temperature of the device increases continuously as the dose accumulates after tsc = 7 µs, as shown in Figure 11. Figure 11a–c shows the lattice temperature distribution of the device with tsc = 20 µs before and after irradiation, respectively. From Figure 11, it can be seen that the lattice temperature of the device is the highest at higher dose levels. A higher temperature will cause the device to heat up, causing the device to fail. When the device fails after a SC process, the physical phenomenon of the device after the failure shows that the electric field distribution around the drifting area and p-base decreases, as shown in Figure 12. In addition, the impact ionization distribution in these regions is also reduced, as shown in Figure 13. However, the total current density increases in these regions, as shown in Figure 14.
Figure 10. Simulated (a) drain current and (b) maximum lattice temperature of SiC MOSFET during SC test before and after irradiation with $N_{\text{not-GOX}} = 1.8 \times 10^{12}$/cm$^2$ and $N_{\text{not-GOX}} = 2.5 \times 10^{12}$/cm$^2$.

Figure 11. Simulated lattice temperature distribution of the SiC MOSFET with tsc equal to 20 µs (a) before irradiation and after irradiation with (b) $N_{\text{not-GOX}} = 1.8 \times 10^{12}$/cm$^2$ and (c) $N_{\text{not-GOX}} = 2.5 \times 10^{12}$/cm$^2$.

Figure 12. Simulation results of electric field distribution under the short-circuit state of tsc equal to 20 µs (a) before irradiation and after irradiation with (b) $N_{\text{not-GOX}} = 1.8 \times 10^{12}$/cm$^2$ and (c) $N_{\text{not-GOX}} = 2.5 \times 10^{12}$/cm$^2$.

Figure 13. Simulated impact ionization distribution of the SiC MOSFET with tsc equal to 20 µs (a) before irradiation and after irradiation with (b) $N_{\text{not-GOX}} = 1.8 \times 10^{12}$/cm$^2$ and (c) $N_{\text{not-GOX}} = 2.5 \times 10^{12}$/cm$^2$. 
5. Conclusions

This paper experimentally measured the SCWE and SCWT variations for 1200 V commercial planar and trench SiC MOSFET power devices induced by TID. The SCWE and SCWT variations of planar and trench SiC MOSFET power devices behave differently before and after irradiation. Compared with the SCWE and SCWT variations of the planar and trench, the SCWE and SCWT of the planar changes greatly before and after irradiation, while the SCWE and SCWT of the trench are almost unchanged. These behaviors indicate that the SCWE and SCWT of different structural devices are greatly affected by the dose level. The higher dose level will make the SCWE and SCWT of these devices change greatly. The SCWE and SCWT variations of the planar SiC MOSFET can be attributed to radiation-induced charges in the GOX. These results provide some insights for the SiC MOSFET to be used in space radiation environments.

Author Contributions: Conceptualization, L.S.; methodology, S.-W.L.; software, X.-Y.F.; validation, T.-D.L.; and L.W.; formal analysis, L.S.; investigation, L.S. and Y.-Y.L.; resources, J.W.; data curation, F.-Z.; writing—original draft preparation, L.S.; writing—review and editing, Y.-F.Z.; visualization, Z.-Y.W.; supervision, H.-L.L.; project administration, Y.-F.Z.; funding acquisition, L.S. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported, in part, by the National Natural Science Foundation of China under Grant 62204019 and 52207199, and in part, by the Science and Technology Innovation Program of Hunan Province under Grant 2021RC2044.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

2. Na, J.; Kim, K. A Novel 4H-SiC Double Trench MOSFET with Built-In MOS Channel Diode for Improved Switching Performance. Electronics 2023, 12, 92. [CrossRef]


12. Hazdra, P.; Popelka, S. Displacement damage and total ionization dose effects on 4H-SiC power devices. IET Power Electron. 2019, 12, 3910–3918. [CrossRef]


Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.