Memristor-Based D-Flip-Flop Design and Application in Built-In Self-Test

Guangzhen Dai 1,2, Wenxin Xie 2, Xingyan Du 2, Mingjun Han 1,2, Tianming Ni 1,2 and Daohua Wu 1,2,*

Abstract: There are several significant advantages of memristors, such as their nano scale, fast switching speed, power efficiency and compatibility with CMOS technology, as one of the alternatives in the next generation of semiconductor storage devices. D-flip-flops (DFFs) based on the traditional CMOS process have some shortcomings, including a large area, high power, and charge leakage when scaling down. However, memristors offer a new approach to the design of DFFs with improved performance. Two simplified edge-triggered DFFs are proposed to reduce the number of devices via the Memristor-Rationed Logic (MRL) method, which utilizes the characteristic of transmitting signals in the two-stage inversion structure. In addition, two new 4-bit Linear Feedback Shift Registers (LFSRs) are designed and verified using the proposed DFFs. Compared to the partially existing LFSRs, the designed LFSRs reduce the number of devices significantly, decrease the power consumption by 32.7% and 33.3% and shorten the delay time by 34.5% and 30.7% for the NOR and NAND gates, respectively. Finally, the proposed falling-edge-triggered DFF is used to implement the major blocks of the Built-In Self-Test (BIST) circuit, and the simulation results confirm their correctness and feasibility.

Keywords: memristor; MRL; DFF; register; BIST

1. Introduction

In 1971, Professor Chua predicted the existence of the fourth passive component besides resistance, capacitance and inductance, namely the memristor, which has a unique hysteresis curve in the I–V plane [1]. However, the memristor remained a theoretical concept for many years, until the HP Lab team implemented the first physical memristor using titanium dioxide in 2008 [2]. This proved the feasibility of the memristor and was marked as a significant milestone. Since then, the memristor has received considerable attention from researchers and scientists.

Despite improvements in CMOS technology, the scaling down of devices has become increasingly challenging due to leakage, power increases and circuit reliability reductions, etc. Consequently, energy-efficient and high-speed switching is no longer the main focus. However, the rise of memristors offers a promising approach to improving the performance of computer systems because of their advantages, such as their small size, high density, low power consumption, fast switching speed and even in-memory computing, which can break through the bottleneck of the Von Neumann architecture. In recent years, memristors have been applied in various fields, including chaotic circuits [3–5], digital circuits [6–12] and neural networks [13–15]. Several logic operations based on memristors have been proposed so far, such as Memristor-Aided Logic (MAGIC) [16], Material Implication (IMPLY) [17] and Memristor-Ratioed Logic (MRL) [18]. However, the fan-out number of cascade MAGIC is limited by its weak driving ability, because series resistors have a partial voltage determined the memristors’ resistance. Additionally, the logic operation can be
destructive for above-threshold voltages. IMPLY needs additional operational steps and has similar limitations. Hence, it is necessary to use active devices such as transistors to power passive components such as memristors and circuits. Herein, hybrid CMOS–memristor logic gates are employed to design subsequent sequential circuits.

Significant efforts have been made to enhance the performance of flip-flops, to obviate the shortcomings of the traditional CMOS technology in terms of chip area and power dissipation. An area-efficient flip-flop triggered by a dual-edge implicit pulse has been successfully developed by researchers using MOSFETs, reducing the power consumption by improving clock gating using a modified particle swarm optimization (MPSO) algorithm and decreasing the delay time via tristate inverters [19]. A flip-flop with an improved display pulse was proposed in ref. [20] to reduce the number of transistors while optimizing the speed and power dissipation compared to the existing display-pulse ones. In 2020, a thin-film complementary flip-flop circuit based on full-oxide thin-film transistors (n-type indium gallium zinc oxide and p-type tin monoxide) was proposed for the first time [21]. To further reduce the chip area, nanotechnology was applied, and a carbon nanotube field-effect transistor (CNFET) was also introduced to replace the traditional CMOS transistors in the design of a dynamic double-edge-triggered DFF, which reduced the power dissipation and delay time [22].

Although parameters such as the power and area of devices are improved as they are scaled down, the traditional CMOS process is unable to maintain Moore’s law. The MRL method is not only compatible with CMOS, but also has area and energy efficiency. Therefore, a linear feedback shift register was reported in ref. [23] using the hybrid CMOS–memristor, which has the characteristics of low power consumption and a fast conversion speed. However, there are more transistors applied in the design of this register.

As integrated circuit (IC) manufacturing process technologies have advanced to the deep sub-micron or even nanometer scale, the complexity and integration of circuit architectures is increasing more significantly. Consequently, the testing of ICs has already become a critical factor in terms of reducing the possibility of product failures and ensuring market competitiveness without full testability. Although automatic test equipment (ATE) can be used to test and analyze ICs, it is a time-consuming and costly process. To deal with this, an automatic on-chip testing methodology with a built-in self-test (BIST) was proposed in ref. [24]. Additionally, a hybrid logic built-in self-test (LBIST) was reported in ref. [25], which has the advantages of reducing the test time and quickly locating faults in the circuit during detection.

Therefore, NOR and NAND gate circuits are designed using the MRL structure, which has been optimized by adopting transistors implemented with a 50nm BSIM4 model [26]. Based on these two logic gates, two types of DFFs with different trigger modes and structures are proposed. In comparison, there are fewer devices employed in the edge-triggered structure to maintain blocking. Then, new linear feedback shift registers are designed with these DFFs and used in a built-in self-test (BIST) and other aspects. The circuit architecture of the traditional CMOS processes not only occupies a large amount of chip area but also increases the costs. Therefore, nanoscale memristor devices are introduced into the BIST circuit design herein, in order to reduce the area and power consumption and improve the speed, etc., efficiently.

2. Memristor-Based Logic Gates
2.1. Memristor Model

HP Labs fabricated the first physical memristor device using titanium dioxide [2], as shown in Figure 1, where $D$ is the total length, and $W_1$ and $W_2$ are the widths of the doped region and the undoped region, respectively. When a forward bias is applied to the device, oxygen vacancies with a positive charge are diffused to the undoped terminal, resulting in an increase in the width of $W_1$; thus, the resistance status of the device becomes low, as $R_{\text{ON}}$ [27]. Conversely, the resistance increases with $R_{\text{OFF}}$. Hereby, a SPICE model with a definite hysteresis curve and threshold is proposed, as in Equation (1), for generalized
memristor devices [28], where $a_1$, $a_2$ and $b$ are real factors, and $I(t)$ and $V(t)$ are the current and voltage, respectively.

$$I(t) = \begin{cases} 
  a_1 x(t) \sinh(bV(t)), & V(t) \geq 0 \\
  a_2 x(t) \sinh(bV(t)), & V(t) \leq 0 
\end{cases}$$ (1)

$x(t)$ in Formula (2) is written as

$$\frac{dx}{dt} = \eta g(V(t)) f(x(t))$$ (2)

where $\eta$ determines the positive and negative polarity of the voltage, and $g(V(t))$ is expressed as

$$g(V(t)) = \begin{cases} 
  A_p(e^{V(t)} - e^{V_p}), & V(t) > V_p \\
  -A_n(e^{-V(t)} - e^{V_n}), & V(t) < -V_n \\
  0, & -V_n \leq V(t) \leq V_p 
\end{cases}$$ (3)

where $V_p$ and $V_n$ are positive and negative threshold voltages, and $A_p$ and $A_n$ are adjustable amplitudes. $f(x)$ is the following expression, $w_n$ and $w_p$ are window functions, and $x_n$ and $x_p$ are state values near the negative and positive ends of the memristor, respectively.

$$f(x) = \begin{cases} 
  e^{-\Delta_p(x-x_p)w_p(x,x_p)}, & x \geq x_p \\
  1, & x \leq x_p 
\end{cases}$$ (4)

$$f(x) = \begin{cases} 
  e^{\Delta_n(x+x_n-1)w_n(x,x_n)}, & x \leq 1-x_n \\
  1, & x > 1-x_n 
\end{cases}$$ (5)

This model is simulated in LTspice, and its hysteresis curve is shown in Figure 2. The parameters of the model defined for the simulation are listed in Table 1.

Figure 1. Model of HP memristor.

$$I(t) = \begin{cases} 
  a_1 x(t) \sinh(bV(t)), & V(t) \geq 0 \\
  a_2 x(t) \sinh(bV(t)), & V(t) \leq 0 
\end{cases}$$ (1)

$x(t)$ in Formula (2) is written as

$$\frac{dx}{dt} = \eta g(V(t)) f(x(t))$$ (2)

where $\eta$ determines the positive and negative polarity of the voltage, and $g(V(t))$ is expressed as

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  1, & x \leq x_p 
\end{cases}$$ (4)

$$f(x) = \begin{cases} 
  e^{\Delta_n(x+x_n-1)w_n(x,x_n)}, & x \leq 1-x_n \\
  1, & x > 1-x_n 
\end{cases}$$ (5)

This model is simulated in LTspice, and its hysteresis curve is shown in Figure 2. The parameters of the model defined for the simulation are listed in Table 1.
Table 1. Parameters of the memristor model.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( a_1 )</th>
<th>( a_2 )</th>
<th>( b )</th>
<th>( V_p )</th>
<th>( V_n )</th>
<th>( A_p )</th>
<th>( A_n )</th>
<th>( x_p )</th>
<th>( x_n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>Value</td>
<td>0.12</td>
<td>0.12</td>
<td>0.05</td>
<td>0.16</td>
<td>0.15</td>
<td>30,000</td>
<td>30,000</td>
<td>0.3</td>
<td>0.3</td>
</tr>
</tbody>
</table>

2.2. Logic Gates Based on Memristor

The performance of logic circuits can be improved efficiently by MRL based on nanoscale memristors. Some logic gates, such as NOR and NAND, have been implemented utilizing MRL [18]. Herein, the inverters in the logic gates are designed using MOS transistors with 50 nm BSIM4 models [26]. Supposing that \( V_{\text{high}} = 1, V_{\text{low}} = 0 \), as shown in Figure 3a, if \( A = 1 \) and \( B = 0 \), then the output of memristor \( V_1 \) is

\[
V_1 = \frac{R_{\text{OFF}}}{R_{\text{ON}} + R_{\text{OFF}}} V_{\text{high}} = 1
\]  

(6)

When \( V_1 = 1 \), PMOS transistor \( T_2 \) is cut off and NMOS \( T_1 \) is switched on. Therefore, the output of the NOR gate \( V_{\text{out}} = 0 \). Analogously, when input signals \( A \) and \( B \) take other values, the corresponding outputs are consistent with the logic truth table of the NOR gate. The working process of the NAND is roughly the same. The simulation results of the logic gates displayed in Figure 4 are in agreement with the corresponding truth table.

![Figure 3. Memristor-based logic circuits: (a) NOR gate, (b) NAND gate.](image)

![Figure 4. Simulation results of (a) NOR gate, (b) NAND gate.](image)

3. DFF Design

3.1. Design of Level DFF Circuit

Based on the NOR and NAND gates, two structures of a DFF are designed, as displayed in Figure 5a,b, respectively, where (a) is a low-level flip-flop and (b) is a high-level flip-flop. The simulation results obtained when they are implemented in LTspice are illustrated in Figure 6. The output \( Q_s \) of these two DFFs vary with the input \( D_s \) when the clock input is low and high, respectively, as shown in Figure 6a,b.
Figure 5. Schematics of DFFs based on (a) NOR (triggered at low level) and (b) NAND gate (triggered at high level).

Figure 6. Simulated results of DFFs based on (a) NOR gate and (b) NAND gate.

The simulation results demonstrate the feasibility of DFFs based on memristors. However, the level-triggered mode may cause the DFF to flip several times during the effective clock signal, leading to a weak anti-interference ability. Therefore, DFFs with an edge-triggered mode are designed below to improve the reliability and anti-interference ability.

3.2. Design of Edge DFF Circuit

Two edge-triggered DFFs with master and slave latches have been designed, as shown in Figure 7. These DFFs are effectively triggered by the falling edge and rising edge of the clock signal, respectively, as illustrated in Figure 8a,b. Table 2 describes the functions of these DFFs (* denotes times other than the falling edge; • indicates times other than the rising edge). These DFFs have also been implemented and simulated in LTspice, and the simulation results are depicted in Figure 8.

Table 2. Master–slave DFF truth table based on NOR and NAND gates.

<table>
<thead>
<tr>
<th></th>
<th>CLK</th>
<th>D</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOR</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
<td>0</td>
<td>maintain</td>
</tr>
<tr>
<td>↓ (falling edge)</td>
<td></td>
<td>1</td>
<td>set 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>set 1</td>
</tr>
<tr>
<td>NAND</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>•</td>
<td></td>
<td>0</td>
<td>maintain</td>
</tr>
<tr>
<td>↑ (rising edge)</td>
<td></td>
<td>1</td>
<td>set 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>set 1</td>
</tr>
</tbody>
</table>
Figure 7. Schematics of master–slave DFFs based on (a) NOR and (b) NAND gate.

Figure 8. Simulation results of master–slave DFFs designed using (a) NOR and (b) NAND gate.

The master–slave DFFs above consist of two identical flip-flops; each has a two-stage inversion structure. Therefore, the master flip-flop’s output can be fed back to the input and the constructed NOR memristors can be combined to simplify the structure of the circuit, resulting in more area and energy efficiency. Furthermore, the proposed DFFs maintain the blocking characteristics during maintenance, as shown in Figure 9. The simulation results of these DFFs, illustrated in Figure 10, are consistent with the truth table presented earlier. The improved DFFs have 3 fewer memristors and 10 fewer CMOS transistors than their predecessors. Table 3 shows the parameters for the improved DFFs.

Figure 9. Improved DFFs with blocking-maintaining structure based on (a) NOR and (b) NAND gate.
Figure 10. Simulation of DFFs with blocking-maintaining structure based on (a) NOR and (b) NAND gate.

Table 3. Improved parameters of DFFs.

<table>
<thead>
<tr>
<th>Design</th>
<th>Input Voltage (V)</th>
<th>Power (µW)</th>
<th>Delay (ns)</th>
<th>Memristor</th>
<th>MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFF (NOR)</td>
<td>1</td>
<td>44.72</td>
<td>0.497</td>
<td>13</td>
<td>12</td>
</tr>
<tr>
<td>DFF (NAND)</td>
<td>1</td>
<td>41.96</td>
<td>0.508</td>
<td>13</td>
<td>12</td>
</tr>
</tbody>
</table>

To verify the proposed DFFs’ feasibility, two test circuits are designed by connecting LEDs as loads to their outputs. The circuit and simulation results are shown in Figures 11 and 12, respectively, where (a) and (b) are triggered at the falling edge and the rising edge, respectively.

Figure 11. Schematic diagram of DFFs with load triggered at (a) falling edge and (b) rising edge.

Figure 12. Simulation of DFFs’ load based on (a) falling edge and (b) rising edge.
The simulation results show that the LEDs light up when the outputs of the DFFs are high.

4. Linear Feedback Shift Register Design

Registers are critical components in digital sequential circuits and are in high demand in processors. Although latches are usually used to store bit data, flip-flops entail a large area and power overhead. As very important high-speed storage components, registers temporarily store instructions, data and addresses and are widely applied in various digital systems and microcontrollers. Figure 13 shows the two structures of a 4-bit linear feedback shift register (LFSR) mainly designed via the aforementioned improved DFFs. The driving equation and the state equation of the two 4-bit LFSRs are defined in Equations (7) and (8), respectively. Both of these DFFs have an identical state transition diagram (STD), as shown in Figure 14. Each DFF of the 4-bit LFSR is triggered at each falling edge of clk, as shown in Figure 15a. However, input D does not change immediately due to the transmission delay between the time that the falling edge of clk arrives and the established time of the new state of a DFF. Consequently, the state of the subsequent DFF varies according to the original Q state of the previous DFF. The final result is that all the initial codes in the 4-bit LFSR are shifted one bit to the right at each falling edge of clk. Figure 15b shows that the DFF is triggered at the rising edge of clk. The simulation results of the two 4-bit LFSRs shown in Figure 15 are consistent with the STD in Figure 14.

\[
\begin{align*}
D_0 &= Q_0 \oplus Q_3 \\
D_i &= Q_{i-1} (i = 1, 2, 3) \\
Q_0^* &= Q_0 \oplus Q_3 \\
Q_i^* &= Q_{i-1} (i = 1, 2, 3)
\end{align*}
\]

Figure 13. Four-bit LFSRs based on (a) NOR gate, (b) NAND gate.

Figure 14. STD of the 4-bit LFSR.
Figure 15. Simulation results for the 4-bit LFSRs based on (a) NOR gate and (b) NAND gate.

The functionality of the proposed register circuits is verified through LTSpice simulations carried out with the settings listed in Table 4. The comparison results of the partial existing LFSRs and the ones proposed in this work are demonstrated in Table 5, where the power delay product (PDP) effectively demonstrates the characteristics of circuit power consumption and delay. It represents the product of power consumption and the delay time. The smaller the PDP, the better the working performance of the circuit. The two LFSRs reported in refs. [29,30], engineered with the traditional MOS transistors, require an excessive number of devices, resulting in high power consumption and a long delay time. The LFSR reported in ref. [23] is more energy-efficient than the former ones, although it employs 64 memristors and transistors. In contrast, the two LFSRs proposed herein optimize both the number of devices and the power consumption.

Table 4. Simulation settings.

<table>
<thead>
<tr>
<th>Technology</th>
<th>Supply Voltage</th>
<th>Timestep</th>
<th>Temperature</th>
<th>Default Integration Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 nm</td>
<td>1 V (based on NOR/NAND)</td>
<td>0.1 µs</td>
<td>27 °C</td>
<td>modified trap</td>
</tr>
</tbody>
</table>

Table 5. Comparison of different works.

<table>
<thead>
<tr>
<th>Design</th>
<th>Ref. [30]</th>
<th>Ref. [29]</th>
<th>Ref. [23]</th>
<th>This Work (NOR)</th>
<th>This Work (NAND)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay (ns)</td>
<td>0.813</td>
<td>0.841</td>
<td>0.551</td>
<td>0.583</td>
<td></td>
</tr>
<tr>
<td>Input Voltage (V)</td>
<td>1.8</td>
<td>1.8</td>
<td>4</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Memristor</td>
<td>0</td>
<td>0</td>
<td>64</td>
<td>56</td>
<td>56</td>
</tr>
<tr>
<td>MOSFET</td>
<td>318</td>
<td>81</td>
<td>64</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>9360</td>
<td>188</td>
<td>94.15</td>
<td>63.4</td>
<td>62.8</td>
</tr>
<tr>
<td>Power Delay Product (µJ)</td>
<td>7.609</td>
<td>0.079</td>
<td>0.035</td>
<td>0.037</td>
<td></td>
</tr>
</tbody>
</table>

5. Application of LFSR in Built-In Self-Test

With the increasing scale and complexity of ICs, the built-in self-test (BIST) has become an indispensable part of circuit and chip design. Direct testing methods rely on automatic test equipment (ATE) to detect the circuit under test (CUT), which can be expensive and time-consuming. Under the BIST test mode, these challenges can be overcome. The architecture block diagram of the traditional BIST scheme is shown in Figure 16 and consists of test pattern generation (TPG), the circuit under test (CUT), an output response analyzer (ORA) and a BIST controller. The TPG comprises an n-bit LFSR (as shown in Figure 17 with \( C_i = 1, C_i = 0 \) and \( L_i \) indicating connection, disconnection and logical operation, respectively) that generates pseudo-random test vectors that are supplied to the CUT. The output signal of the CUT is then received and detected by the ORA module.
Herein, a logic BIST (LBIST) approach is designed for self-testing logic circuits. Specifically, a 16-bit LFSR is implemented to generate a large number of pseudo-random test vectors in each cycle, which are then provided to the CUT module for testing. The TPG is composed of the 16-bit LFSR as displayed in Figure 18. The simulation results of the 16-bit LFSR are depicted in Figure 19.

A simple 4-bit ORA is designed to simulate the process of receiving and checking the output signal of the CUT. The simulation results of this 4-bit ORA are presented in Figure 20. In this figure, V(1), V(2), V(3) and V(4) represent the output results of the CUT, and V(out) is the output of this ORA. It is obvious that the 4-bit ORA is a parity checker, and V(out) is of a high level when the number of “1”s in V(1) to V(4) is odd, and low otherwise.
6. Conclusions

In this paper, the design method for a memristor proportional logic circuit is adopted to realize a register based on a memristor–CMOS hybrid circuit. First, level-triggered DFFs are designed using NAND and NOR gates based on memristors, and two edge-triggered DFFs are implemented while applying the master–slave structure. Then, two simplified edge-
triggered DFFs are proposed, utilizing the signals transmitted in the two-stage inversion. Compared to the reported designs, the new edge-triggered DFFs require fewer devices. Two new 4-bit LFSRs are engineered based on these DFFs and verified by simulation. In comparison to the partial existing LFSRs, this work improves the performance of the LFSR by reducing the number of devices significantly, decreasing the power consumption by 32.7% and 33.3% and optimizing the delay time by 34.5% and 30.7% for the NOR- and NAND-gate-based LFSRs, respectively. Finally, the proposed DFF triggered at the falling edge of the clock is applied to realize the main function of the BIST circuit, and a simulation is implemented to verify its correctness and feasibility.

Author Contributions: Conceptualization, G.D.; Formal analysis, T.N.; Investigation, M.H.; Writing—original draft, W.X.; Visualization, D.W.; Supervision, X.D. All authors have read and agreed to the published version of the manuscript.

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References
4. Li, K.; Li, R.; Cao, L.; Feng, Y.; Onasanya, B.O. Periodically Intermittent Control of Memristor-Based Hyper-Chaotic Bao-like System. Mathematics 2023, 11, 1264. [CrossRef]


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