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A Novel Three-Dimensional Sigma–Delta Modulation for High-Switching-Frequency Three-Phase Four-Wire Active Power Filters

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Abstract: This article presents a new modulation technique called three-dimensional sigma–delta (3D-ΣΔ) modulation for high-frequency three-leg four-wire voltage source converters (VSCs) that use wide-bandgap (WBG) semiconductors. These WBG devices allow for the use of high switching frequencies with a greater efficiency than silicon devices. The proposed 3D-ΣΔ technique enables operation at a variable switching frequency, resulting in a significant reduction in switching losses compared to classical pulse-width modulation (PWM) techniques. Moreover, the 3D-ΣΔ technique uses a fast-processing 3D quantiser that simplifies implementation and considerably reduces computational costs. The behaviour of the 3D-ΣΔ modulation is analysed using MATLAB/Simulink and PLECS. The experimental results performed on an active power filter that uses silicon carbide (SiC) MOSFETs demonstrate an improvement in converter efficiency compared to the conventional SPWM technique. Additionally, the experimental results show how 3D-ΣΔ allows for the compensation of harmonics and homopolar currents, thereby balancing the electrical grid currents. The experiments also show that the proposed 3D-ΣΔ modulation outperforms an SPWM technique in terms of power quality, since the former achieves a larger reduction in the harmonic content of the power grid. In conclusion, the proposed modulation technique is an attractive option for improving the performance of four-wire converters in active power filter applications.

Keywords: active power filter; fast algorithm; modulation technique; power converter; power electronics; power quality; power conversion harmonics; sigma–delta modulation; wide-bandgap semiconductors

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1. Introduction

Distorted power grids can damage the loads connected to them. For example, these distortions can cause malfunctions, reduce service life, decrease performance and even cause plant shutdowns and increase economic losses [1–3]. Usually, the equipment in a facility, such as power electronics devices with non-linear characteristics [1,4], distorts the power supply. In four-wire systems, a common problem is the flow of excessive currents through the neutral conductor. These currents are caused by unbalanced loads or non-linear loads that generate third harmonics and their multiples.

Shunt-connected active power filters (APFs) can solve this problem. In particular, four-wire APFs are those capable of compensating homopolar currents. In general, there are two modes for connecting the fourth wire [5–8]. The first type is connecting this wire from the midpoint of the DC-bus to the grid neutral. The converters that use this system are known as three-leg four-wire converters (3L4Ws). The 3L4W configuration offers a simple design and

balanced load distribution, presenting a cost-efficient solution. However, challenges related to load symmetry and harmonic compensation limitations warrant careful consideration. For all these reasons, 3L4W active power filters are widely used in the industry due to their lower cost and simplicity [8–11]. The second one is connecting the fourth wire to an additional leg. These converters are called four-leg four-wire converters (4L4Ws). Many works focus on 4L4W converters because of their higher capacity to compensate for homopolar currents and greater design flexibility [6,12–16]. Despite its potential for higher efficiency, concerns regarding system complexity and cost implications persist, since this configuration requires more semiconductors and components than 3L4W converters.

Figure 1 shows a 3L4W voltage source converter. In these power converters, zero currents flow through the neutral wire, so the phase currents may not be balanced. Therefore, the reference vector may not be contained in the $\alpha\beta$ plane—i.e., γ can be different from 0—so these converters require specific modulation techniques.

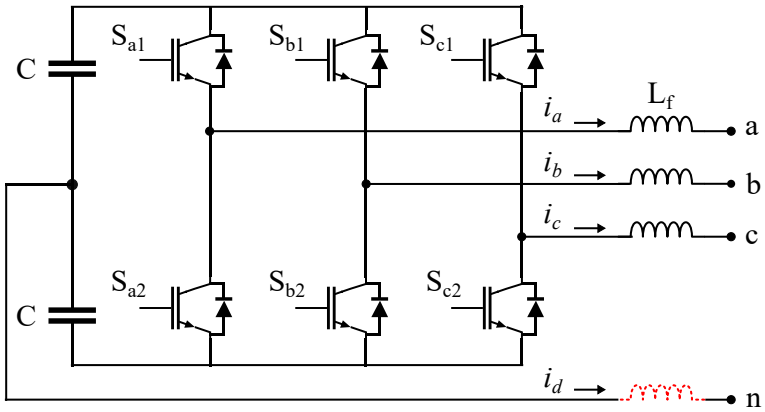

Figure 1. Three-leg four-wire voltage source converter. The red dashed line indicates the option for connecting an optional inductance to the neutral wire.

1.1. Modulation Techniques

Many modulation techniques for 3L4W converters have been proposed in the literature. Prats et al. proposed a generalised 3D space vector modulation for all types of three-leg converters, including multilevel and three-wire converters [17]. This vector modulation approach is computationally inexpensive, as it does not use trigonometric functions or look-up tables. Another generalised algorithm was presented in [18]. The paper introduced a 3D direct pulse-width modulation (PWM) for 3L4W and 4L4W converters. This strategy is a simplification of the 3D space vector modulation that can be applied to two-level and multilevel converters. Mandrioli et al. developed a variable switching-frequency PWM strategy that enhances the performance of 3L4W converters [19]. The modulation relies on the prediction of the phase current ripple and achieves a flat ripple profile with an optimal and low switching frequency range (from 1.6 to 5.1 kHz). Reference [20] analyses the output current ripple in grid-connected 3L4W converters using various continuous and discontinuous PWM schemes. The article examines the phase and neutral current ripple features, the switching losses and the harmonic performance of the PWM strategies. Moreover, it demonstrates that discontinuous PWM schemes achieve lower losses than continuous schemes while maintaining comparable current ripples. Multilevel converters based on silicon have better properties than their two-level counterparts. Therefore, many articles propose modulations for multilevel silicon-based converters. A simplified pulse-width modulation was proposed as an alternative to classical 3D modulations [21]. This modulation was designed for 3L4W neutral-point clamped (NPC) converters and allowed for determining which vectors to apply using only the polarity of the three-phase reference voltage. Reference [22] proposed a carrier-based pulse-width modulation for 3L3W and 3L4W NPC and T-type converters. The proposed technique uses a simple algorithm, balances the capacitors of the DC-bus and controls the oscillations in the midpoint. In [23],

the authors presented a family of 18-mode space vector pulse-width modulations for 3L4W NPC converters. These strategies reduce the switching frequency, so they exhibit higher performance than that of space vector pulse-width modulation. Finally, article [24] proposed using a dipolar pulse-width modulation to balance the midpoint of the DC-bus in 3L4W NPC converters. Additionally, this modulation allows for modifying the zero sequence to extend the modulation index in 3L3W NPC converters. Table 1 summarises the main characteristics of the previous modulations. Although the above modulations have interesting properties, they are all designed for multilevel converters working at low switching frequencies ($\leq$20 kHz).

1.2. Wide-Bandgap Semiconductors

A major trend in power electronics is to build high-frequency power converters based on wide-bandgap (WBG) semiconductors. These semiconductors have properties superior to those of silicon. They allow building high-power-density converters and can work at extremely high switching frequencies ($\geq$100 kHz) with fewer losses than their silicon counterparts [25–27]. Moreover, some two-level WBG converters exhibit lower losses than multilevel converters at several switching frequencies [28]. The most mature WBG semiconductors are gallium nitride (GaN) and silicon carbide (SiC). GaN devices are limited to low-voltage applications ($<$650 V), whereas SiC devices are preferred for high-voltage operations [26]. WBG devices have already been successfully used on several power electronics applications, such as microgrids [29], on-board chargers [30], electric vehicles [31], and APFs [32]. Furthermore, two-level 3L3W SiC converters are becoming the preferred topology in electric vehicles [31].

Table 1. Scope of previous modulation works.

Reference	Year	Modulation	Converter Topology	Modulation Type	Max. Switching Frequency
[17]	2003	3D SVM	3L4W	Vectorial	—
[18]	2008	3D PWM	3/4L4W	PWM	5 kHz
[19]	2021	VSF-PWM	3L4W	Spread-spectrum	5.1 kHz
[20]	2020	Several PWM	3L4W	PWM	3.6 kHz
[21]	2018	Simplified PWM	3L4W	PWM	10 kHz
[22]	2020	CB-PWM	3L3/4W	PWM	20 kHz
[23]	2018	18-mode SVPWM	3L4W	PWM	10 kHz
[24]	2018	Dipolar PWM	3L3/4W	PWM	10 kHz
This paper	2023	3D-ΣΔ	3L3/4W	Spread-spectrum	200 kHz

New modulation techniques designed to work at high switching frequencies are necessary to take advantage of these new WBG devices. Sigma–delta (ΣΔ) modulations are attractive techniques since they are spread-spectrum techniques. Hence, their switching frequencies are variable, so they produce fewer EMIs and losses than other modulation techniques, such as space vector pulse-width modulation [32,33]. Recently, these techniques have been proposed for two-level 3L3W converters [33,34] and two-level five-phase converters [35].

1.3. Proposal

This article proposes a generalisation of the sigma–delta strategy called three-dimensional sigma–delta (3D-ΣΔ) modulation. The proposed modulation is suitable for high-frequency, two-level 3L3W and 3L4W converters based on WBG semiconductors. Using the proposed modulation in two-level converters allows building high-power converters with fewer components, making them smaller and more affordable than classical multilevel converters. However, the proposed modulation could be adapted to work with multilevel power converters. Moreover, the proposed technique allows the following:

1. Working with a variable switching frequency and, consequently, reducing the switching losses;
2. Compensating for homopolar currents in four-wire systems when applied in 3L4W converters.

Furthermore, we propose a fast-processing quantiser for the 3D-ΣΔ technique to simplify its implementation and reduce the number of mathematical operations of the proposed modulation. The impact of the 3D-ΣΔ strategy is evaluated based on simulation studies using MATLAB/Simulink (version R2021b) and PLECS (version 4.7.6) software. Finally, the results are experimentally validated by implementing the proposed technique on a SiC-based 3L4W converter.

The rest of this article is organised as follows. Section 2 presents the 3D-ΣΔ modulation and its fast-processing quantiser. Section 3 introduces the control strategy. Section 4 analyses the behaviour of the proposed technique. Section 5 validates the previous results in a SiC-based 3L4W active power filter. Finally, Section 6 concludes this article.

2. Proposed Three-Dimensional Sigma–Delta

The scheme of the 3D-ΣΔ strategy is illustrated in Figure 2.

To analyse the proposed modulation, it is necessary to define the vector spaces $V = \{(a,b,c)^t \in \mathbb{R}^3\}$ and $W = \{(\alpha,\beta,\gamma)^t \in \mathbb{R}^3\}$. Hence, $T : V \rightarrow W$ is then defined as

$$T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (1)$$

which is a Clarke transformation.

The 3D-ΣΔ technique works in $\alpha\beta\gamma$ reference, so it is necessary to express the reference vector in these coordinates using T. Then, the modulation compares the reference vector to the quantiser outputs $(V'_\alpha, V'_\beta, V'_\gamma,)$ and integrates the resulting errors $(e_\alpha, e_\beta, e_\gamma)$. It may be necessary to add gains before the integrations to guarantee the system stability, as is detailed in [33]. Additionally, the modulation may include more integration loops. However, a maximum of two integrators should be used since the modulation may become noisy if three or more integrators are employed [36]. Finally, the integrated errors $(U_\alpha, U_\beta, U_\gamma)$ are the inputs of the quantiser, whose outputs are compared to the next reference vector.

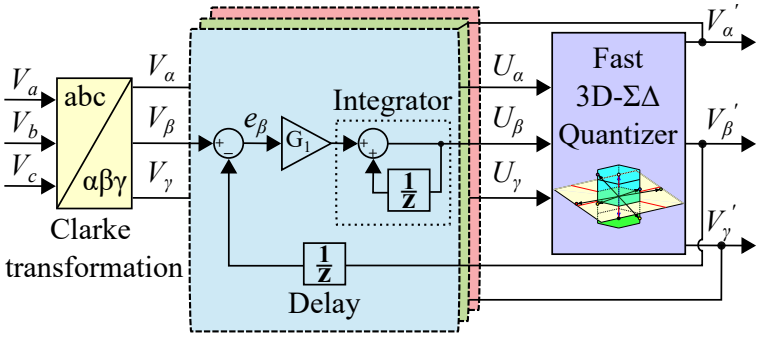

Figure 2. Three-dimensional sigma-delta modulation loop. The nominal value of all gains is unity.

The quantiser divides the vector space W into eight sectors: one for each possible switching vector. Figure 3 shows the sectors of the 3D-ΣΔ modulation. At each sampling instant, the quantiser determines the position and sector of the reference vector and synthesises it by applying the corresponding vector. Note that the switching vector may not be the closest one to the reference vector.

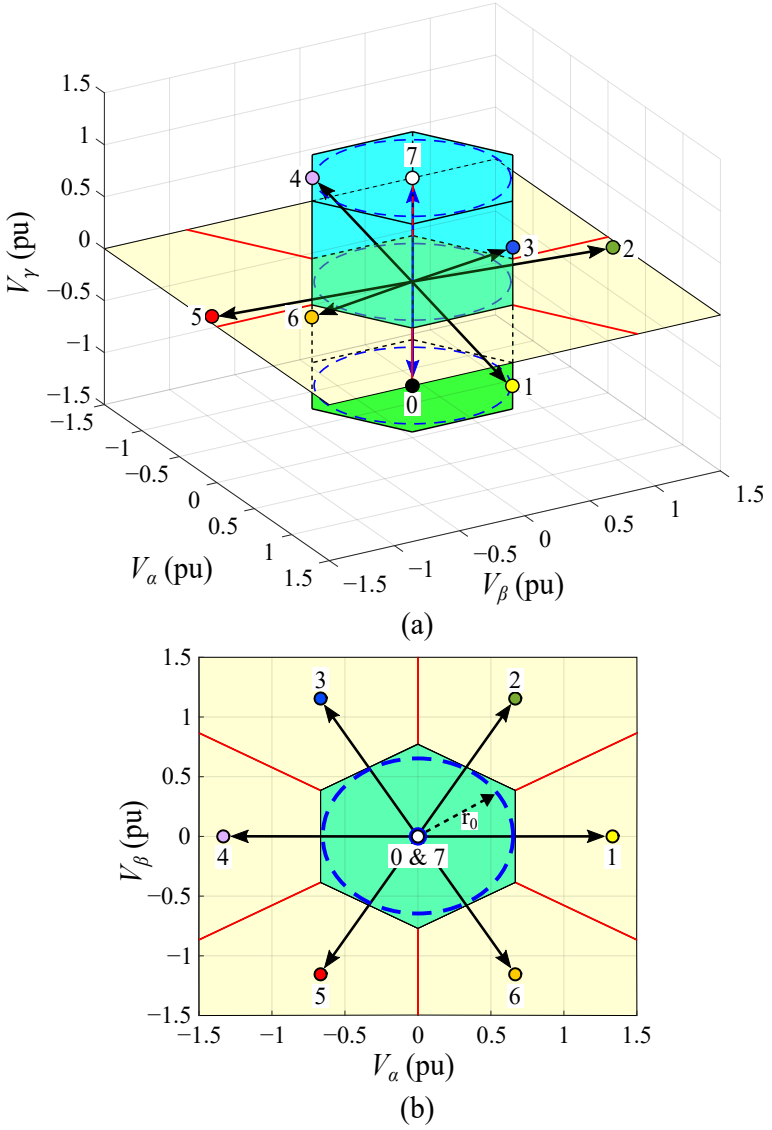

Figure 3. Two-level, three-phase converter switching states: (**a**) isometric view and (**b**) view from the zero-sequence axis.

As in H-ΣΔ modulation, the sector can be determined with branch and bound algorithms and by calculating distances from the reference vector to the projection of the possible switching vectors [33]. However, this paper proposes a fast quantiser that simplifies its implementation and reduces the number of required calculations.

The proposed fast quantiser is an improvement on those presented in [34], as the new algorithm allows for working in systems where the homopolar component is not zero. The presented fast quantiser defines the sectors of W as follows:

$$B_0 = \{x \in W : (\alpha^2 + \beta^2 \leq r_0^2) \wedge (\gamma < 0)\} \tag{2}$$

$$B_1 = \{x \in W : (\alpha^2 + \beta^2 > r_0^2) \wedge (\alpha \geq 0) \wedge (-k\alpha \leq \beta < k\alpha)\} \tag{3}$$

$$B_2 = \{x \in W : (\alpha^2 + \beta^2 > r_0^2) \wedge (\alpha \geq 0) \wedge (\beta \geq k\alpha)\} \tag{4}$$

$$B_3 = \{x \in W : (\alpha^2 + \beta^2 > r_0^2) \wedge (\alpha < 0) \wedge (\beta \geq -k\alpha)\} \tag{5}$$

$$B_4 = \{x \in W : (\alpha^2 + \beta^2 > r_0^2) \wedge (\alpha < 0) \wedge (k\alpha \leq \beta < -k\alpha)\} \tag{6}$$

$$B_5 = \{x \in W : (\alpha^2 + \beta^2 > r_0^2) \wedge (\alpha < 0) \wedge (k\alpha > \beta)\} \tag{7}$$

$$B_6 = \{x \in W : (\alpha^2 + \beta^2 > r_0^2) \wedge (\alpha \geq 0) \wedge (-k\alpha > \beta)\} \tag{8}$$

$$B_7 = \{x \in W : (\alpha^2 + \beta^2 \leq r_0^2) \wedge (\gamma \geq 0)\} \quad (9)$$

where $k = \tan(\pi/6)$ and $r_0 = [0.67, 0.77]$. Note that r_0 can take any value within the specified range, as this does not significantly affect the modulation, as shown in [34].

Given a point in space W, the above expressions can used to determine which sector the point belongs to. The procedure to determine the sector is as follows. First, the boundary values are calculated from the input, i.e., $U_\alpha^2 + U_\beta^2$ and $\pm kU_\alpha$. Then, the quantiser compares the input with them and with r_0. Notice that r_0 has been defined previously. The comparison result is a 5 b word that is used as the address of a read-only memory (ROM). The output of the ROM is the corresponding switching vector, as detailed in Table 2. Figure 4 depicts the flowchart of the proposed fast 3D-ΣΔ modulation. Table 3 quantifies the operations of the proposed fast quantiser and compares them with those of a standard quantizer.

Table 2. Determination of the sector in 3D-ΣΔ.

$U_\alpha^2 + U_\beta^2 \leq r_0^2$	$U_\gamma \geq 0$	$U_\alpha \geq 0$	$U_\beta \geq kU_\alpha$	$U_\beta \geq -kU_\alpha$	Sector	Switching State
0	Indifferent	0	0	0	B_5	−1−11
0	Indifferent	0	0	1	—	Indifferent
0	Indifferent	0	1	0	B_4	−111
0	Indifferent	0	1	1	B_3	11−1
0	Indifferent	1	0	0	B_6	1−11
0	Indifferent	1	0	1	B_1	1−1−1
0	Indifferent	1	1	0	—	Indifferent
0	Indifferent	1	1	1	B_2	11−1
1	0	Indifferent	Indifferent	Indifferent	B_0	−1−1−1
1	1	Indifferent	Indifferent	Indifferent	B_7	111

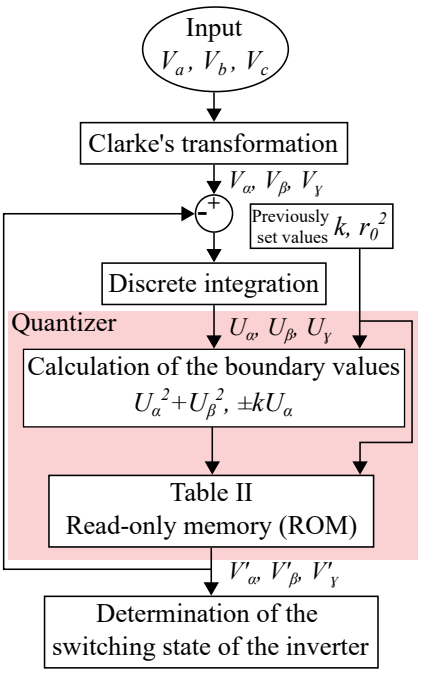

Figure 4. Flowchart of the proposed 3D-ΣΔ technique.

Table 3. Operations of the different quantisers for 3D-ΣΔ.

	Standard 3D-ΣΔ	Fast 3D-ΣΔ
Additions	7	1
Subtractions	14	0
Multiplications	14	4
Comparisons	1	5
ROM	No	Yes
Total	36	10

3. Control Strategy

Figure 5 shows the control system used in the active filter. This system allows the compensation of harmonics, reactive power and unbalances in the grid.

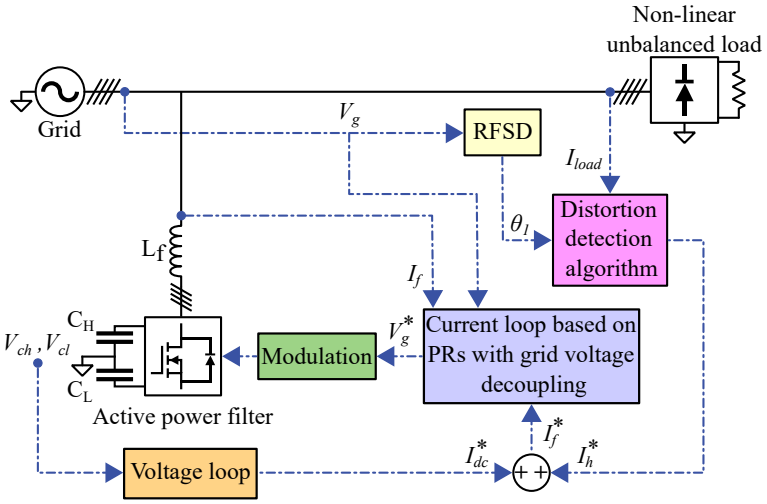

Figure 5. Overall block diagram control of the active power filter.

First, the algorithm uses a PLL specifically designed to work on distorted and unbalanced grids. This PLL is a rotationary frame sequence detector (RFSD), and its operation is detailed in [37]. The distortion detection algorithm determines the harmonics to be compensated by the filter, the reactive power and the current required to balance the electrical grid. In the filter under study, it is not necessary to determine the harmonics to be compensated, since the current loop incorporates resonant controllers [38]. However, the algorithm does determine the currents required to balance the grid when the load is unbalanced. After determining the required filter currents (I_f^*), these are controlled through cascaded resonant controllers within the current loop. These controllers ensure there are no errors in the harmonic frequencies [39,40]. Finally, the current loop outputs are the reference voltages of the 3D-ΣΔ modulation.

In addition to the previous algorithms, the control incorporates a voltage loop to balance the DC-bus and its capacitors. According to [41], the transfer function of the DC-link is

$$V_c(s) = \frac{3v_d}{2C_{dc}V_c s} I_{dc}^* \tag{10}$$

where v_d is the direct input voltage and V_c is the total DC-bus voltage at the operation point. Notice that V_c is the sum of the capacitor voltages ($V_c = V_{ch}^2 + V_{cl}^2$). Using (10), a PI controller can be designed to control the DC-bus voltage and balance the capacitors.

The current loop consists of several cascaded PR controllers. Cascaded non-ideal resonant controllers are defined using

$$G_{PR}(s) = k_p + \sum_{h=n}^{h=m} \frac{2k_{ih}\omega_c s}{s^2 + 2\omega_c s + (h\omega_1)^2} \tag{11}$$

where ω_1 is the fundamental frequency, h is the harmonic order to be compensated for, k_p is the proportional constant, k_{ih} is the individual resonant gain, and ω_c is the bandwidth around the resonant frequency. Notice that the bandwidth can be adjusted by setting ω_c appropriately. It may be necessary to tune each resonant controller separately to achieve accurate control.

Resonant controllers can be implemented digitally using second-order IIR filters with the following transfer function:

$$H(z) = \frac{b_1 z^{-1}}{a_2 z^{-2} + a_1 z^{-1} + a_0}. \tag{12}$$

The filter parameters can be calculated from k_i, the resonant frequency ($h\omega_1$), the bandwidth and the sampling time (T_s). The filter constants are defined as

$$b_1 = 4k_i T_s \omega_c \tag{13}$$

$$a_0 = T_s^2 (h\omega_1)^2 + 4T_s\omega_c + 4 \tag{14}$$

$$a_1 = 2T_s^2 (h\omega_1)^2 - 8 \tag{15}$$

$$a_2 = T_s^2 (h\omega_1)^2 - 4T_s\omega_c + 4. \tag{16}$$

4. Simulation Results

This section evaluates the impact of the proposed 3D-ΣΔ techniques on a VSC with SiC MOSFETs (Figure 1) operating as an APF. To assess the effects of the proposed modulations, the results are compared with those of the SPWM.

An important difference between SPWM and ΣΔ techniques is the switching frequency. The switching frequency is variable in ΣΔ modulations. In these techniques, the maximum switching frequency is always half the sampling frequency. Hence, this work uses the maximum switching frequency (f_{max}) as a comparison parameter between SPWM and 3D-ΣΔ. The maximum switching frequency is

$$f_{max} = \begin{cases} f_s \text{ for SPWM} \\ \frac{f_s}{n} \text{ for 3D-}\Sigma\Delta \end{cases} \tag{17}$$

where f_s is the sampling frequency, and n is an integer such that $n \geq 2 \; \forall \; n \in \mathbb{Z}$ $(n = 2, 3, 4, \ldots, \infty)$. The modulation index m is within the range of [0, 1].

4.1. System Model

The studied VSC is modeled using MATLAB/Simulink and PLECS Blockset. The rated power of the converter is 25 kVA; the DC-bus voltage is 400 V; and the AC-side currents are constant at their rated values (15 A). The maximum switching frequency is 200 kHz. The SiC MOSFET module FS45MR12W1M1_B11 manufactured by Infineon is used to simulate the converter switches. This module features a maximum drain source voltage (V_{ds}) of 1.2 kV and a continuous drain current (I_d) of 25 A at 75 °C. Each transistor has an external gate resistance of only 10 Ω, the deadtime is 100 ns and their junction temperatures are 90 °C. The PLECS software calculates the losses according to the thermal datasheet and the equations provided by the manufacturer [42]. The electrical grid used for the simulation is a European one with a phase-neutral voltage of 230 V and a frequency of 50 Hz.

4.2. Analysis of Simulation Results

The modulation techniques are studied in a grid-connected active power filter. The simulated APF compensates for the currents generated by a diode rectifier and an unbal-

anced load. In particular, the filter compensates for current unbalances and all harmonics up to 17. The resonant controllers have been designed to ensure a phase margin of more than 60° and a gain margin of more than 10 dB.

The harmonics and THD of the current have been meticulously calculated using the methodology specified by the IEC 61000-3-2 [43] and IEC 61000-4-7 [44] standards. Consequently, this analysis focuses solely on the initial 40 harmonics. The analysis excludes voltage harmonics, since shunt-connected active power filters are specifically designed to address and compensate for current harmonics. For a comprehensive examination of voltage harmonics resulting from ΣΔ modulations, a detailed analysis is provided in [33]. Regarding efficiency, it is determined through

$$\eta = 100 \cdot \left(1 - \frac{P_{loss}}{P_{in}}\right), \tag{18}$$

where P_{loss} represents the converter losses and P_{in} represents the input power to the converter.

Figure 6 shows the currents produced by the load. These current waveforms are typical of a diode rectifier and are highly non-linear. The load remains constant throughout the simulation, so the whole system is at steady state. Since the load is unbalanced, the magnitude of the harmonics and THD will vary between phases. The figure only shows phase A in the frequency domain, but all other phases are equivalent. Mainly, the load generates 5th and 7th harmonics, but it also produces other harmonics of significant amplitude, such as the 11th and the 13th. Additionally, the studied load is unbalanced, so currents flow through the neutral of the grid.

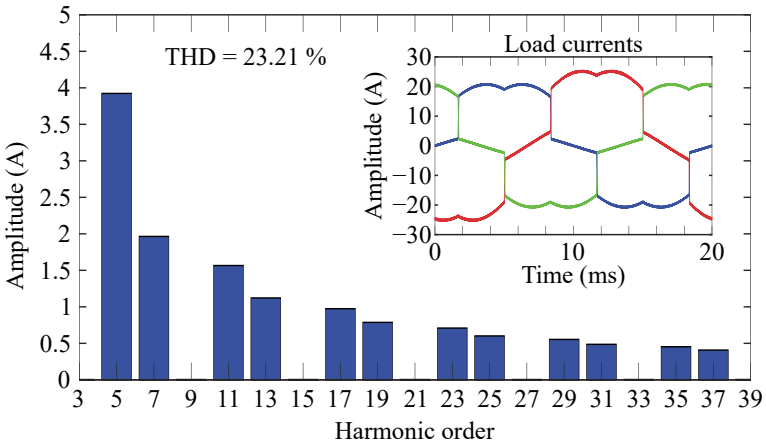

Figure 6. Characteristics of the simulated load.

Figure 7 plots the simulated grid currents when the APF is compensating for harmonics and unbalances. Figure 7a displays the grid currents when the modulation technique is the SPWM. The three grid currents are balanced, so the APF compensates for unbalances properly. The main current harmonics are lower than those produced by the load. However, some additional harmonics appear, such as 3rd, 9th and 15th harmonics, and others are slightly higher than those generated by the load. This behaviour happens because SPWM modulation may generate harmonics at low frequencies when the switching frequency is high, as discussed in [33,45]. Moreover, the figure shows that the efficiency of SPWM modulation is 94.67%. Figure 7b plots the currents when the APF uses the proposed 3D-ΣΔ strategy. This modulation also balances the currents, but, in addition, it fully compensates all harmonics up to the 17th. This technique does not produce additional harmonics, such as those at low frequencies. However, the ripple of the currents is slightly higher than that produced by an SPWM, since ΣΔ modulations distribute the switching harmonics at medium frequencies [34]. The efficiency of 3D-ΣΔ modulation is 96.40%, which is higher than that of SPWM modulation. This is because ΣΔ modulations operate with a

variable switching frequency, enabling them to switch at high frequencies with less loss than modulations that use fixed switching frequencies.

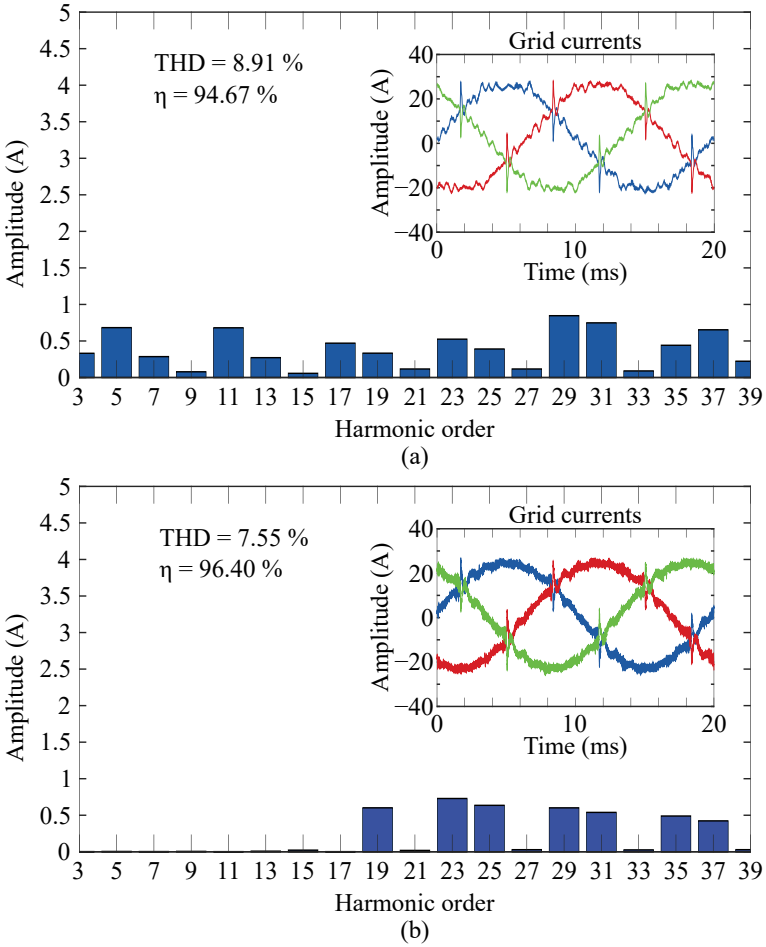

Figure 7. Simulated grid currents when the active power filter is compensating for harmonics and balancing the grid using different modulation strategies: (**a**) SPWM and (**b**) 3D-ΣΔ.

5. Experimental Results

To experimentally validate the 3D-ΣΔ modulation, we used a prototype that incorporates SiC semiconductors (FS45MR12W1M1_B11 from Infineon) from Infineon that were previously simulated. This prototype is designed to withstand powers up to 25 kVA. The SiC module features a maximum drain-source voltage of 1.2 kV and a continuous drain current of 25 A at 75 °C. On the DC side, there was a constant 400 Vdc source. On the AC side, there was a load. The modulation techniques were implemented on a dSPACE DS1006 platform and a DS5203 FPGA board. The 3D-ΣΔ modulation uses the fast quantiser proposed in Section 2 and the control detailed in Section 3. Grid currents were measured with a high-resolution oscilloscope (Agilent InfiniiVision MSO7104A: 1 GHz bandwidth and 4 GS/s sample rate) and current probes (Keysight N2783B: 100 MHz bandwidth). The THD measurement considers only the first 40 harmonics, as detailed in the standards IEC 61000-3-2 [43] and IEC 61000-4-7 [44]. The converter efficiency was measured using a digital power meter (Yokogawa WT1600: 1 MHz bandwidth).

The first experiment aims to compare the efficiency of the proposed 3D-ΣΔ modulation with the SPWM technique. To this end, a three-phase RL load with R = 45.3 Ω and L = 470 µH was connected to the AC side of the converter in an open loop. Moreover, the maximum switching frequency of the converter was 200 kHz. The open loop control was used to adjust the modulation index and examine the converter's efficiency at different operating points.

Figure 8 shows the experimental efficiencies of the converter. The results demonstrate that the efficiencies obtained using the 3D-ΣΔ modulation are higher than those obtained using the SPWM technique at all operating points. However, as the modulation index increases, the difference between the two techniques decreases. At m = 0.9, SPWM exhibits slightly lower efficiency than 95%, while 3D-ΣΔ achieves an efficiency close to 99%. This efficiency behaviour is consistent with previous work on ΣΔ modulations [33].

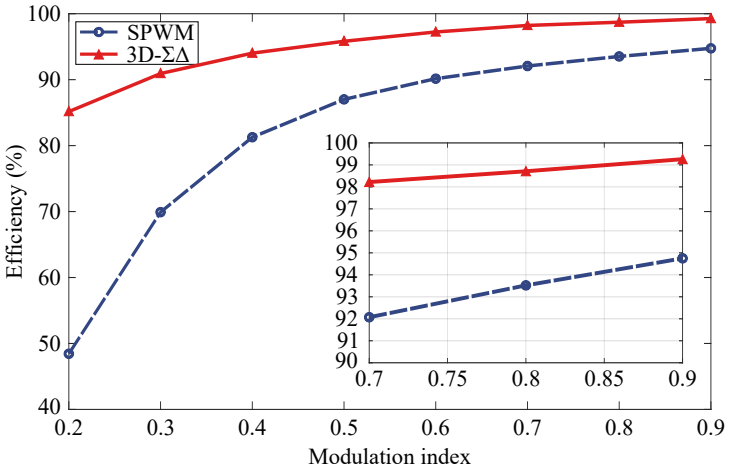

Figure 8. Experimental converter efficiency curves at f_{max} = 200 kHz.

The second experiment employs the converter working as an APF using both the SPWM modulation and the proposed 3D-ΣΔ technique at f_{max} = 200 kHz. Figure 9 shows the experimental setup. In this experiment, two loads are connected on the AC side: a non-linear load consisting of a diode rectifier and resistors with R = 40.5 Ω and an unbalanced resistive load with R = 57.6 Ω in phase A and R = 100 Ω in phases B and C.

Figure 10 illustrates the results obtained with the converter operating as an APF, i.e., in a closed loop. Figure 10a–c display the results without connecting the filter, i.e., the currents and distortion produced by the load. Figure 10a shows the currents produced by the load. These currents have the typical shape produced by a diode rectifier, and it can be observed that phase A is higher than the others since it has a less resistive load. Figure 10b shows the current in the neutral wire of the grid. This current is produced due to the unbalanced load and is a 50 Hz sine waveform. Figure 10c shows the THD and harmonic distribution of the currents produced by the load. The diode rectifier mainly produces odd harmonics of positive and negative sequences. The most prominent harmonics are the 5th and 7th, but others such as the 11th, 13th, and 17th are also significant. All THDs are similar, but phase A exhibits slightly less THD than the others. Figure 10d–f depict the experimental grid currents when the APF compensates for current harmonics and imbalances using the proposed 3D-ΣΔ. In this experiment, the active filter was compensating for all odd harmonics up to the 17th. Figure 10d illustrates the current supplied by the electrical grid. These currents are sinusoidal and balanced, although they present some harmonic distortion. However, the fact that the grid currents maintain a sinusoidal form indicates that the filter is compensating for harmonics correctly. Additionally, the balanced currents indicate that the APF compensates for the homopolar current that circulates through the neutral. Figure 10e shows the waveform of the neutral current of the electrical grid. The amplitude of this current is low, although it exhibits some ripple. The low value of this current is due to the APF compensating for imbalances. Therefore, there is virtually no homopolar component in the grid. Finally, Figure 10f illustrates the harmonic distortion or THD in the electrical grid currents. The APF compensates for all harmonics up to the 17th, resulting in a significant decrease in the THD to about 5% from around 21%. Figure 10g–i illustrate the results using an SPWM. In this case, the compensation is limited to the 15th harmonic, since a resonance frequency occurs in the 17th harmonic due to the different harmonic spectrum

of this modulation. Figure 10g depicts the grid currents. The currents are sinusoidal and nearly balanced, but they have more ripple and imbalance than those achieved using the 3D-ΣΔ modulation. Figure 10h displays the neutral current. The magnitude of this current is low as the filter compensates for the imbalances. However, it shows some ripple. Lastly, Figure 10i presents the grid currents in the frequency domain. The harmonic content and the THD of these currents are higher using the SPWM modulation than the 3D-ΣΔ modulation, as was also observed in the simulation. The increased harmonic content at low frequency is responsible for the ripple seen in the time domain. The THD is slightly reduced in all phases, but the reduction is not as remarkable as that achieved using the 3D-ΣΔ modulation.

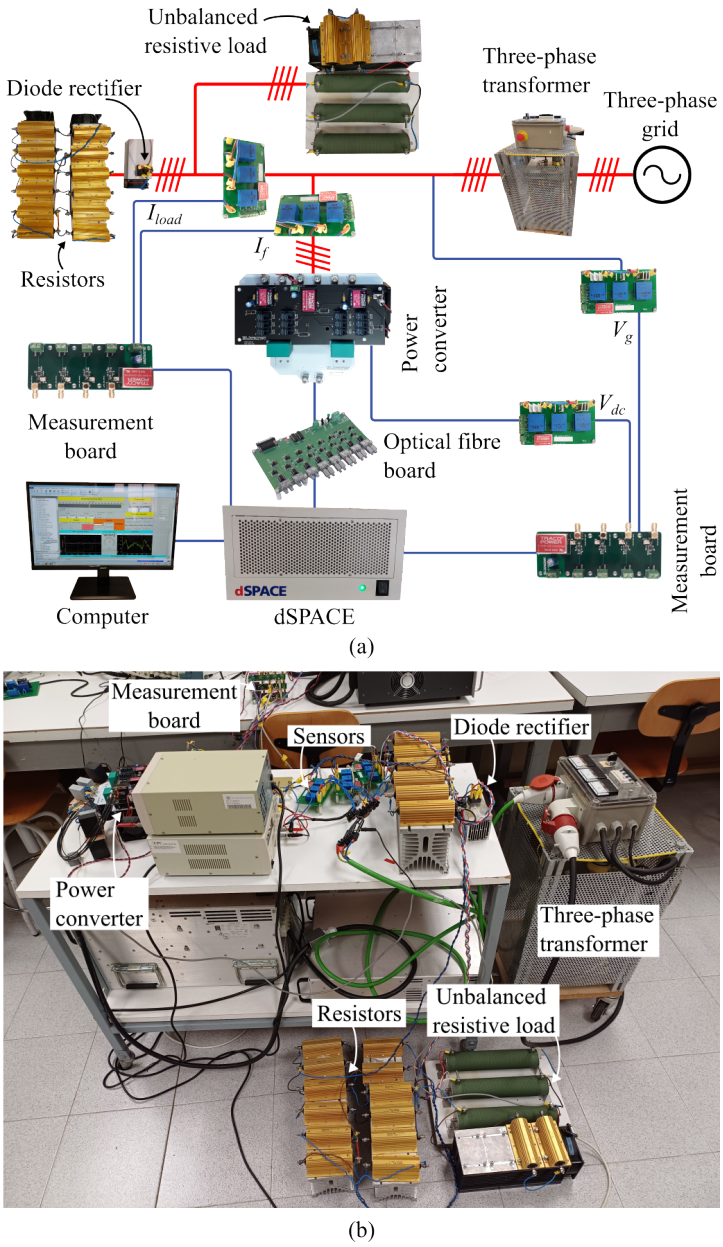

Figure 9. View of the experimental setup: (**a**) schematic; (**b**) photographic depiction.

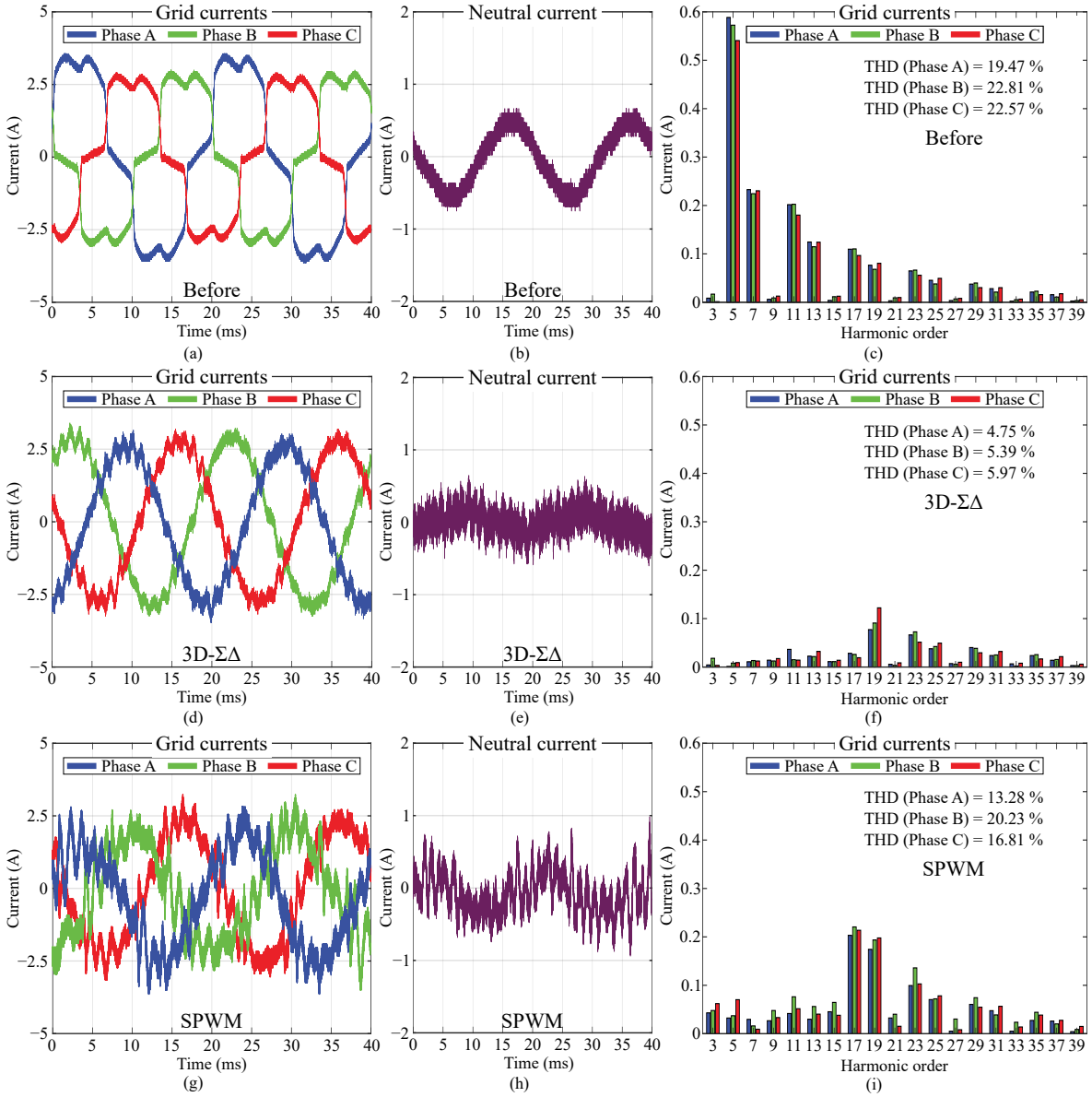

Figure 10. Experimental results. (**a**–**c**) Before filtering and balancing. (**d**–**f**) After filtering and balancing using 3D-ΣΔ. (**d**–**f**) After filtering and balancing using SPWM. (**a**,**d**,**g**) Grid current waveforms. (**b**,**e**,**h**) Neutral current waveforms. (**c**,**f**,**i**) Grid currents in frequency domain.

In summary, the experimental results presented in Figure 10d–f demonstrate the effectiveness of the APF in compensating for current harmonics and imbalances in the electrical grid using the proposed 3D-ΣΔ modulation. Moreover, this modulation enables a higher THD reduction and a higher performance than using the SPWM technique.

6. Conclusions

This article proposes a novel 3D-ΣΔ modulation technique for three-leg four-wire voltage source converters based on wide-bandgap semiconductors. This technique enables a variable switching frequency, which significantly reduces losses compared to fixed switching frequency modulations. Moreover, the proposed technique allows compensating for homopolar currents in four-wire systems. Additionally, a fast quantiser is proposed to simplify the implementation of the proposed modulation and reduce its computational cost. Experimental results demonstrate the effectiveness of the proposed technique. The performance of the 3D-ΣΔ modulation is compared with the SPWM technique at different operating points. The results show that the 3D-ΣΔ modulation produces much lower

losses at high switching frequencies than the classical SPWM modulation. Moreover, the proposed modulation is implemented in a power converter operating as an active power filter and compared with an SPWM technique. The experimental results demonstrate that the 3D-ΣΔ technique effectively compensates for positive and negative sequence harmonics as well as zero sequence currents. Furthermore, it is able to reduce the harmonic distortion in the electrical grid more than the SPWM modulation can, making it a better solution for maintaining a high power quality. In summary, the proposed 3D-ΣΔ technique is suitable for application to three-leg three-wire and four-wire active power filters and can compensate for harmonics and unbalances in the electrical grid more effectively than other fixed-frequency modulations with fewer losses.

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