

Article

A Reconfigurable Hybrid ADC Using a Jump Search Algorithm

Sung Kwang Oh ¹, Kwang Sub Yoon ¹ and Jonghwan Lee ^{2,*} 

¹ Department of Electronic Engineering, Inha University, Incheon 22212, Republic of Korea; ohsk@inha.edu (S.K.O.); ksyoon@inha.ac.kr (K.S.Y.)

² Department of System Semiconductor Engineering, Sangmyung University, Cheonan 31066, Republic of Korea

* Correspondence: jhlee77@smu.ac.kr

Abstract: This paper presents a reconfigurable hybrid Analog to Digital Converter (ADC) designed specifically for bio-signal processing, aiming to achieve low power consumption and high area efficiency. The proposed ADC utilizes a combination of 10-bit Most Significant Bit (MSB) Successive Approximation Register (SAR) and 2–4-bit Least Significant Bit (LSB) Single Slope (SS) architectures. The SS architecture incorporates the Dummy Capacitor Quantization Method (DCQM) which employs a 10-bit MSB dummy capacitor. This dummy capacitor can be configured to represent the 2-LSBs or reconstruct 4-LSBs. The reconfigurability of the ADC is achieved through the control of the reset timing of a 5-bit counter enabled by an external signal. The proposed ADC was fabricated using a Complementary Metal Oxide Semiconductor (CMOS) n-well 1-poly 8-metal process. Experimental measurements revealed that the ADC operates at a speed of 454 kS/s with power consumption of 18.7 μ W. The Effective Number of Bits (ENoB) achieved by the ADC is 10.9 bits based on a 14-bit scale or 10.2 bits based on a 12-bit scale. The Figure of Merit (FoM) for the ADC is calculated to be 21.5 fJ/step for the 14-bit scale and 22.1 fJ/step for the 12-bit scale.

Keywords: reconfigurable; jump search algorithm; hybrid; SAR; single slope; ADC



Citation: Oh, S.K.; Yoon, K.S.; Lee, J. A Reconfigurable Hybrid ADC Using a Jump Search Algorithm. *Electronics* **2024**, *13*, 606. <https://doi.org/10.3390/electronics13030606>

Academic Editors: Andrzej Jan Kos and Marcin Janicki

Received: 13 December 2023

Revised: 29 January 2024

Accepted: 30 January 2024

Published: 1 February 2024



Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

1. Introduction

Electroencephalograms (EEG), electrocardiograms (ECG), and electromyograms (EMG) are common bio-signals used in modern clinical practice. Each of these bio-signals requires different bandwidths and resolutions. Especially, EEG signals [1], being in the range of 10–50 μ V, are usually amplified by using a low-noise amplifier with a gain of 90–100 dB. After amplification, signal processing is performed with resolutions of 8 to 10 bits to mitigate the noise. Therefore, the proposed ADC in this paper can be applied to the portion corresponding to 10 bits. Due to the different resolutions and bandwidths for each bio-signal, it is necessary to design an ADC with specifications that can handle the highest resolution and bandwidth, or to employ multiple ADCs with different specifications. The former involves additional power consumption, while the latter requires an additional layout area. This attracts a hybrid ADC structure capable of reconfiguring the resolution and bandwidth.

Among recently researched ADCs [2–20], various hybrid structures [11–19] are being explored. However, the SAR ADC architecture is required due to the low power consumption, bandwidth, and resolution for biomedical signal processing. Therefore, hybrid ADC structures incorporating SAR ADCs into the conventional ADC designs have been investigated as follows.

Firstly, the hybrid structure [11] that combines a pipeline ADC and an SAR ADC utilizes comparator metastability to achieve a quick approximation process. This structure introduces three-state SAR logic, operates at a high speed of 625 MS/s, but consumes high power of 7.05 mW, offering an ENoB of 10-bit, thus being more suitable for high-speed signal processing. Another architecture merges a SAR ADC and a delta-sigma ADC into a

noise-shaping ADC [12,13]. The 3rd order NS-SAR ADC in [12] features a hybrid structure mixing cascaded integrator feed-forward methodology and error feedback, with digital calibration applied to alleviate harmonic distortion due to a capacitor mismatch. It operates at a speed of 2 MS/s and a bandwidth of 125 kHz, achieves ENOB of 12.93-bits, and consumes power of 96 μ W. The 4th order NS-SAR ADC in [13] utilizes an error feedback-cascaded resonant feed-forward structure, achieving lower power consumption of 73.8 μ W and an improved ENOB of 13.67-bits, despite being of the 4th order. However, due to the inherent nature of NS-SAR ADC, the implementation of an op-amp is mandatory, making it challenging to implement below 50 μ W. The 8-bit 2nd NS-SAR ADC in [14] employs dynamic amplifier-assisted integrator, showing an FoM of 168 dB (post-simulation result) with 0.417-mW. The resolution and power consumption of this ADC is not suitable for bio-signal processing.

The programmable SAR ADCs within hybrid structures are inherent for low power consumption [15–19]. The SAR-SS ADCs in [15] comprised a 6-bit SAR ADC and a 6-bit SS ADC, using a ramp generator in the dummy capacitor beneath the C-DAC of the 6-bit SAR ADC, applied with a resistor array. Due to the utilization of a 6-bit SS ADC, it operates at a slower speed of 370 kS/s and consumes power of 56 μ W. However, the ramp function generated by the resistor array is vulnerable to process variation. The programmable SAR and SS hybrid ADC in [18] utilizes a sub-binary capacitor weighting and crossover redundancy with a digital error correction circuit. It achieved a high ENOB of 9.1 bits at a 10-bit resolution with large power consumption of 376 μ W due to the complex control logic and the use of an op-amp to implement the ramp generator. The hybrid ADC in [19] is constructed with a 3-bit SS ADC and an 8-bit SAR ADC. This structure minimizes the voltage switching amplitude in the C-DAC of the SAR ADC, reducing power consumption to 7 μ W with an FoM of 37.8 fJ/step.

Lastly, the 12-bit SAR ADC in [20] with the S/H block is separated from the C-DAC to address the high input capacitance of conventional SAR ADCs. It reduces the offset by controlling the gain of the comparator in the S/H block to mitigate the nonlinear input-related offset and kickback noise caused by the variations in the input common-mode voltage of the comparator. It achieved an ENOB of 11.1-bits and significant power of 117.9 μ W due to the large C-DAC.

This paper proposes an SAR/SS hybrid ADC structure with reconfigurable circuitry and a jump search algorithm capable of changing the resolution to fit three EEG, ECG, and EMG signals. The proposed ADC operating at 14-bits employs a jump search algorithm [21] to enhance the operational speed of the SS ADC. This results in at least a 20% improvement of the operational speed of the SS ADC with respect to the conventional linear search algorithm [22]. Section 2 discusses the proposed architecture with a jump search algorithm. Measurement results are discussed in Section 3 and conclusions are drawn in Section 4.

2. Proposed Architecture

The proposed architecture of the hybrid ADC, as shown in Figure 1, consists of a 10-bit capacitor digital-to-analog converter (C-DAC) that employs split capacitors (64/63), a 4-bit C-DAC, latched comparators, a preamp, a reconfigurable timing block, a SS counter, and an output register based on bit control signals. The proposed ADC is functional in either the 12-bit or 14-bit mode. Both modes follow the same operational technique of the conventional SAR ADC for the first upper 10 bits, and depending on the external input signal, LSB 2 bits or 4 bits are reconfigured by the SS ADC. The 12-bit ADC and 14-bit ADC are functional based on the linear search algorithm and the jump search algorithm, respectively. The number of cycles driven by both the linear search and jump search algorithm are presented as a function of bits, as shown in Figure 2, generated by MATLAB R2023a.

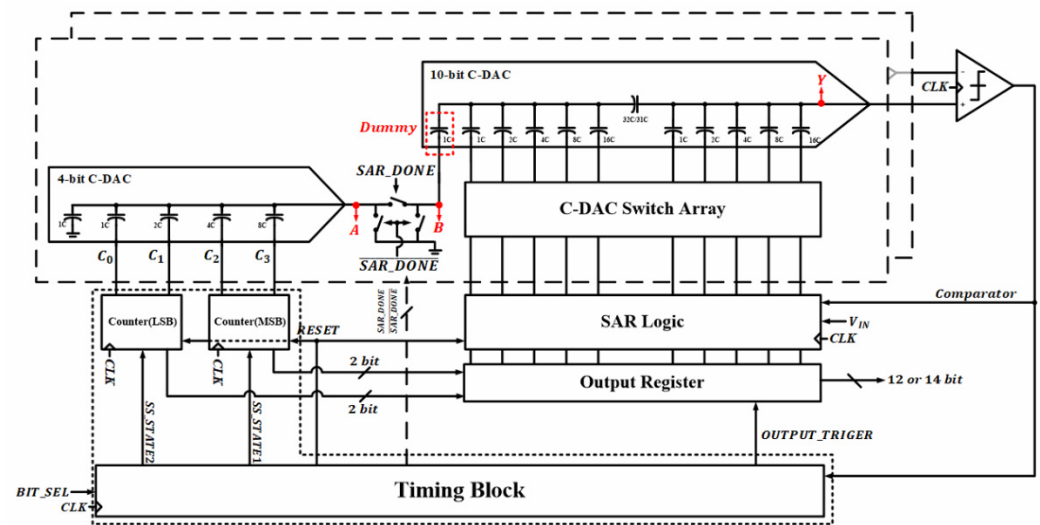


Figure 1. Block diagram of the proposed ADC.

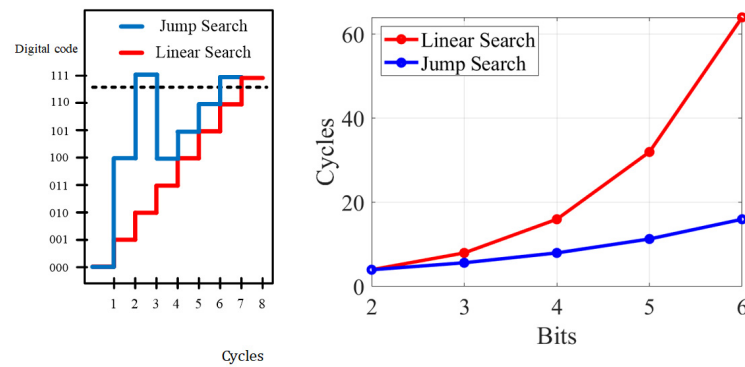


Figure 2. The number of cycles driven by linear search algorithm (3-bit) and jump search algorithm (2–6-bit).

The jump search algorithm is presented as superior to the linear search algorithm over 3 bits with respect to the number of cycles. To reduce the design complexity of the proposed ADC, the linear search algorithm and jump search algorithm are applied to the 12-bit mode and 14-bit mode, respectively.

The flow chart of the linear search algorithm (12-bit mode) and jump search algorithm (14-bit mode) of the proposed ADC is presented in Figure 3. The residue voltage $V_{res,n}$ of the conventional 10-bit C-DAC is applied to the negative input of the comparator to make a comparison with the sampled target voltage V_{target} at the starting point of the algorithm when the SS ADC begins to operate. If $V_{res,n}$ becomes less than V_{target} , the residue voltage $V_{res,n}$ continues to be renewed to $V_{res,n-1} + nV_{LSB,12bit}$, where $V_{LSB,12bit}$ is the voltage associated with the least significant bit of the 12 bits. If $V_{res,n}$ becomes greater than V_{target} and $BITS_SEL$ (bit selection external signal) is equal to 12 bits at the same time, MSB 2-bits (C_3C_2) are determined by the linear search algorithm and stored in the register of the 12-bit mode, as shown in the dotted upper box of Figure 3. Otherwise, $V_{res,n}$ and n are set to $V_{res,n-1}$ and 0, respectively, and $V_{res,n}$ continues to be renewed to $V_{res,n-1} + nV_{LSB,14bit}$ until $V_{res,n}$ becomes less than V_{target} . If $V_{res,n}$ becomes less than V_{target} , LSB 2-bits (C_1C_0) is determined by the jump search algorithm and stored in the register of the 14-bit mode, as shown in the dotted lower box of Figure 3.

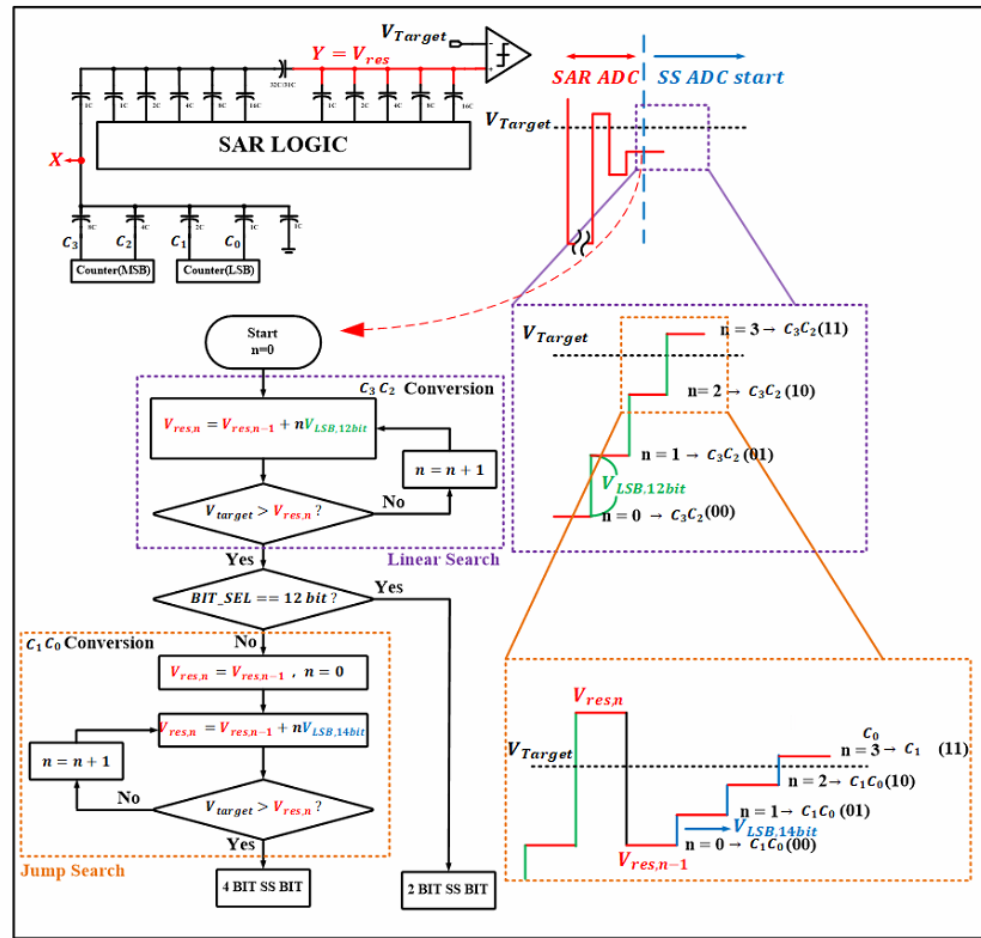


Figure 3. Flow chart of Linear Search Algorithm and Jump Search Algorithm on 4-bit SS ADC.

The DCQM employed by the proposed ADC takes advantage of the fact that the weighted factor of the dummy capacitor is 1 LSB. However, this technique suffers from large power consumption and vulnerability to process variations due to its implementation utilizing resistor arrays and op-amp-based ramp function generators [14]. In order to avoid this problem, the proposed C-DAC employs a digital ramp function based on the digital counter without an op-amp and a sub C-DAC on the bottom plate of the dummy capacitor, so that it alleviates the issues of large power consumption and process variations.

The proposed method involves scaling the voltage at the bottom of the dummy capacitor in a 10-bit C-DAC using a 4-bit C-DAC. Specifically, it divides the weight of the 10-bit dummy capacitor, which is $1\text{LSB}_{10\text{bit}}$ ($V_X = V_{DD}$), to implement it as $1\text{LSB}_{12\text{bit}}$ ($V_X = 1/4 V_{DD}$) or $1\text{LSB}_{14\text{bit}}$ ($V_X = 1/16 V_{DD}$).

$$1024C(V_{CM} - V_{IN}) = \sum_{n=1}^{10} 2^{n-1}C(V_Y - V_{B_{SARn-1}}) + C_{dummy,10\text{bit}}(V_Y - V_X) \quad (1)$$

In the previous equation, V_Y is the residual voltage in the 10-bit C-DAC and V_X is the voltage at the bottom of the dummy capacitor in the 10-bit C-DAC. To understand how $1\text{LSB}_{12\text{bit}}$ and $1\text{LSB}_{14\text{bit}}$ are implemented, we first need to determine the V_X voltage. Hence, we will calculate it for three cases (I, II, III). Case I represents the scenario immediately after the SAR conversion when all the SS bits are 0. Case II denotes when the SS bits implementing the $1\text{LSB}_{12\text{bit}}$ are applied to the 10-bit C-DAC. And Case III represents when the bits implementing the $1\text{LSB}_{14\text{bit}}$ are present.

Three examples (I, II, III) of DCQM on a C-DAC of the proposed ADC are illustrated in Figure 4. The amount of charge stored in the 4-bit C-DAC at each step can be represented as follows.

$$Q = \sum_{n=1}^4 2^{n-1} C (V_X - V_{B_{n-1}}) \quad (2)$$

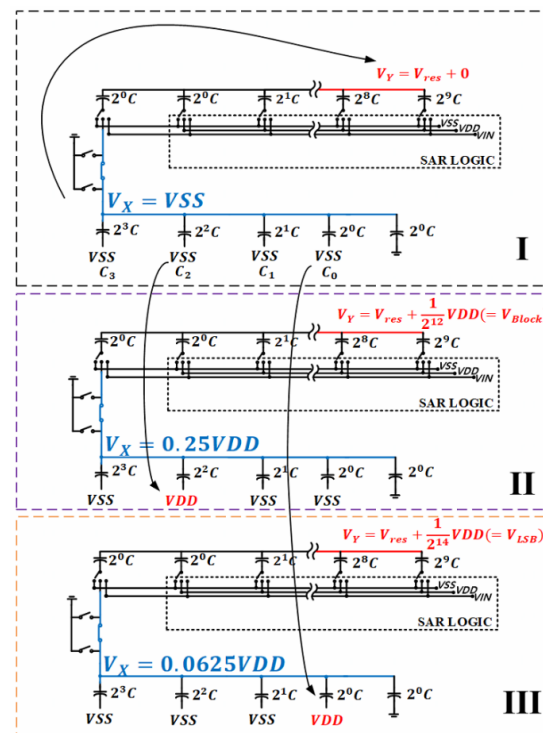


Figure 4. Three examples of dummy capacitor quantization method on C-DAC of the proposed ADC.

In Figure 1, when the SAR_DONE signal is activated, nodes A and B connect, entering the initialization state (I). Since the voltages at nodes A and B were V_{SS} , V_X becomes V_{SS} . Furthermore, since $C_3C_2C_1C_0$ are all in the reset state, the digital code is set to 0000. In part I of Figure 4, as the voltage across the entirety of the 16C capacitors is uniformly V_{SS} , the charge Q is given by $Q = 16C \times (V_{SS} - V_{SS})$, which simplifies to 0. Moving on to stage II, with the code changing to 0100, the X terminal becomes floating. As the C_2 terminal switches to VDD , the charge Q is described as $12C(V_{X_{II}} - V_{SS}) + 4C(V_X - VDD)$. Since the charges in stages I and II must be equivalent, on simplification, this results in $0.25VDD$. Stage III can be determined using a similar approach. The charges and V_X values for stages I, II, and III are summarized in Table 1.

Table 1. Q , V_X , Q_{SAR} and V_Y for three examples (I, II, III) associated with $C_3C_2C_1C_0$ of 0000, 0100, and 0001.

	C_3	C_2	C_1	C_0	Q	V_X	Q_{SAR}	V_Y
I	0	0	0	0	0	V_{SS}	$1023C(V_{res} - VDD) + C(V_{res} - V_{SS})$	V_{res}
II	0	1	0	0	$12C(V_{X_{II}} - V_{SS}) + 4C(V_{X_{II}} - VDD)$	$0.25VDD$	$1023C(Y_{II} - VDD) + C(Y_{II} - \frac{1}{4}VDD)$	$V_{res} + \frac{1}{2^{12}}VDD$
III	0	0	0	1	$15C(V_{X_{III}} - V_{SS}) + C(V_{X_{III}} - VDD)$	$0.0625VDD$	$1023C(Y_{III} - VDD) + C(Y_{III} - \frac{1}{16}VDD)$	$V_{res} + \frac{1}{2^{14}}VDD$

Next, the voltage value V_X should be reflected as the residual voltage (V_Y) of the 10-bit C-DAC, and the LSB value of 12-bit or 14-bit should be applied. Here, we utilize the fact that the weight of the Dummy Capacitor is 1 LSB. To represent this in a formula, we first

need an assumption. What we want to see now is “how the voltage value is transferred to V_Y when the SS ADC operates”. Thus, the SAR Conversion has already been completed. Therefore, we need to assume a digital code value from the SAR. For simplicity, let us assume that the 10-bit SAR conversion has resulted in 1111111111. Then, the amount of charge stored in the 10-bit C-DAC at each step can be represented as follows.

$$Q_{SAR} = \sum_{n=1}^{10} 2^{n-1} C (V_Y - V_{B_{SAR,n-1}}) + C_{dummy,10bit} (V_Y - V_X) \quad (3)$$

In Table 1 for stage I, given that the SAR 10-bit is 1111111111, the bottom of the capacitors in the C-DAC from $1C$ to 2^9C will have V_{DD} , while the top will have V_{res} . Moreover, because the voltage value of terminals A and B (as shown in Figure 1) for the Dummy capacitor ($1C$) was V_{SS} , it appears as described. For stages II and III, since the voltage at the bottom of the Dummy capacitor changes, the value of V_Y also changes. Thus, the respective values are denoted as $V_{Y_{II}}$ and $V_{Y_{III}}$. By applying the law of charge conservation to the above table, we can derive the values for V_Y as in Table 1.

In the given context, for stage II, the LSB based on the 12-bit standard can be applied to the 10-bit C-DAC, and for stage III, the LSB based on the 14-bit standard can be applied. This method demonstrates how to implement 12-bit and 14-bit resolutions using a 10-bit C-DAC and a 4-bit C-DAC.

The advantage of using DCQM is that it allows for a reduction in the number of capacitors compared to the conventional SAR ADC's C-DAC. A typical C-DAC doubles the number of capacitors required as the resolution increases. With DCQM, the resolution of the C-DAC can be halved, so the same operation can be implemented with fewer capacitors. Table 2 shows the number of capacitors in the conventional C-DAC with a split capacitor and the proposed ADC's 12-bit and 14-bit modes. It shows a 37% capacity reduction in the 12-bit mode and a 68% reduction in the 14-bit mode.

Table 2. Conventional C-DAC vs. This work.

	Conventional		This Work	
	12 bits	14 bits	12 bits	14 bits
Total Cap	130 C	258 C	82 C	

When the SS_STATE1 signal from the timing block is input to the counter and the conversion of the MSB 2 bits (C_3C_2) is finished, the SS_STATE2 is applied to the counter. After the lower 2 bits (C_1C_0) are converted, the operation is completed with the RESET signal activated. Figure 5 shows the timing diagram for the proposed ADC.

SAR conversion and SS conversion require 11 clocks and 10 clocks, respectively.

Figures 5 and 6 illustrates a detailed timing diagram of the proposed ADC and the block diagram of block and counter, respectively. It comprises a 5-bit counter, four types of decoder arrays, and a combination of the counter and capture cells. In the 12-bit mode, the SS_STATE2 does not operate, and the 2 bits of C_1C_0 are fixed to V_{SS} by default. This is done to utilize C_1C_0 as dummy capacitors. Therefore, in the 12-bit mode, the operation concludes after only converting C_3C_2 . In the 14-bit mode, the C_1C_0 portion operates fully, resulting in a total of 4 bits for SS.

The capture cell is a circuit that corrects and stores the output value. When the SS ADC operates, the comparator inverts depending on the residue voltage. However, because the inversion timing is one bit higher than the desired output value as in Figure 7, it acts to subtract one bit with the subtractor and then maintains it.

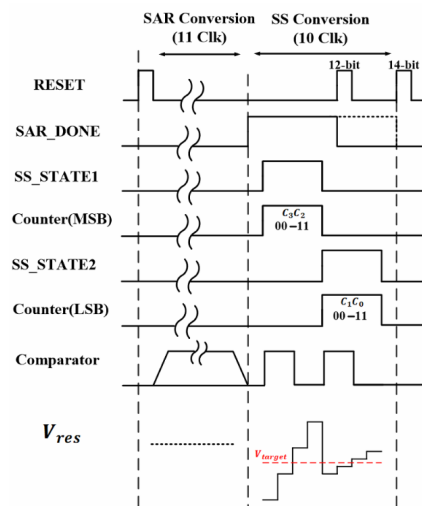


Figure 5. Timing diagram of proposed ADC.

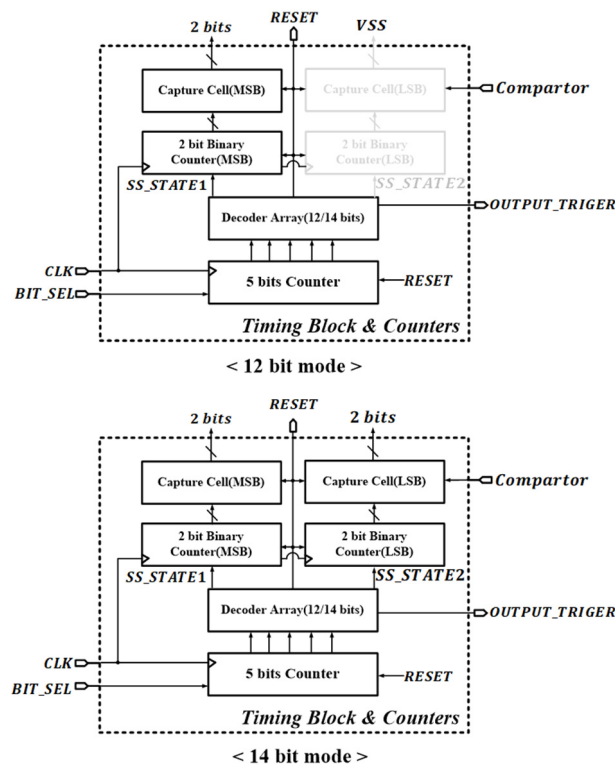


Figure 6. Detailed timing block & counters.

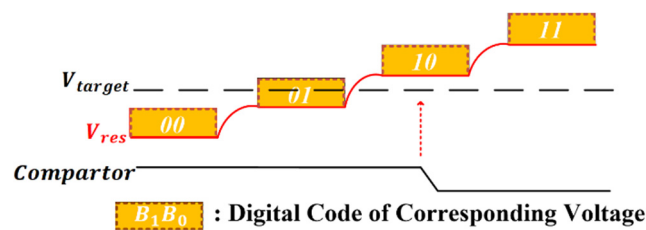


Figure 7. Comparator vs. residue voltage.

3. Measurement Results

The proposed SAR/SS ADC is designed with a 28-nm CMOS n-well, 8-metal process. Figure 8a shows the layout of the designed circuit and the design area, which is

$650 \times 550 \mu\text{m}^2$. The 10-bit capacitor DAC and 4-bit capacitor DAC, as well as the comparator, are located at the top. The middle consists of the SAR logic and switch array, and the timing block and output register are arranged at the bottom. The top is divided into an analog section, and the middle and bottom are digital sections, making a structure that suppresses interference between analog and digital signals. The chip's photograph with bonding pads is shown in Figure 8b.

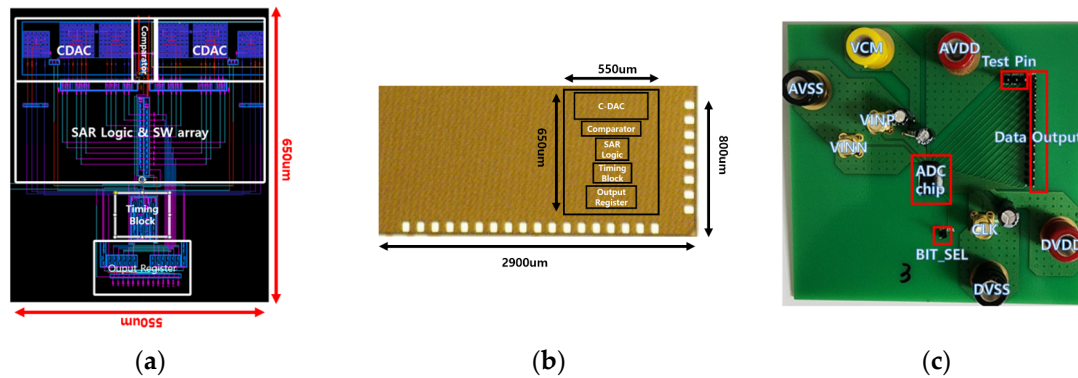


Figure 8. Layout of PCB process of the proposed ADC (a) layout, (b) chip photograph, (c) PCB.

The photograph presented in Figure 8c shows a printed circuit board (PCB) with the proposed ADC integrated. The PCB includes a total of three SMA connectors. Two for the input signal (VINP, VINN) and one for the clock signal (CLK). Additionally, the PCB features analog power supply connections (AVDD, AVSS) and digital power supply connections (DVDD, DVSS). There is a 1-bit BIT_SEL signal that allows changing the resolution to either 12 bits or 14 bits. The SS_STATE1 and RESET signals from the timing diagram are routed to test pins, and the comparator output signal is also accessible through a test pin. The 14-bit digital output pins are arranged in a single column on the right-hand side of the PCB.

Figure 9 shows a photograph taken with an oscilloscope from the timing diagram of the proposed ADC. It shows the SS_STATE1 and RESET signals as the BIT_SEL signal switches between 0 and 1. In both the 12-bit and 14-bit modes, the SAR operation takes place for a duration of 10 clock cycles. However, in the 14-bit mode, due to the longer SS operation, it can be observed that the RESET signal is delayed by an additional 5 clock cycles.

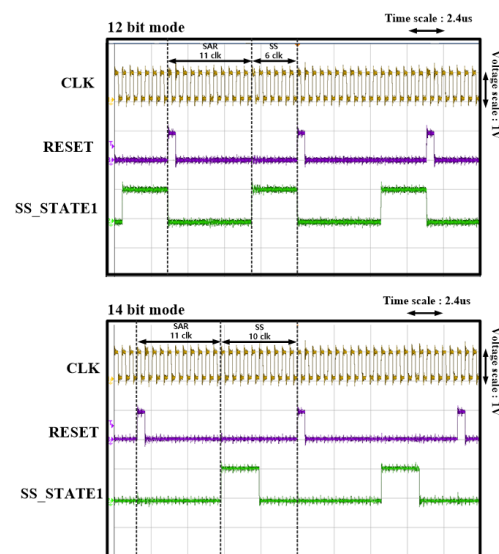


Figure 9. Waveforms of the RESET, SS_STATE.

In the SS phase of the proposed ADC, the comparator output remains either consistently high or low based on how V_{res} changes with respect to V_{target} . It can only transit from low to high or from high to low during this phase. Consequently, as evident in Figure 10, during the SS segment, it can be observed that the comparator output changes once or twice, or even remains unchanged.

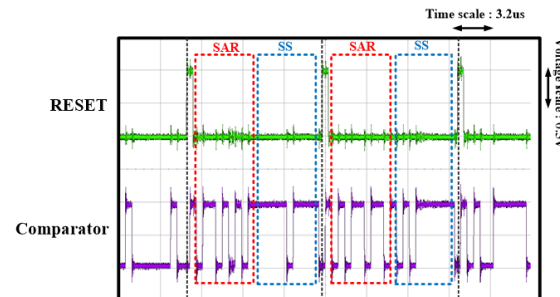
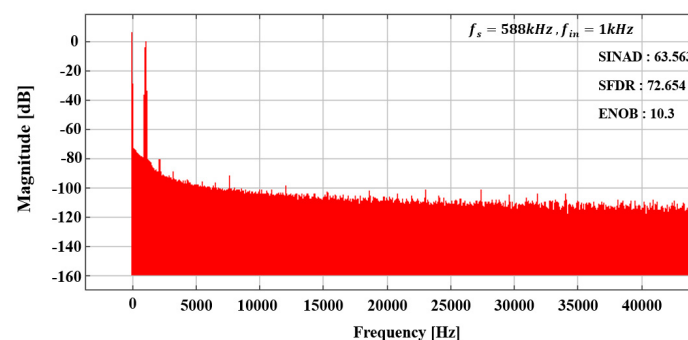


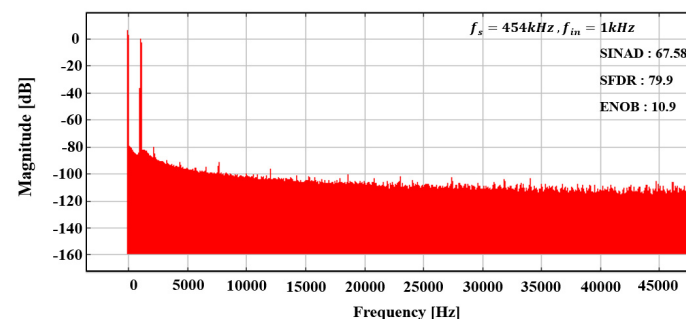
Figure 10. Waveforms of the RESET, SS_STATE.

The DNL and INL of the ADC associated with the 14-bit mode (10-bit SAR and 4-bit SS) have been measured as $-3.4/3.1$ LSB and $-2.8/3.2$ LSB, respectively. The measured power consumption, based on the 14-bit mode, amounts to a total of $18.7 \mu\text{W}$, with $8.2 \mu\text{W}$ for analog power consumption and $10.5 \mu\text{W}$ for digital power consumption.

The measured fast Fourier transform (FFT) results are presented in Figure 11 in order of resolution (12 or 14 bits). The input frequencies are 1 kHz, respectively. In the 14-bit mode, the signal-to-noise and distortion ratio (SNDR) is 67.5 dB, and the effective number of bits (ENOB) is 10.9 bits.



(a)



(b)

Figure 11. FFT result for an input frequency of 1 kHz (a) 12-bit, $f_s = 588 \text{ kS/s}$, (b) 14-bit, $f_s = 454 \text{ kS/s}$.

Figure 12 depicts the variation of ENOB for the proposed ADC as the clock frequency changes. The clock frequency ranges from 100 kHz to 20 MHz, while the input frequency remains fixed at 1 kHz. The measured ENOB maintains 10.9 bits up to a clock frequency

of 2 MHz, and then starts to degrade. Figure 13 illustrates the ENOB variation when the clock frequency is fixed at 2 MHz and the input frequency is varied from 1 kHz to 60 kHz. ENOB remains at 10.9 bits up to 5 kHz, after which it decreases.

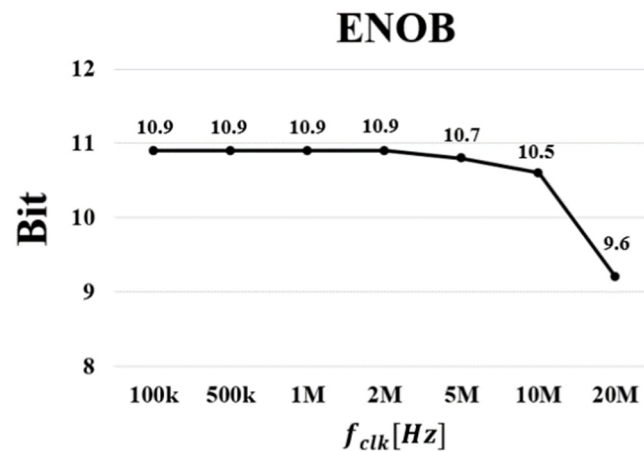


Figure 12. Plot of ENOB as a function of clock frequency ($f_{in} = 1$ kHz).

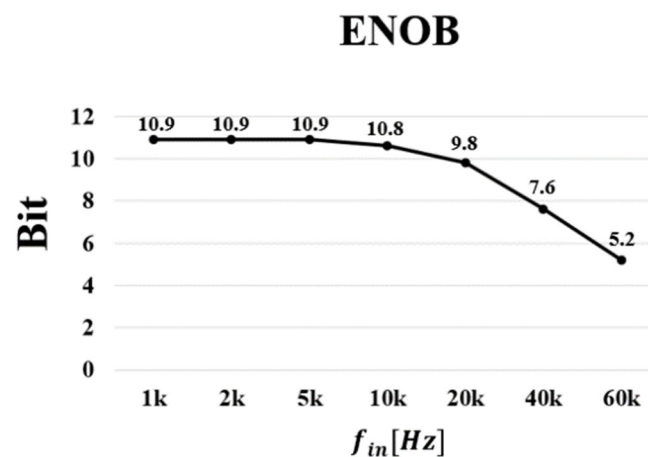


Figure 13. Plot of ENOB as a function of the input frequency ($f_{sample} = 454$ kS/s).

Analyzing the impact of supply voltage noise on the high-resolution ADC performance [23] is crucial because the power supply voltage to the ADC serves as the voltage reference to the C-DAC. The behavioral model set up in the MATLAB is utilized to simulate the ENOB as a function of power supply noise. The simulation result in Figure 14 illustrates that the ENOB of the proposed ADC degrades below 13-bits at the power supply noise of 70 μ V. In other words, the ENOB of the ADC should be able to maintain 13-bits or greater if the power supply noise is less than 70 μ V.

In Table 3, a comparison between the static and dynamic performance parameters of the proposed ADC and existing ADCs is provided. Refs. [12,13] are ADCs based on the NS-SAR architecture, which is why they exhibit high ENOB values of 12.93 and 13.67, respectively. Compared to the 14-bit mode of this design, they achieve an 18–25% higher ENOB and operate at 5–10 times the speed. Despite consuming 4–5 times more power, they still outperform this design with an FoM of 5–6 fJ/step. However, considering the importance of low power and a small area in biomedical signal processing, this design is considered superior due to its structure, which does not require the essential OP-AMP in the NS-SAR structure.

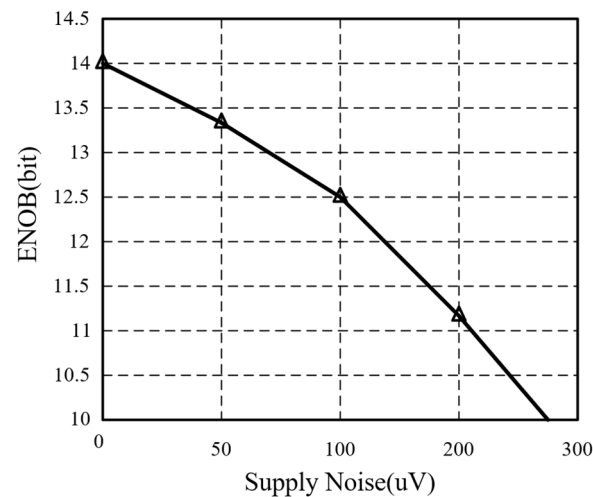


Figure 14. Behavioral simulation of ENOB vs. power supply noise.

Table 3. Comparison of performances of the proposed and conventional ADCs.

Parameter	[12]	[13]	[15]	[18]	[19]	[20]	This Work	
Process	130 nm	65 nm	90 nm	180 nm	180 nm	180 nm	28 nm	
Architecture	NS-SAR	NS-SAR	SAR-SS	SAR-SS	SAR-SS	SAR	SAR-SS	
Supply voltage [V]	1.2	1.2	1.2	1.8	1.8	1.8	1	
Resolution [bit]	N/A	14	12	10	11	12	12	14
ENOB [bit]	12.93	13.67	11.4	9.1	N/A	11.1	10.2	10.9
Sampling rate [S/s]	2 M	5 M	370 k	1.25 M	83 k	1 M	588 k	454 k
DNL [LSB]	N/A	N/A	−0.45/0.84	−0.61/0.60	−1.45/1.65	−0.5/0.5	−1.9/2.0	−3.4/3.1
INL [LSB]	N/A	N/A	−1.5/0.74	−0.89/0.82	N/A	−1/1.5	−1.6/1.8	−2.8/3.2
Power [W]	96 μ	73.8 μ	56 μ **	376 μ	7 μ	117.9 μ	15.3 μ	18.7 μ
FoM * [fJ/step]	6.1	5.6	36.9	52.5	37.8	54.4	22.1	21.5

* FoM = [Power]/(2^{ENOB} × [sampling rate]); ** power dissipation of [4] is divided by the number of channels.

However, in refs. [15,18–20], the ADCs are based on the SAR-SS and SAR ADC architectures. In refs. [15,20], they achieve an 8–11% higher ENOB than the 12-bit mode of this design. However, in ref. [15], it operates at a slower speed and consumes approximately three times more power than this design due to the resistance array-based ramp generator, making this design's FoM superior. In ref. [20] it operates at roughly twice the speed (1 MS/s), but, due to the bootstrap S/H circuit, it consumes 8 times more power than this design, resulting in this design having a better FoM. In ref. [18] it operates at approximately twice the speed compared to this design. However, when operating as an SS ADC, it does not function as fully differential, which is why the one in this paper outperforms it with a 10% higher ENOB and 40% lower power consumption. In ref. [19] power consumption is reduced by 50% compared to this paper. Nonetheless, due to the error correction circuit, its operational speed is slower by a factor of approximately 7 at 83 kS/s, making the one in this paper superior in terms of FoM.

Based on the following measurement results, the aspect that requires improvement in this design is the ENOB in the 14-bit mode. When establishing the design specifications, a target of 10 nV/ $\sqrt{\text{Hz}}$ for the input-related noise of the comparator was set. The simulation results indicated around 86 nV/ $\sqrt{\text{Hz}}$, but the offset calibration was excluded to reduce additional power consumption. The value of 86 nV/ $\sqrt{\text{Hz}}$ was attained after excluding the offsets caused by driver MOSFET mismatches. However, it is anticipated that the measured results could deteriorate in the 14-bit mode due to the additional offset introduced by the

mismatches. Therefore, it seems necessary to incorporate a calibration circuit to reduce the comparator offset caused by mismatches.

4. Conclusions

The proposed ADC first converts the upper 10 bits using an SAR ADC and then transforms the lower 2 or 4 bits using a highly linear SS ADC. In the case of the 4-bit SS ADC, a jump search algorithm was employed to enhance the operational speed, and a reconfigurable architecture was designed to handle various bio-signals. It was designed using a CMOS 28 nm 1-poly 8-metal process, with a layout area of $550\ \mu\text{m} \times 650\ \mu\text{m}$. The measurement results indicate a power consumption of $18.7\ \mu\text{W}$, an operational speed of 454 kHz, an ENOB of 10.9 bits, DNL/INL values of $-3.4/3.1$ LSB and $-2.8/3.2$ LSB, and an FoM of 21.5 fJ/step. Although not particularly outstanding in terms of ENOB, this design excels in its low power consumption and improved operational speed, leading to an enhanced FoM. Leveraging its reconfigurable nature, this design is expected to find widespread application in wearable devices for bio-signal processing or IoT platforms.

Author Contributions: Conceptualization, S.K.O. and K.S.Y.; methodology, S.K.O. and K.S.Y.; software, S.K.O.; validation, S.K.O.; formal analysis, S.K.O. and K.S.Y.; writing—original draft preparation, S.K.O. and K.S.Y.; writing—review and editing, J.L.; visualization, S.K.O.; supervision, K.S.Y. and J.L.; project administration, K.S.Y. and J.L.; funding acquisition, K.S.Y. and J.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (No. 2022R111A3064285).

Data Availability Statement: The data present in this study are available on request from the corresponding author.

Acknowledgments: The chip was fabricated under the support of IDEC MPW program and Cadence design tools were supported by IDEC.

Conflicts of Interest: The authors declare that they have no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog to Digital Converter
C-DAC	Capacitor Digital to Analog Converter
CMOS	Complementary Metal Oxide Semiconductor
DCQM	Dummy Capacitor Quantization Method
DNL	Differential Non-Linearity
ECG	Electrocardiography
EEG	Electroencephalography
EMG	Electromyograms
ENOB	Effective Number of Bits
FFT	Fast Fourier Transform
FoM	Figure of Merit
INL	Integral Non-Linearity
LSB	Least Significant Bit
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NS	Noise Shaping
PCB	Printed Circuit Board
S/H	Sample and Hold
SAR	Successive Approximation Register
SNDR	Signal-to-Noise and Distortion Ratio
SS	Single Slope

References

1. Tohidi, M.; Kargaard Madsen, T.; Moradi, F. Low-Power High-Input-Impedance EEG Signal Acquisition SoC with Fully Integrated IA and Signal-Specific ADC for Wearable Applications. *IEEE Trans. Biomed. Circuits Syst.* **2019**, *13*, 1437–1450. [\[CrossRef\]](#)
2. Lakshmi, P.V.; Musala, S.; Srinivasulu, A.; Ravariu, C. Design of a 0.4 V, 8.43 ENOB, 5.29 nW, 2 kS/s SAR ADC for Implantable Devices. *Electronics* **2023**, *12*, 4691. [\[CrossRef\]](#)
3. Huang, Y.; Luo, C.; Guo, G. A Cryogenic 8-Bit 32 MS/s SAR ADC Operating down to 4.2 K. *Electronics* **2023**, *12*, 1420. [\[CrossRef\]](#)
4. Faghani, M.; Rezaee-Dehsorkh, H.; Ravanshad, N.; Aminzadeh, H. Ultra-Low-Power Detection System Using Level-Crossing Sampling. *Electronics* **2023**, *12*, 795. [\[CrossRef\]](#)
5. Baek, J.; Lee, J.; Kim, J.; Chae, H. 2nd-Order Pipelined Noise-Shaping SAR ADC Using Error-Feedback Structure. *Electronics* **2022**, *11*, 3072. [\[CrossRef\]](#)
6. Kim, K.; Oh, S.; Chae, H. Conception and Simulation of a 2-Then-1-Bit/Cycle Noise-Shaping SAR ADC. *Electronics* **2021**, *10*, 2545. [\[CrossRef\]](#)
7. Benvenuti, L.; Catania, A.; Manfredini, G.; Ria, A.; Piotta, M.; Bruschi, P. Design Strategies and Architectures for Ultra-Low-Voltage Delta-Sigma ADCs. *Electronics* **2021**, *10*, 1156. [\[CrossRef\]](#)
8. Seo, M.-J. A Single-Amplifier Dual-Residue Pipelined-SAR ADC. *Electronics* **2021**, *10*, 421. [\[CrossRef\]](#)
9. Verma, D.; Shehzad, K.; Khan, D.; Kim, S.J.; Pu, Y.G.; Yoo, S.-S.; Hwang, K.C.; Yang, Y.; Lee, K.-Y. A Design of Low-Power 10-bit 1-MS/s Asynchronous SAR ADC for DSRC Application. *Electronics* **2020**, *9*, 1100. [\[CrossRef\]](#)
10. Shehzad, K.; Verma, D.; Khan, D.; Ain, Q.U.; Basim, M.; Kim, S.J.; Pu, Y.; Hwang, K.C.; Yang, Y.; Lee, K.-Y. Design of a Low Power 10-b 8-MS/s Asynchronous SAR ADC with On-Chip Reference Voltage Generator. *Electronics* **2020**, *9*, 872. [\[CrossRef\]](#)
11. Guo, X.; Chen, R.; Chen, Z.; Li, B. A 13b 600-675MS/s Tri-State Pipelined-SAR ADC With Inverter-Based Open-Loop Residue Amplifier. *IEEE J. Solid-State Circuits* **2023**, *58*, 624–633. [\[CrossRef\]](#)
12. Zhang, Q.; Ning, N.; Zhang, Z.; Li, J.; Wu, K.; Chen, Y.; Yu, Q. A 13-Bit ENOB Third-Order Noise-Shaping SAR ADC Employing Hybrid Error Control Structure and LMS-Based Foreground Digital Calibration. *IEEE J. Solid-State Circuits* **2022**, *57*, 2181–2195. [\[CrossRef\]](#)
13. Xie, T.; Wang, T.-H.; Liu, Z.; Li, S. An 84-dB-SNDR Low-OSR Fourth-Order Noise-Shaping SAR With an FIA-Assisted EF-CRFF Structure and Noise-Mitigated Push-Pull Buffer-in-Loop Technique. *IEEE J. Solid-State Circuits* **2022**, *57*, 3804–3815. [\[CrossRef\]](#)
14. Cui, D.; Wang, Z.; Jiang, M.; Chen, Z. A 78 dB 0.417 mW Second-Order NS SAR ADC with Dynamic Amplifier-Assisted Integrator. *Electronics* **2024**, *13*, 371. [\[CrossRef\]](#)
15. Kim, M.K.; Hong, S.K.; Kwon, O.K. An Area-Efficient and Low-Power 12-b SAR/Single-Slope ADC Without Calibration Method for CMOS Image Sensors. *IEEE Trans. Electron Devices* **2016**, *63*, 3599–3604. [\[CrossRef\]](#)
16. Zhu, Z.; Xiao, Y.; Song, X. VCM-based monotonic capacitor switching scheme for SAR ADC. *Electron Lett.* **2013**, *49*, 327–329. [\[CrossRef\]](#)
17. Warchall, J.; Theilmann, P.; Ouyang, Y.; Garudadri, H.; Mercier, P.P. Robust biopotential acquisition via a distributed multi-channel FMADC. *IEEE Trans. Biomed. Circuits Syst.* **2019**, *13*, 1229–1242. [\[CrossRef\]](#) [\[PubMed\]](#)
18. Dai, S.; Hu, K.; Rosenstein, J.K. A Segmented SAR/SS ADC with Digital Error Correction and Programmable Resolution for Column-Parallel Sensor Arrays. In Proceedings of the 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 10–21 October 2020.
19. Tang, F.; Chen, D.G.; Wang, B.; Bermak, A. Low-Power CMOS Image Sensor Based on Column-Parallel Single-Slope/SAR Quantization Scheme. *IEEE Trans. Electron Devices* **2013**, *60*, 2561–2566. [\[CrossRef\]](#)
20. Shahpari, N.; Habibi, M.; Malcovati, P.; De La Rosa, J.M. A 12-Bit Low-Input Capacitance SAR ADC With a Rail-to-Rail Comparator. *IEEE Access* **2023**, *11*, 67113–67125. [\[CrossRef\]](#)
21. Shneiderman, B. Jump searching: A fast sequential search technique. *Commun. ACM* **1978**, *21*, 831–834. [\[CrossRef\]](#)
22. Arora, N.; Bhasin, G.; Sharma, N. Article: Two-way Linear Search Algorithm. *Int. J. Comput. Appl.* **2014**, *107*, 6–8.
23. Zhu, Y.; Chan, C.H.; Chio, U.F.; Sin, S.W.; Seng-Pan, U.; Martins, R.P.; Maloberti, F. Split-SAR ADCs: Improved Linearity with Power and Speed Optimization. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2014**, *22*, 372–383. [\[CrossRef\]](#)

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.