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Analysis of a Graphene FET-Based Frequency Doubler for Combined Sensing and Modulation through Compact Model Simulation

Monica La Mura *, Patrizia Lamberti and Vincenzo Tucci

Department of Information and Electrical Engineering and Applied Mathematics, University of Salerno, 84084 Fisciano, SA, Italy; plamberti@unisa.it (P.L.); vtucci@unisa.it (V.T.)
* Correspondence: mlamura@unisa.it

Abstract: The ambipolar conduction property of graphene field-effect transistors (GFETs) and the inherent square-like dependence of the drain current on the gate voltage, enable the development of single-device architectures for analog nonlinear radiofrequency (RF) circuits. The use of GFETs in novel RF component topologies allows leveraging graphene's attractive thermal and mechanical properties to improve the miniaturization and weight reduction of electronic components. These features are specifically appealing for integrated sensing, modulation, and transmission systems. However, given the innovative nature of emerging graphene-based technology, a complete performance analysis of any novel electronic component is essential for customizing the operating conditions accordingly. This paper presents a comprehensive circuital analysis of a GFET-based frequency doubler, exploiting a compact model for GFET circuit simulation to assess the device's performance parameters, including power conversion gain bandwidth and saturation. The performed analysis proposes to support the design of GFET-based harmonic transponders, offering integrated sensing and signal manipulation capabilities.

Keywords: circuit simulation; frequency multiplication; graphene field-effect transistor; radiofrequency

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1. Introduction

Frequency multiplication is a common operation performed by nonlinear electronic circuits for a wide plethora of applications. Shifting the frequency of a reference signal is generally easier than generating a signal at an arbitrary frequency, and allows relaxing the complexity of other parts of the electronics for the signal manipulation, allowing the design of more performing circuits under less demanding requirements. The frequency up conversion therefore enables the development of electronic circuits capable of enhancing either data transmission capacity and rate, or spatial resolution, miniaturization, power consumption, based on the considered application. In general, frequency multipliers are relevant for any improvement related to the increase of the system's operating frequency. Hence, research in novel devices and architectures for frequency multiplication is powered by the interest in opening new possibilities for applications in the sub-THz and THz frequency range [1].

The key application of electronic circuits performing frequency multiplication has historically been that of signal modulation and mixing for wireless communication systems. However, frequency multipliers are also a basic component of test and measurement equipment, such as spectrum analyzers, and medical imaging equipment, such as magnetic resonance and ultrasound devices.

Traditional Silicon-based frequency multiplier circuits include diode-based multipliers (varistor or varactor type), known for wideband and low-noise operation, and active transistor-based multipliers, with higher conversion gain but increased noise. In these

two cases, the generation of higher harmonics is obtained either by clipping the output waveform or by exploiting the nonlinearity of the input-output relation. Concerning nonlinear analog circuits for high-frequency RF applications, graphene has shown great potential among the emerging technologies [2]. The peculiar capability of tuning the polarity of charge carriers across the channel of a graphene field-effect transistor (GFET) by simply acting on the gate bias inspires the development of single-device ambipolar circuits that are usually made of several transistors, with the consequent area, mass, and power saving, which are crucial for several critical applications [3]. Circuits that typically exploit the ambipolar conduction and the nonlinear relation between the drain voltage and the gate voltage of GFETs are mixers, phase shifters, frequency multipliers.

The first experimental demonstration of a GFET-based frequency doubler dates back to 2009 [4], when a 10 kHz sine waveform was multiplied by a single back-gated GFET obtaining >90% RF power delivered to the second harmonic. Shortly after, an improved GFET with a top-gate design allowed better performance providing frequency multiplication from 100 kHz to 200 kHz [5], and then from 700 MHz to 1.4 GHz, achieving a spectral purity >90% [6] against the ~35% obtained from traditional unipolar field-effect devices. Following, the progress in the RF-GFET transistor fabrication allowed achieving the first above-cut-off 3-GHz frequency doubler [7], and the first single-transistor frequency doubler operating in the Ku-band, up to 16 GHz [8]. From that moment, inspired by the impressive results obtained for the frequency doublers, GFETs were proposed also for the design of frequency triplers [9] and quadruplers [10] by exploiting a W-shaped drain current-gate voltage transfer curve, achieved by using two GFETs in series and a double-gate GFET configuration, respectively. Overall, the GFET-based frequency multipliers have outperformed other transistor technologies [11]. However, technological limitations are still hindering the widespread diffusion of graphene-based electronic devices, due to the issues related to graphene deposition and transfer process and non-negligible sensitivity to manufacturing-related uncertainties [12]. These issues hold graphene-based components from achieving the high-frequency performance of state-of-the-art traditional silicon electronics and III-V compound semiconductor technology. Both technologies can deliver gain up to frequencies above 100 GHz, making them readily applicable to cutting-edge high-frequency RF wireless communications. Nevertheless, the interest towards graphene electronic devices lies in their versatility, allowing multiple applications to be integrated into a single component, rather than on achieving top-level performance.

Besides the interesting opportunities in RF electronics, GFETs have gained great attention mostly as high-sensitivity chemical sensors and biosensors [13–15]. Thanks to the successful demonstration of single-molecule high-sensitivity sensing property, and being the simplest device capable of delivering high-purity frequency multiplication (especially at double-frequency harmonic component), the GFET was considered for the realization of nanomaterial-based harmonic transponders [16,17]. In this application, the GFET acts as a chemically-sensitive frequency multiplier: the chemical gating effect causes a shift of the transistor's Dirac point, thus modulating the second-harmonic output signal and affecting the nonlinear conversion gain. Based on the fact that graphene can also be employed for energy harvesting applications and for tunable high-frequency antennas, it is possible to envisage all-graphene systems for combined sensing, modulation, and transmission, with the added value of being light-weight, small-footprint, low-power, in line with the ongoing Internet of Things and forthcoming Internet of Everything scenario. This envisaged application takes advantage of the unique characteristics of GFETs, offering the potential to integrate the functionality of sensing and modulation within a single component. Due to the frequency limitation and the fabrication-related performance impairment, at the present stage of technological implementations, graphene technology can be explored to develop integrated systems working below the sub-THz frequency range. The advantage related to the shift towards this novel technology remains in the development of lightweight, small, thermally-efficient, power-saving components. On the other hand, as nanotechnology is still in the first stages, the absence of established design rules poses a significant challenge

for designers seeking to define optimal operating conditions and selection criteria during the system parameter setup. To address this challenge, this work proposes an original analysis of the performance of a GFET-based frequency doubler model, providing choice criteria for making informed decisions during the design of operating conditions of GFET-based signal modulators. Building on our previous activity [3,12,18] and exploiting a GFET Verilog-A model of proven reliability, the proposed work explores the application of a recently presented high-performing GFET [19] to the frequency doubling operation by carrying out circuit simulations. The analysis is approached by comprehensively computing relevant figures of merit under varying conditions, such as different bias points and operating frequencies. In this way, the proposed study targets the definition of criteria not yet available in the literature for the design of the intrinsic GFET operating conditions. Therefore, it supports the simulation-based design of novel components bypassing the need for expensive prototypes and time-consuming measurements.

In this paper, the operational principle of a single-device frequency doubler based on an intrinsic (i.e., without any external component) graphene field-effect transistor device is described in Section 2, discussing the relevance of the bias point for the frequency multiplication. In Section 3, the simulated GFET device is described, and the model validity is verified by comparing the simulation results with available measurement data. The frequency doubler's performance in the frequency domain and its dependence on the input power level is explored in Section 4, by evaluating relevant figures of merit such as the power conversion gain and the output power delivered at doubled frequency. The presented results are discussed in Section 5, drawing some considerations on the application of GFETs in combined sensing and modulation applications. Finally, the conclusions are reported in Section 6.

2. Operational Principle of a Single-Device GFET-Based Frequency Doubler

The ambipolar conduction of charge carriers across the graphene channel is a consequence of the V-shaped transfer curve of GFETs, which enables changing the polarity of the current, I_D, by varying the gate-source voltage, V_{GS}. The polarity of the drain-source current (I_{DS}) switches from p-type to n-type when the gate-source bias V_{GS} crosses the minimum conduction point (Dirac point), generally referred to as the Dirac voltage, V_{dirac}. Figure 1a reports the I_{DS}-V_{GS} transfer curve of a typical GFET simulated by a compact model for DC operation. In Figure 1a, the transfer curve is symmetrical because the model adopted for the circuit simulation assumes that, as in [20], the mobility of both holes and electrons is the same, and the saturation velocity is independent on the carrier density. Under these assumptions, the value of V_{dirac} is roughly given by $V_{dirac} = V_{G0} + (V_D + V_S)/2$ [21], where V_{G0} is the gate voltage offset due to charges trapped in the graphene channel, and V_D and V_S are the voltage values at the drain and source terminal, respectively.

The static gate and drain bias point (V_{GS}, V_{DS}) is fundamental for the correct operation of the frequency doubler: it is important that, at the chosen operating point, the small-signal variation of the drain current depends on the square of the gate voltage while being linearly dependent upon the drain voltage [22]. When the transistor is biased at the Dirac point and a drain voltage is applied, both types of carriers are injected in the channel and recombine. This condition is represented in Figure 1b by the region in proximity of $V_{DS} = 0.5$ V. For this reason, even by increasing the V_{DS}, the I_{DS} does not increase, and the current curve shows the typical inflection point related to the carrier polarity inversion [23,24]. If biased in this flat region, in which the odd symmetry property is lost, odd harmonics of the input signal can appear in the output waveform, impairing the output voltage spectral purity and reducing the power transfer to the harmonic of interest [22], that, in the case of the frequency doubler, is the first even harmonic component.

The GFET frequency doubler circuit configuration is shown in Figure 2a and the operational principle at the basis of the frequency doubling operation is explained in Figure 2b. In this common-source configuration, the source voltage is $V_S = 0$, and therefore $V_{GS} = V_G$. When the gate is biased at the minimum conduction point $V_G = V_{G0} + (V_D + V_S)/2$, and an alternating signal at frequency f_{in}, $v_{in} = V_{in} \sin(2\pi f_{in} t)$, is applied to the gate so that

$v_G = V_{dirac} + v_{in}$, the conduction is hole-based for one half of the period $T = 1/f_{in}$, and electron-based for the other half period. This concept is described in Figure 2b, where the red curve representing the drain current I_D has a minimum in $V_G - V_{dirac} = 0$ and the left and right branches of I_D are related to holes (h+) and electron (e−) current, respectively. When the ac component of the gate voltage v_g oscillates between $+V_{in}$ and $-V_{in}$, as indicated by the green dotted lines in Figure 2b, the operating point shifts alternatively from the hole-based to the electron-based branch of I_D, and, due to the square-law dependence of the drain voltage on the gate voltage (see the blue curve in Figure 2b), the signal $v_D = V_D + v_d$ at the drain terminal oscillates at twice the input frequency, $2f_{in}$ ($v_d \propto \sin^2(2\pi f_0 t)$). The load is $R_{load} = 50\ \Omega$, i.e., no output impedance matching network is applied to maximize the power transfer, and therefore the circuit analysis of the schematic in Figure 2a describes only the intrinsic device behaviour.

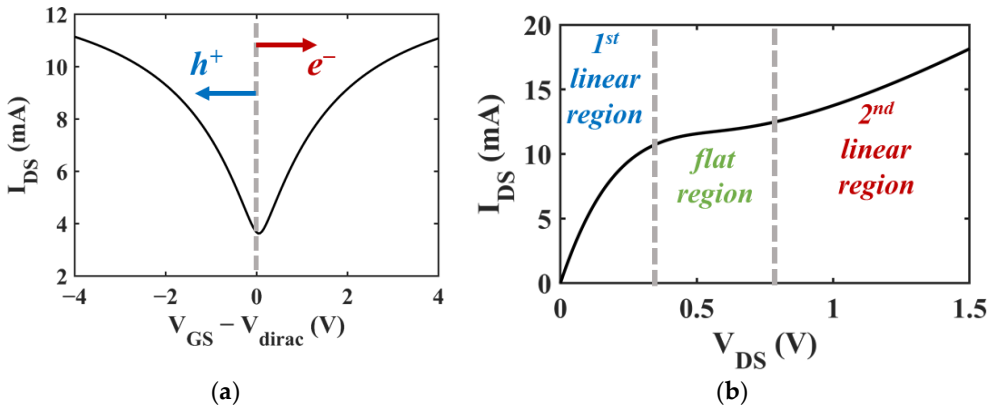

Figure 1. (**a**) Simulated transfer curve of a generic GFET. The left branch before the minimum conductivity point ($V_{GS} = V_{dirac}$) corresponds to a p-type charge transport; the right branch corresponds to an n-type charge transport. Operating the GFET around the V_{dirac} allows doubling the frequency of the gate signal at the device drain terminal. (**b**) Simulated static I/O curve of a generic GFET. The static characteristic of this device shows a flat region in the V_{DS} range corresponding to the minimum charge density point entering the channel, determining the charge polarity inversion in the channel. The first linear region of the curve is related to hole conduction, and the second to electron conduction.

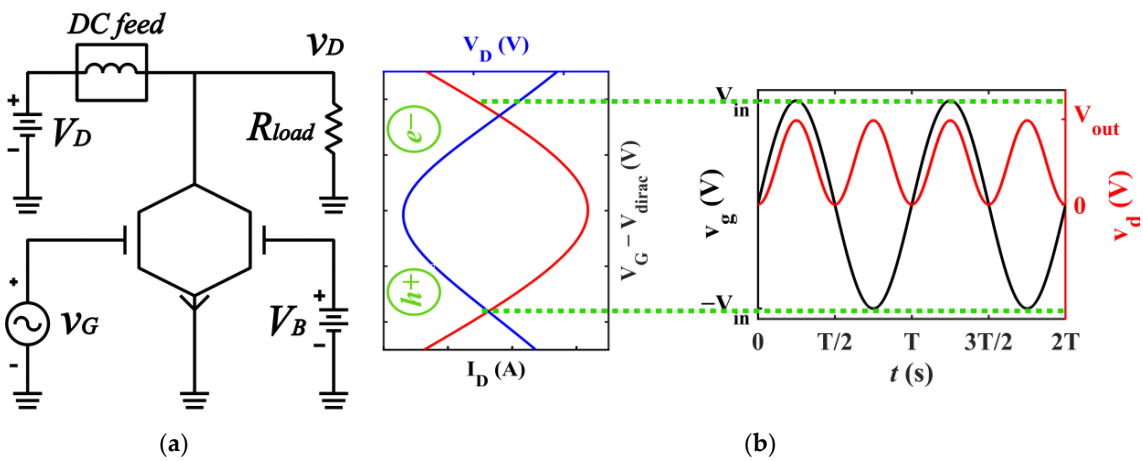

Figure 2. (**a**) Schematic of the GFET-based frequency doubler biased by the top gate ($v_G = V_{dirac} + v_{in}$), drain (V_D), and back-gate (V_B) voltage sources. The drain bias is provided through a DC feed (to decouple RF and DC components). (**b**) Operational principle of the GFET frequency doubler: the drain current (I_D) and the drain voltage exhibit a quadratic dependency on the gate bias voltage. The output signal at the drain terminal (v_d), completes one full oscillation cycle during half a period T of the input signal (v_g).

3. The Simulated GFET Device

The circuit simulation of the GFET-based frequency doubler was performed by using the RF design commercial software suite Advanced Design System−ADS® (Keysight Technologies, Inc., Santa Rosa, CA, USA) and a GFET compact model [25]. The adopted model was presented in [26] and validated in [27]. The model reproduced successfully the nonlinear behaviour of GFET-based ambipolar components for RF applications [28–30], proving to be a valuable tool for the purpose of predicting the GFET frequency doubler's performance. The device model considered in our simulations is the top-gated graphene FET described in [19]. Employing an Al_2O_3 substrate (relative dielectric permittivity $\varepsilon_{ox} = 7.5$), with higher optical phonon energy compared to traditional SiO_2 substrates, the device exhibited enhanced high-frequency performance. This improvement was achieved thanks to the reduced impact on charge carrier saturation velocity of impurities injected into the graphene channel from the substrate. The geometrical parameters and the graphene electronic properties of the simulated top-gate GFET device were taken from [19], which reports mobility up to $\mu = 2000\ cm^2\ V^{-1}\ s^{-1}$ and saturation velocity up to $v_{sat} = 2 \times 10^7\ cm\ s^{-1}$ for a transistor with channel length L = 0.5 µm and width W = 2 × 15 µm. The gate voltage offset V_{G0} was determined from $V_{G0} = V_{dirac} - (V_D + V_S)/2$ with V_{dirac}, V_D, V_S taken from the drain resistance curve shown in [19]. The surface potential inhomogeneity Δ was fixed considering a fluctuation of ±50 mV [31], corresponding to an energy variation of 0.1 eV. A sketch of the considered device is shown in Figure 3. The complete set of the model input parameters used in the simulations and their description are reported in Table 1.

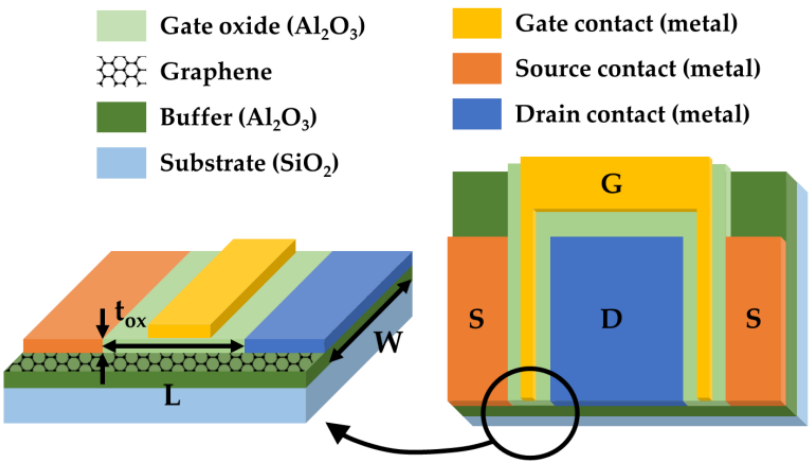

Figure 3. Sketch of the simulated GFET device described in [19]. On the left, an expanded view of the GFET gate region, corresponding to the circled area on the schematic view of the entire device, shown on the right.

Table 1. GFET model input parameters.

Parameter	Value	Description
W	30 µm	channel width
L	0.5 µm	channel length
t_{ox}	22 nm	top gate oxide thickness
t_{bot}	1 µm	bottom gate oxide thickness
ε_{ox}	7.5	top oxide relative permittivity (Al_2O_3)
ε_{bot}	7.5	bottom oxide relative permittivity (Al_2O_3)
µ	$2000\ cm^2V^{-1}s^{-1}$	graphene mobility
V_{G0}	2 V	gate voltage offset due to trapped charges
V_{B0}	0 V	back-gate voltage offset
Δ	0.1 eV	surface potential inhomogeneity
v_{sat}	$2 \times 10^7\ cm\ s^{-1}$	carrier saturation velocity

Due to the lack of experimental data concerning the use of the considered GFET in frequency doubling operation, the model performance was compared to the available data reported in [19]. The comparison between the simulated and measured short-circuit current gain, h_{21}, and its transition frequency, f_T, computed for increasing values of the drain bias, V_D, is shown in Figures 4a and 4b, respectively. The simulations match the experiments quite well, however the model fails to catch the high-frequency behaviour in high-field condition, as can be noticed by the deviation of f_T from the measured values when $V_D > 1$ V. This issue is related to the emergence of phenomena linked to the high-field condition which is not accounted for by the GFET compact model. For instance, the effects related to carrier saturation velocity necessitate a more refined model. Moreover, a high drain field induces a non-negligible temperature increase, intensifying the scattering of charge carriers due to their increased interactions with lattice vibrations, impurities, and defects. Additionally, the increase in power consumption amplifies the self-heating of the device, further enhancing the temperature rise and its related effects. These circumstances ultimately lead to a significant impairment of channel mobility, with a consequent impact on the output current. The multifaceted nature of high field condition, therefore, demands more complex models to achieve accurate experimental fitting. To avoid this issue, the following simulations are performed at $V_D < 0.5$ V, in low-field condition.

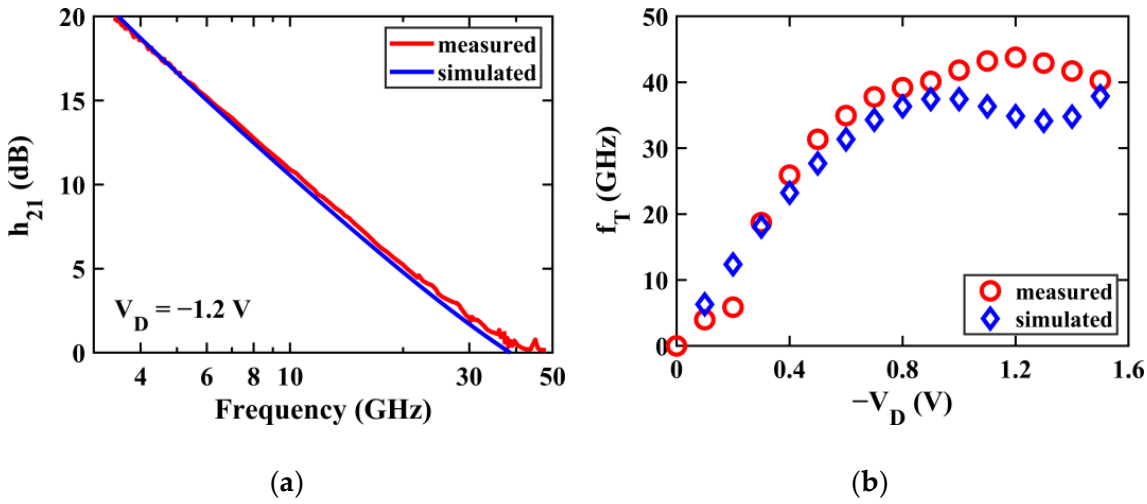

Figure 4. Simulation-experiment comparison of the short-circuit current gain h_{21} (**a**) and its cut-off frequency f_T (**b**) of the considered GFET. Measured data extracted from [19].

It is worth noting that, since the considered device was never characterized as frequency multiplier, the proposed work relies on the consistency of the simulation framework. However, because the adopted model underwent validation for the specific device under consideration (see Figure 4), and for the frequency doubling operation in the time domain [26], we infer that the model can be assumed to describe accurately the combination of this device in frequency doubling operation.

Moreover, the input and output impedance matching networks are intentionally excluded in the performed analysis. By investigating the intrinsic GFET behaviour in frequency doubling operation, the conditions where the device performs more effectively without any other external component are identified. In this way, by exploiting the device functionality at its best, the complexity of matching networks that must be later designed can be reduced, and the design constraints relaxed. This approach allows preserving the simplicity of the circuit, aiming at minimizing the number of components to safeguard footprint, weight, energy consumption, and cost. Furthermore, optimizing the operating conditions to enhance performance of the intrinsic device mitigates the impact of unavoidable parasitic elements (e.g., pad capacitance, contact resistance, interconnect parasitics), which typically impair overall circuit efficiency.

4. Performance of the GFET Frequency Doubler

4.1. Time-Domain Performance Analysis

The circuit shown in Figure 2a was implemented in ADS® and used to analyze the GFET-based frequency doubler performance in the time domain by simulating the schematic shown in Figure 5. The device was biased by setting V_G = 2 V, V_D = 0.1 V, and grounding the back gate (V_B = 0 V). In this way, the GFET was biased at the Dirac point (see Table 1) and in low-field condition. A sinusoidal voltage $v_{in} = V_{in} \sin(2\pi f_{in} t)$ with V_{in} = 0.3 V and f_{in} = 0.2 MHz, 2 MHz, 20 MHz was provided to the gate terminal, and the output signal was taken across the load resistor R_L.

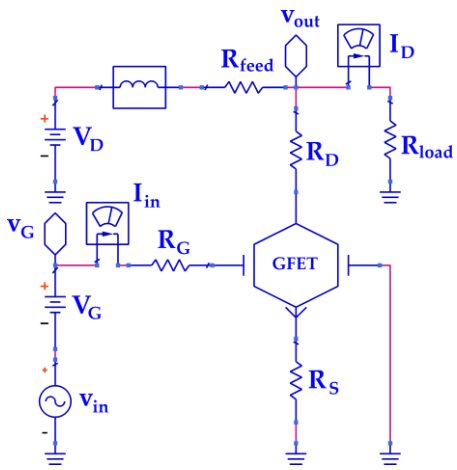

Figure 5. Schematic of the frequency doubler circuit based on a GFET in common-source configuration. The extrinsic resistances R_G, R_D, R_S are included to represent the contact resistance between graphene and metal, and set according to [19].

Figure 6 (left side) shows the ac component of the output waveform, $v_{out}(t)$, computed by increasing the f_{in} over three decades. The double-frequency component is clearly dominant in the case of f_{in} = 0.2 MHz, though the voltage gain is very weak due to the low transconductance of the device at the chosen bias point and to the absence of an impedance matching network. In Figure 6 (right side) is shown that, by raising the input signal frequency f_{in}, the power delivered at the double frequency, $P_{out}(2f_{in})$, remains approximately unchanged. On the other side, the output power at the fundamental frequency, $P_{out}(f_{in})$, changes significantly. This is evident also in the time-domain curves (Figure 6a–c), where the fundamental frequency component becomes increasingly visible on the drain voltage, degrading the purity of the output waveform. At f_{in} = 20 MHz, the fundamental tone amplitude prevails on the second harmonic amplitude, suggesting that the intrinsic device is scarcely efficient for the application to frequency doubling at that frequency.

During normal operation, the fundamental frequency component of the frequency doubler's output signal is rejected by a high-pass filter, and input and output matching networks enable maximum power transfer to the component, by matching the input impedance, and to the harmonic of interest, by ensuring that the load impedance causes short-circuiting the other harmonics. However, in order to improve the efficiency of the circuit and allow relaxing the complexity of matching networks and filters, it is important to set the operating point where the RF power delivered at the frequency of interest is greater than the power diverted towards other harmonics for the intrinsic device. For this purpose, the power conversion gain CG, defined as the ratio between the output power at twice the input frequency and the input power, according to

$$CG = P_{out}(2f_{in})/P_{in}(f_{in}) \quad (1)$$

and the output power ratio P_{21}, defined as the ratio between the output power delivered at $2f_{in}$ and the one at f_{in}, as in

$$P_{21} = P_{out}(2f_{in})/P_{out}(f_{in}) \quad (2)$$

can be computed as figures of merit of the frequency doubler performance. The values of CG and P_{21} corresponding to the data shown in Figure 4, obtained by providing $v_{in} = V_{in}\sin(2\pi f_{in}t)$ with $V_{in} = 0.3$ V, are listed in Table 2.

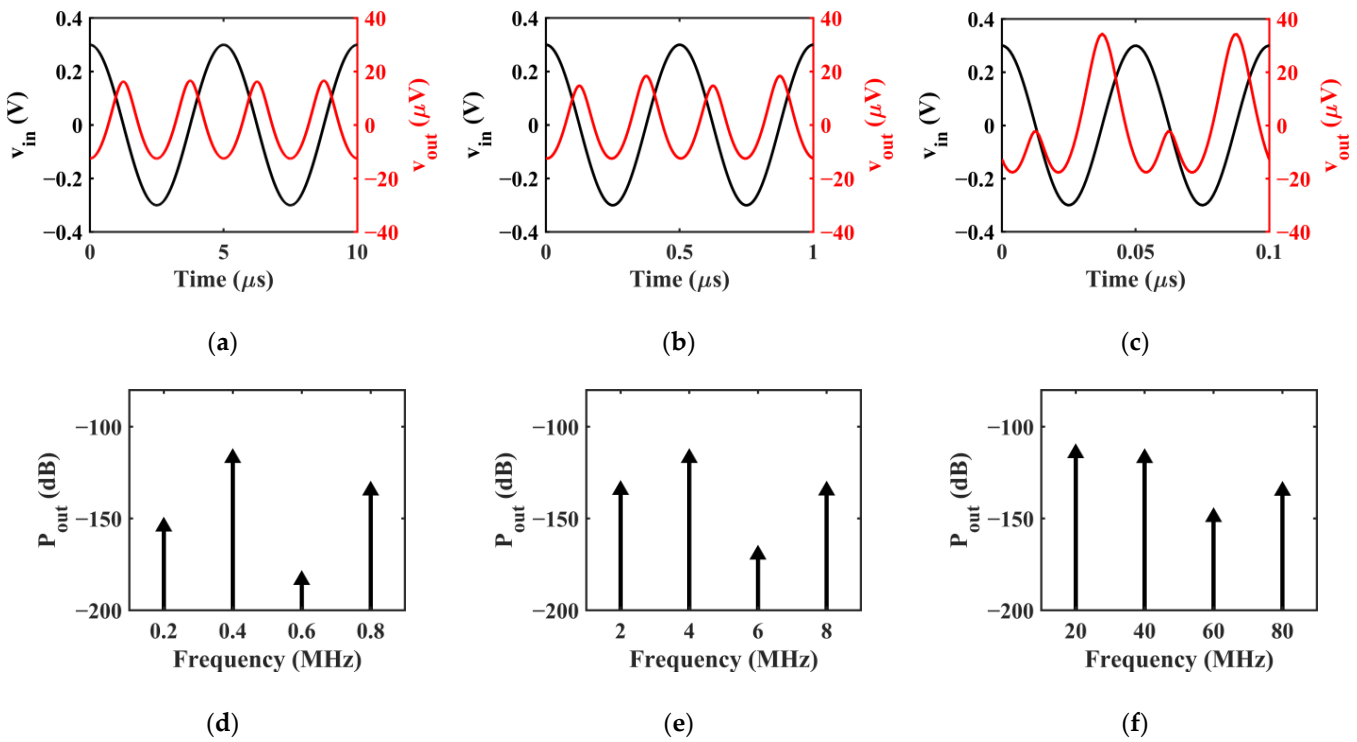

Figure 6. (**a**–**c**) GFET frequency doubler input and output voltage, $v_{in}(t)$ and $v_{out}(t)$, and (**d**–**f**) output power, P_{out}, computed at (**a**,**d**) $f_{in} = 0.2$ MHz, (**b**,**e**) $f_{in} = 2$ MHz, (**c**,**f**) $f_{in} = 20$ MHz.

Table 2. CG and P_{21} at different f_{in}.

Input Frequency	CG	P_{21}
$f_{in} = 0.2$ MHz	9.38 dB	37.4 dB
$f_{in} = 2$ MHz	−0.43 dB	17.4 dB
$f_{in} = 20$ MHz	−10.9 dB	−2.6 dB

4.2. Frequency-Domain Performance Analysis

Since the power ratio P_{21} is assumed as a figure of merit for the frequency doubler efficiency, its frequency-dependent behaviour is further investigated by performing a harmonic balance (HB) analysis. The HB analysis allows simulating the behaviour of nonlinear circuits excited by large-signal inputs in the frequency domain with good accuracy and low computational effort, because the nonlinear model remains formulated in the time domain but the solution is computed for a specified number of harmonics of the fundamental tone, under the hypothesis of steady-state operation and thus disregarding time transients.

Figure 7a shows the P_{21} computed when the input signal is a sinusoidal voltage with amplitude $V_{in} = 0.3$ V and the frequency sweeps from $f_{in} = 1$ kHz to $f_{in} = 1$ GHz. In this way, it is possible to identify the frequency at which the harmonic component at double frequency drops below the fundamental tone, f_C. The values of P_{21} computed by the transient analysis and reported in Table 2 match the results of the HB analysis. The P_{21} crosses the 0-dB line (i.e., the output power at doubled frequency falls below the output

power at the fundamental tone) at the crossing frequency $f_C \approx 15$ MHz. Considering the current gain of the simulated device (see Figure 4), it is clear that f_C is well below the transit frequency in the same static bias condition, $f_T = 6.3$ GHz. Interestingly, these two frequencies are not directly correlated. On one hand, f_T represents the maximum frequency at which the GFET can amplify the input current, inversely proportional to the input capacitance and directly proportional to the transconductance, a function of the bias point. On the other hand, the crossing frequency f_C represents the highest frequency at which the GFET amplifies the input current while generating higher power at the first harmonic compared to the fundamental tone. The distribution of the output power across the fundamental tone, first-order, and higher-order harmonics depends on the transconductance at the minimum conduction point and at the specific frequency of each harmonic component. Additionally, it also depends on the amplitude of the nonlinear terms in the relationship between I_{DS} and the gate voltage other than the assumed squared dependence. The complex nature of the output power is the reason why it is better computed numerically.

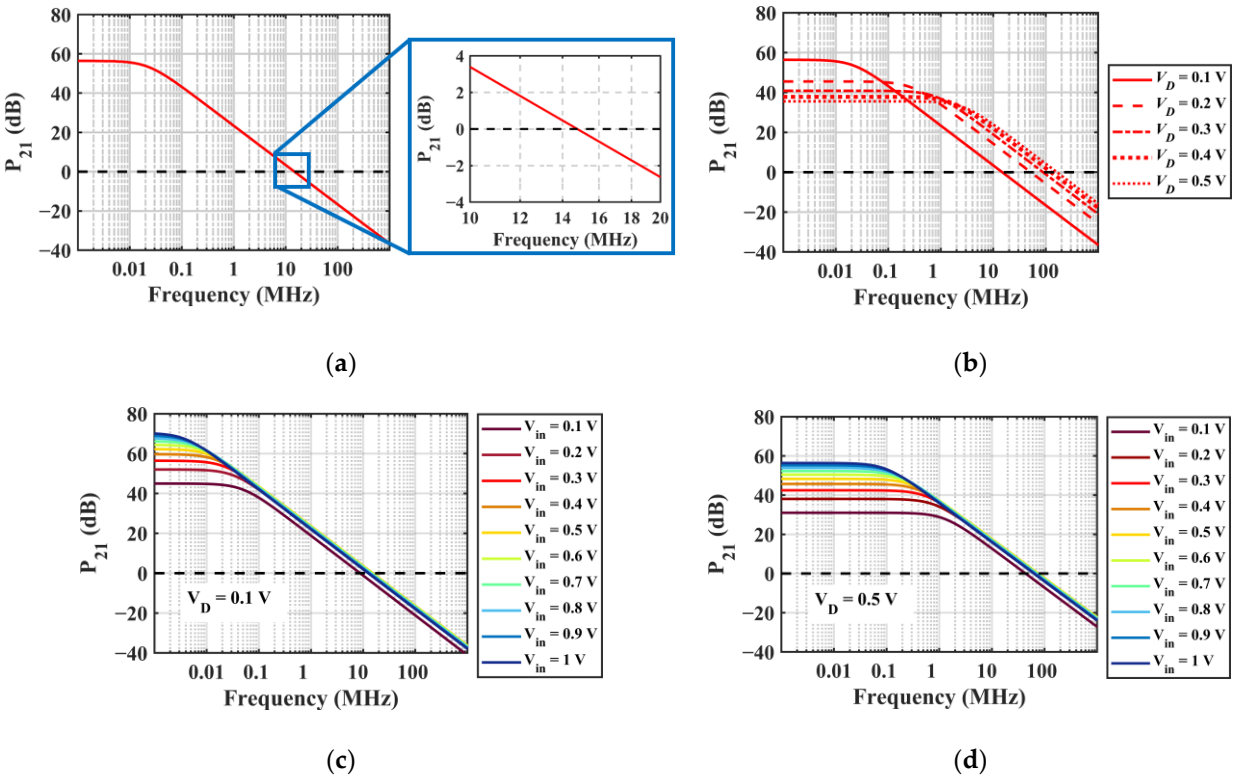

Figure 7. Frequency dependence of P_{21} (**a**) at $V_D = 0.1$ V, and (**b**) by increasing the drain bias. P_{21} computed by varying the input signal amplitude in the case of (**c**) $V_D = 0.1$ V and (**d**) $V_D = 0.5$ V.

As already assessed for f_T and f_{MAX} [18], the value of f_C is also strictly related to the operating point, due to the influence of the bias condition on the transconductance and on the input power. It can be noticed, by observing Figure 7b, that the crossing frequency of P_{21} increases by increasing the drain bias voltage, V_D. Thus, the frequency performance of the intrinsic GFET in frequency doubling operation depends on the amplification capabilities of the device, as determined by the fixed bias point. This explains that the small value of V_D used in the simulations ($V_D = 0.1$ V) is the reason for the low cut-off frequency f_C observed. In addition to the dependence on the bias point, P_{21} also depends on the input signal amplitude, V_{in}. Figure 7c,d explore the dependence of P_{21} on V_{in} in two different drain bias conditions: $V_D = 0.1$, in Figure 5c; $V_D = 0.5$ V, in Figure 7d (greater values of V_D were not considered due to the reduced model accuracy in high-field conditions). It can be seen that the crossing frequency f_C is not very much affected by the variation of V_{in}, whereas the low-frequency value and the bandwidth of P_{21} change significantly. The P_{21} dependence

on V_{in} is attributed to the impact of V_{in} on the input power, P_{in}, a factor that subsequently affects the output power at both f_{in} and $2f_{in}$, and therefore their ratio P_{21}. Moreover, because the frequency multiplication is based on the nonlinear dependence of operation of the drain voltage on the gate voltage (see Figure 2b), increasing V_{in} triggers nonlinear amplification of the output current and consequently affects the harmonic components of the output power. This altered distribution of energy across higher-order harmonic components reflects in changes of the ratio between $P_{out}(2f_{in})$ and $P_{out}(f_{in})$, leading to the P_{21} shown in Figure 7. Finally, harmonic distortion in large-signal operation also leads to conversion gain saturation, further affecting P_{21}.

4.3. Power Conversion Performance Analysis

The efficiency of the GFET frequency doubler can be measured by observing its power conversion gain CG. For the intrinsic device, CG is strongly limited by the GFET input impedance mismatch with both source and load impedance, and can only be improved with tailored matching networks.

Due to the harmonic distortion introduced by the nonlinear behaviour of transistors in large-signal conditions, increasing the input power above a given threshold leads to saturation of the power conversion gain. It is therefore relevant to consider also the conversion gain saturation when designing the operating conditions of the frequency doubler. Figure 8 reports the simulated P_{21} and CG computed by harmonic balance analysis while varying the input power, P_{in}. The simulations were performed using V_D = 0.1 V, V_G = 2 V, and considering the input signal frequencies f_{in} = 0.2 MHz, 2 MHz, 20 MHz. In accordance with the expectation, both P_{21} and CG increase with a +10 dB/dec slope. For the considered device, the saturation of the output power starts around $P_{in} \sim -10$ dBm (100 μW), and the curves reach the maximum value at $P_{in,sat}$. This value is reportedly affected also by the device contact resistance [7].

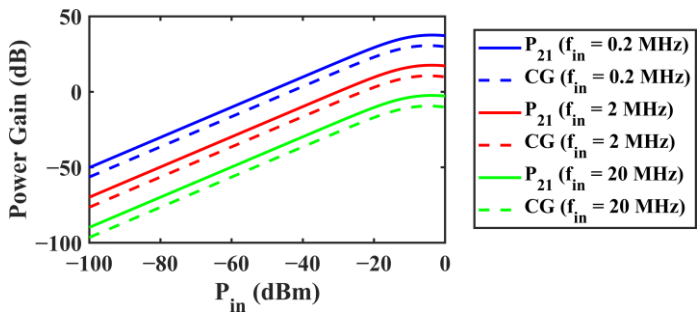

Figure 8. Simulated power gain P_{21} and CG plotted against P_{in} for f_{in} = 0.2 MHz, 2 MHz, 20 MHz. Saturation appears above $P_{in} \sim -10$ dBm.

5. Discussion

The proposed work supports the design of GFET-based frequency doublers for application to signal modulation systems in the MHz-range, such as harmonic transponders and integrated sensing and modulation systems. Based on the findings presented in Section 4, concerning the performance of a recent GFET device in frequency doubling operation, informed criteria for the selection of the optimal operating conditions can be obtained. In particular, the results of this study restrict the range of frequencies for selecting the operating frequency of the system to those in which the device demonstrates higher efficiency, and provides information that can guide the shaping the input signal interrogating the sensor.

Indeed, the design of nonlinear circuits for frequency multiplication starts with the optimization of the bias levels. To operate as frequency multiplier, the GFET must be biased at the Dirac point, posing a first constraint on the gate bias. Following the analysis reported in Figure 7b, it becomes evident that increasing the drain voltage is advantageous when the specific application demands a shift towards higher frequencies. This adjustment

allows enhancing the rejection of the fundamental tone by design. Once the static operating condition is fixed, the input signal can be tailored.

Both the amplitude and frequency of the input signal can be set aiming at maximizing the device performance. To improve the power conversion efficiency of the intrinsic device, the most suitable operating frequency can be fixed based on the P_{21} bandwidth (see Figure 7b). It is important to bear in mind, during this phase, that increasing the frequency unavoidably worsens the power conversion gain, regardless of the input signal power level, as can be seen in Figure 6. After fixing the signal frequency, appropriate measures for output impedance matching can be implemented, so that undesired harmonic components can be effectively driven through low-impedance paths (ideally, short-circuited) and the power transfer from the input to the double-frequency harmonic component can be enhanced. Concerning the input signal level, Figure 7c,d show that higher amplitude of the input signal supports higher rejection of the fundamental tone, and improves the conversion gain through the greater input power, as proven by Figure 8. However, it is worth noting that high amplitude of the input signal may lead to greater harmonic distortion due to the nonlinear behaviour in large-signal operation of the GFET. Figure 8 shows that this may lead to saturation of the conversion gain. Therefore, the input signal amplitude should be set to achieve an input power level, based on the chosen operating frequency, that prevents saturation of the conversion gain.

Finally, the doubler should be cascaded with high-pass filters to remove the DC offset and enhance the rejection of the fundamental tone, and eventually with selective filters to relax the requirements on the impedance matching networks.

Although the operating conditions can be designed to maximize the efficiency of the GFET for its specific use as frequency doubler, it is worth discussing also the open issues related to the use of GFETs, and more broadly of graphene components, for the proposed application. Currently, the performance of GFETs in terms of amplification properties and maximum operating frequency still lags behind state-of-the-art components, mainly due to the poor conversion gain and impurity-related impairments. Moreover, shifting from traditional electronics to all-graphene electronics will require technological improvements in the manufacturing and transfer of graphene, to enhance the reliability and repeatability of graphene components. Nevertheless, simulation works suggest new possibilities and applications not affordable by traditional technology, inspiring the exploration of innovative solutions to overcome current technological limitations and drive graphene electronics towards its full potential.

6. Conclusions

This work investigated the performance of a single-device GFET-based frequency doubler by means of circuit simulations. The observed performance indicators include the ratio between the output power at double-frequency and that at fundamental frequency, and the power conversion gain at double frequency. The performed analysis offers guidelines for the design of operating conditions that maximize the device efficiency, thereby relaxing constraints on signal conditioning circuits and impedance matching networks. By providing the knowledge required to perform the tuning of the GFET frequency doubler design, the findings of this study can support the development of all-graphene sensing, modulation, and transmission systems. This study, combined with the envisioned future research directions, aims to contribute to the ongoing technological transition towards lightweight, small, thermally-efficient, power-saving carbon-based components for the pervasive Internet-of-Everything scenario. Future research will focus on the analysis of the frequency doubler's robustness against fabrication-related uncertainties, addressing the concern about the process-induced non-uniformity of the device performance. Further, the development of criteria for designing input and output impedance matching network will be investigated, based on the latest advancements in graphene passive components. Finally, the GFET frequency doubler's integration into highly-efficient and compact all-graphene systems will be explored.

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