

Article

A Novel Impedance Matching of Class DE Inverter for High Efficiency, Wide Impedance WPT System

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Abstract: In high-frequency wireless power transfer (WPT) applications, Class D, E, and F inverters are most widely used. Class DE inverters combine the respective advantages of Class D and Class E inverters. However, the Class DE inverter is sensitive to changes in impedance, which can easily lead to the loss of soft switching characteristics, thereby reducing efficiency. In this paper, an impedance-matching compensation design method is proposed to expand the high-efficiency region of the Class DE inverter by matching impedance and parameters. The effect of the method on the zero-voltage switching (ZVS) characteristic of Class DE inverters is analyzed in detail. The proposed WPT system maintains a constant voltage and zero phase angle by employing PS/PS compensation topology. Theoretical analysis shows that the impedance can be compressed for the design of resonant network impedance, and the method can expand the high-efficiency region with a reasonable choice of parameters to match the phase. Finally, a 500 kHz, 1 kW WPT prototype was constructed with a coupling factor of 0.25–0.4 and a load range of 30–80 Ω . The inverter's efficiency exceeds 95%, with optimal efficiency reaching 97.3%. The system efficiency is greater than 87%.

Keywords: resonant network; zero voltage switch region; impedance matching compensation; high-frequency; wireless power transfer



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1. Introduction

Magnetic resonance-based wireless power transfer (WPT) technology is being continuously developed, and it is widely used in electronics, electric vehicles, and other consumer fields. It also plays a vital role in some special charging applications [1–5]. In terms of charging for light rail trains, a coupling mechanism is installed on the rail and the train chassis to obtain stable power transfer for train operation [6]. In the field of implantable medical devices, WPT technology makes it more convenient to charge implantable devices, such as heart pumps, without the need for surgery, thereby reducing the difficulty of treatment [7–9]. Some scholars have designed WPT systems for underwater equipment, which effectively improves their endurance [10].

In order to optimize and improve the efficiency of the WPT system, researchers have conducted in-depth studies on inverters, coupling coil design, compensation networks, and control methods. References [11–13] utilized control strategies such as phase shift, maximum efficiency point tracking (MEPT), and pulse density modulated (PDM) approaches to improve system efficiency and achieve a stable output. This type of control method is usually based on a full-bridge inverter to produce a stable output, and its operating frequency for electric vehicles is typically fixed at 85 kHz. In high-frequency WPT systems, reducing the parasitic resistance of coupling coils can improve transmission efficiency. In publications [14,15], the authors studied the impact of coil parasitic resistance and skin effect on system power and efficiency. They proposed a compromise solution to lower coil resistance and skin effect, thereby improving transmission efficiency. By designing the coil

compensation method, reactive power compensation can be achieved, thereby maximizing the transmission power. Yeong H. Sohn et al. conducted a comprehensive comparison of eight basic compensations, including SS, SP, etc. They found that SS and SP compensations exhibited superior properties in terms of maximum efficiency, maximum power transfer, load decoupling, and coupling coefficient decoupling. However, the primary side input impedance varied dramatically, and there were disadvantages, such as short circuits [16–18]. On the basis of single-element compensation, researchers have proposed many novel compensations. LCC/S and LC/S compensation structures have been proposed, which also exhibit constant current and constant voltage characteristics, as well as coupling independence and better ZVS or ZCS characteristics [19,20]. Si Li et al. successively proposed a tuning method for the LCC/LCC compensated topology in the application of wireless charging for electric vehicles. This method can easily achieve characteristics such as ZVS and constant voltage [21,22]. The research above focussed more on compensation methods for decoupling coupling coils. In the design of a high-frequency WPT system, more Class E and Class D inverters are used to improve transmission efficiency. However, these types of inverters are sensitive to variations in loads and coil position. The impedance matching method in RF is more suitable for high-frequency situations when using Class E and Class D inverters. When considering the coupling dependence during impedance matching, it is important to accurately analyze the impedance of the inverter.

An increase in operating frequency will lead to higher losses in the switching transistor at the transmitter side when designing high-frequency, high-power WPT systems. In order to solve this issue, Class E inverters can improve the transmission efficiency of the system by achieving ZVS and ZVDS characteristics with only one transistor [23–25]. However, Class E inverters are sensitive to variations in loads and component parameters, which often leads to impedance mismatch and decreased efficiency. Design methods for impedance extension have been introduced in order to overcome this drawback [26,27]. It improves the robustness of the system; however, it does not address the high voltage and current stresses. Therefore, new and improved single-transistor inverters of Class F and Class Φ have been developed from Class E, utilizing harmonics for waveform peak shaping, which can effectively reduce the occurrence of high stress [28–30]. However, it still fails to meet the requirements of high power due to the use of one single transistor. Class D inverters have low voltage stress, making them widely used in the field of high-frequency, high-power WPT systems [31]. However, the nonlinearity of the MOSFET's parasitic capacitance makes it challenging to accurately implement ZVS characteristics. Hamed T. addressed this problem by constructing an LC auxiliary network at the midpoint of the H-bridge. It achieves the ZVS characteristics over a wider range of Smith impedance circles [32–35]. The introduced LC auxiliary network is sensitive to the voltage stress on the MOSFET because it is positioned at the midpoint of the bridge. Furthermore, redundant auxiliary networks are not appropriate for high-power applications. Based on a 6.78 MHz Class E inverter, publications [36,37] proposed methods for optimizing a two-port impedance matching network and impedance compression network design. These methods have the advantage of enhancing the robustness of the coil in misalignment. Paper [38] utilized an adaptive impedance matching network based on Class E to address changes in the load and coil position. However, this method requires array capacitance and search algorithms, making it more complex to implement. There are various design methods for parameters and impedance in WPT systems. Intelligent algorithms and deep learning can also be used to optimize these parameters and impedance [39,40]. Combining the advantages of Class D and Class E inverters, Hirotaka K. et al. first proposed a Class DE-tuned power amplifier, which achieved a power transmission efficiency of 96% at 1 MHz [41]. Researchers have provided accurate time domain analysis waveforms and a parameter design approach for the half-bridge Class DE [42,43]. On this basis, the steady-state time-domain analysis of the full-bridge Class DE was proposed [44]. However, few people have investigated the application of Class DE inverters in wireless power transfer, although some researchers have described the use of half-bridge Class DE inverters in WPT systems at low power,

which enables low-power and high-efficiency power transfer at fixed loads [45]. Previous studies [46] have utilized Class DE inverters to achieve applications of wireless power transfer such as 100 W LED lighting. The aforementioned studies focus on the application and tuning of Class DE inverters in wireless power transfer in engineering. They did not discuss or study changes in load and coil position offsets like Class E inverters, nor did they propose corresponding impedance-adaptive solutions. Inheriting the load-sensitive characteristics of Class E inverters, Class DE inverters exhibit high sensitivity to components and loads. We can use impedance matching network optimization to achieve ZVS over a wide range of loads and enhance the impedance robustness of Class DE inverters in WPT systems. Currently, few studies have been conducted on the ZVS characteristics of Class DE inverters in WPT regarding impedance changes. Based on this issue, this article focuses on a design approach using impedance analysis that is suitable for high-frequency Class DE inverters in WPT systems.

Therefore, this paper will investigate how the ZVS characteristics of Class DE inverters are affected by changes in the impedance during impedance matching of the WPT system. We introduce a coil impedance matching compensation method tailored for Class DE inverters and suggest a $\pi 1a$ resonant network [47] and a parameter design approach suitable for Class DE inverters. This design approach achieves the ZVS characteristics in a wide impedance range of Class DE inverters, while maintaining the high efficiency of the inverter and system. This article is structured as follows: Section 2 presents the coil PS/PS impedance matching compensation structure, along with an analysis of how variations in load magnitude and coil position affect the input impedance. Section 3 analyses the effect of impedance on ZVS. The Class DE inverter for wide impedance ZVS is designed and optimized. Building the system based on the design for experiments is the focus of Section 4. We will discuss the experimental and simulation results and verify the feasibility of the method. The conclusion is finally presented in Section 5.

2. Characterization of Coupling Coils for PS/PS Impedance Matching Compensation

As shown in Figure 1, the Class DE wireless power transfer system mainly consists of the Class DE inverter, symmetrical PS/PS capacitor compensation network, coupling coils, and rectifier. The system is designed using a component impedance matching method. On both the primary and secondary sides of the coupling coil, resonance compensation is achieved through the use of symmetrical parallel-series capacitors. When the coupling coil is in its ideal position, the equivalent input impedance Z_R of the rectifier is directly reflected onto the inverter's load. The impedance seen from the transmit port is Z_{in} , therefore the equivalent load of the inverter is Z_R .

$$Z_{in} = Z_R, \quad (1)$$

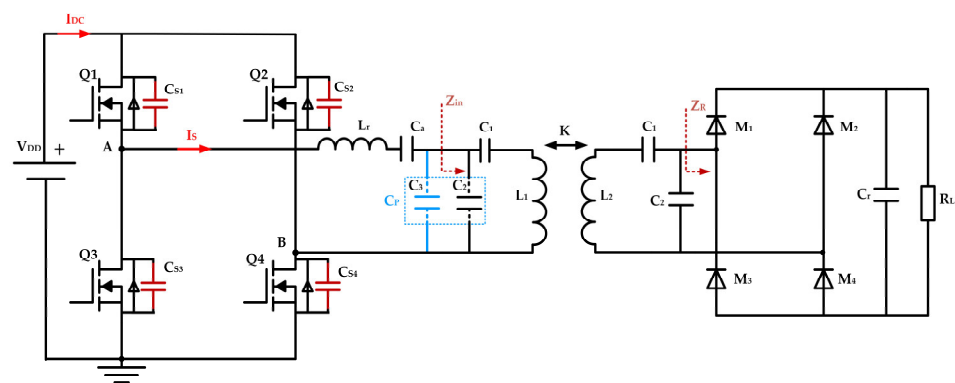


Figure 1. Class DE wireless power transfer system.

The Class DE inverter utilizes a composite resonant network, which includes a $\pi 1a$ impedance matching network, with shunt capacitance $C_P = C_3 + C_2$. The load of the

receiving coil mentioned above is equivalent to the input impedance of the full-bridge rectifier circuit, denoted as Z_R [48]:

$$Z_R = \frac{8}{\pi^2} R_L. \quad (2)$$

2.1. Coils PS/PS Impedance Matching Compensation

The decoupled equivalent circuit model is displayed in Figure 2. We disregard the parasitic characteristics of the transmitter and receiver coils' inherent capacitance and inductance and treat them as a two-port network. To finish the impedance matching, we used symmetrical PS/PS capacitors, C_1 and C_2 . By adopting the impedance matching approach, we can more effectively determine the matching parameters L_1 and L_2 of the coupling coils to achieve reactive power compensation at various locations. Based on the KVL and KCL equations, we can describe the circuit model shown in Figure 2. The currents and voltages in the equation below are in phase form.

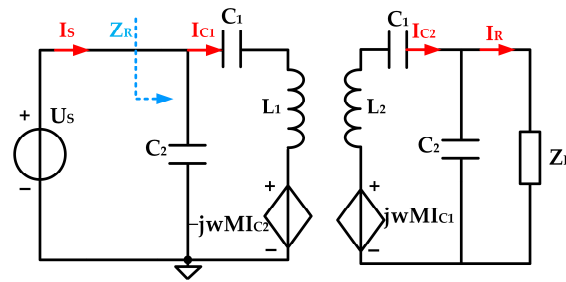


Figure 2. Symmetrical PS/PS impedance matching compensation topology.

$$\begin{cases} (I_S - I_{C1}) \frac{1}{j\omega C_2} - jI_{C1} \left(\omega L_1 - \frac{1}{\omega C_1} \right) + j\omega M I_{C2} = 0 \\ -j\omega M I_{C1} + I_{C2} \left[j \left(\omega L_2 - \frac{1}{\omega C_1} \right) + \frac{Z_R}{1 + j\omega Z_R C_2} \right] = 0 \\ -U_S + (I_S - I_{C1}) \frac{1}{j\omega C_2} = 0 \\ I_R Z_R - (I_{C2} - I_R) \frac{1}{j\omega C_2} = 0 \end{cases} \quad (3)$$

By introducing intermediate impedance variables Z_1 and Z_2 , the analysis can be further simplified to assist in solving Equation (3):

$$\begin{cases} Z_1 = \omega L_1 - \frac{1}{\omega C_1} \\ Z_2 = j \left(\omega L_2 - \frac{1}{\omega C_1} \right) + \frac{Z_R}{1 + j\omega Z_R C_2} \end{cases} \quad (4)$$

The coupling factor k of the coils can be expressed as the relationship between the mutual inductance M and L_1, L_2 .

$$M = k \sqrt{L_1 L_2}, \quad (5)$$

Combining Equations (2)–(5), they can be solved to obtain the receiving coil input impedance Z_{in} :

$$Z_{in} = \frac{U_S}{I_S} = j\omega C_2 + \frac{Z_2}{Z_1 Z_2 - (\omega k)^2 L_1 L_2}. \quad (6)$$

To achieve port impedance matching, the load can be directly reflected back to the transmitter, satisfying the scattering S-parameter matching condition in the RF field. As

shown in Equation (7), Z_{in} is based on the values of the real and imaginary parts. We are able to determine the required matching capacitors, C_1 and C_2 :

$$\begin{cases} Z_{in} = R_e(Z_{in}) + jI_m(Z_{in}) \\ R_e(Z_{in}) = Z_R \\ I_m(Z_{in}) = 0 \end{cases} \quad (7)$$

According to the impedance expressions (6) and (7) for the real and imaginary parts, we can determine the trends of $R_e(Z_{in})$ and $I_m(Z_{in})$ of the equivalent load Z_{in} of the Class DE inverter under variations in the load and coupling coefficient. Figure 3a,b shows that the load $Z_R = 50 \Omega$. There is a decrease in real impedance $R_e(Z_{in})$ to less than 50 when the coupling coefficient k is varied between 0.2 and 0.4. Pulling the coils farther away results in a decrease in k , while $I_m(Z_{in}) > 0$ indicates the introduction of inductive variations. Conversely, pulling the coils closer raises k , and $I_m(Z_{in}) < 0$ indicates the introduction of capacitive changes. Therefore, with the PS/PS impedance matching compensation method, the coupling coil offset will cause changes in both the real and imaginary parts. Meanwhile, the coil offset will only result in a smaller real part than Z_R . The imaginary part is negatively correlated with the change in the coupling coefficient. When $k = 0.3$ is fixed, the load Z_R varies from 30Ω to 80Ω . In Figure 3a, it can be seen that $R_e(Z_{in})$ follows the load, presenting a single increasing linear change with $I_m(Z_{in}) = 0$. All these impedance changes will directly affect the equivalent load of the Class DE inverter.

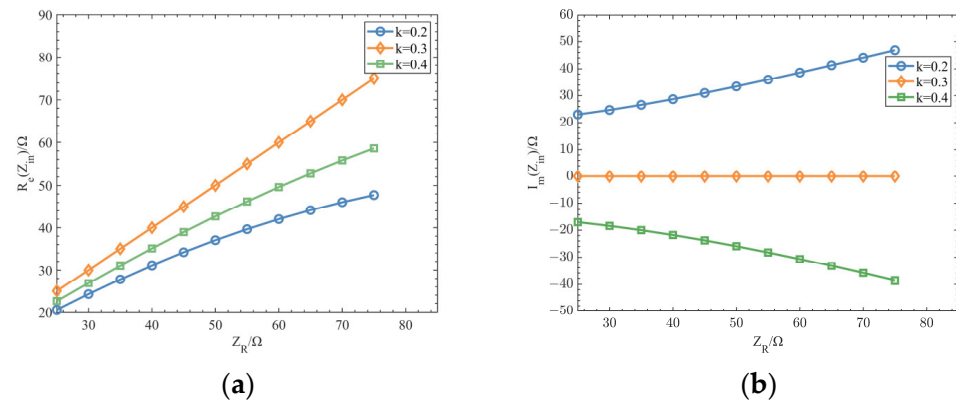


Figure 3. Effect of variation of k and Z_R on input impedance Z_{in} : (a) effect of k and Z_R on the real part of Z_{in} , (b) effect of k and Z_R on the imaginary part of Z_{in} .

2.2. Voltage Gain and Constant Voltage Characteristics

In contrast to the conventional compensation topology, the coupling coils are compensated by PS/PS impedance matching, which also exhibits constant voltage characteristics in terms of voltage gain and other factors. Based on the system of Equations (2)–(5), we can derive the expression for the magnitude of voltage gain, as shown in Equation (8):

$$G_V = \left| \frac{U_R}{U_S} \right| = \left| \frac{\frac{Z_R}{C_2} k \sqrt{L_1 L_2}}{\left(Z_R + \frac{1}{j\omega C_2} \right) \cdot \left(Z_1 Z_2 + (k\omega)^2 L_1 L_2 \right)} \right| \quad (8)$$

Based on the voltage gain expression, a gain plot can be obtained. In Figure 4, the horizontal axis of the graph represents the normalized frequency, while the vertical axis represents the voltage gain. We can see that this impedance-matching compensation method has two constant voltage output points.

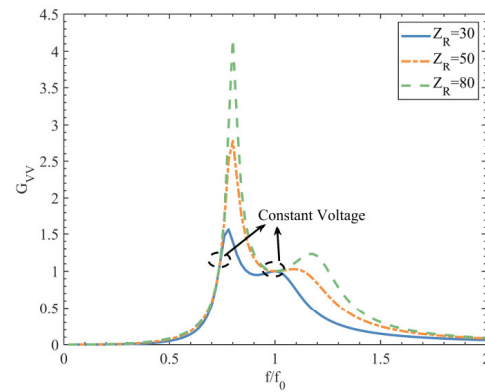


Figure 4. Voltage gain curve.

To fit the coupling coils to compensate the design and load output characteristics of the actual Class DE inverter, it is essential to achieve zero phase angle characteristics and constant voltage features. As a result, we need to ensure that the constant voltage point falls at the $f/f_0 = 1$.

3. Theoretical Analysis and Design of Class DE Inverters

3.1. Theoretical Description of Class DE Inverter

In Figure 1, a Class DE inverter is used as the transmitter-side power DC-AC converter. Based on the conventional full-bridge Class D inverter, four identical capacitors C_{S1} – C_{S4} are used in parallel with the MOSFETs. Table 1 displays the switching modes in the range $(0, 2\pi)$ for one cycle following the stabilized operation of the Class DE inverter, where D represents the duty cycle of the PWM signal that controls the MOSFETs. During mode ①, Q_1 and Q_2 are turned on, and the current $i_s(\theta)$ flows positively (setting the flow from point A to point B as positive). During mode ②, all MOSFETs are off, so the resonant cavity must be designed to be weakly inductive. Consequently, the current $i_s(\theta)$ cannot be mutated. It will continue to flow in the positive direction and charge the capacitors C_{S2} and C_{S3} . Modes ③ and ④ will repeat the process of the first half cycle, so they will not be further elaborated. A sine wave can be used to express the current $i_s(\theta)$, assuming that it is in a steady-state condition. Where I_m is the current amplitude and the phase angle $\theta = \omega t$, setting the initial phase induced by the resonant network to be φ :

$$i_s(\theta) = I_m \sin(\theta + \varphi). \quad (9)$$

Table 1. Class DE inverter working state.

Operation Modes		Switching Status			
		Q_1	Q_2	Q_3	Q_4
①	$0 < \theta < 2\pi D$	ON	OFF	OFF	ON
②	$2\pi D < \theta < \pi$	OFF	OFF	OFF	OFF
③	$\pi < \theta < \pi + 2\pi D$	OFF	ON	ON	OFF
④	$\pi + 2\pi D < \theta < 2\pi$	OFF	OFF	OFF	OFF

We can obtain the expression for the input voltage U_{AB} at port AB of the resonant network by following the description of the four operating modes, which are based on Kirchhoff's law and capacitor charging and discharging analysis in the time domain [42].

As demonstrated by Equation (10), where the operating frequency of the system is set as f_0 , and the angular frequency $\omega = 2\pi f_0$:

$$U_{AB} = \begin{cases} -V_{DD} & \textcircled{1} \\ \frac{2I_m}{\omega C_S} [\cos(\theta + \varphi) - \cos(2\pi D + \varphi)] - V_{DD} & \textcircled{2} \\ V_{DD} & \textcircled{3} \\ \frac{2I_m}{\omega C_S} [\cos(\theta + \varphi) + \cos(2\pi D + \varphi)] + V_{DD} & \textcircled{4} \end{cases} \quad (10)$$

The inverter resonant network allows only the fundamental wave component of U_{AB} to transfer power through the coupling coil. Since L_r and C_r resonate in series at operating frequency f_0 , as shown in Figure 5b, theoretically, $X_r = 0$. The L_f represents the phase-shifted inductance of the capacitor C_S for charging and discharging. Therefore, according to the Fourier series decomposition, we can decompose U_{AB} into the phase-shifted inductance component and the load R_S component. The load voltage U_{R_S} can be expressed as Equation (11).

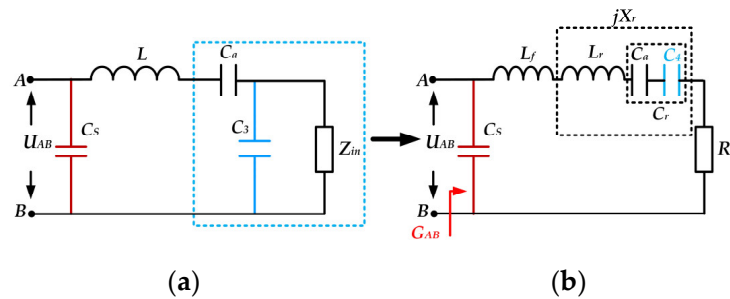


Figure 5. Equivalent circuit of $\pi 1a$ impedance-matched resonant network for Class DE inverter: (a) $\pi 1a$ matched resonant circuit, (b) $\pi 1a$ matched resonant equivalent circuit.

$$U_{R_S} = i_s(\theta)R_S = U_m \sin(\theta + \varphi). \quad (11)$$

According to Equation (10), we use Fourier series to decompose U_{AB} , and the amplitude U_m on the equivalent load R_S can be easily obtained.

$$U_m = \frac{1}{\pi} \int_0^{2\pi} U_{AB} \sin(\theta + \varphi) d\theta = \frac{4 \sin(\pi D + \varphi) \sin(\pi D)}{\pi} V_{DD}, \quad (12)$$

The DC input current I_{DC} of the inverter is an average of the total current of the four modes. In modes ② and ③, the bus does not supply energy; instead, the capacitor C_S undergoes charging and discharging cycles. Thus, the total current i_a is equal to the sum of the currents $i_{Q1}(\theta)$ and $i_{Q4}(\theta)$ flowing on Q_1 and Q_4 in mode ① and mode ④. Thus, the DC current can be expressed as the average amount of current i_a :

$$I_{DC} = \frac{1}{2\pi} \int_0^{2\pi} i_a d\theta = -\frac{2 \sin(\pi D + \varphi) \sin(\pi D)}{\pi} I_m. \quad (13)$$

In the ideal case, the output power P_{out} of the Class DE inverter should, theoretically, be equal to the input power P_{in} . In the design, we can determine the relationship between the input and output power and R_S according to Equation (14):

$$P_{in} = P_{out} = \frac{U_m^2}{2R_S} = \frac{I_m^2 R_S}{2} = V_{DD} I_{DD}. \quad (14)$$

Combining Equations (12) and (14), the solution for the input voltage of the Class DE can be found:

$$V_{DD} = \sqrt{\frac{R_S \pi^2}{8 \sin^2(\pi D + \varphi) \sin^2(\pi D)} P_{out}}. \quad (15)$$

3.2. Analysis of Wide Load ZVS Conditions

After the MOSFET is turned off, three corresponding states exist for the capacitor charging and discharging process due to the inertial current $i_s(\theta)$ caused by inductive reactance. In the initial condition, the MOSFET is unable to attain the ZVS characteristic since $i_s(\theta)$ is unable to completely extract the charge in the capacitor. At the moment the MOSFET is turned on, the charge will be instantaneously drained through the on-resistance. This results in the MOSFET current overshoot, as shown in Figure 6. It can be stated in terms of the voltage of the MOSFET, $V_{S4}(2\pi)$:

$$V_{S4}(2\pi) > 0 \text{ Non ZVS}. \quad (16)$$

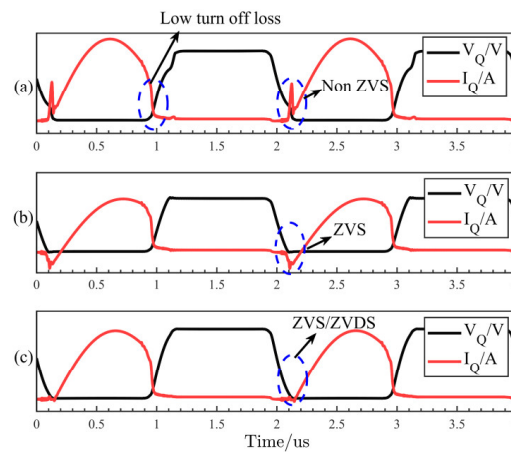


Figure 6. ZVS voltage and current waveforms: (a) In first state, MOSFETs can't attain the ZVS characteristic, (b) In second state, MOSFETs can attain the ZVS characteristic, (c) In third state, MOSFETs can attain both the ZVS and ZVDS characteristics.

The second state occurs when $i_s(\theta)$ crosses the zero point just as the charge in C_{Si} is drawn out and the voltage across the capacitor becomes zero. As a result, the ZVS characteristic is satisfied and also has the zero derivative ZVDS turn-on for Class E inverters, and optimal operation for Class DE. The voltage on Q_4 can be similarly represented in the second half cycle:

$$\begin{cases} V_{S4}(2\pi) = 0 & \text{ZVS} \\ \frac{dV_{S4}(\theta)}{d\theta} = 0 & \text{ZVDS} \end{cases}. \quad (17)$$

The third state occurs when $i_s(\theta)$ can fully discharge the charge in the capacitor C_{Si} . The current $i_s(\theta)$ keeps flowing in the original direction, and it will charge the capacitor in the opposite direction. When $V_{S4}(\theta) \approx -0.7$ V, the capacitor voltage will be clamped by the body diode. The ZVS characteristics of the inverter are displayed in the third plot in Figure 6. The inverter can be operated in a suboptimal state. Thus, the ZVS necessary condition at $\theta = 2\pi$ can be expressed as Equation (18):

$$\begin{cases} V_{S4}(2\pi) \approx 0 & \text{ZVS} \\ \frac{dV_{S4}(\theta)}{d\theta} < 0 & \text{Non ZVDS} \end{cases}. \quad (18)$$

Achieving ZVS across a wide range of load conditions requires finding a balance between the charging and discharging states of the capacitor. For state I, the capacitor can

not be fully discharged, and the loss is larger. State II allows the inverter to work optimally; however, it has to finish charging and discharging the capacitor when the current crosses zero. This approach has a high sensitivity to components, making it the best option for state III to obtain robust impedance characteristics. We select an appropriate initial phase angle φ to achieve high efficiency with minimal loss and impedance perturbation capability. The shunt capacitor C_{S_i} will significantly reduce the turn-off loss.

According to the above description, combining Equations (9), (10), and (18), we can derive the sufficient condition of ZVS, which is met by the condition of state III:

$$V_{DD} = -\frac{I_m[\cos(\varphi) + \cos(2\pi D + \varphi)]}{\omega C_s}. \quad (19)$$

The capacitance in the above equation meets the requirement of the sum of the parallel capacitance C_{S_i} in the same bridge, i.e.,

$$C_s = C_{S1} + C_{S3} = C_{S2} + C_{S4}. \quad (20)$$

Combining Equations (13) and (19), we can determine the magnitude of the shunt capacitance C_s :

$$C_s = \frac{2\sin[2(\pi D + \varphi)]\sin(2\pi D)}{R_s \pi \omega}. \quad (21)$$

3.3. Wide Load ZVS Matched Resonant Network Design

The idea of this system design is to achieve an impedance-matching design from R_s to Z_{in} by using Z_R as the impedance-matching node. An $\pi 1a$ impedance matching network is introduced from Figure 5b to Figure 5a. The total impedance of the parallel capacitor C_3 and impedance Z_{in} in Figure 5a needs to exactly match the total impedance value of the series capacitor C_4 and load R_s in Figure 5b. In Figure 5, the reactance factor q of the Z_{in} - C_3 and R_s - C_4 equivalent two-port can be expressed by Equation (22):

$$q = \frac{Z_{in}}{X_{C3}} = \frac{X_{C4}}{R_s}. \quad (22)$$

From the property of equal impedance of Z_{in} - C_3 and R_s - C_4 , we can determine the value of R_s :

$$R_s = \frac{Z_{in}}{1 + q^2}. \quad (23)$$

From Equations (22) and (23), the capacitive resistance X_{C4} of C_4 can be obtained here:

$$X_{C4} = \frac{Z_{in}q}{1 + q^2}. \quad (24)$$

The total impedance Z_1 of the parallel Z_{in} - C_3 can be expressed as follows:

$$Z_1 = \frac{1/\omega C_3}{1/\omega C_3 Z_{in} + \omega C_3 Z_{in}} + j \frac{-Z_{in}}{1/\omega C_3 Z_{in} + \omega C_3 Z_{in}}. \quad (25)$$

In Equation (25), a relationship is defined by the function $1/x + x > 2$. This indicates the presence of maximum points in both the real and imaginary parts of the impedance Z_1 .

In Figure 7 the reactance factor $q = 1$. When the equivalent load Z_{in} is varied, the load R_s will be compressed below the maximum value, while the imaginary part of the capacitive reactance X_{C4} can be compressed below the capacitive reactance X_{C3} . Consequently, we can accomplish simple impedance compression using this $\pi 1a$ Impedance matching network, appropriately extending the range of ZVS for the load.

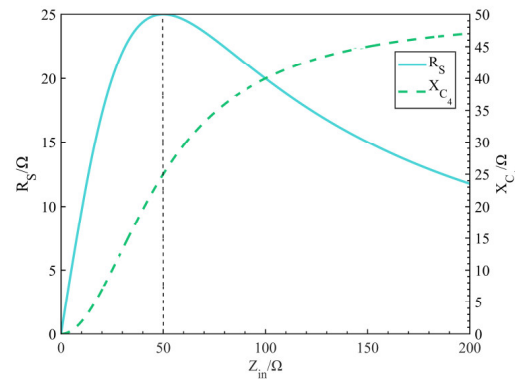


Figure 7. Impedance characteristics of $\pi 1a$ matching network.

In Figure 5b, the admittance seen from port AB is denoted as Y_{AB} . We can think of the resonant network as capacitor C_S in parallel with the back-end series resonant circuit. In Figure 5b, jX_r represents the total impedance value of inductor L_r and capacitor C_r , where C_r is composed of series capacitors C_a and C_4 . Hence, we can determine the conductance Y_{AB} :

$$\begin{cases} Y_{AB} = G + jB \\ G = \frac{R_S}{R_S^2 + X_S^2} \\ B = \omega C_S - \frac{X_S}{R_S^2 + X_S^2} \\ X_S = \omega L_f + X_r \end{cases} \quad (26)$$

The initial phase and amplitude of the current $i_s(\theta)$ are mainly caused by the conductance Y_{AB} . We can derive the relationship equation between the initial phase φ and the impedance:

$$\varphi = \pi + \tan^{-1}\left(\frac{B}{G}\right). \quad (27)$$

Combining Equations (26) and (27), we can solve the relational function for L_f and φ from the impedance perspective and derive L_f according to Equation (28):

$$\omega C_S (\omega L_f)^2 - \omega L_f = \tan(\varphi) R_S - \omega C_S R_S^2. \quad (28)$$

In the inverter, we have utilized the circuit topology of LC series resonance, allowing us to determine L from the quality factor Q :

$$L = \frac{Q R_S}{\omega}. \quad (29)$$

Based on Equations (28) and (29), we have solved for L_r :

$$L_r = L - L_f. \quad (30)$$

Since L_r and C_r resonate at the operating frequency f_0 , the value of C_r can be obtained:

$$C_r = \frac{1}{\omega^2 L_r}. \quad (31)$$

In the impedance transformation compression network, setting the reactive power factor q to 1 allows us to obtain the values of capacitors C_3 and C_4 based on Equation (22).

As shown in Figure 5b, the capacitor C_r is composed of C_a and C_4 in series, so that the value of C_a can be obtained:

$$C_a = \frac{1}{\omega^2 C_r} - \frac{1}{\omega^2 C_4}. \quad (32)$$

3.4. Analysis of the Effect of Parameter Variations on the Wide Load ZVS

The design methodology for all parameters has been provided in the previous sections. However, further investigation is required to explore the impact of component parameter variations and load variations on the ZVS of the Class DE inverter. To maximize the wide load ZVS characteristics of Class DE inverters with minimal losses. It is necessary to explore the effect of impedance on the initial phase angle φ . In Figure 5b, the impedances jX_r and R_S actually change with the impedance Z_{in} . Since wireless power transfer is influenced by the coupling coefficient k and the equivalent load Z_R , there are two situations for the variation of Z_{in} .

The first situation occurs when the coils are in an optimal state. In this case, there is only a change in the load R_{in} . According to Figure 3, it is known that the equivalent impedance Z_{in} of the Class DE inverter will not have an imaginary part; only the real part of the impedance changes. According to Equation (25) and Figure 7, it can be observed that $R_S < 0.5Z_{in}$ holds constantly. According to Figure 5b and Equation (25), the variation of impedance X_r can be expressed as:

$$X_r = \omega L_r - \frac{1}{\omega C_a} - \frac{Z_{in}}{1/\omega C_3 Z_{in} + \omega C_3 Z_{in}}. \quad (33)$$

The second situation is when there is an offset in the coupling coils. Figure 3b shows that using this compensation design method introduces an imaginary part, while the real part changes less than Z_{in} . Thus, the impedance Z_{in} reflected to the inverter will have both real and imaginary parts:

$$Z_{in} = R_{in} + jX_{in}. \quad (34)$$

Due to the presence of the imaginary part, the $\pi 1a$ impedance matching network will not exhibit typical impedance compression characteristics. It has a direct effect on the equivalent impedances R_S and X_r in Figure 5b. A complex impedance matching equation can be obtained from Equations (25) and (34):

$$\begin{cases} R_S = \frac{(1-X_{C_3}X_{in})R_{in}+X_{C_3}X_{in}R_{in}}{(1-X_{C_3}X_{in})^2+(X_{C_3}R_{in})^2} \\ X_r = \omega L_r - \frac{1}{\omega C_a} + \frac{(1-X_{C_3}X_{in})X_{in}-X_{C_3}R_{in}^2}{(1-X_{C_3}X_{in})^2+(X_{C_3}R_{in})^2} \end{cases}. \quad (35)$$

It has been clearly analyzed earlier that the ZVS necessary condition for wide loads needs to be satisfied in Equation (18). From the impedance design perspective, the wide load necessary condition is to ensure that the input current of the resonant network input current lags behind the voltage. Thus, according to Equations (27) and (28), we can obtain the optimality condition for the existence of a wide load ZVS, which is required to keep the conductance angle β at the AB port of the resonant network less than or equal to 0, i.e.,

$$\beta = \tan^{-1}\left(\frac{B}{G}\right) \leq 0. \quad (36)$$

We can directly determine whether the resonant network is inductive or not based on the admittance angle β . Figure 8 illustrates the effect of shunt capacitance C_S with different multiples of α on the admittance angle β at the optimum distance of the coils. It can be seen that a larger load Z_R leads to an increase in β , and there exists a value such that $\beta = 0$. This is the critical value for the realization of ZVS. The range of load Z_R for $\beta < 0$ can be expanded when the design value αC_S is less than or equal to the theoretical value C_S . There

will be a decrease in the load Z_R range for $\beta < 0$ When $\alpha C_S < C_S$. Therefore, to achieve wide load ZVS, $\alpha < 1$ can be taken moderately in designing the parameters. In this paper, the α coefficient is set at 0.85, which expands the ZVS region. However, an excessively small α can also lead to increased reactive power and longer body diode recovery time.

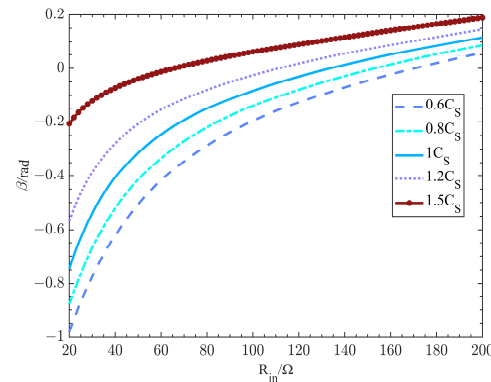


Figure 8. Variation of coil alignment load Z_R and variation of C_S with different ZVS ranges.

Figure 9 illustrates the variations in R_S and X_r in the resonant network of the inverter, which result from changes in the imaginary and real parts caused by coil offsets. In Figure 9a, according to the resonance network in Figure 5, we designed the theoretical value $X_r = 0$. However, the variation in the coil position will lead to a change in the imaginary part. In Figure 9a, when $X_{in} > 0$, this results in $X_r > 0$, leading to a smaller conductance angle β . At this point, ZVS state III is still satisfied and can be said to be over ZVS. Conversely, working in state II, ZVS is completely lost. In Figure 9b, the imaginary part X_{in} is excessively large, leading to a significant variation of R_S , indicating the failure of the $\pi 1a$ impedance matching network.

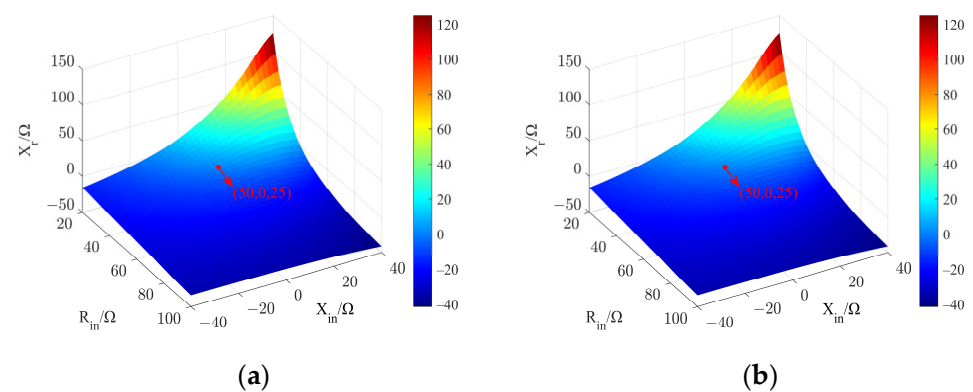


Figure 9. Effect of coil offset on resonant network X_r and R_S : (a) coil offset reflected impedance causes X_r change, and (b) coil offset reflected impedance causes R_S change.

Figure 10 illustrates the impact of variations in R_S , X_r , and αC_S on the ZVS region. Where the color change represents the magnitude of β at the theoretical value of C_S , the dashed region indicates $\beta < 0$, which we consider achievable for ZVS. We can see that $\alpha < 1$ for coils offset also widens the ZVS region, thus canceling out the effect of the imaginary part introduced by coils offset on the Class DE inverter.

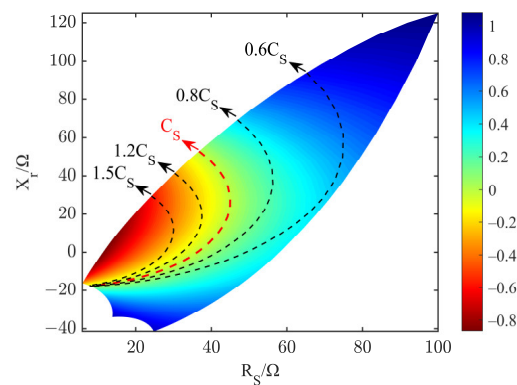


Figure 10. Effect of different values of the C_S parameter on the ZVS region under coil offset.

In summary, lowering the value of C_S to sacrifice a small portion of reactive power can widen the ZVS region of the Class DE inverter and improve the overall system efficiency, regardless of whether the coil is offset or the load is altered. The combination of impedance transformations in compression networks, along with selected values of C_S can enhance the impedance robustness characteristics of wireless power transfer systems without escalating the cost of hardware and software.

4. System Validation and Loss Analysis

Simulators using Semitrix-SIMPLIS 8.3.Ink software were run to confirm the viability of the suggested system parametric design method described above. The purpose of these simulations was to validate the accuracy of the previous analysis. For this purpose, we utilized the SPICE model of semiconductor devices, with a specific focus on the MOSFET—an Infineon SiC-MOSFET with model number IMZ120R060M1H. Additionally, the rectifier bridge was represented by a Rohm SiC Schottky diode with model number SCS220AM. Better compatibility between the ZVS simulation details and the experimental procedure was ensured by this selection. For inductor and capacitor simulations, ideal passive devices were utilized. The specific experimental parameters for the simulation were carefully designed and summarized in Table 2.

Table 2. System parameter design.

Symbol	Parameter	Value
k	Coil coupling coefficient	0.3
α	Shunt capacitance factor	0.85
φ	Initial phase shift capacitance	2.82 rad
C_1	compensation series capacitance	5.36 nF
C_2	compensated shunt capacitance	6.32 nF
C_P	compensated shunt capacitance	12.43 nF
L_1/L_2	Primary and secondary inductance	27.3 μ H
R_L	Load resistance	35~110 Ω
L	Inverter resonant cavity inductance	40.23 μ H
D	Duty cycle	0.423
Q	Quality factor	5.05
C_S	MOSFET parallel total capacitance	1.2 nF
f_0	Operating frequency	500 kHz
C_a	resonant compensation capacitance	3.776 nF

4.1. System Loss Analysis

In real circuits, the main sources of loss in high-frequency WPT systems are the semiconductor devices, the parasitic resistance of the components, and the resistance of the coupling coils. In this paper, we have used the design method of soft-switching Class DE inverter technology. This approach reduces most of the MOSFET switching losses, and the

impact of switching losses is no longer considered in the analysis. Thus, the main energy loss of the system depends on the impact of parasitic resistance in the component and the on-state voltage drop of diodes. Assuming consistency in the power device parameters, we consider that the on-resistance of the MOSFET is $r_{Q1} = r_{Q2} = r_{Q3} = r_{Q4} = r_Q$. Hence, the on-resistance loss of the MOSFET in one cycle is obtained:

$$P_{S_{Q1}} = P_{S_{Q4}} = \frac{1}{2\pi} \int_0^{2\pi} i_s^2(\theta) \cdot r_Q d\theta = \frac{1}{2\pi} \int_0^{2\pi D} i_s^2(\theta) \cdot r_Q d\theta \\ = \frac{r_Q \cdot I_m^2}{8\pi} \{4\pi D - [\sin(4\pi D + 2\varphi) - \sin(2\varphi)]\} \quad (37)$$

$$P_{S_{Q2}} = P_{S_{Q3}} = \frac{1}{2\pi} \int_0^{2\pi} i_s^2(\theta) \cdot r_Q d\theta = \frac{1}{2\pi} \int_{\pi}^{\pi+2\pi D} i_s^2(\theta) \cdot r_Q d\theta \\ = \frac{r_Q \cdot I_m^2}{8\pi} \{4\pi D - [\sin(4\pi D + 2\varphi) + \sin(2\varphi)]\} \quad (38)$$

Therefore, according to the above equation, the total loss of on-resistance in one cycle can be obtained:

$$P_{S_Q} = \frac{r_Q \cdot I_m^2}{2\pi} [4\pi D - \sin(4\pi D + 2\varphi)]. \quad (39)$$

During operating situation ② and ④ of the Class DE inverter, currents are renewed through the body diode. We assume that the turn-on voltage of the body diode is about 0.7 V. Therefore, the loss on the body diode can be obtained in one cycle:

$$P_{Q_{D1}} = P_{Q_{D4}} = \frac{1}{2\pi} \int_{2\pi D}^{\pi} 0.7 \cdot i_s(\theta) d\theta \\ = \frac{0.7 I_m}{2\pi} [\cos(\varphi) + \cos(2\pi D + \varphi)] \quad (40)$$

$$P_{Q_{D2}} = P_{Q_{D3}} = \frac{1}{2\pi} \int_{\pi+2\pi D}^{2\pi} 0.7 \cdot i_s(\theta) d\theta \\ = \frac{0.7 I_m}{2\pi} [\cos(2\pi D + \varphi) - \cos(\varphi)] \quad (41)$$

According to Equations (40) and (41), the total losses can be obtained which are generated by the body diodes:

$$P_{Q_D} = \frac{1.4 I_m}{\pi} \cos(2\pi D + \varphi). \quad (42)$$

In the impedance resonant network, we assume that the total parasitic equivalent resistance of the inductance and capacitance is r_{LC} , we can obtain the total resonant network parasitic resistance loss power.

$$P_{r_{LC}} = \frac{1}{2\pi} \int_0^{2\pi} i_s^2(\theta) \cdot r_{LC} d\theta = \frac{r_{LC} \cdot I_m^2}{2}, \quad (43)$$

Coupling coils are used as loosely coupled transformers, and their primary losses in power transmission are categorized into two types: the loss generated by the DC internal resistance $r_{dc-coil}$ of the coil and the AC internal resistance $r_{ac-coil}$ loss generated by the skin effect. We only consider the skin effect and ignore the proximity effect. Therefore, based on the previous analysis of the coupling coil, the DC loss can be obtained:

$$P_{r_{dc-coil}} = \frac{[|I_{C1}|^2 + |I_{C2}|^2] \cdot r_{dc-coil}}{2}. \quad (44)$$

However, the main source of heat in the coupling coil is the AC internal resistance. Where the AC internal resistance arises due to the skin effect at high frequencies, it is a

function of frequency and skin depth. According to paper [49], an approximate expression for the AC resistance $r_{ac-coil}$ can be obtained:

$$\begin{cases} r_{ac-coil} = r_{dc-coil} \frac{t}{\delta(1-e^{-t/\delta})(1+\frac{t}{w})} \\ \delta = \frac{1}{\sqrt{\pi\mu f\sigma}} \end{cases} \quad (45)$$

In the above equation, σ represents the conductivity, μ represents the permeability of copper, t represents the coil line width, and w represents the line thickness. In this paper, copper line is used as the design material for the coil. Therefore, $t/w = 1$. Finally, according to Equation (45), we can obtain AC loss caused by the skin effect:

$$P_{r_{ac-coil}} = \frac{[|I_{C1}|^2 + |I_{C2}|^2]}{2} \cdot r_{dc-coil} \cdot \frac{t}{\frac{2}{\sqrt{\pi\mu f\sigma}} \left(1 - e^{-\frac{t}{\sqrt{\pi\mu f\sigma}}}\right)} \quad (46)$$

4.2. Simulation Verification

Based on the analysis above, the circuit simulation was constructed using Semitrix-SIMPLIS 8.3.Ink software, and only the switching losses were taken into account in the simulation. Each of the three working conditions was simulated in Semitrix simulation software. The first scenario involved a static wireless power transfer where the rectifier load Z_R was varied from 30Ω to 80Ω . The second scenario included dynamic wireless power transfer with coupling coils position offset, where the impedance matching design method results in changes in the real and imaginary parts. The third case examined transmission for various power levels at optimal loads and distance of coupling coils.

In the first scenario, the simulation was conducted with the coupling coils in their optimal state while varying the load. According to Figure 11a, we can ensure that the Class DE inverter operates in the ZVS region when the equivalent load Z_R varies from 30Ω to 80Ω . The turn-off of the MOSFET will reduce the turn-off loss caused by the capacitance C_s connected in parallel. Figure 11b shows the curves of the input voltage V_{AB} and input current I_{AB} for the load-varying resonant port AB. ZVS can be reached for all load variations, but the diode's turn-on time is prolonged because of the excessively large initial phase. However, its overall efficiency is higher than that of hard switching. In the second case, coils change position. Figure 11c,d indicates that achieving ZVS characteristics with low turn-off losses is possible for Class DE inverters with coupling coefficients ranging from 0.25 to 0.45.

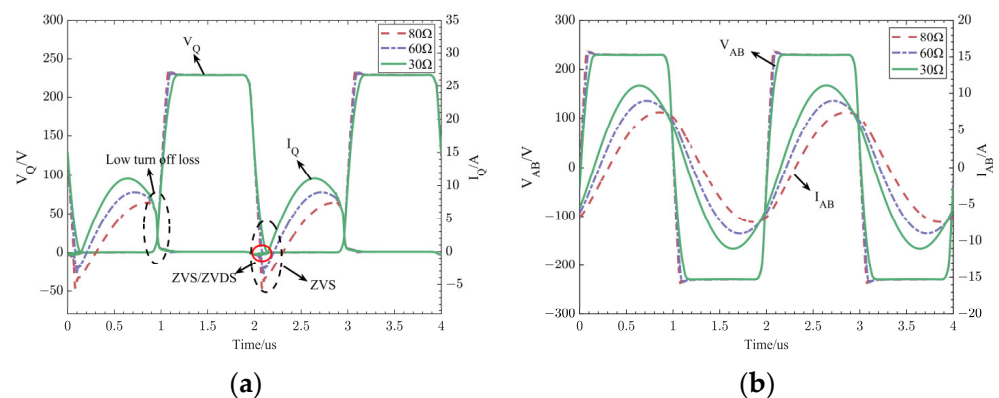


Figure 11. Cont.

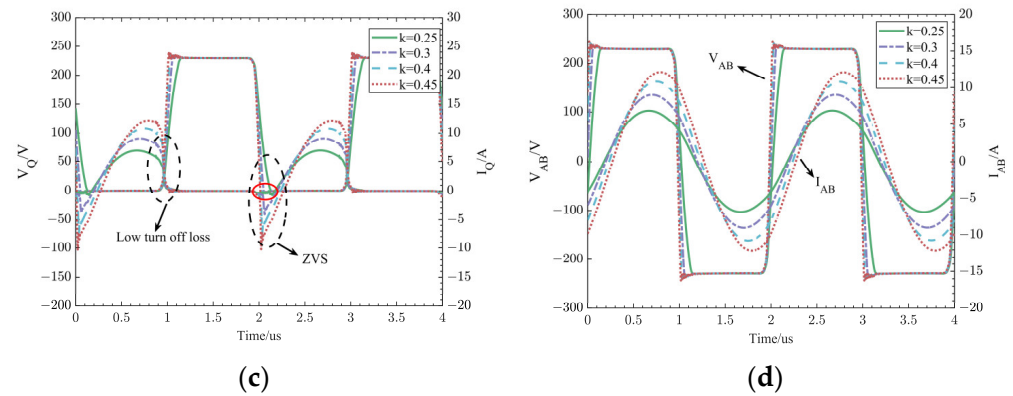


Figure 11. Load and coupling factor variation ZVS curves: (a) load variation ZVS curve, (b) load change port AB voltage-current curve, (c) ZVS curve for variation of coupling factor k , and (d) AB voltage-current curves for ports with varying coupling factor k .

In conclusion, it is known from simulation and theory that the ZVS region occurs when $Z_R > 30 \Omega$ and $k > 0.25$. The coil coupling factor and load become larger, causing the initial phase to increase, which will also prolong the diode conduction time and increase reactive power. Therefore, it is advisable to carefully select the appropriate value of C_S during the design phase.

4.3. Experimental Verification

Figure 12 shows an experimental prototype of a 1 kW system constructed using the impedance-matching design method. In Figure 12, we measured the high-frequency AC output voltage of the Class DE inverter using a Tektronix THDP0200 high-voltage probe made by Tektronix in Beaverton, OR, USA, and the high-frequency AC output current using a HIOKI 3276 current probe made by HIOKI in Ueda, Nagano, Japan. The bandwidth of the voltage probe was 200 MHz, while the bandwidth of the current probe was 30 MHz. The operating frequency of the prototype is 500 kHz, so the accuracy of the voltage and current measurement instruments was good. For high-power and high-frequency power transfer, we calculated the efficiency of Class DE inverters by measuring the root mean square (RMS) values of voltage and current. However, the measurement accuracy of the current probe may be affected by nearly electromagnetic interference, and the voltage-current probe will produce the effect of temperature drift and other measurement errors. In fact, these effects are negligible. All MOSFETs and diodes are identical to those in the simulation, and the specific design parameters can be found in Table 2. To simulate load variations, the rectifier load was utilized as an adjustable electronic load based on the three different working conditions that were confirmed in the simulation mentioned earlier. For the first scenario, the DC input supply was fixed at 260 V, the coupling coil was aligned, and the equivalent load Z_R was varied. An oscilloscope was used to measure the voltage and current curves of the MOSFETs in the Class DE inverter.

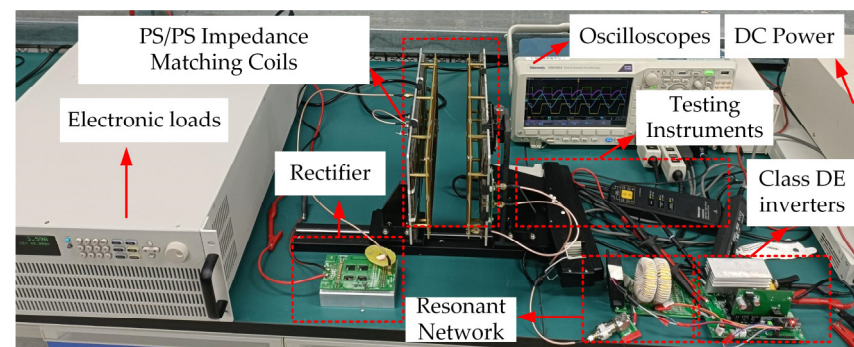


Figure 12. Experimental prototype platform.

The ZVS curves and the voltage-current curves of the resonant network for the tested MOSFETs with load resistance Z_R of 30 Ω , 60 Ω , and 80 Ω , respectively, are displayed in Figure 13a–c. We can observe that the inverter consistently followed the ZVS soft-switching characteristics and exhibited low turn-off losses based on the voltage-current curves of the MOSFETs. As the value of Z_R increased, the initial phase angle of the input current to the AB port also increased, resulting in a longer time for it to pass through the body diode. The inverter exhibited ZVS characteristics, resulting in lower overall losses at high frequencies compared to the hard-switched state. This verifies the effectiveness of resonant network design for wide-load ZVS of inverters.

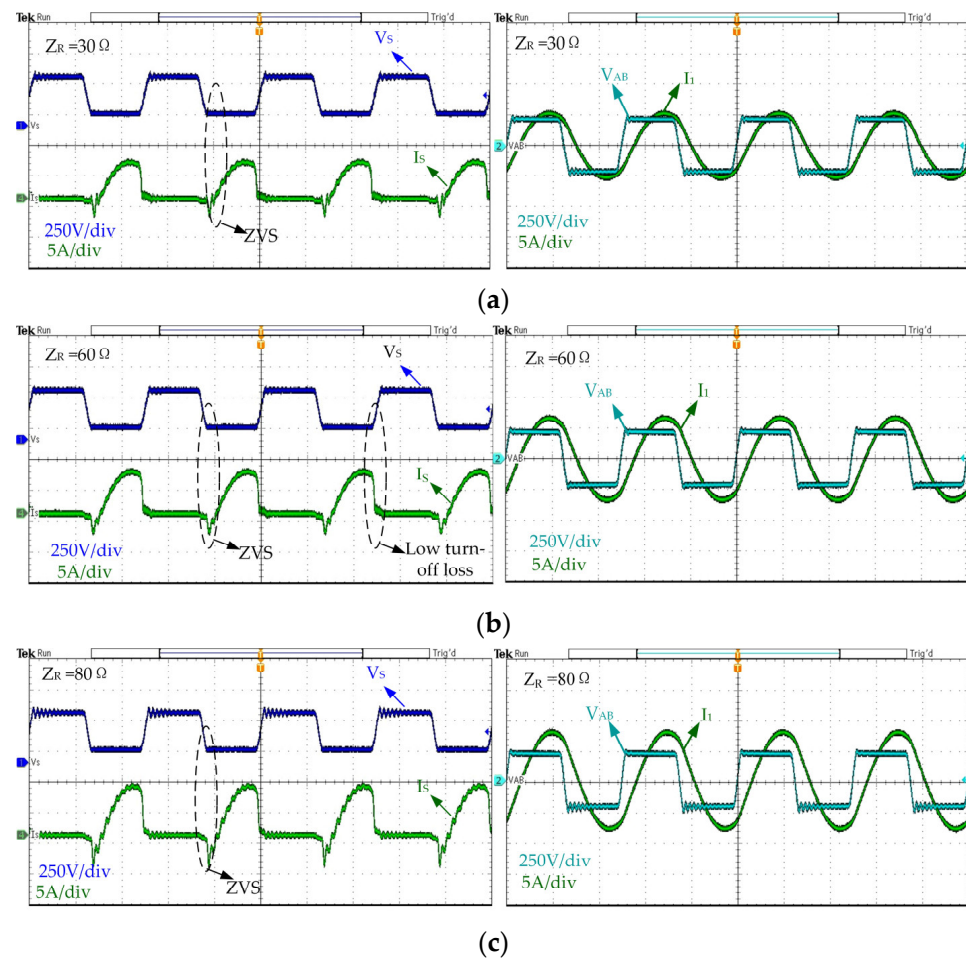


Figure 13. Load variation ZVS curve and input voltage-current curve: (a) test curve for load equal to 30 Ω , (b) test curve for load equal to 60 Ω , and (c) test curve for load equal to 80 Ω .

In the second scenario, experiments are conducted to observe changes in the real and imaginary parts of the impedance resulting from the coil position offset. The ZVS curves of the MOSFETs and the voltage-currents curves of the resonant network were tested at coil distances d of 4 cm, 5.5 cm, and 6.5 cm in Figure 14a–c. From Figure 14, it can be seen that the Class DE inverter operates in the ZVS state when the distance was varied from 4.5 cm to 6 cm. The initial phase angle of the input current to the AB port of the resonant network increased as the coil distance increased. This resulted in a longer time for the current to pass through the body diode, an increase in reactive power, and a reduction in efficiency.

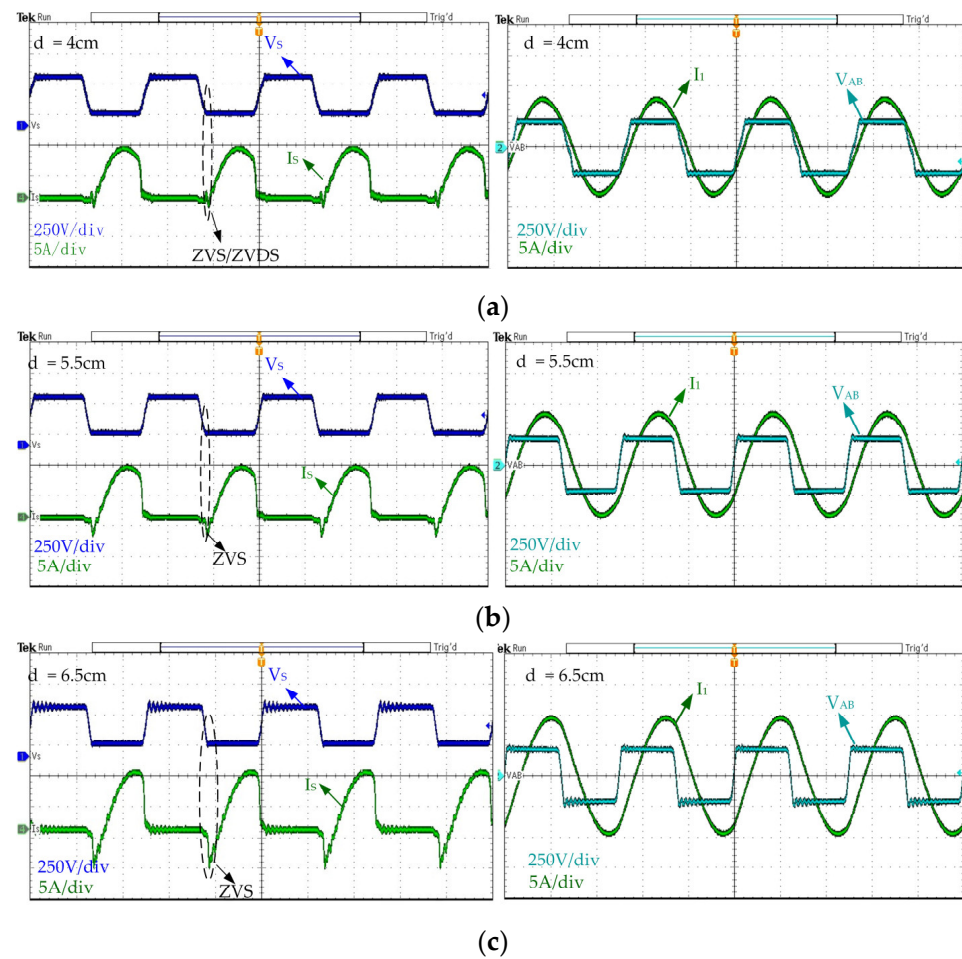


Figure 14. Coil position offset ZVS curve and input and output voltage and current curves: (a) coupling coil distance $d = 4$ cm test curve, (b) coupling coil distance $d = 5.5$ cm test curve, and (c) coupling coil distance $d = 6.5$ cm test curve.

Figure 15 shows that the trends in simulated and experimental efficiency were similar when the load and the distance between coupling coils were changed. In Figure 15a, Z_R changed from 30Ω to 80Ω . We can see that the inverter efficiency was greater than 95%, with the highest efficiency being 97.3%, and the system efficiency consistently exceeded 87.5%. In Figure 15b, the coil distance d ranged from 4.5 to 6 cm. The efficiency of Class DE inverters is shown to be above 95% in Figure 15b, where the coil distance d varied from 4.5 to 6 cm. The highest efficiency, meanwhile, reached 96.3%. Additionally, the system efficiency was greater than 87%. Figure 15 also shows that the small phase shift angle and the small reactive power introduced were what caused the highest efficiency point to exist. Figure 16 illustrates the third test condition, showing that the system's output power capability increased linearly with load variation. It also illustrates the direct introduction of the load into the load side of the inverter through impedance matching. It should be noted that the simulated passive components were all ideal components. The actual efficiency of the system simulation is generally higher than the experimental efficiency. This is mainly because this paper focuses solely on the Class DE inverter and coupling coil compensation. The receiver-side rectifier in the experiment was not best matched or optimized.

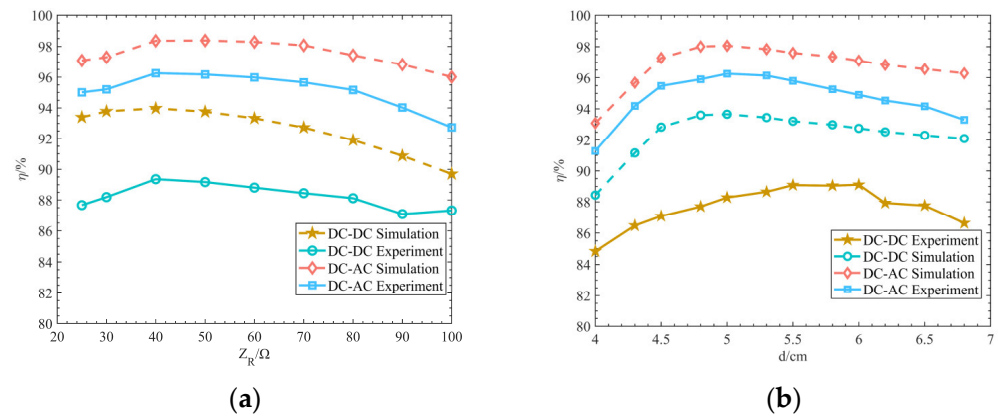


Figure 15. Efficiency curves for load and coupling factor variation: (a) load variation efficiency curve, and (b) coupling factor variation efficiency curve.

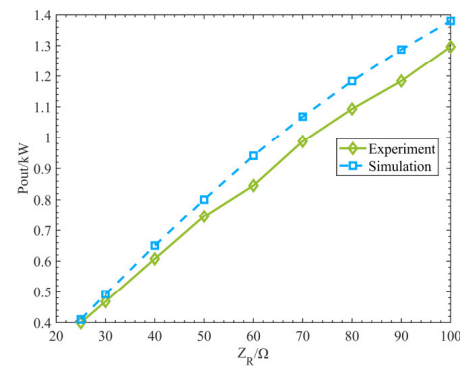


Figure 16. Variation curve of output power capacity.

This impedance-matching compensation method can be implemented using RF tools like vector network analyzers. From the impedance matching perspective, it is easier for us to adjust and optimize the coil to achieve the best impedance design conditions for the system. In the later stages, without communication, closed-loop control can be implemented through a secondary DC-DC converter to achieve a controllable and stable voltage output of the system. Variable compensation capacitors or phase shifts on the secondary side can be built to achieve Class DE inverters with full impedance ZVS and ZVDS characteristics.

5. Conclusions

This paper analyses the impedance characteristics of Class DE inverters under various operating conditions. In the WPT system, the proposed symmetrical PS/PS impedance matching design method is used to compensate for the coupling coils. Meanwhile, Class DE inverters are load-sensitive and have an optimum design load. It is more suitable for impedance matching. The impact of load and coil position variations on the impedance of Class DE inverters is detailed in the analysis of this paper. To overcome the sensitivity of Class DE inverter impedance, a proposed impedance transform resonant network is used to broaden the purely resistive ZVS operating region of Class DE inverters. Furthermore, the impact of resonant network and shunt capacitance parameters on the ZVS region of Class DE inverters is analyzed. To enhance the wide impedance perturbation capability of Class DE inverters, we can reasonably choose the parameters of the shunt capacitance, which also helps in lowering the turn-off losses. Finally, the article presents a comprehensive impedance-matching design process for WPT systems and validates it through experiments and simulations. A prototype WPT system was constructed, and the Class DE inverter can achieve soft-switching characteristics when $Z_R > 30 \Omega$ or $k > 0.25$. The efficiency of Class DE inverter is over 95% when Z_R ranges from 30Ω to 80Ω or d ranges from 4.5 cm to

6 cm. The system efficiency is greater than 87%. The output power had an approximate linear relationship with the load, and the load exhibited an approximately constant current characteristic. This paper is more informative for the system design of static wireless power transfer systems in specific applications.

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