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A Highly Flexible Passive/Active Discrete-Time Delta-Sigma Receiver

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Abstract: This paper presents a fourth-order discrete-time direct RF-to-digital Delta-Sigma receiver architecture for flexible receivers with a wide frequency range. The use of a current-driven passive mixer with RF feedback enables high-Q bandpass filtering and relaxes the linearity requirement of the RF amplifier. In addition, the reconfigurable passive/active loop filter offers a good compromise between power consumption, linearity, and dynamic range. The other important feature of the proposed architecture is the use of a sampling frequency that is a divisor of the LO frequency. This solves several problems such as the upmixing of quantization noise, the need to reconfigure the Delta-Sigma loop when changing the LO frequency, and the use of two independent clocks for the LO and the sampling frequency. The circuit was implemented using 65 nm CMOS technology. The I/Q Direct Delta-Sigma receiver has an RF bandwidth of 20 MHz and a sampling frequency of 400 MHz. Measurement results show a very high dynamic range of up to 80 dB with a peak SNDR of 46 dB for a power consumption of 46 mW at 800 MHz.

Keywords: RF to digital receiver; Delta Sigma modulation; CMOS implementation

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1. Introduction

Recently, the number of applications requiring efficient connectivity has grown considerably. Wireless communication, one of the main means of communication, is currently driven by mobile traffic with classic communication standards such as LTE, 5G, or WiFi, as well as newer standards grouped under the IoT umbrella. Radio frequency (RF) receivers have to cope with many frequency bands that can be as low as 300 MHz or as high as 6 GHz [1]. This very crowded spectrum imposes very high in-band and out-of-band linearity constraints on the receiver, which has to cope with blockers whose levels are several tens of dB higher than the received signal [2].

Therefore, receivers nowadays need to be more flexible in terms of LO frequency coverage to be able to cover the communication standard frequency bands. Gain flexibility is needed to relax the dynamic range constraints on the analog-to-digital converter. Adjusting the signal bandwidth, noise figures, and filtering capability is also required to switch between modes and standards as discussed in [3,4]. Using artificial intelligence has also been explored to optimize the flexibility and performance of receivers [5].

In the last few decades, many receiver architectures have been proposed to meet these requirements. The passive mixer-first receiver architecture was presented for the first time in [6,7]. Improved implementations of this architecture include a noise canceling technique

to improve its Noise Figure (NF) with acceptable linearity degradation and additional power consumption [8]. Linearity improvements were also proposed in [9] and harmonics rejection in [10]. The harmonic canceling receiver architecture was introduced to reduce odd harmonic aliasing of the LO frequency by using an eight-phase LO clock and by scaling/summing different signal paths [11]. Numerous implementations [12–14] have integrated these two architectures, combining their features and functionalities, enabling a family of high linearity/low NF/harmonic rejection receivers.

All of the above-mentioned architectures are highly flexible in terms of frequency bands and bandwidth thanks to their adopted N-path filter/passive mixer and programmable capacitance loads, baseband filters, and digital filters. Their typical frequency coverage ranges from 80 MHz to 3.0 GHz, while the bandwidth can vary from a few MHz to 40 MHz. However, the linearity problem is traditionally treated as a trade-off between noise and linearity for in-band linearity, and as a trade-off between filtering and complexity for out-of-band linearity. Moreover, they all need high-performance Analog to Digital Converter (ADC)s in the back end to complete the RF-to-digital chain, which is a common path in any telecommunication device.

An alternative family of receivers is the direct RF-to-digital receiver Direct Delta-Sigma Receiver (DDSR). It is an attractive approach for overcoming the challenges faced by modern RF receivers, offering a compact solution where there are no more back-end ADCs. Figure 1 compares a conventional receiver versus a DDSR. Unlike the conventional receivers (on the top) where the typical RF stages, e.g., Low-Noise Amplifier (LNA), mixer, and baseband stages are cascaded, the DDSR architecture (on the bottom) is a direct RF-to-baseband digitizer/RF-ADC with global feedback from the baseband to RF stages. Note that a low-noise transconductance amplifier (LNTA) is used. Therefore, subtraction is performed in current, placing the LNTA within the Delta-Sigma loop. It is also worth mentioning that two mixers are shown in the figure, and as will be shown later, both operations can be conducted using the same mixer.

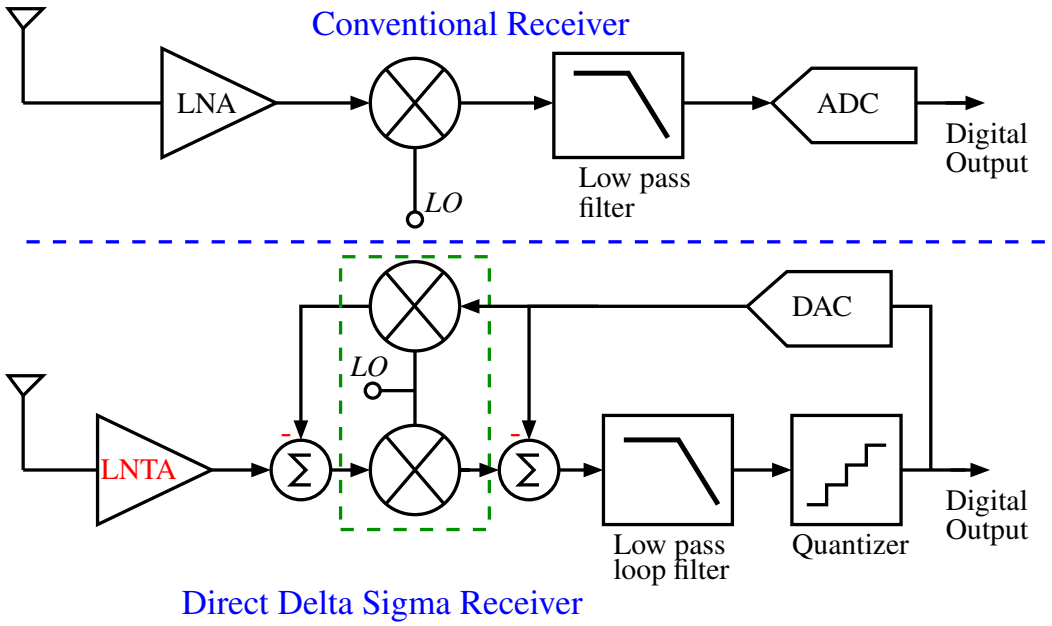


Figure 1. General architecture of a DDSR compared with a conventional receiver.

The presence of the RF blocks inside the ΔΣ loop filter relaxes their linearity requirements as the signal swing is reduced at their output. The integration of the RF blocks into the loop also increases the order of the Noise Transfer Function (NTF) and the Signal Transfer Function (STF), resulting, respectively, in a lower quantization noise floor and better filtering. Similarly to classical ΔΣ modulators, DDSR can be implemented using either Continuous Time (CT) or Discrete Time (DT) loop filters. In [15,16], the CT-DDSRs

show competitive NF and linearity. The design presented in [17] shows that the CT-DDSR can be adapted to multi-band, multi-standard receivers. In [18], the N-path filter was removed to achieve a design with lower power consumption and to prevent quantization noise folding. However, the receiver suffers from a low out-of-band rejection, resulting in a low out-of-band Third Input Intercept point (IIP3). The receiver proposed in [19] uses a second-order loop with Finite Impulse Response (FIR)-Digital-to-Analog Converter (DAC)s to implement the STF in digital. This approach significantly reduces power consumption at the expense of reduced resolution. In [20], a fifth-order architecture is described that offers competitive NF, flexible bandwidth, and central frequency, but its fully active CT implementation limits its linearity and results in high power consumption.

The DT-DDSRs mentioned in [21,22] achieve a wide frequency range and very high linearity. Additionally, as the sampling frequency and LO frequency are equal, clock generation and planning are simplified and the upmixing of quantization noise is avoided. However, having $f_s = f_{LO}$ also presents a drawback in this architecture. On the one hand, at a low LO frequency, the DDSR Oversampling Ratio (OSR) is low, which greatly increases the impact of quantization noise. On the other hand, at a very high LO frequency (>3–4 GHz), the constraints become very strong on the loop filter, particularly the quantizer and feedback DACs.

Based on the brief overview of the literature, DDSRs seem to offer an interesting architecture for flexible receivers but require solutions to deal with several challenges, such as frequency and filtering planning and quantization noise upmixing. This paper presents a novel architecture of DT-DDSR, which retains the well-known advantages and, at the same time, overcomes the limitation of having a sampling frequency equal to the LO frequency. In fact, the key feature of the proposed solution is to use a loop filter sampling frequency as a divided version of the LO clock. A fourth-order DT-DDSR has been designed using 65 nm CMOS technology. Measurement results show a high dynamic range of 80 dB with a peak Signal-to-Noise and Distortion Ratio (SNDR) of 46 dB.

The rest of the paper is organized as follows. The proposed receiver architecture is presented in Section 2. Section 3 presents the design methodology and architecture modeling. The system level design and circuit design are explored in Sections 4 and 5. Measurement results of the fabricated chip are shown in Section 6, and conclusions are drawn in Section 7.

2. Receiver Architecture

Figure 2 shows the proposed receiver architecture. A fourth-order loop filter based on a low-pass cascaded integrator with distributed feedback is used as a good balance among stability, aggressive noise shaping, and complexity. As mentioned earlier, the key feature of the proposed architecture is the use of the loop filter sampling frequency as a divided version of the LO clock. This feature ensures that the loop filter operates at almost the same low sampling frequency, f_s, over a wide LO frequency, f_{LO}, range, leading to the following five advantages:

- In-band noise shaping is centered at any LO harmonics, avoiding the quantization noise folding issue discussed in [15,16].
- Since the quantizers do not operate at the LO frequency, as seen in [21,22], their constraints of metastability and hysteresis are significantly relaxed, especially in high-frequency bands (e.g., 3 to 6 GHz).
- Only one coefficient set is required for the wide LO frequency range, which is much less complex compared with the implemented DDSRs.
- The loop filter's clock buffers and the third and fourth active stages work at lower speeds, significantly reducing power consumption.
- Compared to the DT-DDSRs in [21,22], the adopted low f_s enables a narrower STF bandwidth, providing better out-of-band rejection at the Low-Noise Transconductance Amplifier (LNTA)'s output and lower duplexer selectivity requirements.

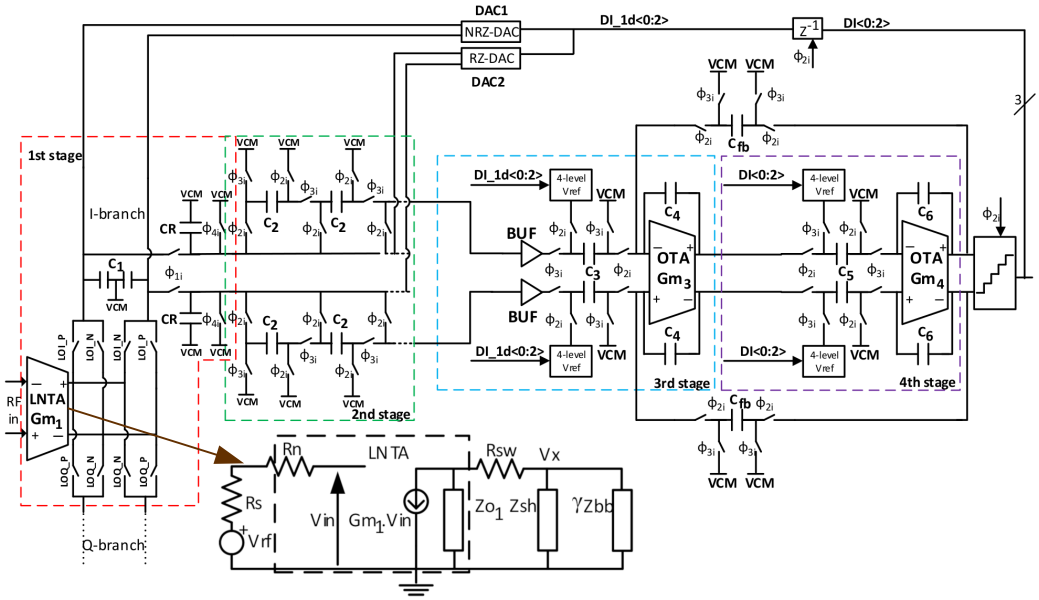


Figure 2. Proposed fourth-order DT-DDSR with the sampling clock of the loop filter running at the LO division. Only the I-branch is shown for clarity.

As shown in Figure 2, the first stage is realized by the LNTA and the 25% duty cycle current-driven passive mixer, adopting high-Q bandpass filtering and high out-of-band linearity [23]. In this stage, the capacitors C_1 and CR are used in the same manner as in [21] to form a lossy integrator. In order to improve the RX Gain as well as RX NF while maintaining a small number of active blocks, passive gain-boosting is employed in the 2nd stage [24]. In phase ϕ_2, N capacitors C_2 are parallel, integrating charge from CR. In the next phase, ϕ_3, N capacitors C_2 are connected in series, and the integration voltage is measured between the first and last capacitors. This configuration results in a DC voltage gain of N times in the second stage. In addition to improving the RX gain, this passive gain-boosting technique also relaxes the integrating gain of the third active stage, helping to further reduce power consumption. Two voltage buffers are used to copy the integration voltage from the second stage to C_3. The 1st feedback current is integrated onto capacitor C_1, and the integrated voltage is up-converted to LNTA's output through the passive-mixer, forming an RF feedback. This RF feedback reduces the LNTA's output swing, relaxing LNTA's linearity requirement. The RF feedback is achieved using a current-steering, not-return-to-zero DAC in order to ensure good immunity to jitter noise. Meanwhile, the second feedback loop, whose jitter error is shaped by the loop, is implemented as a return-to-zero DAC to simplify its clocking constraints [25]. A two-bit quantization is employed as a good compromise between resolution, stability, and complexity. The quantizer output is a three-bit thermometer code that corresponds to the two-bit quantization. These different choices will be discussed in detail in the next section.

3. Design Methodology and System Modeling

3.1. Design Methodology

Before diving into the system-level design of the architecture, it is worth mentioning that the DDSR design is specific due to its feedback nature. In conventional RF design approaches, parameters of each block, such as IIP3, NF, and a full-scale voltage, can be conveniently calculated by cascading equations [26]. This design approach is very common. However, it is not applicable to a closed-loop system like the DDSR. Similarly, conventional design approaches for ΔΣ modulators [27,28] are not applicable for the DDSR either, due to the effect of frequency translation and harmonic folding in the N-path filter and/or the mixer. In order to solve this problem, we developed a top-down modeling and analysis for DDSRs. This approach integrates high-level system simulations,

analytical modeling of imperfections, noise, non-idealities, electrical PSS-PAC simulations, and transient simulations, enabling a fast and accurate design of DDSR. In the two next sub-sections, the noise and transfer function modeling for the proposed architecture will be, respectively, presented. The modeling methodology is detailed in [29].

3.2. Noise Modeling

The analysis approach of the passive mixer proposed in [30] is extended to the receiver's front end [31]. The bottom of Figure 2 shows the single-ended representation of the first integrator. The LNTA is represented by Gm_1, Rn, and Zo_1, which are the transconductance, intrinsic noise equivalent resistance, and output impedance, respectively. Impedances connected to the virtual Vx node are switch ON-resistance Rsw, odd-harmonic folding impedance Zsh, and effective BB load γZbb, where $\gamma = 4/\pi^2$ and $Zbb = R_{DAC1}||(1/sC_1)$. Due to the folding effect, noises coming from Rs, Rn, Zo_1, and Rsw are scaled by $\pi^2/8$. Odd-harmonics current noise folding from Zo_1 and Rsw is represented by $Zsh = (Rsw + Zo_1)/(\pi^2/8 - 1)$ [30]. Moreover, thermal noise In^2_{DAC1} of the first DAC is also scaled by $1/\gamma$. Therefore, the current noise power spectral density (PSD) at the Vx node is equal to the following:

$$In_1^2 = \frac{\pi^2}{8}\cdot\frac{4KT}{(Rsw + Re(Zo_1))} + \frac{4KT}{\gamma\cdot Re(Zbb)} + \frac{In^2_{DAC1}}{\gamma} + In^2_{jitter}\ [\mathrm{A^2/Hz}], \quad (1)$$

with the NRZ DAC jitter noise current

$$In^2_{jitter} = \Delta_y\cdot\frac{2Iu^2_{DAC1}\cdot\sigma^2}{Tlo}\cdot\ [\mathrm{A^2/Hz}], \quad (2)$$

where Iu_{DAC1} and σ are the first DAC cell current and the clock jitter RMS, respectively. Δ_y is the DAC relative number of transitions, which depends mainly on the number of bits. Tlo is the LO period. This current noise PSD is drawn on an impedance of $(Rsw + Zo_1)||Zsh||\gamma\cdot Zbb$, so a voltage noise PSD of $In_1^2\cdot((Rsw + Zo_1)||Zsh||\gamma\cdot Zbb)^2$ appears on the Vx node. The noises are doubled in differential mode. The RF stage input-referred noise is then given by the following:

$$Vn_1^2 = (\frac{\pi^2}{8} - 1)\cdot KTRs + \frac{\pi^2}{8}\cdot 8KTRn + \frac{2\cdot In_1^2\cdot((Rsw + Zo_1)||Zsh||\gamma\cdot Zbb)^2}{Av^2}\ [\mathrm{V^2/Hz}], \quad (3)$$

where the LNTA's voltage gain Av is denoted as follows:

$$Av = \frac{Gm_1\cdot Zo_1\cdot(Zsh||\gamma\cdot Zbb)}{Rsw + Zo_1 + (Zsh||\gamma\cdot Zbb)} = Gm_1\cdot Z_{eff}. \quad (4)$$

The KT/C noises, Vn_2 and Vn_3 of the third and fourth integrators, as well as the quantization noise, Vn_Q, are conventionally modeled as presented in [27].

3.3. Transfer Function Modeling

Similarly, as the last two stages of the designed DDSR loop are classical DT switched-capacitor integrators that have been widely covered in the literature, the transfer function modeling will only be detailed for the first two stages: (i) the LNTA/mixer integrator and (ii) the passive integrator, $C_2 - C_R$.

For the first integrator, in every half period of the LO clock, Tlo, the LNTA sees the capacitors, C_1, in parallel with an effective resistor, $Rx = \pi^2/8\cdot Re((Rsw + Zo_1)||Zsh||\gamma\cdot Zbb)$. Additionally, in each Tlo period, there is a charge loss through the capacitors, CR, with a

lossy factor, $\alpha = C_1/(C_1 + CR)$ [32], and the conversion gain RF-BB is the voltage gain in Equation (4) multiplied with $\pi/2\sqrt{2}$. Hence, the time-domain equation of the voltage on C_1 is written as follows:

$$V_{C_1}(n) = \frac{\pi}{2\sqrt{2}} \cdot Gm_1 \cdot Z_{eff} \cdot V_{in}(n) \cdot [1 - e^{\frac{-Tlo}{2 \cdot Rx \cdot C_1}}] + V_{C_1}(n-1) \cdot \alpha \cdot e^{\frac{-Tlo}{2 \cdot Rx \cdot C_1}}. \quad (5)$$

It leads to the Z-domain transfer function of the first integrator, as follows:

$$I_1(Z) = \frac{\pi}{2\sqrt{2}} \cdot \frac{Gm_1 \cdot Z_{eff} \cdot (1 - e^{\frac{-Tlo}{2 \cdot Rx \cdot C_1}})}{1 - \alpha \cdot e^{\frac{-Tlo}{2 \cdot Rx \cdot C_1}} \cdot Z^{-1}}. \quad (6)$$

The same approach is used to find the transfer functions of the first feedback, the second integrator, and the second feedback, respectively, as follows:

$$F_1(Z) = \frac{Gm_{DAC1} \cdot Rdac_{eff} \cdot (1 - e^{\frac{-Tlo}{Rdac_{eff} \cdot C_1}})}{1 - \alpha \cdot e^{\frac{-Tlo}{Rdac_{eff} \cdot C_1}} \cdot Z^{-1}}, \quad (7)$$

$$I_2(Z) = \frac{(1 - \beta) \cdot e^{\frac{-Tlo}{4 \cdot R_{DAC2} \cdot C_2}}}{1 - \beta \cdot e^{\frac{-Tlo}{4 \cdot R_{DAC2} \cdot C_2}} Z^{-1}}, \quad (8)$$

$$F_2(Z) = \frac{Gm_{DAC2} \cdot R_{DAC2} \cdot (1 - e^{\frac{-Tlo}{4 \cdot R_{DAC2} \cdot (C_2 + CR)}})}{1 - \beta \cdot e^{\frac{-Tlo}{4 \cdot R_{DAC2} \cdot (C_2 + CR)}} \cdot Z^{-1}}, \quad (9)$$

where Gm_{DACi} and R_{DACi} denote the transconductance of the $DACi$ ($i = 1, 2$) and its output resistance, respectively. $Rdac_{eff} = R_{DAC1}||2(Rsw + Re(Zo_1))$ is the effective resistance seen by the first DAC, and $\beta = C_2/(C_2 + CR)$ is the transfer factor between the first and second integrators.

4. System Level Design

In this section, the procedure to build and size the receiver is detailed. The analysis is based on the methodology and models presented in the previous section. As mentioned above, the main feature of the architecture involves using a sampling frequency of the loop that is a divider of the LO frequency; this has several advantages, such as robustness against noise upmixing and an almost constant OSR with respect to the LO frequency. As the designed system is both a Delta-Sigma modulator and a receiver, the calculation of their parameters will be presented separately for the sake of simplicity, but it is obvious that they were designed jointly as there is a high degree of dependency between the choices.

The targeted performance for the DDSR includes a central frequency range from 0.4 to 6 GHz, a dynamic range of 74 dB (12 bits), which is divided into 10 bits of resolution and 2 bits of gain control, an NF of 13 dB, and an IIP3 of 3 dBm.

4.1. Delta-Sigma Loop

As with any Delta-Sigma loop, in the proposed system, the parameters that need to be set are the OSR, the number of bits, the loop order/architecture, the NTF shape/gain, and the STF filtering/gain. There are several constraints due to the RF nature loop of this architecture. Firstly, using feed-in and feed-forward coefficients as in a regular $\Delta\Sigma$ modulator is expensive as it requires having a frequency translation. For this reason, feedback architecture was preferred. Secondly, as the second integrator is implemented with passive components, in order to avoid a power-hungry transimpedance amplifier, having an NTF optimization (adding a notch) for the first stages is excluded. Thirdly, as the

designed system needs to process signals with very low amplitudes (tenths of μV), the STF does not have a unity gain and it should also have low pass filtering behavior to improve the out-of-band rejection.

Table 1 shows the selected loop parameters which, were chosen as a compromise between the aforementioned specifications and constraints, and the implementation requirements that will be discussed later. A loop order of 4 with an H-inf of 2 is chosen as a good compromise among the SQNR performance, stability, and oversampling requirements. A notch is added to the third and fourth integrators to further improve the resolution. The number of bits is chosen to be equal to 2 as a compromise among stability, resolution, and jitter performance, on the one hand, and DAC mismatch and complexity, on the other hand.

Table 1. Modulator specifications. ($OSR = fs/(2Bw)$).

BW (MHz)	f_s (MHz)	OSR	Order	Nbits	SQNR (dB)
10	375–425	17.5–21.25	4	2	71

Figure 3 simulates its impact on the loop performance. The modeling of the system-level simulator uses the description of Section 3. The simulation uses the same parameters as in Table 1. As can be seen in the figure, a higher leakage factor improves the NTF performance but at the cost of a higher attenuation of the signal in the loop [33]. Here, the loop coefficients were adjusted, depending on the value of α to optimize the resolution in each configuration. Reducing α from 0.99 to 0.95 reduces the SQNR by 1.6 dB, and reducing it to 0.9 degrades the SQNR by 6 additional dB. A leakage factor of 0.95 stages is selected as a compromise, translating into a ratio of $\frac{C_1}{C_R}$ of 20 [32]. This trade-off will be discussed further in the next section.

Based on the chosen value, α, the values of the full-scale quantizer and loop gain can be chosen jointly. A full scale of $\pm$80 mV is chosen to keep reasonable constraints on the quantizer in terms of the offset, hysteresis, and noise. This requires an overall gain for the loop of 24 dB, which is implemented by adjusting the ratio between the LNTA and DAC1 currents. The attenuation by β due to the leaky integrator is compensated by the passive gain boosting block.

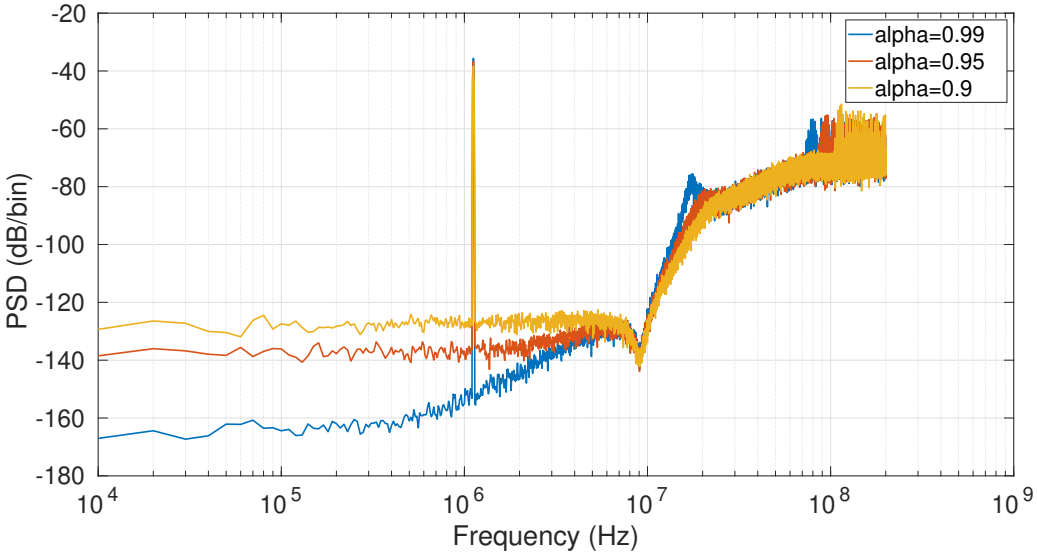


Figure 3. DDSR PSD for three values of α.

For the DAC mismatch, using dynamic element matching techniques can emphasize the impact of inter-symbol interference [34], which can highly increase the non-linearities of the architecture. Figure 4 shows the Dynamic Range (DR) of the receiver with and without DAC mismatch, which is only modeled for the first DAC, the most critical one. The mismatches of positive cells (PMOS transistors in the DAC) and negative cells (NMOS transistors in the DAC) are uncorrelated and the standard variation for both is 0.5%. As can be seen in the figure, the peak SQNR in the ideal case is 71 dB. The DAC mismatch degrades it by 6 dB and as it only affects high input powers, the DR is not impacted. Therefore the DAC mismatch problem was handled in design by adjusting the mismatch of cell currents lower than 0.5%.

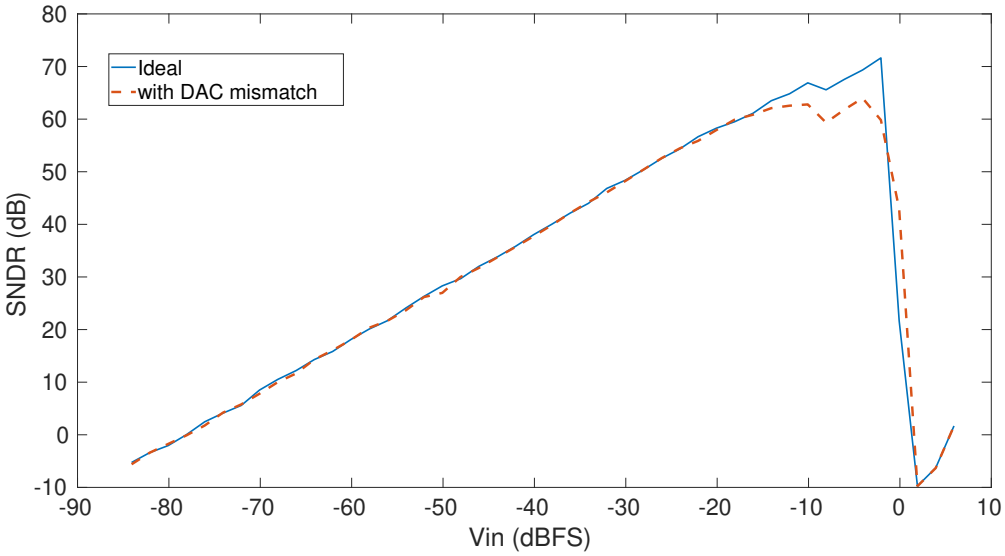


Figure 4. Dynamic range of the DDSR with and without DAC mismatch.

For the DAC currents, the first DAC needs to be scaled by $1/(1-\beta)$ to compensate for the attenuation $(1-\beta)$ of the second integrator. As $Rdac_{eff} \cdot C_1 \gg T_s$ and $4R_{DAC2} \cdot (C_2 + CR) \gg T_s$, their reference currents are given by the following:

$$I_{DAC1} \simeq \frac{Q_{Vref} \cdot b_1 \cdot C_1}{(1-\beta) \cdot T_s}, \quad I_{DAC2} \simeq \frac{Q_{Vref} \cdot b_2 \cdot C_2}{0.25 \cdot T_s}, \tag{10}$$

where Q_{Vref}, b_1, and b_2 are the quantizer's reference voltage, and the first and second feedback coefficients, respectively. Thanks to a small variation of f_s, i.e., 0.375 GHz to 0.425 GHz, over the LO frequency range, one set of DACs can be used without any instability or performance degradation problem. The nominal values of I_{DAC1} and I_{DAC2} are chosen for F_s = 0.4 GHz as this sampling frequency is the most repeated over the LO frequency range. As a result, I_{DAC1} and I_{DAC2} are, respectively, 12.0 µA and 8.0 µA.

4.2. Receiver Specifications

In this subsection, the architecture is analyzed and sized from a receiver point of view. To cover the 0.4–6.0 GHz frequency range with eight common LO frequencies, 0.4 GHz, 0.8 GHz, 1.2 GHz, 2 GHz, 2.4 GHz, 3.6 GHz, 4.0 GHz, and 6.0 GHz, one can notice that with this configuration, the proposed DDSR is not able to continuously cover the LO range from 0.4 to 6 GHz. Nevertheless, this limitation could be overcome by implementing all the division rates from 1 to 15 and by extending the sampling frequency window. We chose this configuration as a compromise between the design interests and circuit complexity, especially concerning the clock generation block, which will be discussed later.

The LNTA is key for both RX NF and RX IIP3. A larger transconductance leads to a better RX NF at the expense of higher power consumption. Moreover, the LNTA's IIP3 dominates the OOB linearity due to the high OOB rejection of the mixer [35]. As the interface to the antenna, the LNTA also provides the means for impedance matching. Hence, an LNTA architecture capable of wideband matching across a decade of frequencies is preferred. The receiver's parameters were optimized using an analytical model, with the selected parameters for the LNTA being $Gm_1 = 40$ mS, $Zo_1 = (250\ \Omega||30$ fF), IIP3 = 0 dBm, NF = 2.5 dB.

The capacitor, C_1, impacts the OOB rejection of the mixer and the RX NF. Using a larger capacitor results in better OOB rejection, but raises the RX NF. A value of 4 pF for both C_1 and C_2 is a compromise. The sizing of CR is solely conducted with C_1. As mentioned earlier, a larger C_1/CR ratio results in better noise shaping but decreases the RX gain, leading to higher constraints on the quantizer. A ratio of 1:20 provides us with a good trade-off. Consequently, the CR value is 0.2 pF.

The active blocks in the loop filter, i.e., the OTAs Gm_3 and the buffers, have a significant impact on the RX NF and the RX gain due to the attenuation in the second integrator. The analysis with the analytical model shows that a voltage gain of 36 dB with a gain–bandwidth product (GBW) of 1.6 GHz (500 fF load) is required for the Gm_3, while an open loop gain of 28 dB with a GBW of 1.6 GHz (500 fF load) is required for the buffers. Interestingly, thanks to the attenuation in the second integrator, the nonlinearity contributions of the OTAs and the buffers are negligible. This fact is confirmed by the Spectre PSS-PAC analysis, showing that the IIP3 of -30 dBm is good enough to guarantee the targeted SNDR.

5. Circuit Implementation

5.1. Low-Noise Transconductance Amplifier

A single LNTA covering of 0.4–6.0 GHz is designed to minimize the complexity of the RF front-end circuit, with two attractive benefits: wideband matching and low power consumption. A common-gate LNTA with low-Q inductive load is chosen [36]. In order to further improve the transconductance gain of the LNTA with the same bias current, a common-source stage with cross-coupling capacitance is stacked on the common-gate stage as shown in Figure 5. In this LNTA, a power supply of 1.5 V is used to ensure the voltage swing at the LNTA's output. The DC voltage at the LNTA's output is optimized at 0.8 V to obtain the best compromise between IIP3 and NF, so it requires an RC coupling at the LNTA's output to bring the common mode voltage down to 0.6 V. A four 3 dB-step gain control is implemented with resistive loads, R_5–R_{11}. The NMOS switches, M_6–M_9, are controlled by a thermometer code from '0000' to '1111', corresponding to the highest and lowest voltage gains of 24 dB and 12 dB, as can be seen in Figure 6. The LNTA performance is summarized in Table 2.

Table 2. Summary performance.

Gain	13.3–24.3 dB
NF	4.3 dB
IIP3 (dBm)	0 dBm
IIP2 (dBm)	42 dBm
S11	<-20 dB
Output current	2.9 mA
Power cons.	9.5 mW
Supply	1.5/1.2 V

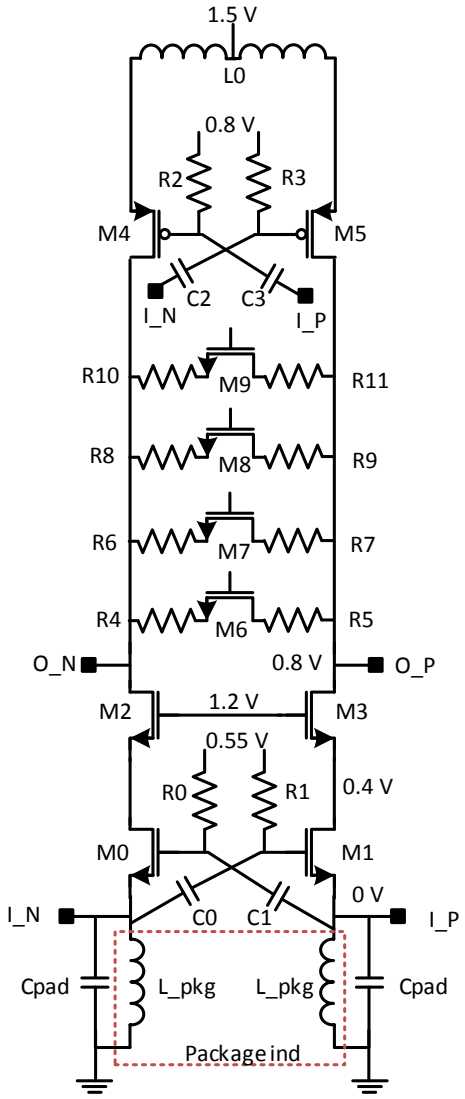


Figure 5. Schematic of the LNTA. Bias and common mode feedback circuits are not shown.

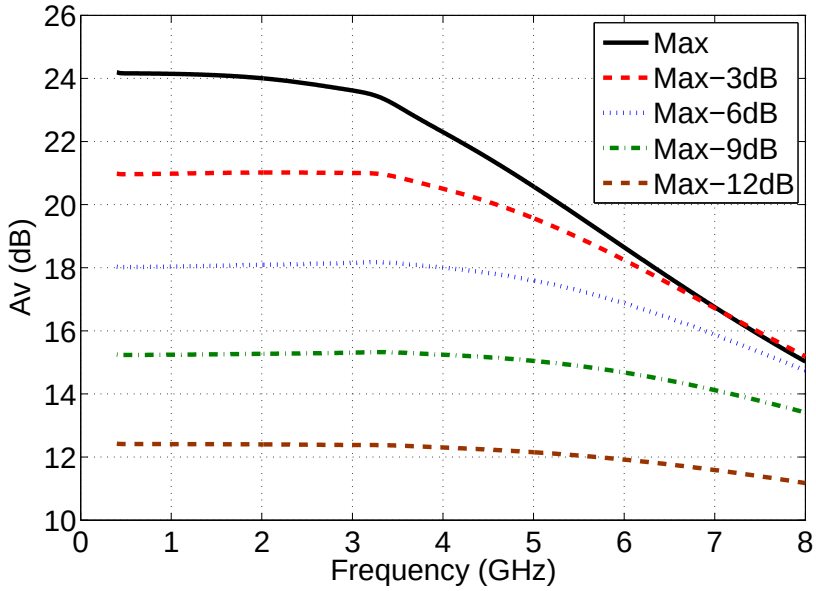


Figure 6. LNTA transfer function for gain configurations.

5.2. Clock Generation Circuit

Figure 7 shows the clock generation of the DDSR. There are two types of clock signals: LO clocks and loop filter clocks. The LO clock drives the mixer switches at a frequency of 0.4–6.0 GHz. The loop filter clock drives the loop filter switches, the quantizers, and the DACs at a low speed, from 0.375 to 0.425 GHz. The loop filter clock is derived by dividing the LO clock, aiming to synchronize the feedback signal with the feed-in signal and relax the design constraints of the loop filter. An external clock source running at twice the LO (0.8 GHz–12.0 GHz) is used to generate the clocks. A signal CLK_SEL$< 0 : 2 >$ is used to select the division ratio of the LO/f_s between [1, 2, 3, 5, 6, 9, 10, 15] to cover the LO frequencies listed earlier.

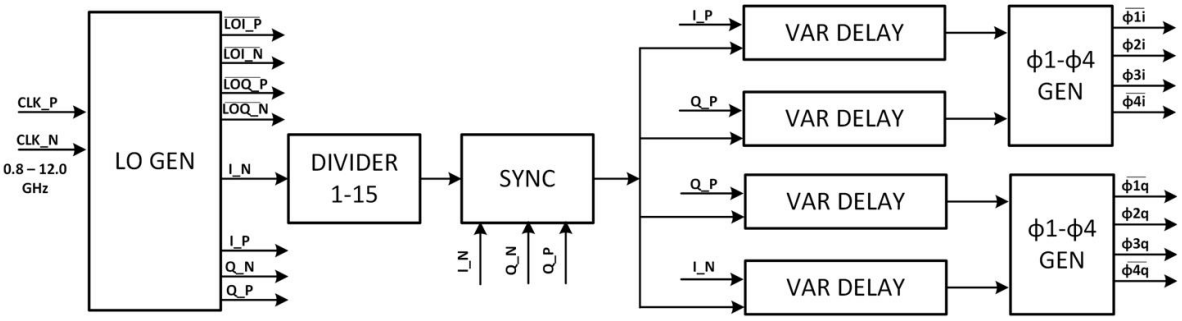


Figure 7. Clock generator.

Regarding the LO clock, as shown in Figure 8, it is a non-overlapping four-phase one: LOI_P, LOI_N, LOQ_P, and LOQ_N. Each has a 25% duty cycle of T_{LO}. The rising and falling times of the LO clock are very tight at 10 ps due to the short integrating period, especially at 6.0 GHz LO. The loop filter clock is also a non-overlapping four-phase one: ϕ_{1i}–ϕ_{4i} and ϕ_{1q}–ϕ_{4q} for the I branch and Q branch, respectively. The Q-branch clocks ϕ_{1q}–ϕ_{4q} are delayed by one-quarter of the LO period with respect to the I-branch clocks. The two phases, ϕ_{2i} (ϕ_{2q}) and ϕ_{3i} (ϕ_{2q}), are relaxed with a 50% duty cycle of T_s. The rising time and falling time are also relaxed at 100 ps. The two phases, ϕ_{1i} (ϕ_{1q}) marked in red and ϕ_{4i} (ϕ_{4q}) marked in purple, are more challenging as their high times are equal to the high times of the LO clock. Moreover, their rising and falling times are also equal to 10 ps, ensuring the synchronization of the 1st integrator with both the LO clock and the loop filter clock.

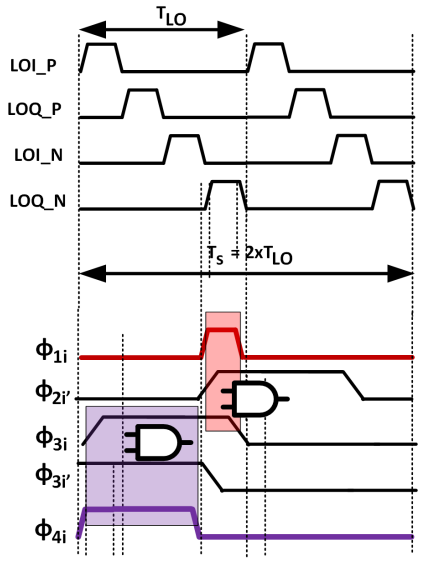


Figure 8. Clock chronogram.

The clock generation block is implemented using high-speed transistors and a 1 V supply. The delays are built using standard cells, t-switches, and multiplexers. An auto-tuning loop is employed to overcome the process variation impact on the delays and to synchronize the divided clocks. The block consumes 8.1 mW for an LO frequency of 400 MHz and 21.7 mW at 6 GHz.

5.3. The Switches and Baseband Blocks

Occupying key positions in the RF-to-BB integrator, which handles high swing signals across a wide LO frequency range, the LO switches (LOI_P, LOI_N, LOQ_P, LOQ_N in Figure 2) are implemented as NMOS ones with a gate AC coupling technique. Furthermore, to achieve high linearity, the bulk and the source of each switch are connected [9]. The DC biasing voltage for the gates of these switches is tunable off-chip from 0.55 V to 0.85 V to optimize the operating point. The size, 15 µm/0.06 µm, of the switches is carefully simulated in order to minimize the parasitics while maintaining the required ON-resistance, *Rsw*. The remaining switches of the loop filter are implemented as classical CMOS switches.

Each unity voltage buffer is formed by a five-transistor OTA due to its sufficient voltage gain and low complexity. The size of the input pair is chosen, as shown in Figure 9, to ensure the required input-referred offset and the input-referred noise. Benefiting from the high speed and moderate voltage gain, the telescopic architecture is chosen to implement the OTAs. Furthermore, continuous common mode feedback (CMFB) is used due to its clock-free circuit and high-speed response to VCM turbulence (Figure 9).

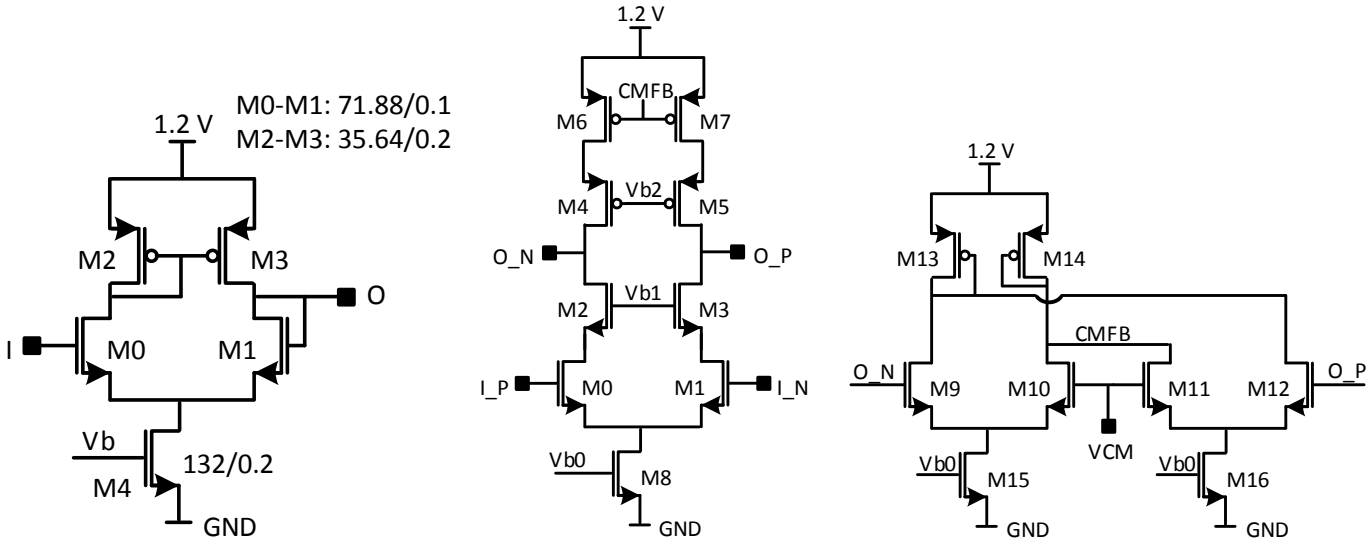


Figure 9. Schematic of the left side: A voltage buffer. Right side: Third and fourth stages of the OTA.

Each active integrator is implemented as a conventional half-delay switched-capacitor cell. Its schematic, shown in Figure 10, is based on the implementation proposed in [27]. The small feedback coefficient around the last two integrators poses a tiny feedback capacitor of 3.5 fF. This tiny capacitor, in fact, is implemented by the T-capacitive network with K = 14 [27]. Moreover, the last two feedback coefficients of the loop filter are implemented by switched-capacitor DACs, requiring the unit capacitors, C_{DAC}, of 50 fF and 100 fF, respectively. The DAC implementation is classical as can be seen in the figure with signals $DI_P < i >$ and $DI_N < i >$, corresponding, respectively, to the positive and negative thermometric quantizer outputs for channel I. The same goes for channel Q. The reference voltages $Vref_P$ = 680 mV, $Vref_N$ = 520 mV are generated off-chip for simplicity and flexibility.

The flash quantizer consists of three comparators with a thermometric code output. The comparator has a classical architecture with a pre-amplifier and a dynamic latch. The comparator transistors are sized small (about 0.14 µm^2). The mismatch-induced offset

is compensated at the same time for each comparator during start-up. The offset after calibration is lower than 5 mV. The implementation is detailed in [37].

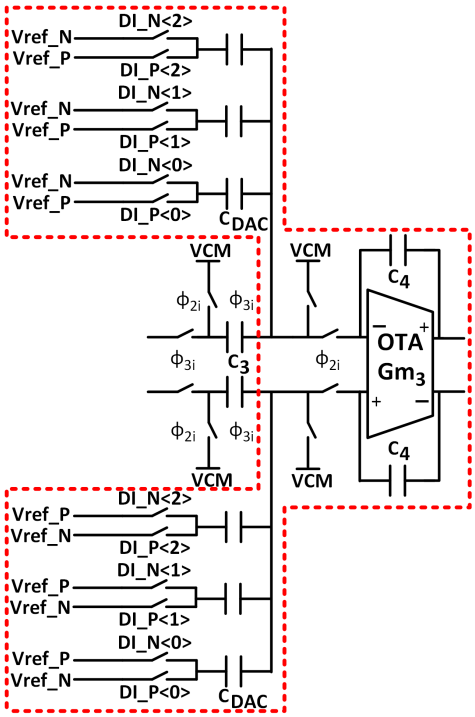


Figure 10. Schematic of an active integrator and its feedback DAC.

5.4. Performance Summary

Table 3 summarizes the performance of the designed DDSR. The electrical simulation results show an NF of 13 dB, an IIP3 of 3 dBm, and a DR of 80 dB for an RF bandwidth of 20 MHz (10 MHz in the baseband). Figure 11 shows the power consumption breakdown for LO values of 0.4 GHz and 6.0 GHz. The power consumption varies from 40.6 mW @0.4 GHz to 68.2 mW @6 GHz. At low frequencies, the power consumption is dominated by analog static currents, with the largest contributions from BB OTAs and the LNTA. When the LO frequency is increased, the dynamic power consumption increases. At 6 GHz, the two largest contributors become LO generations and switch buffers. The results will be further discussed and compared to the state of the art in the next section.

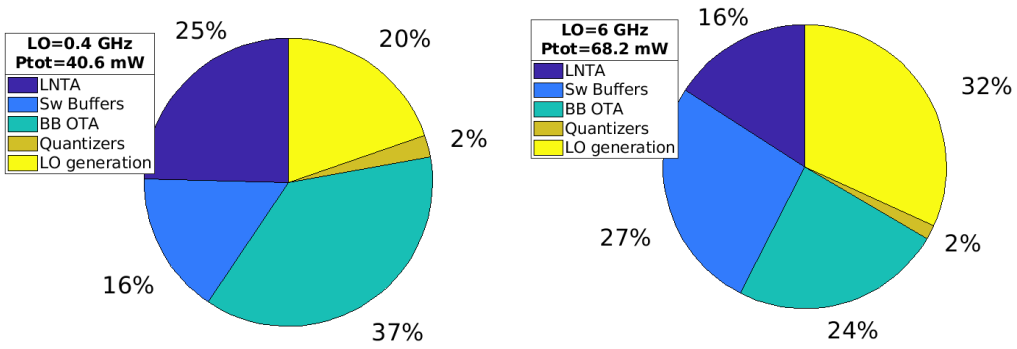


Figure 11. Pie chart of the power consumption.

Table 3. Comparison with state-of-the-art DDSRs.

	Wu-14 [22]	Englund15 [16]	Liu-16 [18]	Subramanian-18 [19]	Sayed-20 [38]	This Work Measure-ment	This Work Simulation
Arch.	2nd order DT loop	4th order CT loop	5th order CT loop	4th order CT loop	2nd order BP LC loop	4th order DT loop	4th order DT loop
Process (nm)	65	40	65	65	65	65	65
LO (GHz)	0.4–4	0.7–2.7	0.6–3.0	0.5–2.75	1.5–3.0	0.4–1.2	0.4–6
f_s (MHz)	Equal to LO	1250	592	200	6000–12,000	375–425	375–425
BW (MHz)	10	15	10	10	47–93	10	10
IN-IIP3 (dBm)	10	−20	−23	−21	5	2.2	3
NF (dB)	16–28.8	5.9–8.8	2.4–3.5	6.1–10.8	36	22	13
Peak SNDR (dB)	52–65	40-43	45–52	36	37	46	52
DR (dB)	70	63	57	52	45	80	80
Power Cons. (mW)	17–70.5	90	20	9.3–16.2	13–20	43.7–48.2	40.6–68.2
Active Area (mm^2)	0.65	1	0.7	0.15	0.3	0.9	0.9

6. Measurement Results

6.1. General

The circuit was fabricated in a 65 nm CMOS process from STMicroelectronics. It occupied, as can be seen in Figure 12, 2.4 mm^2. The chip was encapsulated in an 80-pin quad flat no-lead (QFN) package. It was mounted on a four-layer PCB. The differential input signal and clock signal were generated using baluns. CML buffers were integrated on-chip to drive the digital outputs on a logic analyzer. The I and Q channel DAC currents, the LNTA gain, and the clock division factor could be adjusted off-chip using a 30-bit serial-to-parallel interface.

The measurement procedure is as follows. First, the quantizer offset is calibrated once at the power-up. Then the configuration of the receiver (CLK divider ratio, DAC currents, and gain value) is fixed using the SPI. The I/Q outputs, acquired with the logic analyzer with a synchronous clock generated on the chip, are post-processed using Matlab. The FFT spectrums are calculated for a 2^{18}-point spectrum, which results in a frequency resolution of 1.525 kHz.

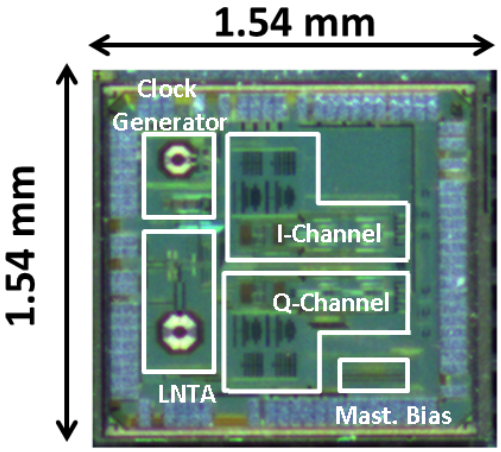


Figure 12. Die photo of the fabricated chip.

Unfortunately, the circuit shows two major measurement problems that limit its performance. The first problem concerns the clocking divider. It does not synchronize for frequencies higher than 1.2 GHz. The second problem involves the input signal power transfer. The peak SNDR is achieved for a value that is 6 dB higher than expected, −30 dBm vs. −36 dBm, which results in degradation by the same amount of the NF. The most probable reason for these limitations is the imprecise modeling of the package. The model provided by the manufacturer is not accurate enough, necessitating the formulation of hypotheses for both the IC design and the PCB design. Several configurations of the PCB (routing, balun models, matching network) have been attempted, but none allowed us to completely overcome the aforementioned problems. In the next subsection, we will show the measurement results for the best PCB configuration.

6.2. Measurements

Figure 13 shows the DDSR Power Spectral Density (PSD) for an input frequency of 801 MHz, a LO frequency of 800 MHz, and a division factor of 2, which results in a sampling frequency of 400 MHz. As can be seen, the behavior is as expected with a flat noise floor in the useful band and noise shaped by the Delta-Sigma loop for higher frequencies. Figure 14 shows the I/Q time domain signals and the reconstructed spectrum after filtering and decimation. As can be noted, the I/Q mismatch image is around −40 dBc without any correction.

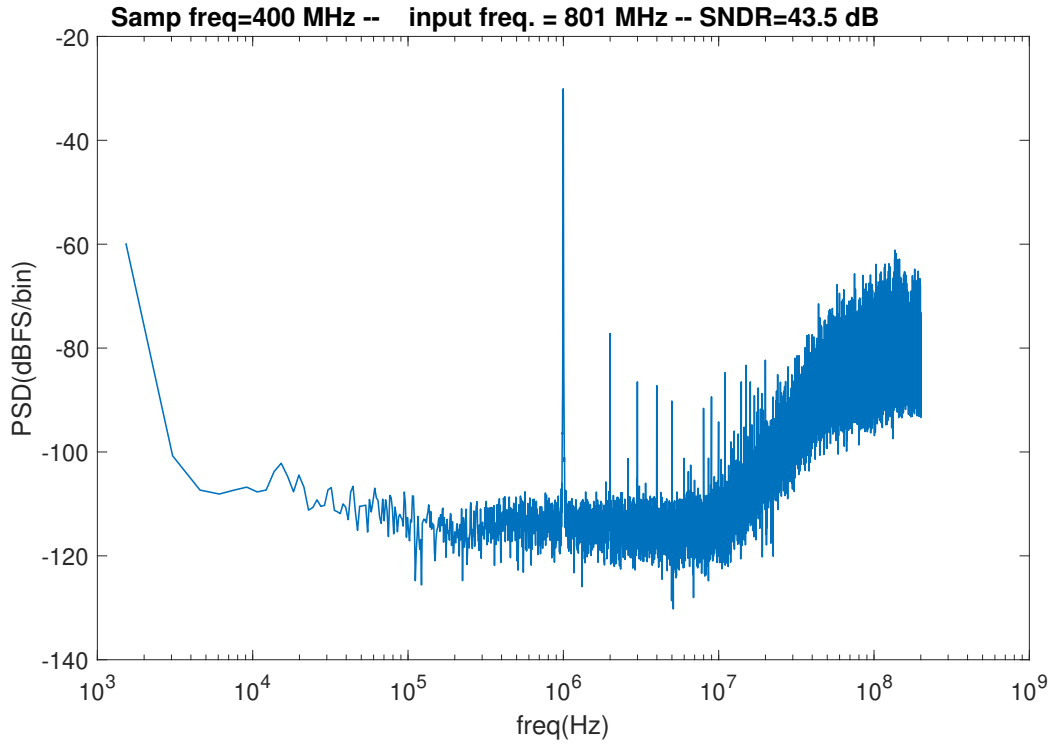


Figure 13. Measured DDSR PSD.

Figure 15 shows a two-tone test of the DDSR at values of 403 MHz and 404 MHz with an input power of −21 dBm. The IM2 image at values of 1 MHz and 7 MHz is at −44.3 dBc, which results in an IIP2 of 23.3 dBm. The IM3 image at 2 MHz (5 MHz) is at −46.4 dBc, resulting in an IIP3 of 2.2 dBm.

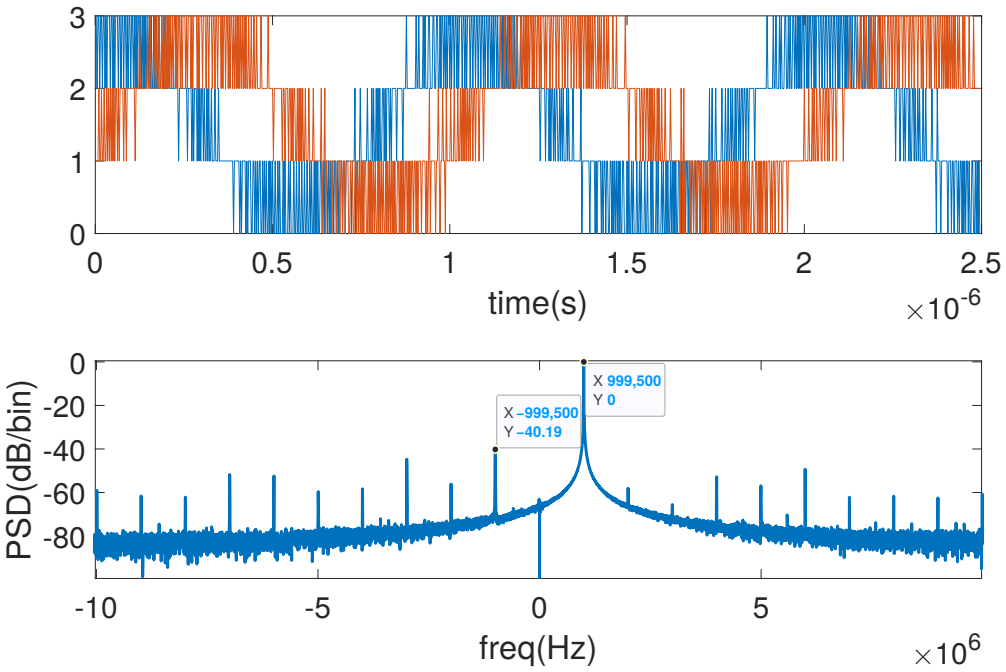


Figure 14. I/Q DDSR output (top) time domain (bottom) PSD. The spectrum was normalized for ease of comparison.

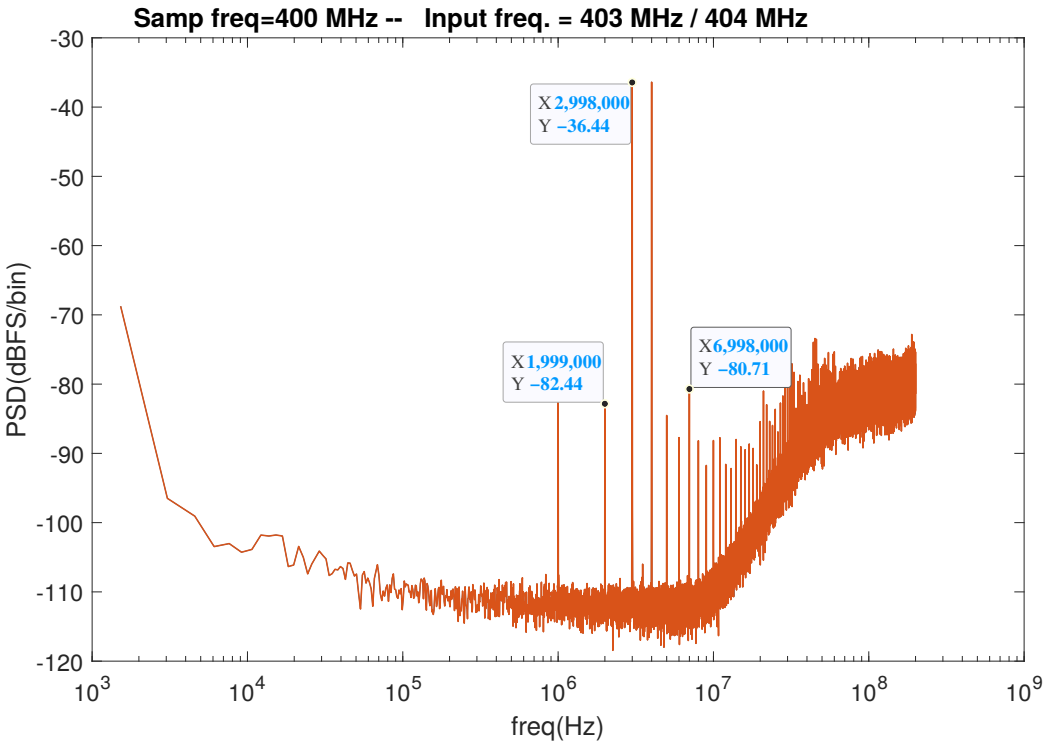


Figure 15. Measured DDSR PSD for a two-tone input.

Figure 16 shows the dynamic range measurements of the DDSR in the highest and lowest gain configurations. The measured peak, SNDR, is 46 dB, and the overall DR (SNDR > 0 dB) is 80 dB, among which, 12 dB is achieved thanks to the gain reconfiguration. The sensitivity value is −79 dBm, which results in an NF of 22 dB.

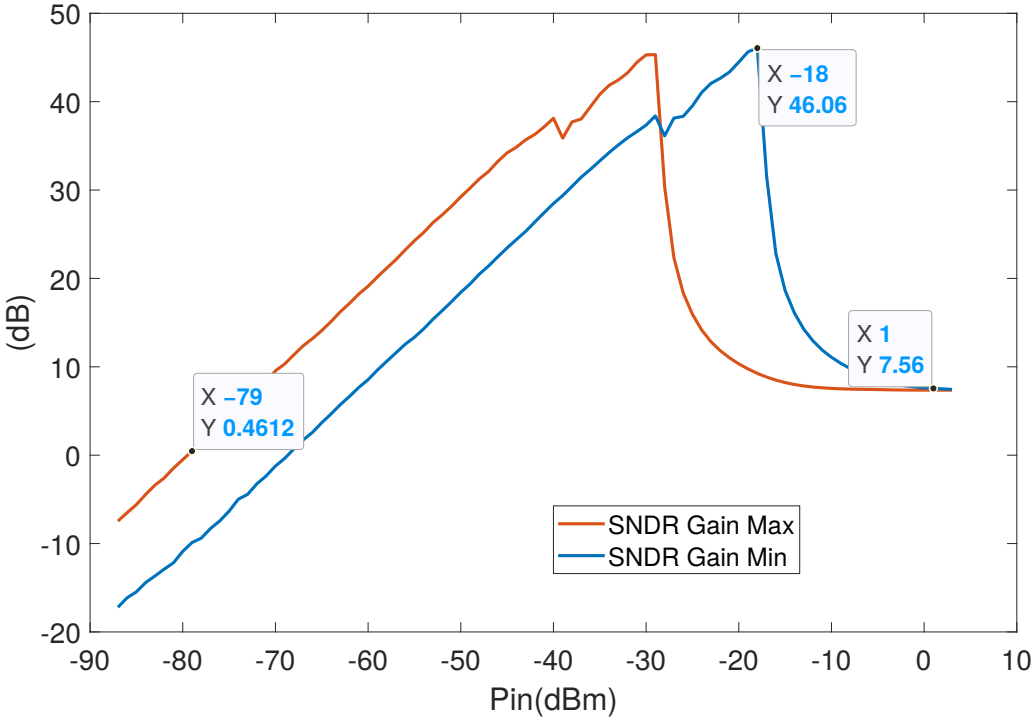


Figure 16. Measured DDSR DR.

6.3. Comparison to the State of the Art

In order to provide a complete comparison of the proposed receiver and its potential with respect to other works in the SOA, both its simulation and measurement metrics will be discussed. First, regarding the LO frequency, the main feature of the proposed receiver, i.e., using a divided version of the LO frequency as a sampling frequency, enables a wider LO coverage in simulations going from 0.4 to 6 GHz. DT architectures where $f_s = LO$ have a high variation in quantization noise contributions. This degrades the performance at a low LO frequency. In [22], the NF increases from 16 dB to 28 dB when the LO decreases from 2 GHz to 400 MHz. Compared to CT architectures, their limitation is for high LO frequencies. As can be seen in the table, they are limited to less than 3 GHz. The BP LC $\Delta\Sigma$ proposed in [38] can cover high frequencies but due to the use of an LC resonator, it comes at the cost of a higher complexity and coverage limited only to one octave. Unfortunately, regarding measurements, the proposed architecture only achieves 0.4 to 1.2 GHz due to the aforementioned problems. In terms of linearity and noise balance, the DT architecture achieves a very good IIP3 of 10 dBm as it only has one active integrator but this comes at the cost of a high NF. On the other hand, the CT architectures have very good noise performance [19], achieving an NF at around 3 dB but this comes at the cost of poorer linearity (around -20 dBm of IIP3). The proposed architecture is somehow a trade-off between the two families as it achieves 2–3 dBm of IIP3 and an NF of 13 dB in the simulation (22 dB in measurements due to the aforementioned problem of power transfer). The choice of the ratio between the LNTA feedforward gain and the feedback gain of the first DAC is an important parameter to set the trade-off between noise and linearity for DT passive/active architectures, like ours and [22]. A high gain improves the NF but degrades the IIP3 and vice-versa. In terms of power consumption, the DT architecture [22] has very good static power consumption but since all the switches operate at the LO frequency, the dynamic power drastically increases for high-frequency LO, from 17 mW for 0.4 GHz to 70 mW at 4 GHz. For the CT architectures and the proposed architecture, the LO dependency of power consumption is lower as the loop operates at a constant f_s. In terms of DR, the proposed architecture achieves very high DR thanks to its good peak SNDR, good stability of its loop, and 12 dB gain control.

7. Conclusions

This paper presented the implementation of a novel DT passive/active DDSR. The main feature of the architecture, with respect to the existing DDSR, is the use of a sampling frequency that is a divider of the LO frequency. This addresses several problems, such as quantization noise upmixing, the need for reconfiguration of the Delta-Sigma loop when changing the LO frequency, and the use of two independent clocks for LO and f_s.

The designed system has very good performance in the post-layout simulation, with a very wide LO range and a very interesting compromise among noise, linearity, and power consumption. Regarding the measurements, the performance is limited by, most likely, a packaging problem. Nevertheless, the results are still very promising with very good linearity (IIP3 of 2.3 dBm and IIP2 of 23.3 dBm), a high peak SNDR of 46 dB, and a very high dynamic range of 80 dB.

Several promising research and development axes for this architecture will take place in the future. First, using this architecture for mmWave applications will require very accurate and careful frequency planning. A second challenge involves decoupling the filtering, or the STF, from the quantization noise performance, or the NTF. In classical Delta-Sigma loops, this is conducted by using feed-in and feedforward coefficients; however, in DDSRs, implementing these types of coefficients presents more challenges and necessitates novel implementations.

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