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A High Dynamic Velocity Locked Loop for the Carrier Tracking of a Wide-Band Hybrid Direct Sequence/Frequency Hopping Spread-Spectrum Signal

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Abstract: For hybrid direct sequence/frequency hopping (DS/FH) spread spectrum signals, even if the relative motion speed between the transmitter and receiver remains constant, the Doppler frequency will vary due to the continuous hopping of the carrier frequency. Under high dynamic conditions, the first-order and second-order change rates of the Doppler frequency attached to the received signal further increase the Doppler frequency agility, making it difficult for the carrier tracking loop to maintain steady-state tracking. To address these issues, a high dynamic velocity locked loop (HD-VLL) is proposed in this paper. Specifically, the accumulated phase tracking error caused by acceleration and jerk is first analyzed. Subsequently, to compensate for this phase tracking error with the system clock, the proposed loop adds an acceleration compensation module and a jerk compensation module. However, this results in the output of the high dynamic loop filter being updated with the system clock, which contradicts the multiplexing design of a traditional loop filter for parallel signal processing, making the hardware implementation of an HD-VLL impractical. Therefore, this contradiction leads us to design an HD-VLL-based multi-carrier NCO (HD-VLL-NCO). The HD-VLL and HD-VLL-NCO are simulated, revealing the HD-VLL's superior dynamic adaptability and steady-state tracking, while the HD-VLL-NCO achieves comparable accuracy with the appropriate truncation bit width.

Keywords: DS/FH; carrier tracking; high dynamic; velocity locked loop

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1. Introduction

The hybrid direct sequence/frequency hopping (DS/FH) spread spectrum technology integrates the strengths of both a direct sequence spread spectrum (DSSS) and a frequency hopping spread spectrum (FHSS), making it a preferred choice for applications in space TT&C (Telemetry, Tracking, and Command), satellite communication, satellite navigation, and various other domains demanding robust anti-interference and anti-interception capabilities [1–6]. In the hybrid DS/FH spread spectrum system, multiple carriers are transmitted in a time-division pattern. Due to the continuous hopping of the carrier frequency, even if the motion speed remains constant, the carrier's Doppler frequency will experience corresponding variations. When the relative motion speed is high, the Doppler frequency differences across different carrier frequencies become greater. The continuous hopping of the Doppler frequency introduces new frequency step excitations to the carrier tracking loop, necessitating constant adjustments to accommodate these changes. As a result, this ongoing frequency step response poses a severe challenge to steady-state tracking. Particularly in high dynamic environments, such as high-speed mobile communication scenarios, the first-order and second-order rates of change of the Doppler frequency become even more significant. These rates of change not only increase the difficulty of tracking but may also lead to the loss of lock. In response to this challenge, we need to conduct in-depth

research on the tracking algorithms for hybrid DS/FH spread spectrum signals under high dynamic conditions.

In recent decades, the tracking technology for a hybrid DS/FH spread spectrum signal has drawn the attention of scholars at home and abroad. The authors of [7] analyze the effects of multiple interferences on the range and velocity measurement performance of a hybrid DS/FH spread spectrum system, providing a reference for the research on hybrid DS/FH spread spectrum signal tracking. A carrier tracking method aided by a frequency hopping pattern is presented in [8]. The Doppler shift variable introduced by the next frequency hopping point is estimated based on the predicted frequency hopping pattern and the current speed measurement. However, the maximum hopping speed is only 1.2 khop/s. The authors of [9] propose a hybrid DS/FH spread spectrum signal tracking approach. Although the hopping rate reaches 10 khops/s, the coherent integration period only occupies one frequency hopping time slot, which is only applicable to high signal-to-noise ratio (SNR) scenarios. The key technologies for the reception of hybrid direct sequence/fast frequency hopping (DS/FFH) spread spectrum signals are investigated in [10], including signal acquisition, tracking, and group delay equalization methods, in which the signal tracking part adopts the same method as that used in [8]. Although the frequency hopping rate involved is up to 100 khops/s, the information rate is set to be the same as the frequency hopping rate, making it only applicable to scenarios with a higher SNR. The authors of [11,12] employ a tracking scheme based on a velocity locked loop (VLL), which utilizes the coherent integration results of multiple hops for discrimination. The employed scheme simultaneously achieves the requirements of a high hopping rate and low SNR, yet the involved dynamic is merely 10 g/s, where g = 9.8 m/s^2. Table 1 lists the hopping rates, dynamics, SNR, and loop structures involved in [8–12].

Table 1. Comparison of hopping rates, dynamics, SNR, and loop structures.

References	Hopping Rates (hops/s)	Dynamics	SNR (dB)	Loop Structures
[8]	≤1.2 k	Acceleration 30 g	≥13	Second-order PLL
[9]	10 k	Unspecified	Unspecified	FLL and PLL Switching
[10]	100 k	Unspecified	≥0	PLL
[11]	10 k	Jerk 10 g/s	≥−30	Second-order VLL assisted third-order PLL
[12]	9 k	Jerk 10 g/s	−25	Second-order VLL assisted third-order PLL

As indicated in Table 1, the research on tracking algorithms for high dynamic hybrid DS/FH spread spectrum signals has remained relatively scarce in recent years. Nevertheless, it is reassuring to note that numerous research achievements have been made in the tracking of high dynamic DSSS signals in recent times. Since the VLL used for hybrid DS/FH spread spectrum signals shares structural similarities with the frequency locked loop (FLL) employed for DSSS signals, we can draw inspiration from the tracking algorithms developed for DSSS signals under high dynamic conditions and design tracking algorithms suitable for VLL.

It was found that the filter parameters (i.e., the loop bandwidth) are essentially governed by the noise characteristic and dynamics. To this end, the authors of [13] derive the optimal loop bandwidth. Furthermore, the authors of [14–16] propose tracking algorithms that can adaptively adjust the loop bandwidth. However, both the dynamic adaptability and real-time performance of these adaptive algorithms are limited to a certain extent. The superiority of an FLL mainly comes from its wide pull-in range. Therefore, an FLL is often used to assist a phase locked loop (PLL) in a coupled structure to maintain the lock of the carrier tracking loop when there is a possible large frequency error under the high dynamic environment. The authors of [17] utilize a tracking algorithm switching between an FLL and PLL; the authors of [18] employ a loop structure of the second-order FLL and serially assisted third-order PLL; the authors of [19] weigh the discriminating results of a second-order FLL and third-order PLL, respectively, and adjust the weights according to different dynamic conditions; and the authors of [20] further analyze the steady-state

tracking performance of a second-order FLL and parallelly assisted third-order PLL. However, these algorithms only discuss the improvement of loop structure without considering the improvement in the loop filter. An iterative filter design for an FLL and parallelly assisted PLL is presented in [21], but the iterative process may increase the computational complexity; the authors of [22] analyze the filter structure of a conventional third-order PLL and design a high dynamic PLL, but by simply considering the PLL-only case. The authors of [23] propose a high dynamic loop filter based on a second-order FLL and serially assisted third-order PLL, which achieves stable tracking in a high dynamic condition with an acceleration of 120 g and a jerk of 30 g/s.

Based on our previous thorough discussions, we recognized the issue of frequency agility in hybrid DS/FH spread spectrum signals. This characteristic of frequency agility poses significant challenges to the traditional structure of an FLL-assisted PLL. However, it is noteworthy that although the carrier frequency of the hybrid DS/FH spread spectrum signal undergoes hops, the relative motion speed remains continuously variable. Consequently, we utilize the VLL instead of FLL to track hybrid DS/FH spread spectrum signals. Nevertheless, when facing high dynamic scenarios characterized by significant acceleration and jerk, the rapid variation in signals makes it difficult for a traditional VLL to effectively cope and maintain stable tracking.

To achieve stable tracking of a hybrid DS/FH spread spectrum signal under high dynamic conditions, a high dynamic VLL (HD-VLL) based on the high dynamic loop filter is proposed in this paper. We initially delve into the accumulated phase tracking error caused by acceleration and jerk. Subsequently, the HD-VLL incorporates an acceleration compensation module and a jerk compensation module within the traditional VLL loop filter, which compensate for the phase tracking error with the system clock. Regarding the hardware implementation of HD-VLL, the output of the HD-VLL loop filter is updated with the system clock, which may conflict with the multiplexing function of traditional filters in parallel signal processing. In light of the aforementioned contradiction and taking into account the fact that the multi-carrier NCO module is also updated with the system clock, we design an HD-VLL-based multi-carrier NCO (HD-VLL-NCO). We conduct simulation analyses on an HD-VLL and HD-VLL-NCO, and the results reveal the following: Firstly, the HD-VLL demonstrates superior dynamic adaptability and steady-state tracking performance. Secondly, with the appropriate truncation bit width set, the HD-VLL-NCO is capable of achieving accuracy comparable to that of HD-VLL.

2. Hybrid DS/FH Spread Spectrum Signal Model

The received hybrid DS/FH spread spectrum signal at the receiver's front end is modeled as follows:

$$r(t) = \sqrt{2P} \cdot D(t - \tau_t) \cdot C(t - \tau_t) \cdot \cos\left[2\pi\left(f_{cj} + f_{dj}\right)t + \varphi_t\right] + n_0(t), \quad (1)$$

where the constituent parameters are defined in Table 2.

Table 2. Parameters in hybrid DS/FH spread spectrum signal model.

Parameters	Definition
P	Received signal power
$D(t)$	Data bit, $D(t) = \pm 1$
$C(t)$	DS code sequence with code rate of R_c
τ_t	Code delay time in seconds
φ_t	Initial carrier phase in radians
$n_0(t)$	Zero-mean Gaussian white noise that has one-sided power spectral density of N_0
f_{cj}	Carrier frequency of jth frequency hopping time slot
f_{dj}	Doppler frequency offset in jth frequency hopping time slot caused by relative motion between transmitter and receiver

The carrier frequency f_{cj} in (1) can be specifically expressed as follows:

$$f_{cj} = f_c + h(j) \cdot \Delta f, \tag{2}$$

where f_c is the carrier center frequency, Δf is the minimum hopping interval, and $h(j)$ is the hopping point corresponding to the frequency hopping pattern.

It is assumed that the relative motion velocity between the transmitter and receiver is v, which is small with respect to the speed of light c. The approximation of the Doppler frequency f_{dj} corresponding to the carrier frequency f_{cj} is as follows:

$$f_{dj} = \frac{v}{c} f_{cj} = \frac{v}{c} f_c + h(j) \cdot \frac{v}{c} \Delta f. \tag{3}$$

Additionally, the FH code designed in this paper is correlated with the DS code, which means the DS code rate is a multiple of the FH code rate, and a frequency hopping time slot contains a fixed number of DS chips. Therefore, the synchronization of an FH code is completed at the same time as the DS code using a traditional delay locked loop (DLL), and there is no need to track the FH code phase independently.

3. HD-VLL for Hybrid DS/FH Spread Spectrum Signals

3.1. A Description of the Problem

It can be seen in (3) that the changing carrier frequency of each hopping time slot leads to the variable Doppler frequency, and the Doppler frequency jump between two adjacent hopping time slots can be expressed as follows:

$$f_{d(j+1)} - f_{dj} = \frac{v_{j+1}}{c}[f_c + h(j+1)\Delta f] - \frac{v_j}{c}[f_c + h(j)\Delta f]. \tag{4}$$

In general, it can be assumed that the velocity is almost the same in two adjacent frequency hopping time slots due to the high frequency hopping rate, so (4) can be written as follows:

$$f_{d(j+1)} - f_{dj} = \frac{v}{c}[h(j+1) - h(j)]\Delta f. \tag{5}$$

Equation (5) indicates that the Doppler frequency jump between adjacent hopping time slots is small when the relative motion velocity between the transmitter and receiver is small. In this case, an FLL can be used for carrier tracking, and the Doppler frequency jump will be huge when the relative motion velocity becomes large. This Doppler frequency jump continuously introduces a frequency step excitation to the FLL, causing a continuous response of the frequency step excitation, which makes it difficult to maintain steady-state tracking.

To address the above problem, considering that the relative motion velocity is almost constant while the Doppler frequency is severely hopping between the two adjacent hopping time slots, we replace the FLL with a VLL in hybrid DS/FH spread spectrum signal carrier tracking. A VLL is much the same as an FLL except for the velocity discriminator. After the synchronization of the FH code, both the transmitter and receiver know the prior information of the FH sequence; thus, the velocity value can be converted to the corresponding Doppler frequency value in the multi-carrier NCO module. The structure of the VLL is shown in Figure 1.

The FLL and serially assisted PLL and the FLL with a parallelly assisted PLL are commonly used coupled structures of FLLs and PLLs for DS spread spectrum signal carrier tracking. Since a VLL is used instead of an FLL for hybrid DS/FH spread spectrum signal carrier tracking, there are corresponding structures of a VLL with a serially assisted PLL (VLL-SA-PLL) and a VLL with a parallelly assisted PLL (VLL-PA-PLL), as shown in Figures 2 and 3, respectively. In addition, note that both the VLL and HD-VLL are second-order and the PLL is third-order in the following discussion and simulation.

There are not only high relative motion velocities, but also large acceleration and jerk in the high dynamic environment. However, the VLL loop filter suffers from insensitivity to acceleration and jerk.

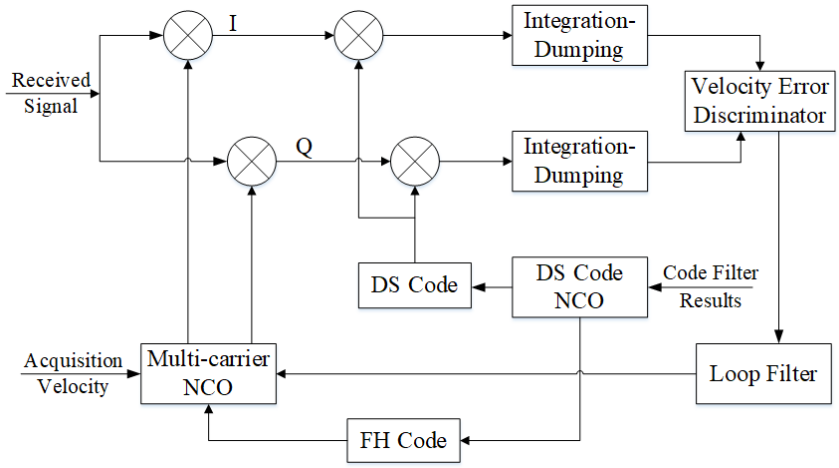


Figure 1. Block diagram of VLL.

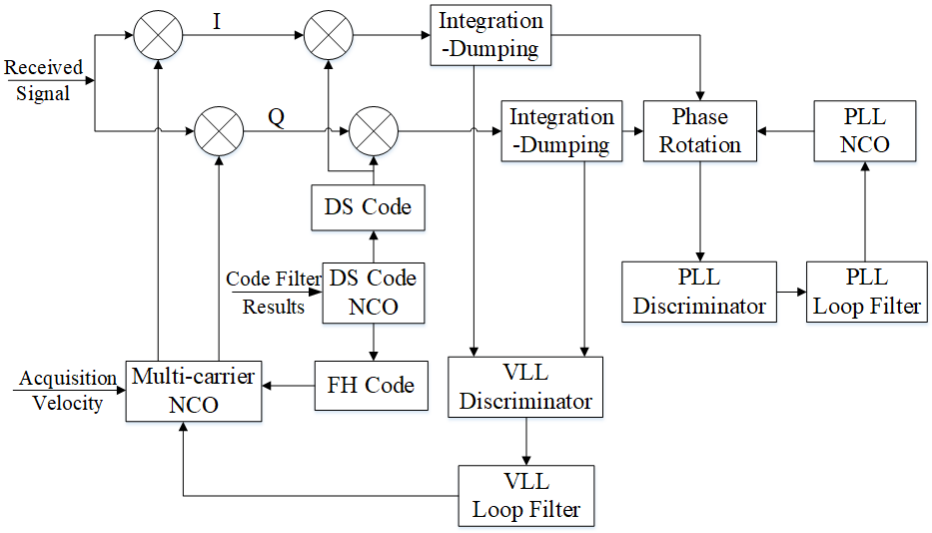


Figure 2. Block diagram of VLL with serially assisted PLL.

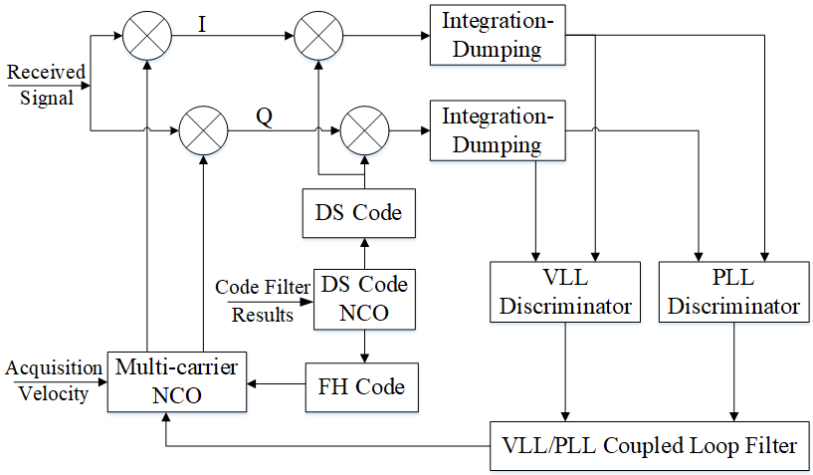


Figure 3. Block diagram of VLL with parallelly assisted PLL.

Taking the second-order VLL loop filter as an example, the filter output is fixed during each loop update period (the loop update period is generally the same as the coherent integration period). Assuming that in the kth loop update period, the initial phase of the multi-carrier NCO accumulator is ϕ_{0k}, the filter output $\hat{v}_{dk}$ in the last period plus velocity by acquisition v_{acq} is taken as an estimated value of the velocity $\hat{v}_d$, which is converted into Doppler frequency according to the carrier frequency of the current hopping time slot. Then, the local instantaneous phase generated by the multi-carrier NCO during the kth loop update period is given by (6) as follows:

$$\phi_{ki} = \phi_{0k} + \frac{2\pi f_{cj}}{c}\left(\hat{v}_{dk} + v_{acq}\right) iT_s = \phi_{0k} + \frac{2\pi f_{cj}}{c}\hat{v}_d iT_s, \;\; i = 0, 1, 2, \ldots, M-1, \tag{6}$$

where T_s denotes the sampling interval, and i and M denote the ith sampling point and the number of sampling points in a loop update period, respectively.

Practically, the instantaneous phase of the received signal is not only affected by velocity, but also by acceleration and jerk. Considering a high dynamic scenario with simultaneous velocity v_d, acceleration a, and jerk $\dot{a}$, the instantaneous phase φ_k of the received signal during the kth loop update period can be expressed as follows:

$$\varphi_k = \varphi_{0k} + \frac{2\pi f_{cj}}{c} v_d (t - nT) + \frac{\pi f_{cj}}{c} a (t - nT)^2 + \frac{\pi f_{cj}}{3c} \dot{a} (t - nT)^3, \tag{7}$$

where φ_{0k} denotes the initial phase of the kth loop update period, T denotes the loop update interval, and $T = MT_s$.

By discretizing the analog signal in (7), we obtain

$$\varphi_{ki} = \varphi_{0k} + \frac{2\pi f_{cj}}{c} v_d iT_s + \frac{\pi f_{cj}}{c} a (iT_s)^2 + \frac{\pi f_{cj}}{3c} \dot{a} (iT_s)^3, \;\; i = 0, 1, 2, \ldots, M-1. \tag{8}$$

The purpose of the carrier tracking loop is to generate a replica signal of the received carrier signal, that is, the error between the local instantaneous phase of the replica signal and the instantaneous phase of the received signal should be as small as possible at each moment. By comparing (6) with (8), it can be seen that (6) only takes into account the effect of velocity on the local instantaneous phase but leaves out the effects of acceleration and jerk. Consequently, there is an accumulated phase tracking error of $\pi f_{cj} a T^2/c + \pi f_{cj} \dot{a} T^3/3c$ at the end of the kth loop update period. This accumulated phase tracking error is little when the dynamic is small; in this case, the impact on the loop can be ignored. However, as the dynamic increases, this accumulated phase tracking error poses challenges to the steady-state tracking of the loop.

3.2. HD-VLL

According to the discussion in Section 3.1, the filter output of the second-order VLL loop filter remains constant during a loop update period without taking into account the phase variation caused by acceleration and jerk, eventually causing the accumulated phase tracking error. To address the accumulated phase tracking error of the second-order VLL under high dynamic conditions, an HD-VLL based on the second-order VLL is proposed, which can simultaneously process jerk, acceleration, and velocity.

By comparing (6) and (8), it can be seen that at the ith sampling point of the kth loop update period, the phase variation generated by jerk and acceleration is $\pi f_{cj} a (iT_s)^2/c + \pi f_{cj} \dot{a} (iT_s)^3/3c$, which should be compensated in real time. However, it is observed that the values of acceleration and jerk cannot be obtained directly; thus, it is necessary to find reasonable estimates of acceleration as well as jerk, respectively.

The structure of the second-order VLL loop filter is depicted in Figure 4.

In the figure, ω_{nv} and K represent the characteristic angular frequency and the gain of the second-order VLL loop filter, and z^{-1} represents the unit delay, respectively.

The corresponding discrete transfer function is

$$V(z) = \frac{(\sqrt{2}\omega_{nv}T + \omega_{nv}^2T^2) - \sqrt{2}\omega_{nv}T \cdot z^{-1}}{K(1 - 2z^{-1} + z^{-2})}, \tag{9}$$

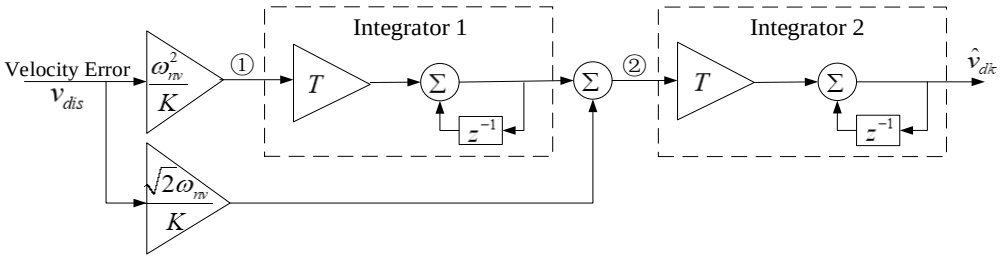


Figure 4. Structure of second-order VLL loop filter.

After filtering the input velocity error signal, the filtered state variables of the high-order loop filter also contain high-order information in addition to the filtered velocity error result, such as acceleration and jerk [24–30]. In the second-order VLL loop filter structure shown in Figure 4, signal ① located before Integrator 1 is actually the filtered second-order change rate of the velocity error (i.e., jerk), and the corresponding discrete transfer function between the input and ① is

$$V_{\dot{a}}(z) = \frac{\omega_{nv}^2}{K}. \tag{10}$$

Signal ②, located before Integrator 2, is actually the filtered first-order change rate of the velocity error (i.e., acceleration), and the corresponding discrete transfer function between the input and ② is

$$V_a(z) = \frac{\sqrt{2}\omega_{nv} + \omega_{nv}^2T - \sqrt{2}\omega_{nv}z^{-1}}{K(1 - z^{-1})}. \tag{11}$$

Hence, there is high-order information in the second-order VLL loop filter, which makes it adaptable to scenarios with certain acceleration and jerk. The filter output $\hat{v}_{dk}$, which is obtained by integrating the filtered acceleration and the filtered jerk, is constant during a loop update period and is actually the estimate of the velocity at the start of the next loop update period. However, as the acceleration and jerk become greater, it is not only necessary to estimate the velocity variation between adjacent loop update periods, but also to provide a reasonable prediction of the velocity variation caused by acceleration and jerk at each sampling point during the loop update period. In this way, the difference between the local instantaneous phase of the replica signal and the instantaneous phase of the received signal at each sampling point can be as small as possible.

Therefore, the structure of the HD-VLL is proposed by adding acceleration and jerk compensation modules operating at the system clock to the second-order VLL loop filter. According to the previous analysis, ① is regarded as the estimated value $\hat{\dot{a}}$ of jerk $\dot{a}$, and ② is regarded as the estimated value $\hat{a}$ of acceleration a, so the acceleration and jerk compensation modules should compensate for a phase of $\pi f_{cj}\hat{a}(iT_s)^2/c + \pi f_{cj}\hat{\dot{a}}(iT_s)^3/3c$ at the ith sampling point.

Since the process of summing i or i^2 by the accumulator is analogous to the integration process of the continuous signal, the workflow of HD-VLL to generate the local instantaneous phase is given below.

Accumulator 1 in the jerk compensation module accumulates the filtered jerk value $\hat{\dot{a}}$ at each system clock, and the output s_{1i} at the ith sampling point can be written as follows:

$$s_{1i} = \sum_{l=1}^{i} \hat{\dot{a}}T_s = \hat{\dot{a}} \cdot iT_s. \tag{12}$$

The output of Accumulator 1 and the filtered acceleration value $\hat{a}$ are added and sent to the acceleration compensation module. Accumulator 2 in the acceleration compensation module accumulates $\hat{a} + \hat{\dot{a}}iT_s$ at each system clock, and the output s_{2i} at the ith sampling point can be written as follows:

$$s_{2i} = \sum_{l=1}^{i} (\hat{a} + \hat{\dot{a}}lT_s) \cdot T_s = \hat{a} \cdot iT_s + \hat{\dot{a}}T_s{}^2 \cdot \frac{i(i+1)}{2} \approx \hat{a} \cdot iT_s + \frac{1}{2}\hat{\dot{a}} \cdot (iT_s)^2, \tag{13}$$

where (13) is an approximation valid for $\hat{\dot{a}}T_s \ll \hat{a}$.

The output of Accumulator 2 and the filtered velocity value $\hat{v}_{dk}$ are added together as the final output s_{3i}, which can be expressed as follows:

$$s_{3i} = \hat{v}_{dk} + \hat{a} \cdot iT_s + \frac{1}{2}\hat{\dot{a}} \cdot (iT_s)^2. \tag{14}$$

The output s_{3i} of the HD-VLL filter and the acquisition velocity v_{acq} are summed and converted to Doppler frequency according to the carrier frequency of the current frequency hopping time slot, which is accumulated by the multi-carrier NCO to produce the local instantaneous phase, and the result is given in (15).

$$\begin{aligned} \phi_{ki} &= \phi_{0k} + \frac{2\pi f_{cj}}{c}\sum_{l=1}^{i}\left(v_{acq} + \hat{v}_{dk} + \hat{a}lT_s + \frac{1}{2}\hat{\dot{a}}l^2T_s^2\right) \cdot T_s \\ &= \phi_{0k} + \frac{2\pi f_{cj}}{c}(v_{acq} + \hat{v}_{dk}) \cdot iT_s + \frac{\pi f_{cj}}{c}\hat{a} \cdot (iT_s)^2 + \frac{\pi f_{cj}}{3c}\hat{\dot{a}} \cdot (iT_s)^3 \\ &= \phi_{0k} + \frac{2\pi f_{cj}}{c}\hat{v}_d \cdot iT_s + \frac{\pi f_{cj}}{c}\hat{a} \cdot (iT_s)^2 + \frac{\pi f_{cj}}{3c}\hat{\dot{a}} \cdot (iT_s)^3,\ i = 0, 1, 2, \ldots, M-1. \end{aligned} \tag{15}$$

Compared to the local instantaneous phase produced by the second-order VLL in (6), which only contains the phase generated by velocity, the local instantaneous phase produced by the HD-VLL in (15) contains the phase generated by velocity, acceleration, and jerk. Hence, (15) better fits the instantaneous phase of the received signal in (8), which reduces the dynamic impact on the loop. A structure diagram of the HD-VLL is shown in Figure 5.

As shown in Figure 5, the structure of a multi-carrier NCO is displayed in the dashed box above, where K_o is the gain of the multi-carrier NCO; the structure of the HD-VLL loop filter is displayed in the dashed box below, where the second-order VLL loop filter structure is shown in the gray area, the jerk compensation module is shown in the purple area, and the acceleration compensation module is shown in the red area.

The workflow of the HD-VLL to generate local phase is summarized in Algorithm 1.

Algorithm 1: Workflow of HD-VLL to Generate Local Phase

1: Input: velocity error v_{dis}, sampling period T_s, loop update interval T, total number of loop update periods L, total number of sampling points in a loop update period M, carrier frequency of the current frequency hopping time slot f_{cj}, acquisition velocity v_{acq}, loop bandwidth B_v.

2 : Initialization : $k = 1,\ i = 1$.
3 : for $k = 1, 2, \ldots, L$ do
4 : Velocity error discriminator module updates the velocity error v_{dis}.
5 : Update $\hat{\dot{a}}$, $\hat{a}$ and $\hat{v}_{dk}$ by formula (10), formula (11) and formula (9).
6 : for $i = 0, 1, \ldots, M-1$ do
7 : Update s_{1i} by formula (12).
8 : Update s_{2i} by formula (13).
9 : Update s_{3i} by formula (14).
10 : Update ϕ_{ki} by formula (15).
11: end for
12: end for
13 : Output : ϕ_{ki}.

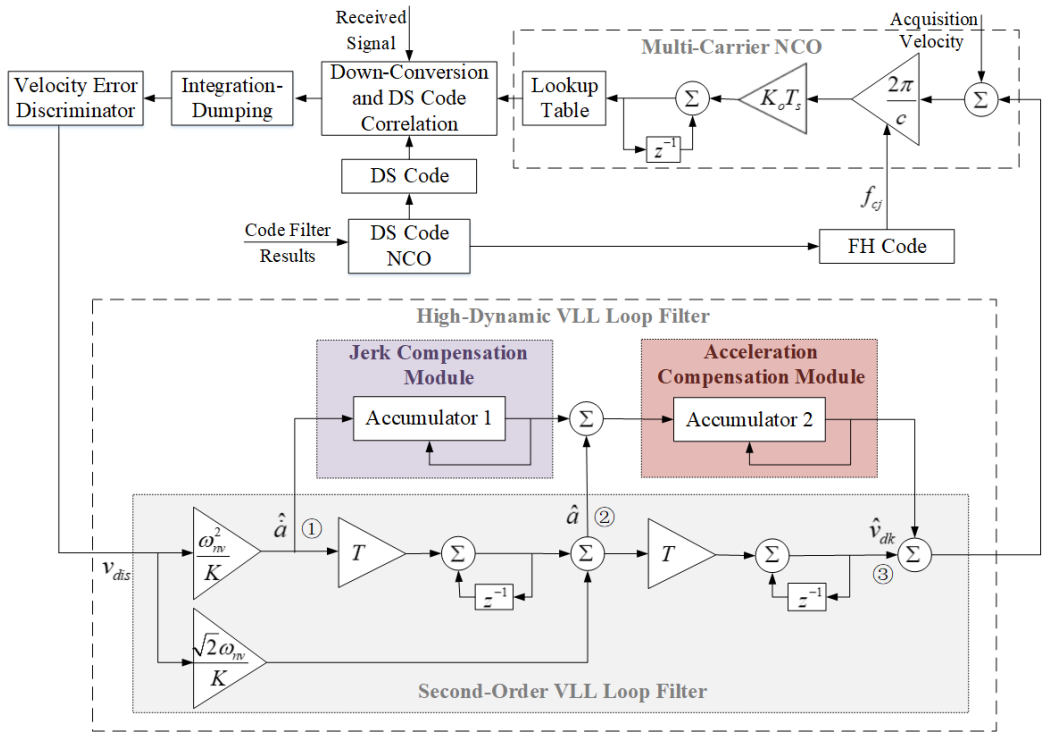


Figure 5. Structure diagram of HD-VLL.

3.3. HD-VLL-NCO

An HD-VLL for hybrid DS/FH spread spectrum signal tracking is proposed in Section 3.2, but the below problems are faced in practical engineering implementation.

When the number of channels involved in a communication system is relatively small, or when hardware resources are sufficient, we typically equip each channel with an independent filter module to ensure independent and stable tracking for each channel. In this case, the HD-VLL mentioned above can be directly adopted. However, when receivers simultaneously need to process signals from multiple channels in order to improve hardware resource utilization, time-division multiplexing technology is widely employed in the design of filter modules. It allows multiple channels to share the same filter module, and through precise timing control, each channel utilizes the filter during different time slots, thus achieving the parallel processing of multi-channel signals without additional hardware costs. However, the output of the HD-VLL loop filter needs to be updated with the system clock, which means the filter must complete data processing within each system clock. This high-frequency update requirement poses a certain conflict with the multiplexing of a traditional filter.

The carrier NCO plays a crucial role in generating a locally replicated carrier signal, which is updated at each system clock. The working principle of the carrier NCO involves calculating the corresponding frequency word based on the input Doppler frequency value. The accumulator then accumulates the frequency words, and the accumulation results are used to look up the table and obtain the corresponding sine and cosine amplitude values.

The multi-carrier NCO, however, differs from the carrier NCO, as illustrated in Figure 6. The workflow is as follows: The input filtered velocity value and acquisition velocity are added together to form a velocity measurement value. Based on the predicted frequency hopping pattern and the current velocity measurement value, the Doppler frequency shift variable introduced by the next frequency hopping point is estimated. Subsequently, this estimated variable is converted into a frequency word, which is then accumulated and used for the lookup table. The hybrid DS/FH spread spectrum system employs multiple carrier frequencies. When utilizing the traditional carrier NCO structure, each carrier frequency necessitates a dedicated NCO, leading to increased resource utiliza-

tion. The multi-carrier NCO, on the other hand, improves efficiency and reduces the use of hardware resources by centrally processing multiple carrier signals.

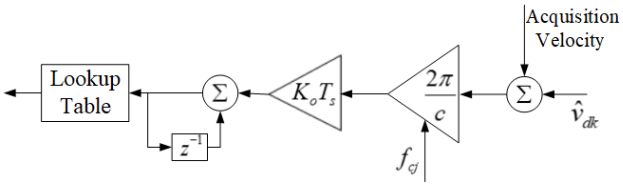


Figure 6. Structure of multi-carrier NCO.

Based on the preceding discussions, the acceleration compensation module and jerk compensation module can be integrated into the multi-carrier NCO module, leading to the design of the HD-VLL-NCO. At each loop update period, the filter module outputs the filtered jerk $\hat{a}$, the filtered acceleration $\hat{a}$, as well as the filtered velocity $\hat{v}_d$ to the multi-carrier NCO module, which uses these values to update the frequency word at each system clock and then accumulates the frequency word and looks up the table to obtain the corresponding amplitude values.

The structure of the HD-VLL-NCO is shown in Figure 7.

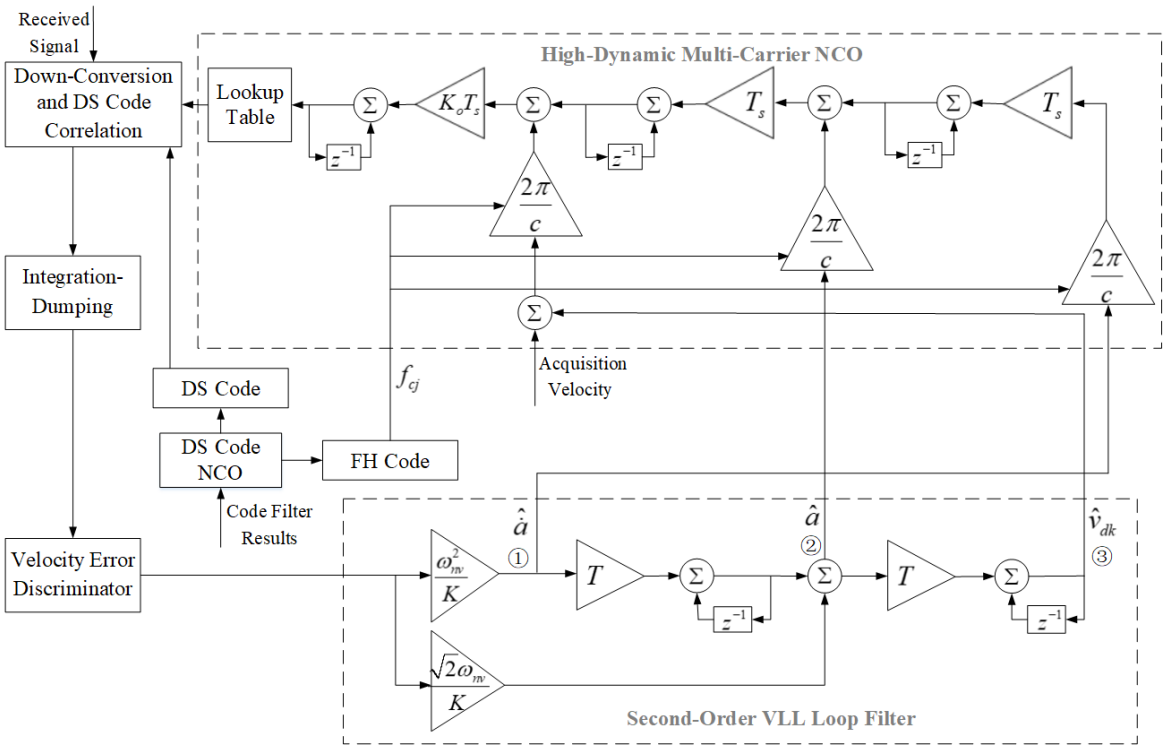


Figure 7. Structure of HD-VLL-NCO.

As is shown in Figure 7, the structure of the second-order VLL loop filter is displayed in the dashed box at the bottom, and the structure of the high dynamic multi-carrier NCO is displayed in the dashed box at the top.

However, this method will bring new problems to the multi-carrier NCO. The dimension difference between jerk, acceleration, and velocity is T_s. Since the sampling frequency f_s can reach tens or even hundreds of megahertz, its reciprocal T_s will be very small. Therefore, in high dynamic cases, it is necessary to comprehensively consider the precision and bit width when selecting the parameters for the multi-carrier NCO so as to ensure that the compensation of jerk and acceleration can be reflected on the frequency word while minimizing the waste of resources.

It can be seen in Figure 7 that there are three accumulators corresponding to three frequency words in the high dynamic multi-carrier NCO, with the name of jerk frequency word, acceleration frequency word, and frequency word, respectively. Three accumulators simultaneously accumulate these three frequency words, and the high N_0 bits of the velocity accumulator are selected to perform a phase query. Finally, the multi-carrier NCO outputs the amplitude values of the sine and cosine wave signals. By appropriately setting the bit widths of the jerk frequency word, the acceleration frequency word, the frequency word, the accumulators, as well as the truncation, it is possible to achieve the accuracy and dynamic requirements while minimizing the waste of resources.

The formulas and bit widths for the frequency words of each order are given below. The first-stage jerk accumulator sum2 accumulates the jerk frequency word f_{2w} and truncates c_2 bits of the result and then adds it to the acceleration frequency word f_{1w}, and the output $\ddot{\theta}$ is

$$\ddot{\theta}(n) = f_{1w} + \frac{1}{2^{c_2}} \sum_{m=1}^{n} f_{2w} = f_{1w} + \frac{n f_{2w}}{2^{c_2}}. \tag{16}$$

The second-stage acceleration accumulator sum1 accumulates $\ddot{\theta}(n-1)$ and truncates c_1 bits of the result and then adds it to the frequency word f_{0w}, and the output $\dot{\theta}$ is

$$\dot{\theta}(n) = f_{0w} + \frac{1}{2^{c_1}} \sum_{m=1}^{n} \theta_2(m-1) = f_{0w} + \frac{n f_{1w}}{2^{c_1}} + \frac{f_{2w}(n^2-n)}{2 \times 2^{c_1+c_2}}. \tag{17}$$

The third-stage velocity accumulator sum0 accumulates $\dot{\theta}(n-1)$ and then truncates c_0 bits of the result, and the output θ_0 is

$$\theta_0(n) = \frac{1}{2^{c_0}} \sum_{m=1}^{n} \theta_1(m-1) = \frac{n f_{0w}}{2^{c_0}} + \frac{f_{1w}(n^2-n)}{2 \times 2^{c_0+c_1}} + \frac{f_{2w}(n^3-3n^2+2n)}{6 \times 2^{c_0+c_1+c_2}}. \tag{18}$$

The phase variation caused by the filtered jerk $\hat{\hat{a}}$, the filtered acceleration $\hat{a}$, and the estimated velocity $\hat{v}_d$ can be expressed as

$$\theta(t) = \frac{2\pi f_{cj}}{c} (\hat{v}_d t + \frac{\hat{a}}{2} t^2 + \frac{\hat{\hat{a}}}{6} t^3). \tag{19}$$

After discretizing the analog signal, that is, $t = nT_s = n/f_s$, the equivalent phase sequence is defined as

$$\theta(n) = \frac{2\pi f_{cj}}{c} (\frac{\hat{v}_d}{f_s} n + \frac{\hat{a}}{2f_s^2} n^2 + \frac{\hat{\hat{a}}}{6f_s^3} n^3). \tag{20}$$

According to the principle of direct digital synthesis (DDS), the output of the accumulator has the following relationship with the phase of simulated signal:

$$\frac{N_{sum}}{2^{N_0}} = \frac{\theta(n)}{2\pi}, \tag{21}$$

where N_{sum} denotes the input of the lookup table and N_0 denotes the bit width of the lookup table.

Hence, N_{sum} can, in turn, be derived as follows:

$$N_{sum} = \frac{2^{N_0}}{2\pi} \theta(n) = \frac{2^{N_0} f_{cj}}{c} (\frac{\hat{v}_d}{f_s} n + \frac{\hat{a}}{2f_s^2} n^2 + \frac{\hat{\hat{a}}}{6f_s^3} n^3). \tag{22}$$

By making the output $\theta_0(n)$ of the HD-VLL based on the multi-carrier NCO equal to N_{sum}, the formulas for the frequency word of each order can be obtained as follows:

$$\begin{cases} f_{0w} = \frac{f_{cj}}{c}\left(\frac{\hat{\dot{a}}}{6f_s^3} + \frac{\hat{a}}{2f_s^2} + \frac{\hat{v}_d}{f_s}\right)2^{N_0+c_0} \\ f_{1w} = \frac{f_{cj}}{c}\left(\frac{\hat{\dot{a}}}{f_s^3} + \frac{\hat{a}}{f_s^2}\right)2^{N_0+c_0+c_1} \\ f_{2w} = \frac{f_{cj}}{c} \cdot \frac{\hat{\dot{a}}}{f_s^3}2^{N_0+c_0+c_1+c_2} \end{cases} . \tag{23}$$

The simplified formulas can be derived as follows:

$$\begin{cases} f_{0w} = \frac{f_{cj}}{c} \cdot \frac{\hat{v}_d}{f_s}2^{N_0+c_0} \\ f_{1w} = \frac{f_{cj}}{c} \cdot \frac{\hat{a}}{f_s^2}2^{N_0+c_0+c_1} \\ f_{2w} = \frac{f_{cj}}{c} \cdot \frac{\hat{\dot{a}}}{f_s^3}2^{N_0+c_0+c_1+c_2} \end{cases} . \tag{24}$$

When the frequency word equals 1, it corresponds to the minimum frequency value, which is also the frequency resolution. The velocity resolution can be deduced from the frequency resolution. To make the frequency word, acceleration frequency word, and jerk frequency word equal to 1, respectively, we obtain the velocity resolution Δv_d, acceleration resolution Δa, and jerk resolution $\Delta \dot{a}$ as follows:

$$\begin{cases} \Delta v_d = \frac{cf_s}{f_{cj}2^{N_0+c_0}} \\ \Delta a = \frac{cf_s^2}{f_{cj}2^{N_0+c_0+c_1}} \\ \Delta \dot{a} = \frac{cf_s^3}{f_{cj}2^{N_0+c_0+c_1+c_2}} \end{cases} . \tag{25}$$

In practical applications, Δv_d, Δa, and $\Delta \dot{a}$ are determined in terms of the accuracy requirements. After determining the lookup table bit width N_0 and sampling frequency f_s, the appropriate truncation widths c_0, c_1, and c_2 can be obtained by solving the above equations.

Figure 8 shows the block diagram of the implementation for the HD-VLL-NCO.

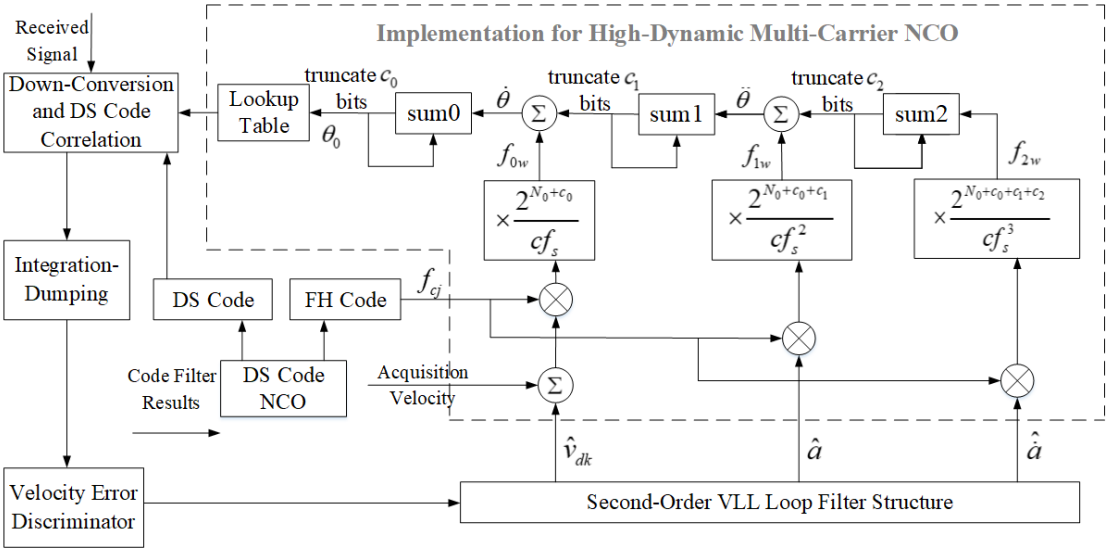


Figure 8. Implementation for HD-VLL-NCO.

4. Simulation and Analysis

For the coupled structures of the VLL and PLL, most of the dynamics are eliminated by the VLL, while the remaining small portion of the frequency and phase differences are eliminated by the PLL. According to the analysis in [31], the serial structure of the VLL and PLL has better tracking performance than a parallel structure under high dynamic

conditions. Therefore, we first simulate different bandwidths of the HD-VLL and select an appropriate bandwidth. Next, the VLL and HD-VLL are both simulated for the purpose of comparing their dynamic adaptabilities and steady-state tracking performance. Then, the VLL-SA-PLL and HD-VLL with a serially assisted PLL (HD-VLL-SA-PLL) are simulated to analyze the effect of two VLLs on the PLL's tracking performance. Finally, the HD-VLL-NCO is simulated and compared with the HD-VLL.

The simulation parameters are set as follows: the DS code rate is 10 Mchips/s, the loop update period is 5 ms, the carrier center frequency is 1.5 GHz, the minimum hopping interval is 50 kHz, the number of hopping points is 4096, and the initial velocity error for tracking is 10 m/s.

4.1. Comparison of Different Loop Bandwidths

The selection of the bandwidth is significant for a carrier tracking loop, so we first simulate the HD-VLL of different loop bandwidths.

Assuming a scenario of relative sinusoidal motion between the transmitter and receiver, the velocity is $[20sin(10t) + 30]$ m/s, the acceleration is $200cos(10t)$ m/s^2, and the jerk is $-2000sin(10t)$ m/s^3. Hence, the maximum acceleration and maximum jerk are 200 m/s^2 and 2000 m/s^3. In practical scenarios, the motion between the transmitter and receiver does not frequently reach maximum acceleration and jerk. However, we can observe the behavior of algorithms under continuously varying acceleration and jerk, including extreme cases by simulating sinusoidal motion. This periodic variation enables us to continuously test and evaluate the algorithm at different time points, providing a more comprehensive understanding of its performance under varying acceleration and jerk conditions.

The frequency hopping rate is set to 100 khops/s, and the carrier-to-noise ratio (CNR) of the received signal is set to 30 dB·Hz. Different bandwidths of 3 Hz, 5 Hz, and 8 Hz are adopted, respectively. The velocity estimate curves and velocity error curves of different bandwidths for the HD-VLL are shown in Figure 9.

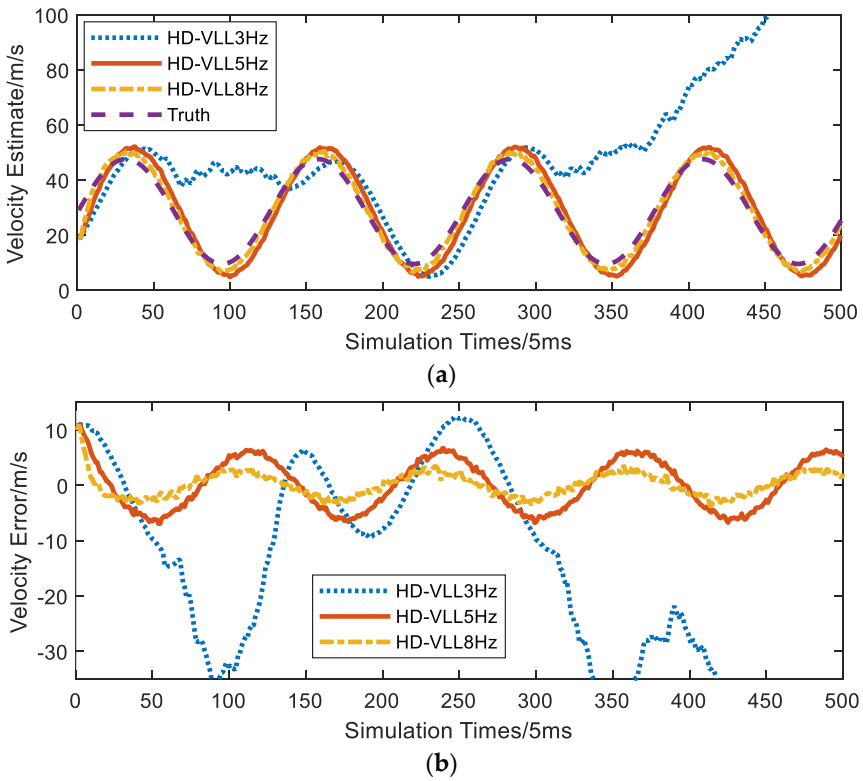


Figure 9. The tracking results of different bandwidths for the HD-VLL. (**a**) The velocity estimate curves of different bandwidths for the HD-VLL. (**b**) The velocity error curves of different bandwidths for the HD-VLL.

Figure 9 shows that the HD-VLL loses lock with the bandwidth of 3 Hz, and for the bandwidths of 5 Hz and 8 Hz, it is able to lock and enter steady-state tracking. The larger the bandwidth, the higher the dynamic the HD-VLL can adapt to. However, as the bandwidth increases, the steady-state tracking error also becomes larger, which will worsen the PLL tracking performance in HD-VLL-SA-PLL structures. Thus, we adopt 5 Hz for the HD-VLL in subsequent simulation.

4.2. Comparison of Dynamic Adaptability

To compare the dynamic adaptability of the standard VLL, the VLL variant described in [11], and the HD-VLL, all three of these systems are simulated and analyzed.

Firstly, we selected the parameters used in reference [11]: a frequency hopping rate of 10 khops/s, dynamics of 10 g/s, and a CNR of 33 dB-Hz. The three VLLs were simulated with a bandwidth of 5 Hz. The velocity estimate curves and velocity error curves of three tracking loop structures are shown in Figure 10.

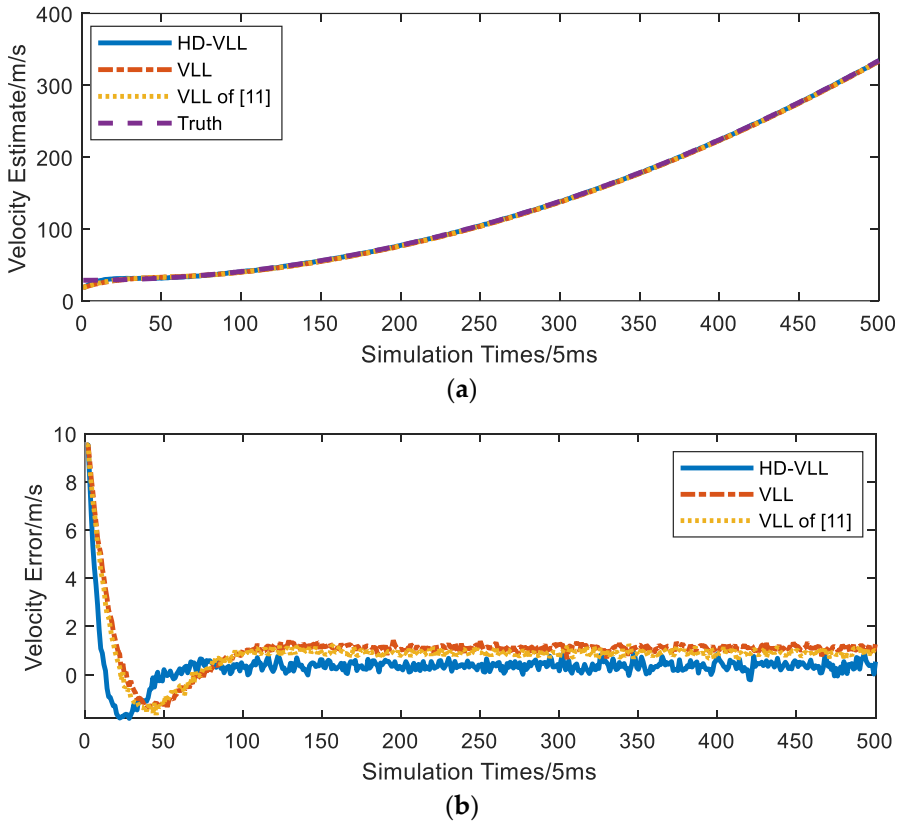


Figure 10. The tracking results of the VLL, the VLL in [11], and the HD-VLL with a jerk of 10 g/s. (**a**) The velocity estimate curve. (**b**) The velocity error curves.

As shown in Figure 10, All three VLLs are capable of steady-state tracking under the parameters used in reference [11].

Next, we increase the dynamics by assuming the same parameters as those used in Section 4.1, and a bandwidth of 5 Hz is adopted for the three VLLs. The velocity estimate curves and velocity error curves of the three tracking loop structures are shown in Figure 11.

In Figure 11, it can be seen that the HD-VLL is able to lock and enter steady-state tracking successfully, while the VLL and the VLL in [11] will lose lock at the moment of maximum jerk in the sinusoidal motion and cannot maintain steady-state tracking.

Then, to further observe the performance of VLL, the VLL in [11], and the HD-VLL under high dynamic conditions, we set up a simulation scenario where the frequency of sinusoidal motion increases with time: the velocity is $[20sin(2t^2) + 30]$ m/s, the acceleration is $80tcos(2t^2)$ m/s^2, and the jerk is $[80\cos(2t^2) - 320t^2\sin(2t^2)]$ m/s^3. It can be seen that the

maximum values of acceleration and jerk will increase with time. The velocity estimate curves and velocity error curves of the three tracking loop structures are shown in Figure 12.

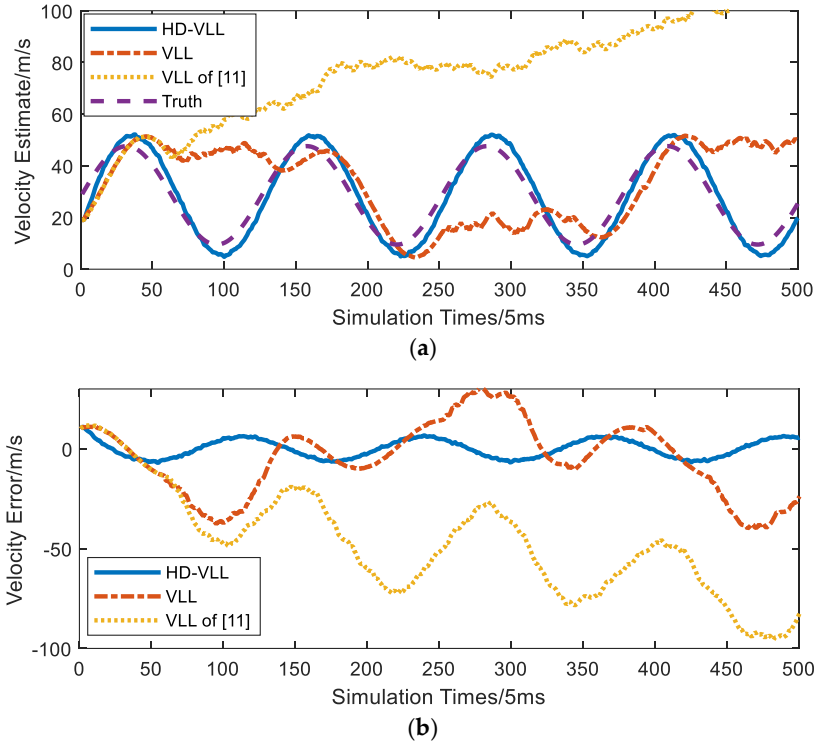


Figure 11. The tracking results of the VLL, the VLL in [11], and the HD-VLL with a velocity of $[20sin(10t) + 30]$. (**a**) The velocity estimate curve. (**b**) The velocity error curves.

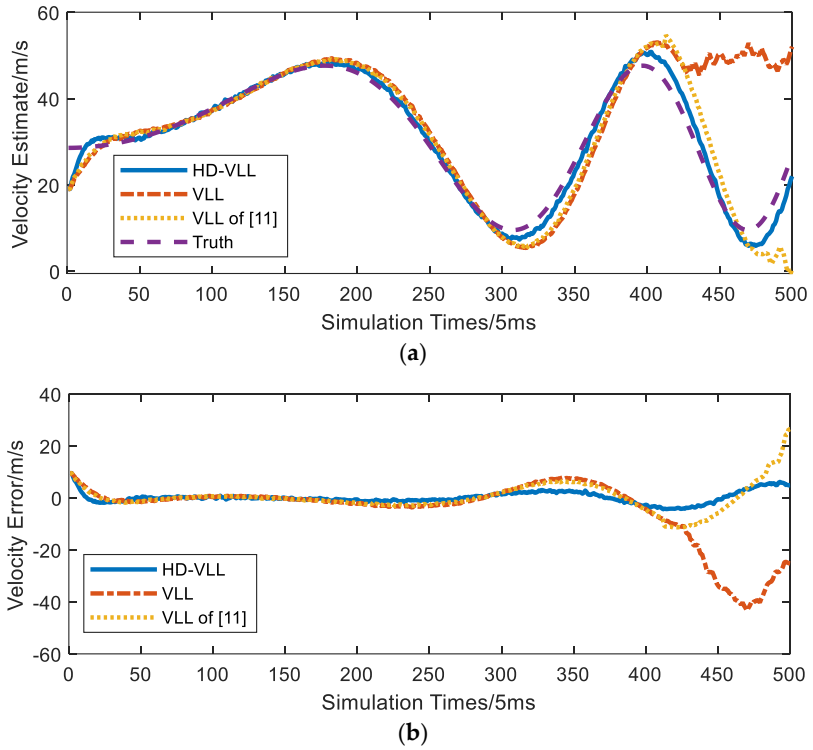


Figure 12. The tracking results of the VLL, the VLL in [11], and the HD-VLL with a velocity of $[20sin(2t^2) + 30]$. (**a**) The velocity estimate curve. (**b**) The velocity error curve.

As shown in Figure 12, at the beginning of tracking, the acceleration and jerk values are small, and the three VLLs are able to track, but as the acceleration and jerk increase, the HD-VLL can still maintain stable tracking, while the VLL and VLL in [11] cannot adapt to high dynamics and thus lose lock. Therefore, the HD-VLL proposed in this paper has better dynamic adaptability than the VLL and VLL in [11].

Finally, in order to make the VLL adapt to the given dynamic condition, the bandwidth of the VLL is increased to 8 Hz and 11 Hz, as shown in Figure 13.

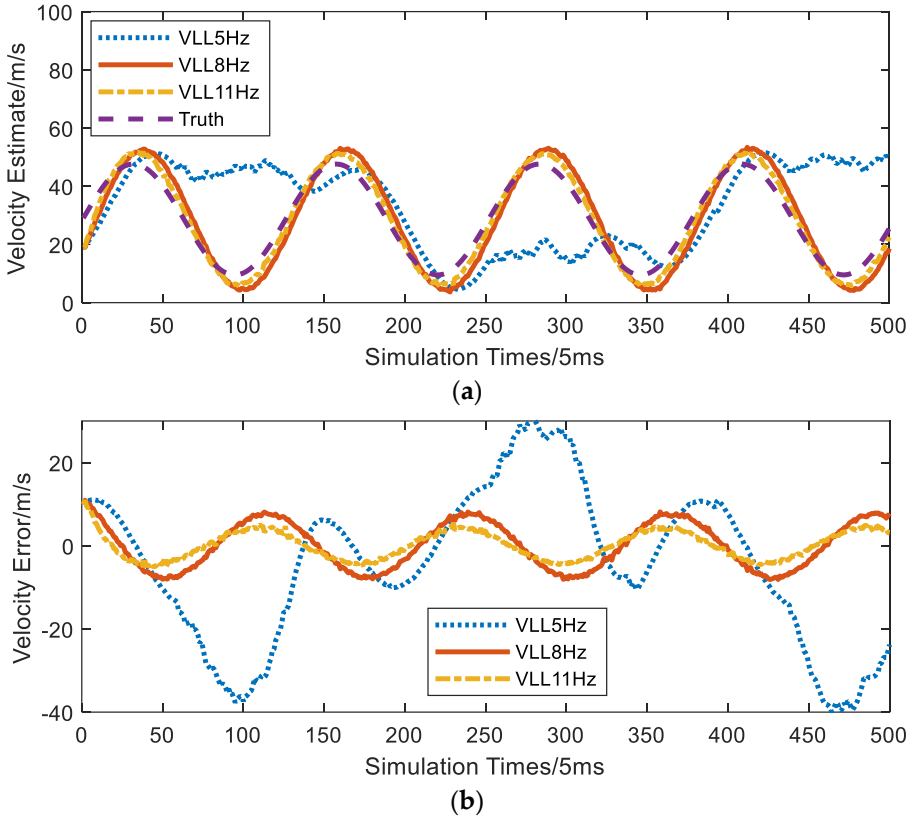


Figure 13. The tracking results of different bandwidths for the VLL. (**a**) The velocity estimate curves of different bandwidths for the VLL. (**b**) The velocity error curves of different bandwidths for the VLL.

It can be seen in Figure 13 that the VLL is able to lock and enter steady-state tracking for bandwidths of 8 Hz and 11 Hz. The larger the bandwidth, the higher the dynamic the VLL can adapt to. However, as the bandwidth increases, the steady-state tracking error also becomes larger, which worsens the PLL's tracking performance in VLL-SA-PLL structures. Thus, we adopt 8 Hz for the VLL in a subsequent simulation.

4.3. Comparison of Steady-State Tracking Performance

To compare the steady-state tracking performance of the HD-VLL and VLL, the tracking errors for both the sinusoidal motion case and fixed jerk case are analyzed, respectively.

The sinusoidal motion case is first simulated with the same sinusoidal motion parameters as those used in Section 4.1. The HD-VLL adopts a bandwidth of 5 Hz, and the VLL adopts a bandwidth of 8 Hz. The velocity estimate curves and velocity error curves of the two loop structures are depicted in Figure 14.

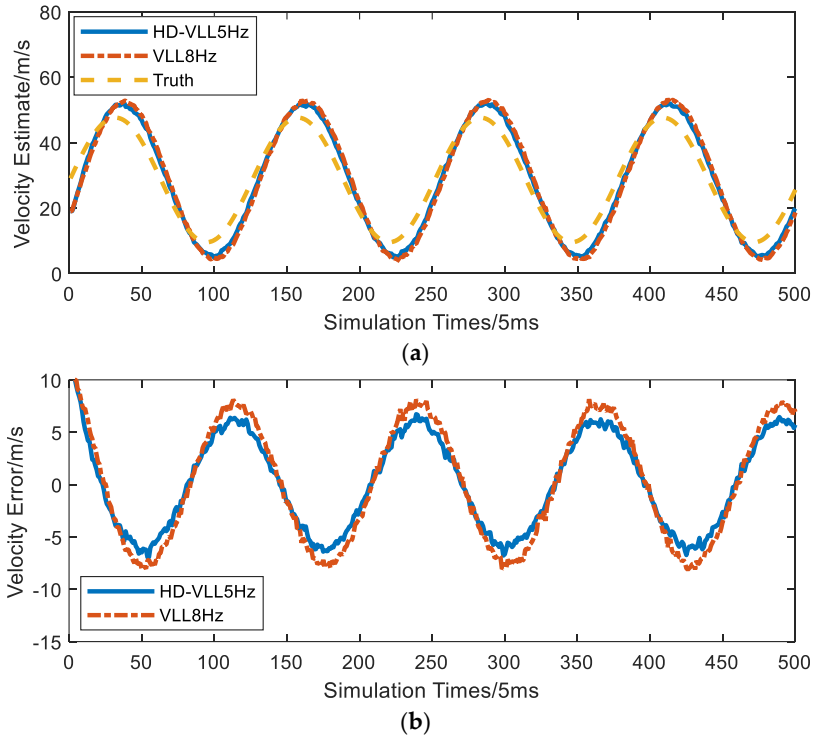


Figure 14. The tracking results of the HD-VLL and VLL in the sinusoidal motion case. (**a**) The velocity estimate curves of the HD-VLL and VLL in the sinusoidal motion case. (**b**) The velocity error curves of the HD-VLL and VLL in the sinusoidal motion case.

The mean value and standard deviation of velocity tracking errors for the HD-VLL and VLL in the sinusoidal motion case are shown in Table 3.

Table 3. Comparison of velocity tracking errors in sinusoidal motion case.

Loop Structure	Bandwidth/Hz	Mean of Velocity Tracking Error/m/s	Standard Deviation of Velocity Tracking Error /m/s
HD-VLL	5	0.25	4.42
VLL	8	0.44	5.60

The fixed jerk case is simulated with a fixed jerk of 150 g/s, and the velocity estimate curves and velocity error curves are shown in Figure 15.

The mean value and standard deviation of velocity tracking errors for the HD-VLL and VLL in the fixed jerk case are shown in Table 4.

Table 4. Comparison of velocity tracking errors in fixed jerk case.

Loop Structure	Bandwidth/Hz	Mean of Velocity Tracking Error/m/s	Standard Deviation of Velocity Tracking Error /m/s
HD-VLL	5	5.52	0.31
VLL	8	6.47	0.33

It can be seen in Tables 3 and 4 that the mean value and standard deviation of the steady-state tracking error of the HD-VLL are smaller than those of the VLL. Therefore, compared with the VLL, the HD-VLL can not only adapt to larger dynamics, but also has better steady-state tracking performance.

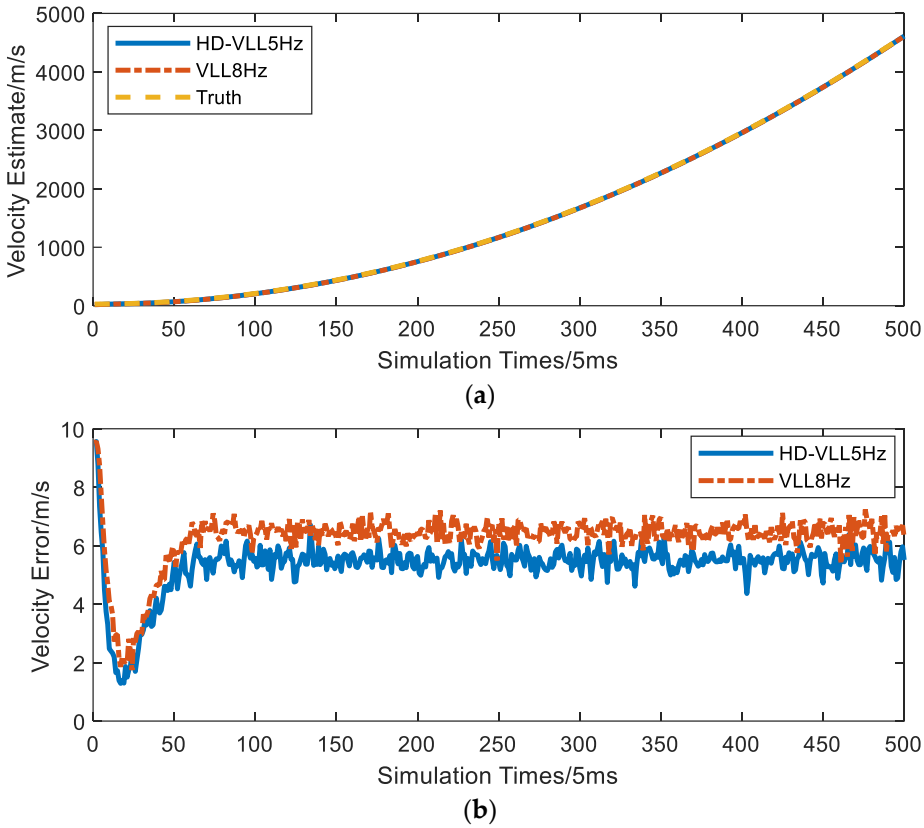


Figure 15. The tracking results of the HD-VLL and VLL in the fixed jerk case. (**a**) The velocity estimate curves of the HD-VLL and VLL in the fixed jerk case. (**b**) The velocity error curves of the HD-VLL and VLL in the fixed jerk case.

4.4. Comparison of PLL Tracking Performance

The steady-state tracking performance of the VLL affects the performance of the PLL, while the performance of the PLL is directly related to the bit error rate of the data demodulation. Therefore, the performance of the PLL both in the VLL-SA-PLL and HD-VLL-SA-PLL is compared and analyzed.

By assuming the same sinusoidal motion parameters as those used in Section 4.1, the HD-VLL adopts a bandwidth of 5 Hz, the VLL adopts a bandwidth of 8 Hz, and the PLL adopts a bandwidth of 20 Hz. The PLL discrimination curves and PLL filtering curves of the two loop structures are depicted in Figure 16.

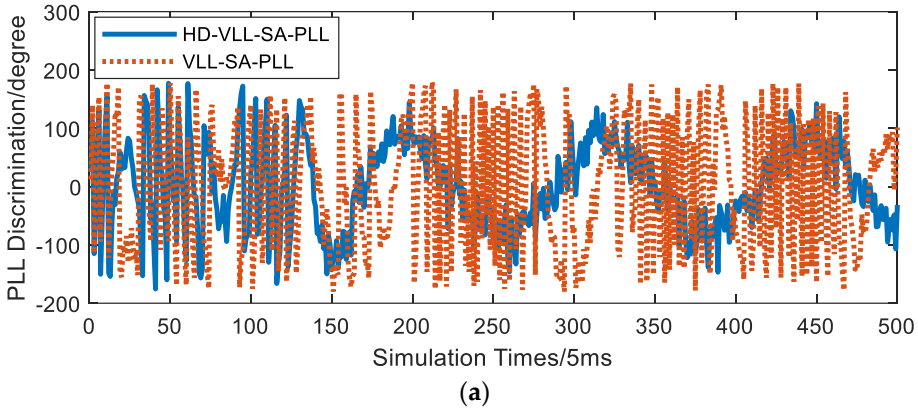
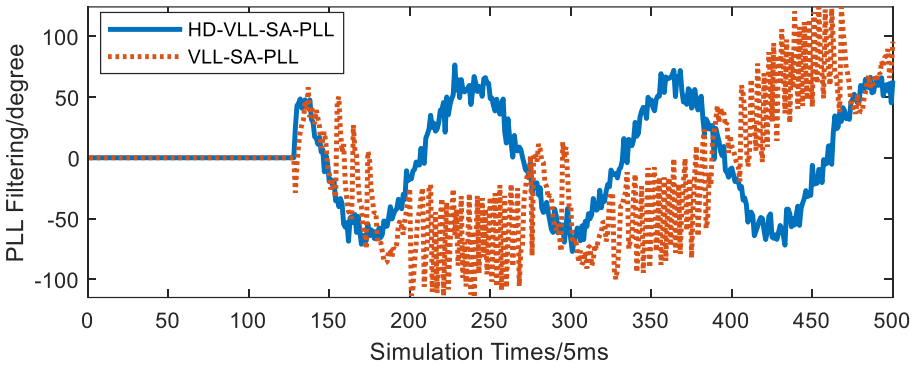


Figure 16. *Cont.*



(**b**)

Figure 16. The PLL tracking results of the HD-VLL-SA-PLL and VLL-SA-PLL. (**a**) The PLL discrimination curves. (**b**) The PLL filtering curves.

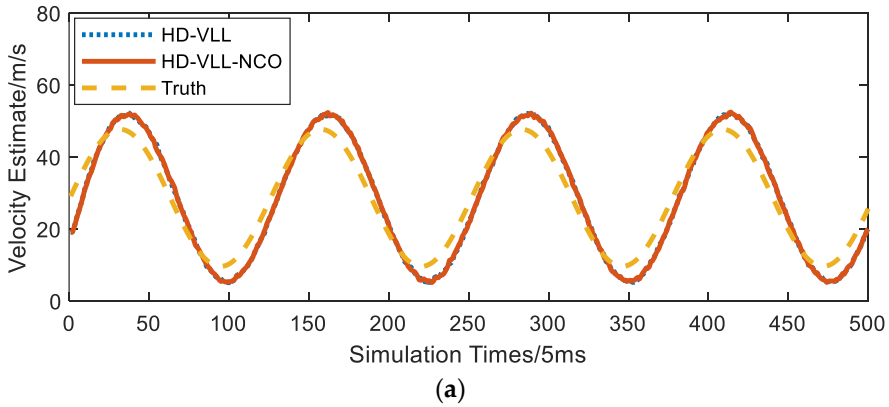
It can be seen that the PLL cannot lock in the VLL-SA-PLL structure, whereas in the HD-VLL-SA-PLL structure, the PLL maintains steady-state tracking. Therefore, the tracking performance of the PLL in the HD-VLL-SA-PLL structure is superior to that in the VLL-SA-PLL structure under high dynamic conditions.

4.5. Comparison of HD-VLL-NCO and HD-VLL

The HD-VLL-NCO is presented for the implementation of the HD-VLL, as discussed in Section 3.3. To demonstrate the effectiveness of the HD-VLL-NCO, the HD-VLL and HD-VLL-NCO are simulated and compared.

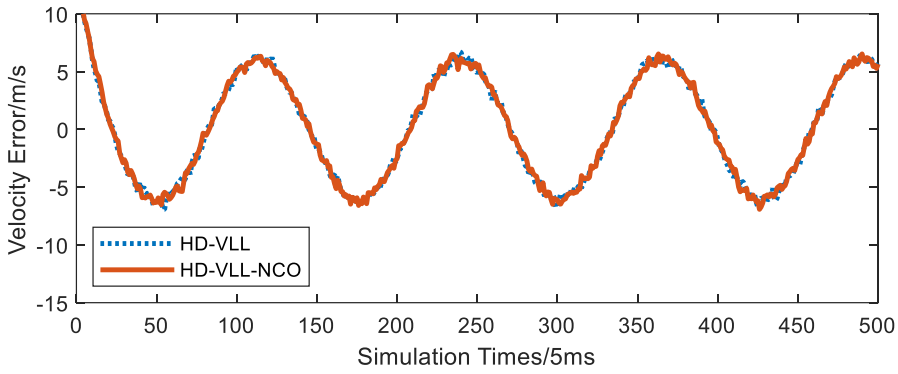
The same sinusoidal motion parameters as those used in Section 4.1 are assumed, and a bandwidth of 5 Hz is adopted. The sampling frequency f_s is 17 MHz, the lookup table bit width N_0 is 12, the velocity resolution Δv_d is 0.001 m/s, the acceleration resolution Δa is 0.1 m/s^2, and the jerk resolution $\Delta \dot{a}$ is 1 m/s^3. Hence, according to (25), the truncation widths c_0, c_1, and c_2 are set as 20, 17, and 21, respectively. The velocity estimate curves and velocity error curves of the two structures are shown in Figure 17.

It can be seen that the HD-VLL-NCO has almost the same tracking results as the HD-VLL. Therefore, in order to preserve the multiplexing of the filter module, the HD-VLL-NCO can be adopted in practical engineering implementation, and the accuracy requirement can be realized by setting appropriate truncation widths.



(**a**)

Figure 17. *Cont.*



(**b**)

Figure 17. The tracking results of the HD-VLL-NCO and HD-VLL (5 Hz). (**a**) The velocity estimate curves. (**b**) The velocity error curves.

4.6. Application Discussion

In this paper, we propose two improved VLL design methods: an HD-VLL based on the loop filter and an HD-VLL-NCO based on NCO. Through a series of simulation experiments, we verified that these two improved VLLs exhibit significant advantages in terms of dynamic adaptability compared to traditional VLL loops. In practical applications, when hardware implementation requires support for multi-channel time division multiplexing, HD-VLL-NCO provides a feasible solution. By setting the bit width and parameters appropriately, the HD-VLL-NCO can support time division multiplexing for loop filter implementation while maintaining signal tracking accuracy, thereby reducing the complexity and cost of hardware implementation. Depending on the specific application requirements, we can reasonably select either of these two loops, as they can both significantly enhance the tracking performance of DS/FH hybrid spread spectrum signals in high dynamic environments.

5. Conclusions

The VLL loop filter only processes velocity and is insensitive to acceleration and jerk, which leads to the difficulty of maintaining steady-state tracking in high dynamic conditions. Therefore, after analyzing the accumulated phase tracking error generated by acceleration and jerk, the HD-VLL is proposed in this paper. The HD-VLL loop filter adds an acceleration compensation module and a jerk compensation module to the VLL loop filter, which compensates the phase variation generated by acceleration and jerk with the system clock. As for the engineering implementation, the HD-VLL-NCO is presented. The formula of each order of the frequency word and the bit width selection scheme are derived. The simulation results show that, compared with the VLL, the HD-VLL has better dynamic adaptability and steady-state tracking performance, and by setting appropriate truncation widths, the HD-VLL-NCO can achieve comparable performance to the HD-VLL. Specifically, the research results of this paper will provide technology support for frequency agile radar applications.

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Data Availability Statement: The data are available from the corresponding author upon reasonable request. The data are not publicly available due to the fact that there are still graduate students using them for research.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

DS/FH	direct sequence/frequency hopping
DSSS	direct sequence spread spectrum
FHSS	frequency hopping spread spectrum
TT&C	telemetry, tracking, and command
SNR	signal-to-noise ratio
DS/FFH	direct sequence/fast frequency hopping
VLL	velocity locked loop
FLL	frequency locked loop
PLL	phase locked loop
HD-VLL	high dynamic VLL
HD-VLL-NCO	HD-VLL based on multi-carrier NCO
DLL	delay locked loop
VLL-SA-PLL	VLL serially assisted PLL
VLL-PA-PLL	VLL parallelly assisted PLL
DDS	direct digital synthesis
HD-VLL-SA-PLL	HD-VLL serially assisted PLL
CNR	carrier-to-noise ratio

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