

Article

An Optimized Fault-Ride-Through Control Strategy of Hybrid MMC with Fewer FBSMs

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Abstract: The modular multilevel converter (MMC) has many advantages of low switching losses, good harmonic performance and high modularity structure in state-of-the-art HVDC applications. The full-bridge submodules (FBSMs) of the hybrid MMC can inherently output negative voltage to absorb fault currents, and consequently the hybrid MMC can ride through severe DC faults without blocking. During the DC fault-ride-through process, the submodule capacitor voltage and arm current of the MMC will be temporarily increased. These characteristics limit the proportion of the FBSMs, which should not be too low and thus increase the cost and operating losses of the hybrid MMC. In this paper, an improved sorting algorithm of SM capacitor voltage is established, and a novel virtual damping control strategy is proposed that can effectively suppress the increase in submodule capacitor voltage and arm current of the hybrid MMC during the DC fault-ride-through process. By adopting this optimization control, the proportion of FBSMs can be reduced significantly without deteriorating the fault-ride-through capability or safety of the MMC. The effectiveness of the proposed control is verified by careful theoretical analysis and detailed simulation results.

Keywords: hybrid MMC; fault-ride-through; DC fault; sorting algorithm; virtual damping



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1. Introduction

The transmission and integration of large-scale renewable energy is a global challenge, and high-voltage flexible DC transmission technology serves as a powerful tool in addressing the difficulties of sending and accommodating large-scale renewable energy [1–3]. The modular multilevel converter (MMC), with its modular structure and strong scalability, is better suited for high-voltage DC transmission scenarios. Additionally, it offers advantages such as excellent output harmonic quality and lower switching losses, making it widely applicable in large-scale renewable energy transmission systems [4–7].

In scenarios involving large-scale onshore integration of new energy sources over long distances, overhead-line flexible DC transmission systems are commonly used for energy export. However, this method is susceptible to geographical factors such as terrain and climate, increasing the probability of DC line faults, especially due to lightning strikes. Handling DC faults in the current context represents a significant technical challenge in the field of flexible DC transmission [8]. For the MMC with half-bridge submodules, it lacks the capability to handle DC faults and can only rapidly suppress the faulty current by configuring a DC circuit breaker (DCCB). However, the DC circuit breaker contains a significant number of electronic power components, making it quite expensive [9,10]. For the MMC with full-bridge submodule, it can block the submodules and utilize the negative

voltage output capability of the full-bridge submodules to absorb the fault current when a AC fault occurs. However, due to submodule blocking during the fault, it renders the MMC incapable of effectively supporting the AC grid during DC faults [11,12]. In order to enable the MMC to effectively support the AC grid during DC faults, numerous studies have investigated non-blocking fault-ride-through control strategies for MMCs [13–15]. By carefully controlling the activation of full-bridge submodules during DC faults, it is possible to clear the fault current and simultaneously provide reactive power support to the AC grid.

During an MMC's fault-ride-through period, the capacitor voltage in the full-bridge submodules increases and the arm currents also rise, posing a threat to the MMC's operating safety [16–18]. To ensure good fault-ride-through capability and safety, the matching of full-bridge submodules should not be too low [19,20]. In [21], the operating mechanism of hybrid MMC under DC fault is explained, and the characteristics of submodule capacitor voltages and fault current during fault ride through are analyzed in detail, but it does not present a detailed optimization control strategy. In [22], an adaptive fault current limiting control is proposed to suppress fault currents. However, the adaptive fault current limiting control can trigger quickly after a fault occurs and does not rely on fault detection. In [23], a virtual reactor control strategy is developed to replace the reactor in HVDC systems, which can effectively limit fault currents. However, the article only analyzed its application in the half-bridge MMC and did not integrate it with non-blocking fault-ride-through control for analysis. In [24,25], the topology of hybrid MMCs is improved to ensure that hybrid MMCs with a low proportion of full-bridge submodules can safely ride through DC faults. The effective suppression of fault currents and the increase in submodule capacitor voltage during DC fault ride through is a critical aspect in reducing the proportion of full-bridge submodules and holds significant research value.

In this paper, the mechanism of fault currents of MMCs developing during DC faults is analyzed. Based on the characteristics of fault currents and submodule capacitor voltage changes during faults, an optimized control strategy is proposed in addition to the non-blocking fault-ride-through control. This strategy includes improvements in sorting algorithms and the introduction of virtual damping control. The proposed approach effectively suppresses fault currents during fault ride through, reducing peak values of bridge arm currents and submodule capacitor voltage of MMCs. This makes the practical implementation of hybrid MMCs with a lower proportion of full-bridge submodules more achievable and thus significantly reduces the investment and operating losses of MMCs.

2. The Non-Blocking Fault-Ride-Through Control of MMC

Figure 1 shows the main circuit of a hybrid MMC. There are in total three phases and six bridge arms in one MMC. Each bridge arm consists of N submodules, which include both full-bridge submodules and half-bridge submodules. U_{dc} represents the DC voltage of the MMC, while I_{dc} is the current on the DC side and u_j and i_j ($j = a, b, c$) are the phase voltage and phase current of the AC grid, respectively. L_t and L_m represent the transformer leakage inductance and MMC bridge arm inductance, respectively.

The full-bridge submodules can generate negative voltage during a DC fault to absorb the fault current, thereby achieving a rapid fault clearance. Non-blocking fault-ride-through control is achieved by controlling the full-bridge submodules during a DC fault. Figure 2 shows the overall structure of the non-blocking fault-ride-through control strategy.

The core of the non-blocking fault-ride-through control strategy is the utilization of the full-bridge submodules' ability to generate negative voltage, allowing for a controlled variation in DC voltage within a certain range. Compared to traditional control algorithms, the main differences in non-blocking fault-ride-through control are as follows.

(1) The active current loop reference value is determined by the submodule average capacitor voltage loop, directly controlling the average submodule capacitor voltage. This is because during fault ride through, the submodule capacitor voltage needs to be maintained near its rated value to support the AC grid with reactive power.

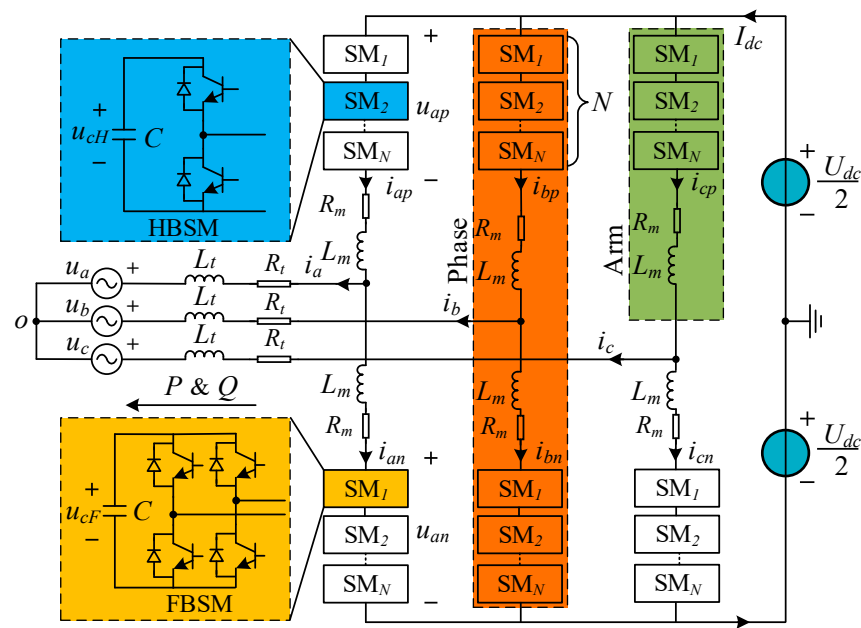


Figure 1. Diagram of the hybrid MMC.

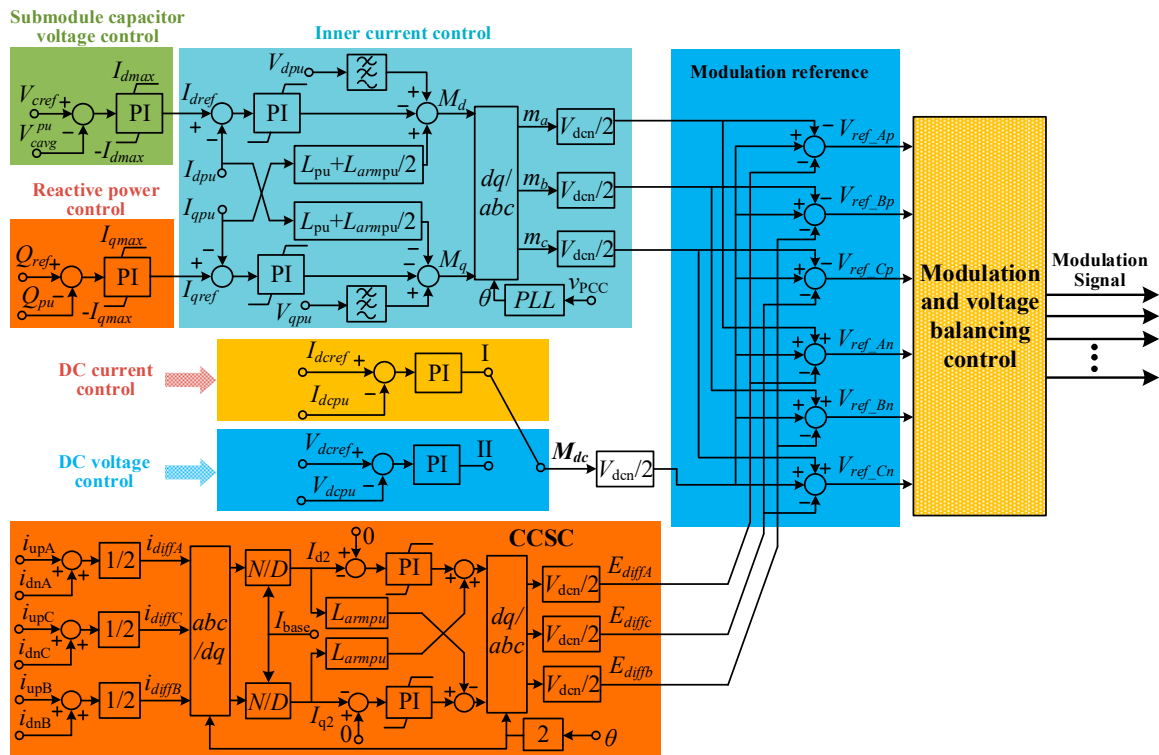


Figure 2. The overall structure of non-blocking fault-ride-through control of MMC.

(2) Depending on whether the converter station is required to control voltage or power, a DC voltage control loop or a DC current control loop is introduced to generate the DC modulation ratio M_{dc} command. Under normal operating conditions, one end of the multi-terminal converter system selects DC voltage outer loop control, while the rest of the ends opt for DC current outer loop control, with a reference value of 1 per unit (1 p.u.). During the DC fault-ride-through period, all of the multi-terminal converter systems choose the DC current outer loop control, and the reference value for all ends is set to 0 per unit (0 p.u.).

In steady-state operating conditions, taking phase A as an example, the output voltage of the MMC bridge arms can be expressed as:

$$\begin{cases} u_{ap} = M_{dc} \frac{V_{dcn}}{2} - M_{ac} \frac{V_{dcn}}{2} \sin \omega t \\ u_{an} = M_{dc} \frac{V_{dcn}}{2} + M_{ac} \frac{V_{dcn}}{2} \sin \omega t \end{cases} \quad (1)$$

M_{dc} represents the modulation ratio of DC voltage, while M_{ac} represents the modulation ratio of AC voltage. When a DC fault is detected, the DC voltage outer loop switches to the DC current outer loop, and the reference value for the DC current outer loop is set to 0. Then, the M_{dc} rapidly decays to 0, and during the DC fault-ride-through period, the bridge arm voltages can be expressed as:

$$\begin{cases} u_{ap} = -M_{ac} \frac{V_{dcn}}{2} \sin \omega t \\ u_{an} = M_{ac} \frac{V_{dcn}}{2} \sin \omega t \end{cases} \quad (2)$$

Considering that only the full-bridge submodules can output negative voltage during the fault-ride-through period, in order to meet the supporting requirements for the AC grid during the DC fault-ride-through period, the output voltage of full-bridge submodules should satisfy the following relationship:

$$N_F U_c \geq M_{ac} \frac{V_{dcn}}{2} \quad (3)$$

Typically, to ensure that the hybrid MMC can successfully achieve non-block fault-ride-through function, the average capacitor voltage of the MMC's submodules (U_c) is controlled to be V_{dcn}/N . As such, the number of full-bridge submodules (N_F) should satisfy:

$$N_F \geq M_{ac} \frac{N}{2} \quad (4)$$

Obviously, when the number of full-bridge submodules N_F is not less than $N/2$, it ensures that the MMC can effectively support the power grid during a fault-ride-through period [22]. The existing project used a hybrid MMC with a 70% full-bridge ratio [26].

Even though M_{dc} can rapidly drop to 0 after a DC fault occurs, it is not initially at 0 when the fault happens. Let us analyze this with an example of the DC current control station. In the early stages of a DC fault, the fault current rapidly increases.

Setting the DC current reference value to 0 results in the difference between the reference and the actual DC current being negative. Under the influence of the PI controller, a negative M_{dc} is output. During this time, the equivalent DC-side circuit is shown in Figure 3.

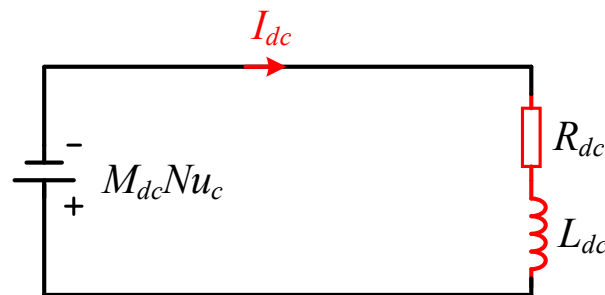


Figure 3. Equivalent DC-side circuit.

In Figure 3, R_{dc} and L_{dc} represent the equivalent resistance and inductance on the DC side respectively, and u_c represents the submodule capacitor voltage. It can be observed that in the early stages of a DC fault, the DC-side output voltage is less than 0, equivalent to charging the submodules with the fault current in the MMC, and thus it can rapidly attenuate the fault current to 0. It should be noted that because of the equivalent inductor L_{dc} in the loop, the current I_{dc} cannot change direction in a short period, even with a negative DC voltage provided by $M_{dc}Nu_c$.

3. Optimized Fault-Ride-Through Control Strategy

In this section, an optimized fault-ride-through control strategy is proposed. It combines optimization of sorting algorithms and virtual damping control, effectively suppressing the growth in fault current and reducing the peak value of the bridge arm current and the submodule capacitor voltage at the same time during the period of fault ride through.

3.1. Optimized Sorting Algorithm

In the early stages of a DC fault, the DC side's equivalent circuit can be represented by Figure 4, which clearly illustrates the relationship between the submodule insertion on the upper and lower arms of the MMC and the fault current.

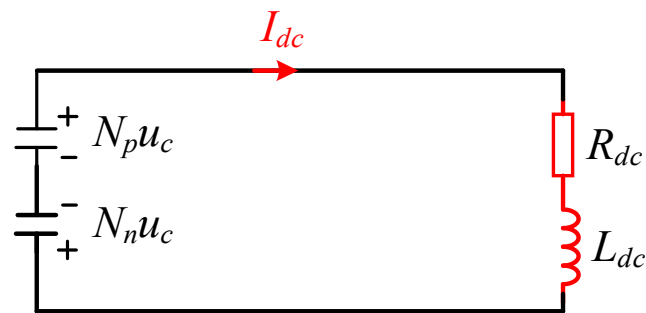


Figure 4. Equivalent DC-side circuit in the early stages of a DC fault.

In Figure 4, N_p and N_n represent the number of submodules inserted on the upper and lower arms, respectively. The diagram only shows the case where submodules on the upper arm generate a positive voltage, while the submodules on the lower arm generate a negative voltage. It is evident that the DC fault current will discharge the submodules producing positive voltage, but charge the submodules generating negative voltage. Since only full-bridge submodules are inserted during the fault, the charging current will cause an increase in the capacitor voltage of submodules.

In conventional non-block fault-ride-through control, the half-bridge submodules are blocked during the fault ride through and only the full-bridge submodules are inserted. However, in this article, the strategy selectively inserts half-bridge submodules during the fault when the bridge arm output voltage reference is greater than 0, as well as when the bridge arm current charges the half-bridge submodules. By utilizing half-bridge submodules to absorb a portion of the charging current, it effectively reduces the peak capacitor voltage of the full-bridge submodules.

To achieve selective insertion of half-bridge submodules, improvements were made to the sorting algorithm, as shown in Figure 5. The optimized sorting algorithm enables selective insertion of half-bridge submodules during a DC fault to absorb charging current without affecting the normal operation of the MMC in steady-state conditions.

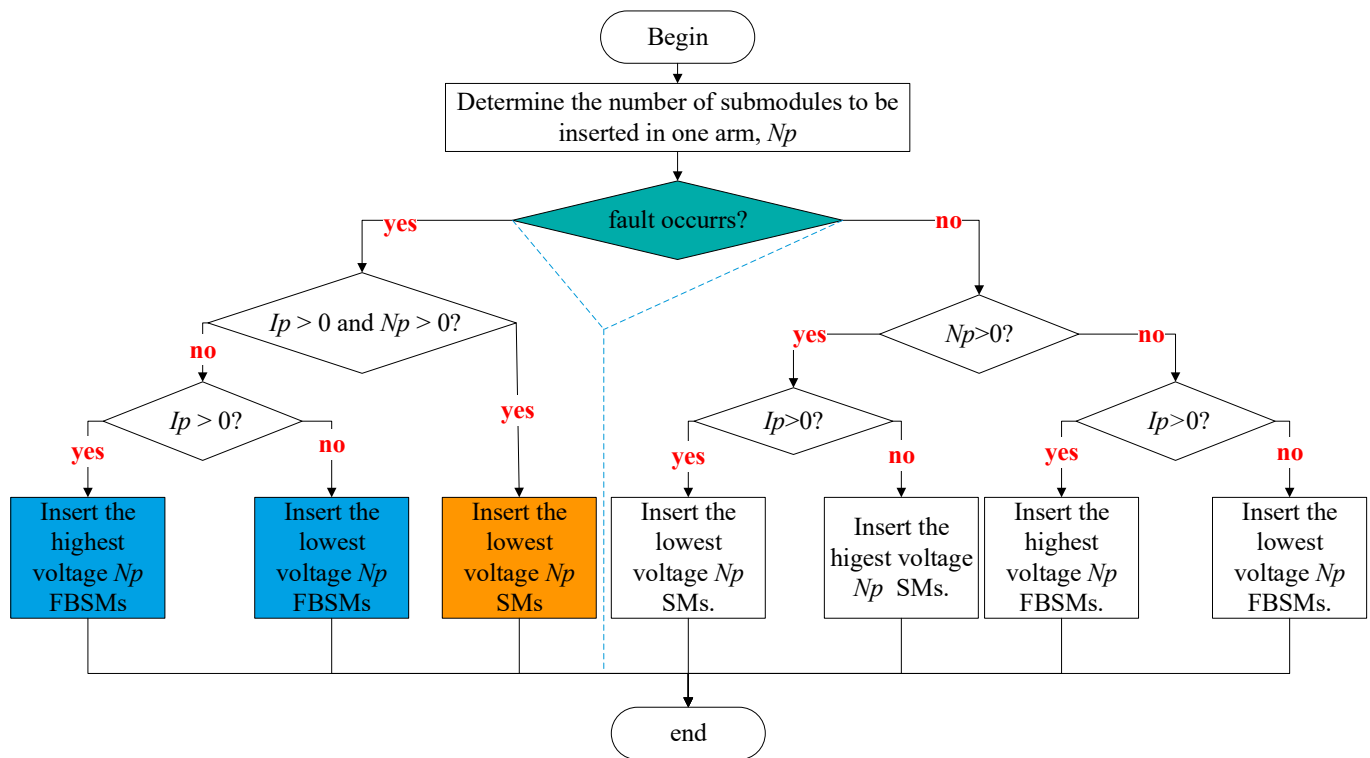


Figure 5. Block diagram of the optimized sorting algorithm.

3.2. Virtual DC Damping Control

The bridge arm current flows through the IGBTs of the submodules, and when it becomes excessively high, it can lead to IGBT breakdown, posing a threat to the safe operation of the MMC. Taking phase A as an example, the currents in the upper and lower arms can be expressed as:

$$\begin{cases} i_{ap} = \frac{I_{dc}}{3} + \frac{I_m}{2} \sin(\omega t - \varphi) \\ i_{an} = \frac{I_{dc}}{3} - \frac{I_m}{2} \sin(\omega t - \varphi) \end{cases} \quad (5)$$

where I_m and φ represent the amplitude and angle of the AC current, respectively. When a DC fault occurs, the DC current rapidly increases, causing the bridge arm current also to increase quickly, which may lead to IGBT breakdown. Therefore, suppressing the development of the DC-side fault current can effectively reduce the peak fault current.

In a practical project, it takes 3–5 ms from the occurrence of a DC fault to the detection of the fault and the change in a control strategy. During this period (3–5 ms), the steady-state control strategy is unable to suppress the fault current, leading to a rapid increase in fault current. This paper proposes a virtual damping control in both the current control station and DC voltage control station to effectively suppress the fault current. The control structures are illustrated in Figures 6 and 7, respectively.

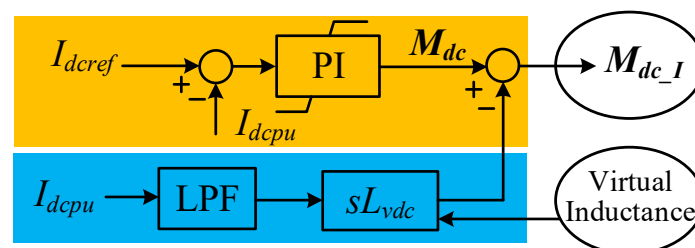


Figure 6. Structure of virtual DC damping control of current control station.

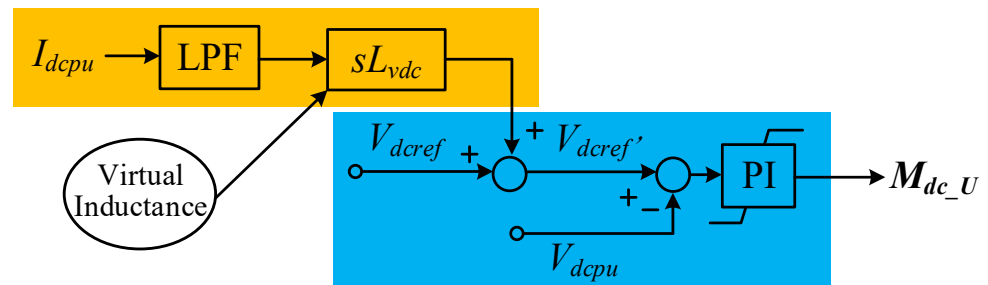


Figure 7. Structure of virtual DC damping control of voltage control station.

Virtual DC damping control improves the DC current control loop by introducing a feedforward element, where LPF represents a low-pass filter and L_{vdc} represents a virtual inductance. With the addition of virtual damping, the expression for DC modulation ratio can be expressed as follows.

$$M_{dc_I} = M_{dc} - L_{vdc} \frac{dI_{dcpu}}{dt} \quad (6)$$

From Equation (4), it can be seen that after a DC fault occurs, the DC current rapidly increases, and the virtual damping element causes a reduction in the output DC modulation ratio. As discussed earlier, a positive DC modulation ratio during a DC fault causes the MMC submodules to discharge, leading to a rapid increase in fault current. The presence of virtual damping ensures that the DC modulation ratio rapidly decays to 0 after a DC fault occurs, thereby suppressing the development of the fault current.

For the voltage control station, virtual damping is introduced into the DC voltage control loop, which modifies the DC voltage reference value. With the addition of virtual damping, the expression for the DC modulation ratio can be expressed as:

$$M_{dc_U} = \left(V_{dcref} + L_{vdc} \frac{dI_{dcpu}}{dt} - V_{dcpu} \right) \left(k_p + \frac{k_i}{s} \right) \quad (7)$$

When selecting the receiving converter station as the voltage control station, after a DC fault occurs, the DC current will decrease to zero before reversing and increasing. Consequently, when a fault occurs, the fault current at the receiving converter station suddenly decreases. Under the influence of virtual damping, the DC voltage reference value in the DC voltage control loop decreases, causing a decrease in the output of the PI controller for the DC modulation ratio. This leads to a reduction in the number of activated submodules, thereby suppressing the development of fault currents.

The derivation component ensures that virtual damping only comes into effect when a fault occurs (when there is a sudden change in DC current), and it does not impact the steady-state operation of the MMC.

Actually, the addition of virtual DC damping is equivalent to introducing an inductor into the circuit, as shown in Figure 8. The virtual DC damping control can increase the equivalent inductance on the DC side without adding the physical inductor, thereby preventing an increase in converter costs. In addition, virtual damping control allows for flexible adjustment of the DC-side equivalent inductance through a controller, and is more convenient than adding the physical inductor.

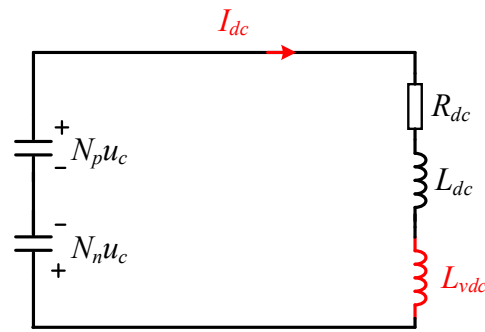


Figure 8. Equivalent DC-side circuit with the addition of virtual DC damping.

3.3. Virtual AC Damping Control

In a multi-terminal DC transmission system, the sending converter station transmits power from the AC side through the DC transmission line. When a DC fault happens, the DC side is unable to transmit power, so the power of DC (P_{dc}) side drops to 0 rapidly, but the power of the AC side (P_{ac}) cannot change quickly. The relationship between AC-side power P_{ac} and DC-side power P_{dc} can be expressed as:

$$P_{ac} - P_{dc} = \frac{d}{dt} \left(\frac{C}{2N} u_{c_avg}^2 \right) \quad (8)$$

where u_{c_avg} represents the average voltage of submodules in the MMC. Obviously, the sudden drop in P_{dc} will result in a power imbalance between the DC side and AC side, causing an increase in the capacitor voltage of submodules.

According to Equation (8), if the AC-side power P_{ac} drops rapidly, the capacitor voltage of submodules will not increase too much. As such, the virtual AC damping control is applied to depress the increase in capacitor voltage after the occurrence of a DC fault. The structure of virtual AC damping control is illustrated in Figure 9, and it is only applied for sending to the converter station.

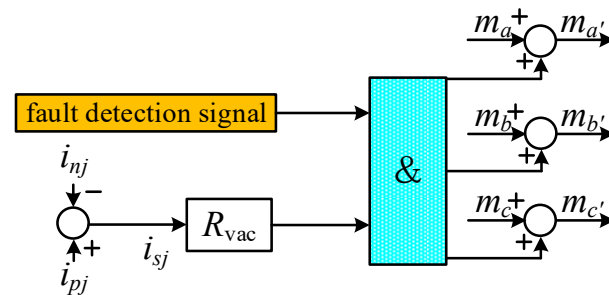


Figure 9. Structure of virtual AC damping control.

The virtual AC damping changes the AC modulation index of the MMC, thereby influencing the AC output voltage of the MMC. The AC modulation index of the MMC after the introduction of virtual damping R_{vac} can be expressed as:

$$m_a' = m_a + i_{sa} R_{vac} \quad (9)$$

As virtual AC damping affects the modulation index of the MMC under steady-state conditions, it is only engaged after a fault is detected. With the fault detection, virtual AC damping will be applied and alter the output electromotive force of the MMC, thereby reducing energy injection from the AC side into the MMC during the fault.

Actually, the addition of virtual AC damping is equivalent to introducing a resistor R_{vac} into the circuit, as illustrated in Figure 10. The virtual AC damping control can increase the equivalent resistance on the AC side, which will reduce the energy injection from the

AC side. As a result, the peak values of bridge arm currents and capacitor voltages during the fault-ride-through period can be effectively reduced at the sending converter station.

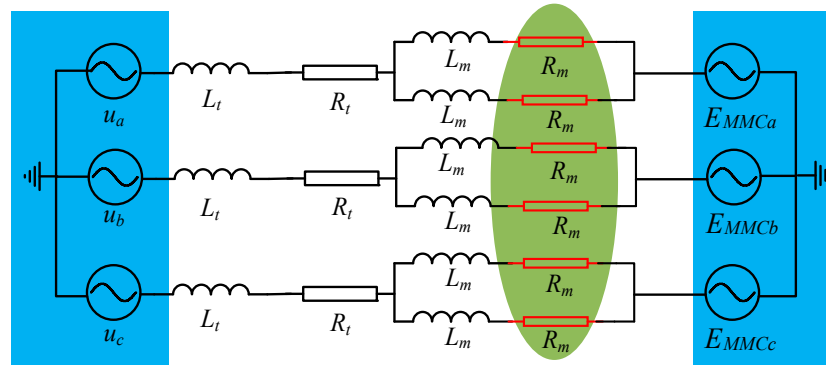


Figure 10. Equivalent AC-side circuit with the addition of virtual AC damping.

Generally speaking, the proposed control combines the optimized sorting algorithm, virtual DC damping control, and virtual AC damping control to suppress the increase in submodule capacitor voltage and arm current of the hybrid MMC during the DC fault-ride-through process.

4. Simulation Verification

In this section, a simulation using MATLAB/Simulink 2021b is detailed to verify the proposed optimized fault-ride-through control strategy. The simulation was set up for a two-terminal HVDC transmission system, with one terminal serving as a voltage control station, using DC voltage control under steady-state conditions. The other terminal served as a current control station, employing DC current control in steady-state conditions. The parameters for the two MMC stations in the simulation are the same. Simulation parameters are given in Table 1. Considering the proposed control is only used in the fault-ride-through process of MMC-HVDC, it has exactly the same control performance for the active and reactive as the conventional one, because: (1) the control algorithms in normal operating conditions for both the proposed control and the conventional control are the same; and (2) in normal operating conditions, all the full-bridge SMs are used as half-bridge SMs, and thus the ratio has no impact on active or reactive power control performance.

Table 1. Main circuit parameters.

Items	Values
Fundamental frequency f	50 Hz
Rated capacity S_{rated}	500 MW
Rated line voltage (rms)	186 kV
DC-side voltage U_{dc}	320 kV
SM capacitance C	16 mF
Arm inductance L_m	30 mH
Rated capacitor voltage	2105 V
Number of submodules per arm N	152
Number of FBSMs per arm N_f	76
Number of HBSMs per arm N_h	76

In the simulation, a DC bipolar-to-ground fault occurs at 1 s. The fault was detected 3 ms after the occurrence, and then the control strategy was switched on.

Considering only a 50% full-bridge SM is used in the proposed control, the efficiency of the proposed control in a steady state is improved by about 10% compared with the conventional one (different IGBT devices may have slightly different results). In the simulation, the peak DC current is compared under different control strategies. In order to validate whether the

optimized control strategy can effectively suppress the development of a DC fault current, simulation analysis is conducted on the DC fault currents for both the current control station and the voltage control station. The results are shown in Figures 11 and 12, respectively.

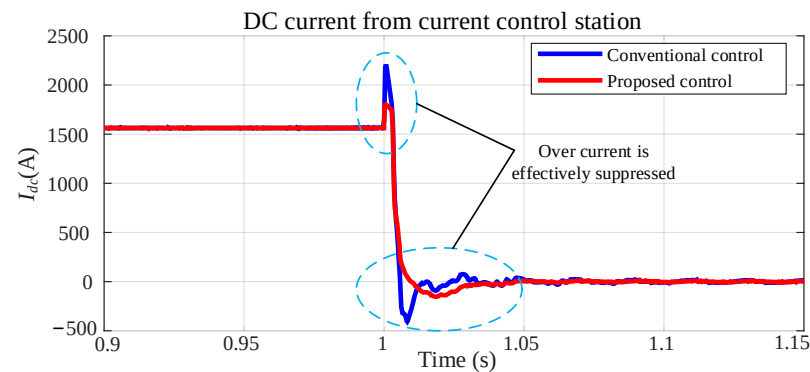


Figure 11. Comparison of DC fault currents from current control station under different control strategies.

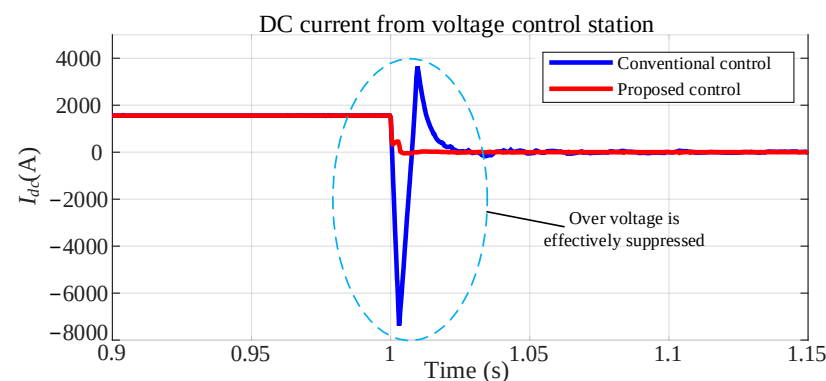


Figure 12. Comparison of DC fault currents from voltage control station under different control strategies.

From the simulation results in Figure 11, it can be observed that the DC current rapidly increases after the fault occurs. Under steady-state conditions, the DC-side current is 1560 A. In the case of the traditional control, the peak DC fault current reaches 2238 A and the maximum bridge arm current is 2762 A. Under the proposed optimized control, the peak DC fault current is 1815 A and the maximum bridge arm current is 2370 A. Furthermore, the DC current decays more rapidly to 0 under optimized control.

In Figure 12, the DC current rapidly decreases after the fault occurs in the voltage control station. In the case of the traditional control, the fault current firstly decreases to 0 and then increases, the absolute value of the fault current reaches 7380 A, and the maximum bridge arm current is 3740 A. Under optimized control, the DC current decays to 0 rapidly, and the maximum bridge arm current is 2150 A.

The simulation results of the voltage control station and the current control station confirm that the optimized control strategy can effectively suppress the development of the fault current, thus reducing the peak value of arm current, which is very important for stable operation of the hybrid MMC.

To verify the effectiveness of the optimized control strategy in reducing the peak capacitor voltage during the fault-ride-through process, detailed simulations were performed to compare the capacitor voltages during fault ride through under different control strategies for both the current control station and the voltage control station. The results are shown in Figure 13, Figure 14, Figure 15, and Figure 16, respectively.

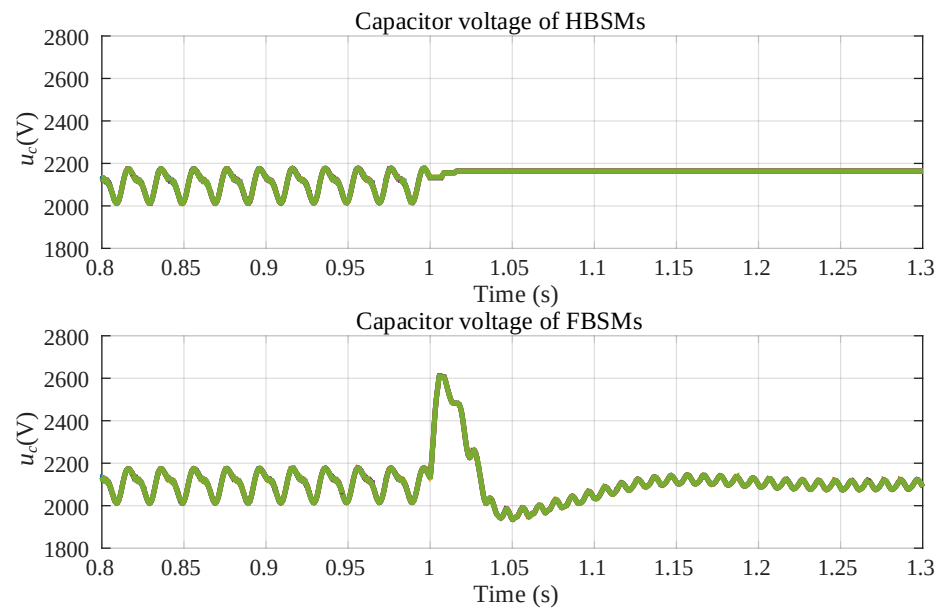


Figure 13. Capacitor voltage under optimized control in current control station.

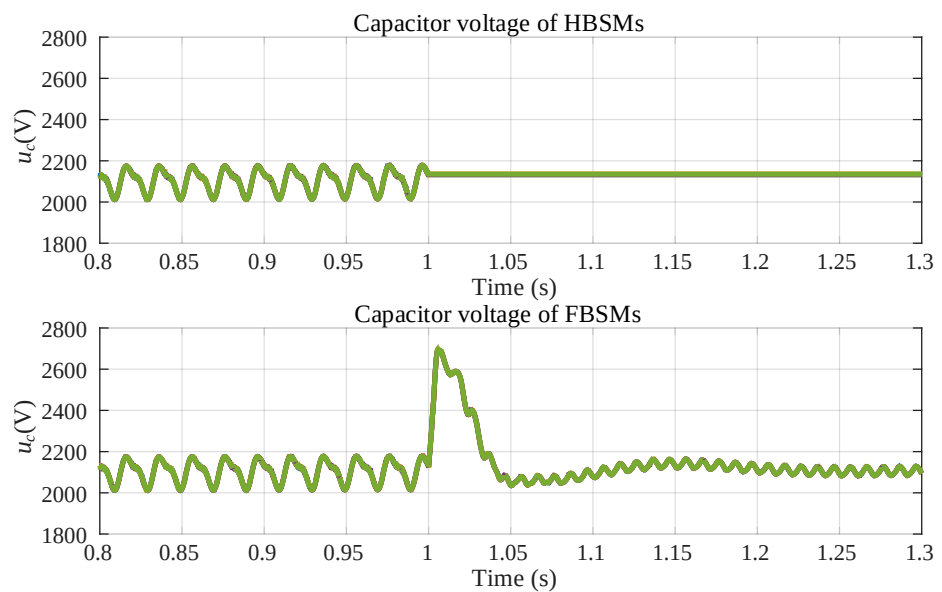


Figure 14. Capacitor voltage under conventional control in current control station.

Both Figures 13 and 14 depict the capacitor voltages of the half-bridge submodules and the full-bridge submodules under a DC fault. The peak capacitor voltage of the full-bridge submodules under optimized control is 2610 V, while under traditional control, it reaches 2713 V. The simulation results demonstrate that optimized control can reduce the peak capacitor voltage of the full-bridge submodules in the current control station under a DC fault, which can ensure safe operation with possibly fewer half-bridge submodules in the hybrid MMC.

In Figures 15 and 16, it can be observed that under the optimized fault-ride-through control strategy, the capacitor voltage at the receiving converter station is significantly reduced during the fault-ride-through process. Under the conventional control strategy, the peak submodule capacitor voltage reaches 2910 V. However, under the optimized control strategy, the capacitor voltage peak is reduced to 2503 V.

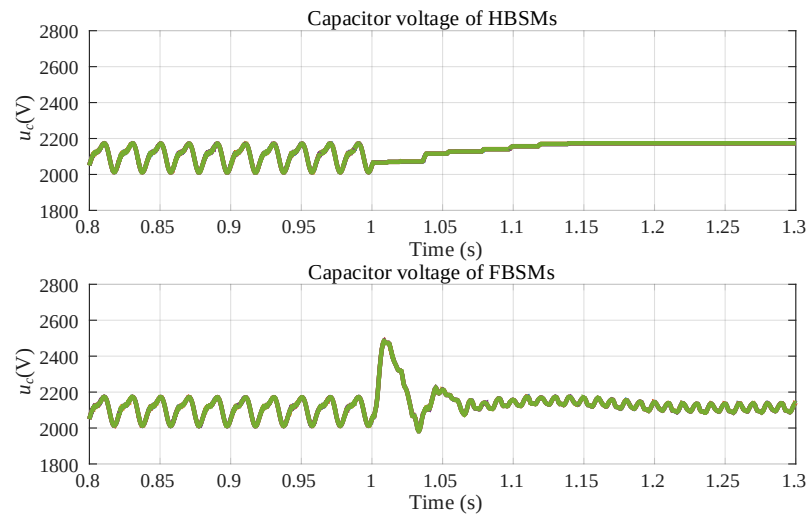


Figure 15. Capacitor voltage under optimized control in voltage control station.

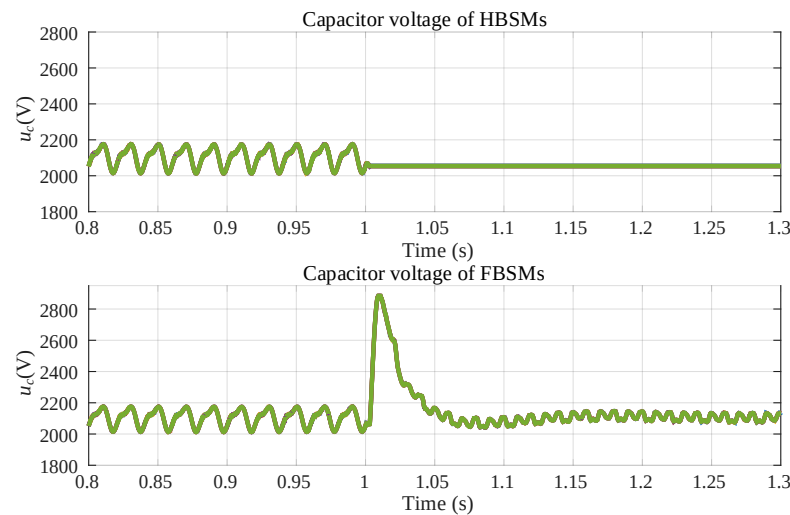


Figure 16. Capacitor voltage under conventional control in voltage control station.

These simulation results of the voltage control station and the current control station verify that the optimized fault-ride-through control strategy effectively reduces the peak submodule capacitor voltage during the fault-ride-through process.

Figures 17 and 18 illustrate the waveforms of AC current, power, and DC voltage during the fault-ride-through period for both the current control station and the voltage control station under the optimized control strategy.

The DC fault occurs at 1 s, is completely cleared by 1.3 s, then the system begins to recover and operate under steady-state conditions. Under steady-state operating conditions, the active power command value for the current control station is set to 1 p.u. and the reactive power command value is set to 0 p.u., while for the voltage control station, the voltage command value is set to 1 p.u. and the reactive power command value is set to 0 p.u. In the fault ride-through-period, both the active power command value and the DC voltage command value are set to 0 p.u. Additionally, the reactive power command value for both the current control station and the voltage control station is set to 0.3 p.u. to provide reliable support to the AC grid.

In Figures 17 and 18, it can be observed that after the fault occurs, the DC voltage rapidly drops, the AC current decreases, and the MMC outputs reactive power to support the AC grid at the same time. After the clearance of the DC fault, the DC voltage can quickly be rebuilt, allowing the sending converter station to resume active power output to a steady-state rated value in a short period. Generally speaking, under optimized control, the MMC

can safely and effectively achieve non-blocking fault ride through, swiftly clearing DC faults and rapidly restoring the operational state prior to the fault.

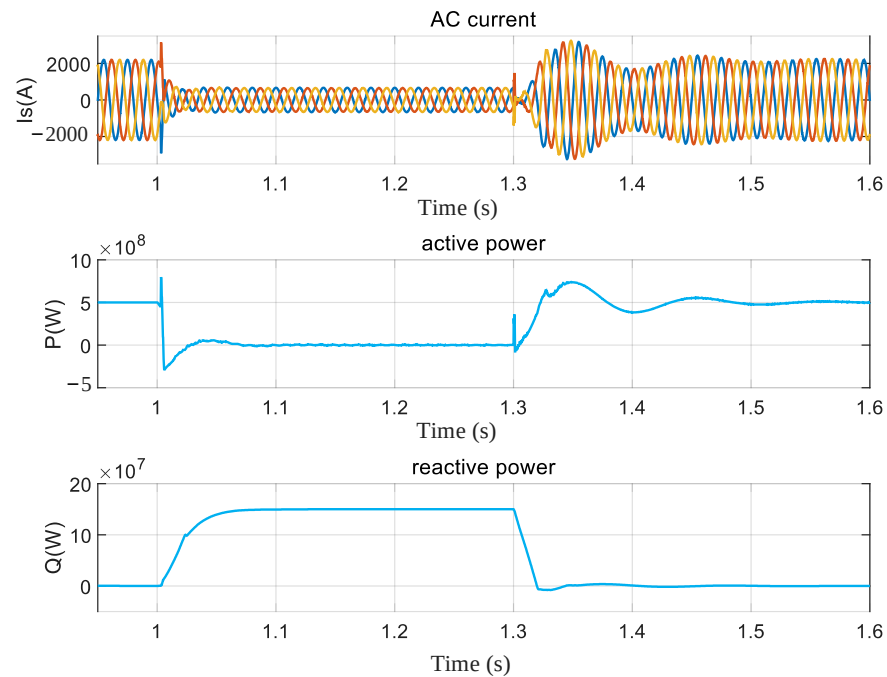


Figure 17. AC current, active power, and reactive power of current control station.

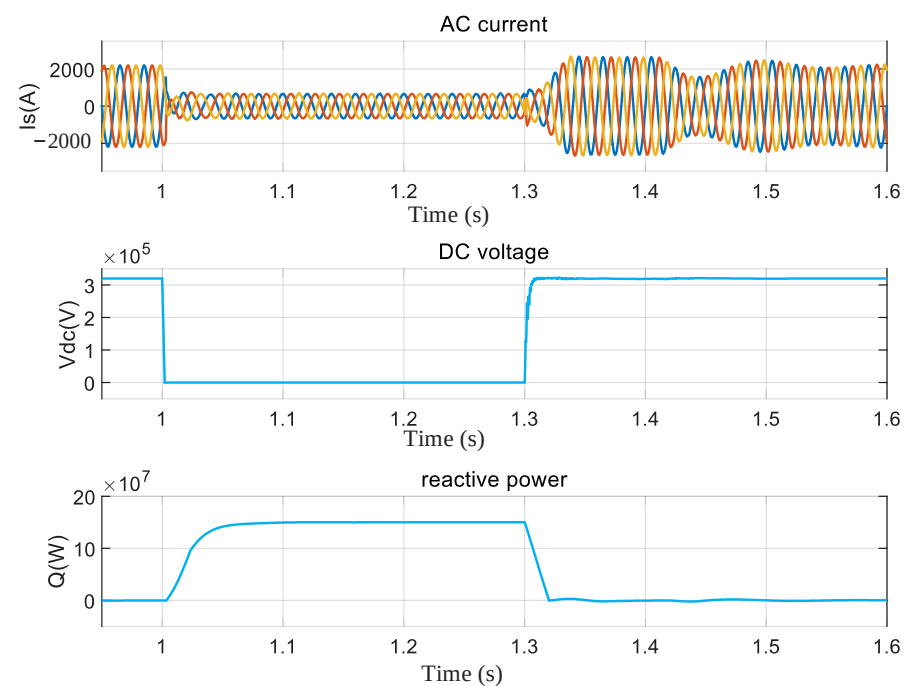


Figure 18. AC current, DC voltage, and reactive power of voltage control station.

The simulation comparison is between the MMC with 70% full-bridge ratio using conventional fault-ride-through control and the MMC with 50% full-bridge ratio configuration using optimized control. Taking the current control station as an example, Table 2 provides a comparison of the peak values of fault currents and submodule capacitor voltages during the fault-ride-through period of the hybrid MMC with 70% full-bridge ratio and hybrid MMC with 50% full-bridge ratio.

Table 2. Comparison of two MMCs.

Items	MMC1	MMC2
Peak value of capacitor voltage u_{cmax}	2565 V	2610 V
Peak value of DC current I_{dcmax}	1930 A	1815 A
Max absolute value of arm current I_{pmax}	2443 A	2370 A

In Table 2, MMC1 represents the hybrid MMC with 70% full-bridge ratio under conventional control, while MMC2 is the hybrid MMC with 50% full-bridge ratio under optimized control. Obviously, by adopting optimized control, the MMC with a 50% full-bridge ratio has lower I_{dcmax} and I_{pmax} than the MMC with a 70% full-bridge ratio. In other words, by utilizing the optimized fault-ride-through control, a hybrid MMC with a 50% full-bridge ratio can safely complete a fault ride through such that the full-bridge ratio can be reduced from 70% to 50% without compromising the safety of the fault ride through.

5. Conclusions

This paper analyzed the mechanisms of the increase in bridge arm current and the rise in capacitor voltage of full-bridge submodules in MMCs during a DC fault process. Based on the characteristics of fault current development during a DC fault, an optimized fault-ride-through control strategy was proposed on the basis of non-blocking fault-ride-through control of the hybrid MMC. The optimized fault-ride-through control combines the developed optimized sorting algorithms and the proposed virtual damping control strategy, effectively reducing the peak bridge arm current and capacitor voltage of full-bridge submodules of the hybrid MMC under severe fault conditions. It has the following features compared with the conventional one.

- (1) It has only 50% full-bridge SMs and thus has a higher efficiency (about 10% higher) compared with the existing ones, which are generally 70% full-bridge SMs of the hybrid MMCs.
- (2) It has the same fault-ride-through capability with the conventional high-ratio full-bridge SM hybrid MMC because of the adopt active AC and DC damping control.
- (3) It has a lower cost as well as lower weight and volume because of the fewer full-bridge SMs and thus fewer IGBTs and corresponding derives and auxiliary circuits (about 12% less).

The effectiveness and reliability of the optimized control strategy are effectively verified by various simulation results.

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Conflicts of Interest: Authors Yue Chen and Chenglin Ren were employed by the company EHV Power Transmission Company, China Southern Power Grid Company Limited (CSG); Authors Junyi Sheng, Runtian Ding and Wujun Wang were employed by the company TBEA China Xinjiang Sunoasis Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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