

Article

Self-Frequency Tracking for Fixed-Ratio Switch-Capacitors in Data Center Application without Extra Sensors

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Abstract: As research into data centers progresses, the importance of resonant switched-capacitor converters in power supply design becomes more evident. Practical applications reveal that the values of resonant capacitors and inductors may deviate from their nominal values due to various factors, leading to resonant frequency instability. This instability poses a challenge to power electronics technology, affecting system reliability and performance. This paper analyzes the effect of frequency deviation on system functionality, identifies the relationship between output voltage and switching frequency, and proposes a self-tracking frequency strategy to address this issue. Through experimental validation, this approach shows that it maintains synchronization between switching and resonant frequencies, reducing losses associated with frequency misalignment. Simulation and experimental results validate the converter's stable operation and its ability to achieve zero-voltage and zero-current switching.

Keywords: resonant switched-capacitor converters; self-tracking frequency strategy; zero-voltage and zero-current switching



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1. Introduction

Resonant converters are indispensable in the realm of Point-of-Load (PoL) circuits, serving as the backbone for powering a myriad of devices that are central to modern technology infrastructure. These devices range from expansive data centers that process and store vast amounts of information, to sophisticated artificial intelligence systems that drive innovation and automation, and to personal computers that are integral to daily productivity and connectivity. The significance of resonant converters in these applications lies in their ability to efficiently manage power distribution at the load point, ensuring optimal performance and reliability of the devices they support. This efficiency is particularly critical given the increasing demand for energy conservation and the need to minimize heat generation in densely packed electronic environments [1–4]. For example, the switched-tank converters (STC) proposed by Google [5], switched capacitors (SC) proposed by UCB (University of California Berkeley) [6–10], products from Vicor [11] and Infineon [12], and research from the University of Cambridge exemplify the significant work in this field [13,14]. A core principle for the resonant frequency (f_r) of resonant converters should be aligned with the switching frequency (f_{sw}). However, parameter drifts,

such as the variation in capacitance and inductance, lead to significant fluctuations of f_r . Therefore, identifying the f_{sw} to match the f_r is extremely important.

The primary factors for f_r variation are the capacitance and inductance variations. In [10], the capacitance of the selected resonant capacitors reduced 95.25% at the rated voltage. Moreover, [15] from TDK points out that the permeability of MnZn reduces 23% at $-40\text{ }^\circ\text{C}$ and increases 8.3% at $+85\text{ }^\circ\text{C}$. Therefore, the f_r variation is a critical issue.

Academic research often neglects this issue and only adjusts the f_{sw} with trial and error. However, ref. [9] from UCB carefully selected the capacitors. Although the selected capacitors are Class II capacitors, the capacitance variation is relatively small so the f_r variation can be reduced. However, these variations still exist (although reduced), even though the inductance variations are not considered. Therefore, the f_r still varies.

To mitigate f_r variability, the industry initially preferred high-precision components. For instance, in 2018, Google used Class I capacitors featuring high-precision dielectrics [5]. However, these Class I capacitors exhibit a significantly lower energy density compared to Class II capacitors, leading to increased size and assembly complexity. Recognizing these limitations, in 2022, Google started a transition toward Class II capacitors [16]. The shift toward intelligent control systems, as opposed to relying solely on precise, yet low-energy-density components, has proven to be an effective strategy for reducing costs, size, and complexity in industrial applications.

Besides reducing variations in f_r , Infineon's circuit architecture can tolerate this f_r variation [14] and maintain a considerable efficiency within the f_r variation range. Nevertheless, [10] also points out that the f_r variation can result in an efficiency decrease and thermal increase.

Zero-crossing detection is effective for identifying f_r . However, this technique is sensitive to noise and demands a detection circuit with exceptionally high bandwidth. As a result, its application is limited to low-frequency applications and is rare in resonant converters in SCs or STCs for data center applications.

This manuscript investigates the relationship between output voltage and switching frequency in resonant capacitor conversion circuits, identifying a voltage behavior pattern relative to resonant frequency. The findings indicate that the output voltage increases with a rise in f_{sw} below the resonant frequency, decreases above it, and peaks when frequencies align ($f_r = f_{sw}$). Consequently, a control strategy is proposed, dynamically adjusting switching frequency based on output voltage feedback to optimize output and achieve frequency synchronization. This approach eliminates the need for additional sensors or precision instruments, maintaining effectiveness amidst capacitance and inductance fluctuations due to input voltage variability. Table 1 provides a comparative overview of four strategies for managing resonance frequency deviations in power converters, detailing their methods, effectiveness, advantages, and application considerations. Theoretical analysis and experimental validation confirm the strategy's efficacy in improving power electronic system efficiency and stability. This research provides essential insights for the design and implementation of efficient, reliable resonant conversion circuits.

Table 1. Overview of Strategies for Managing Resonance Frequency Deviations in Power Converters.

Method Name	Advantages	Considerations for Application
Precise Component Matching and Adjustment	Reduces frequency offsets due to component quality, improves stability	Higher costs, requires high-precision or adjustable components
Control Strategy Optimization	Enhances efficiency, optimizes performance	Complex control systems, requires precise control and algorithm development
Adaptive Control	Fast response, automatically adjusts, strong adaptability	Complex design, increased costs
Soft Switching Techniques and Circuit Optimization	Increases efficiency, reduces losses	Design and implementation are challenging
Monitoring Output Voltage to Match Resonance Frequency	Simple implementation, low cost, easy integration with existing systems	Requires basic stability in the measurement environment

The structure of this paper is as follows: Section 2 offers a comprehensive analysis of the resonant converters. Section 3 examines and verifies the relationship between output voltage and switching frequency in the resonant capacitor conversion circuit. Section 4 provides a detailed examination of experimental outcomes, confirming the effectiveness of a self-tracking switching frequency method to ensure the system operates stably with aligned resonant and switching frequencies. Finally, Section 5 concludes this article.

2. Circuit, Operations, and the Algorithm

2.1. Circuit

Resonant converters aim to improve energy conversion efficiency, especially in data centers and large-scale power systems. If adjusted to closely align with the resonant frequency, the switching frequency enables the resonant converter to achieve lossless switching. Utilizing a resonant loop of inductors and capacitors facilitates soft switching at zero current, thereby reducing energy losses in conversion. Adjusting the switching frequency and duty cycle tailors output voltage and current to meet specific load demands.

2.2. Operations

This manuscript focuses on the basic unit circuit of the resonant converter, as shown in Figure 1. The basic cell of resonant converters. In Figure 1, it connects in+ to out+. The main voltage is applied between in+ and out−. A load is connected between out+ and out− to form a simple 2:1 Switched Capacitor (SC) circuit, as shown in Figure 2a. The operational principle hinges on aligning the switching frequency with the resonant frequency, resulting in the operational waveform shown in Figure 2b, where all switches have a fixed duty cycle of 50%. Q_1 and Q_3 switch synchronously, as do Q_2 and Q_4 , with the latter pair acting complementary to Q_1 and Q_3 . Figures 3–5 provide an in-depth analysis of the circuit operation. The system's main voltage, V_{in} , powers decoupling capacitors C_2 and C_3 , with their voltage increments complementing each other to alternately energize the output resistor R_i . From t_1 to t_2 , Q_1 and Q_3 conduct while Q_2 and Q_4 remain off, allowing L_r and C_r to store energy. The inductor current, taking the form of a sine wave, reaches zero at phase change, effectuating Zero-Current Switching (ZCS), as shown in Figure 3. The system enters a dead time from t_2 to t_3 , with all switches off and the resonant tank (L_r , C_r) current at zero, as demonstrated in Figure 4. Between t_3 and t_4 , with Q_1 and Q_3 off and Q_2 and Q_4 conducting, the current prior to Q_2 and Q_4 conducting drops to zero alongside their V_{DS} , achieving Zero-Voltage Switching (f_{sw}). In this phase, L_r and C_r discharge the energy accumulated from t_1 to t_2 , with the inductor current inverting direction compared to t_1 to t_2 and supplying power to the load, as detailed in Figure 5. The system enters a dead time from t_4 to t_5 , with all switches off and the resonant tank (L_r , C_r) current at zero, as demonstrated in Figure 6.

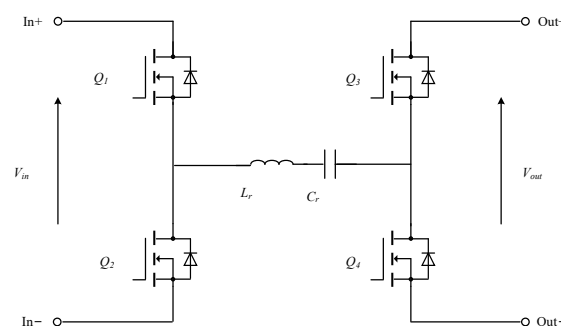


Figure 1. The basic cell of resonant converters.

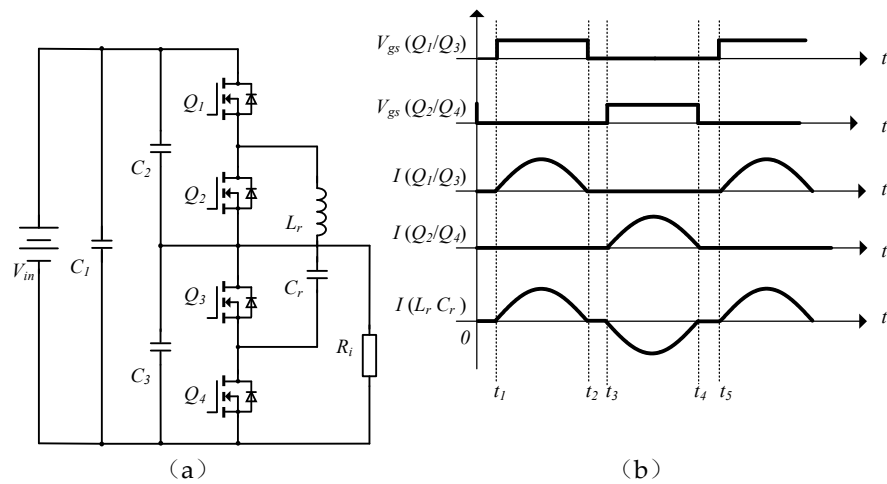


Figure 2. The system circuit topology used in this paper: (a) is the circuit topology diagram, and (b) is the MOSFET gate-source voltage (V_{gs}) and current (I_{Qx}), and resonant inductor current (I_{Lr}) waveform diagram.

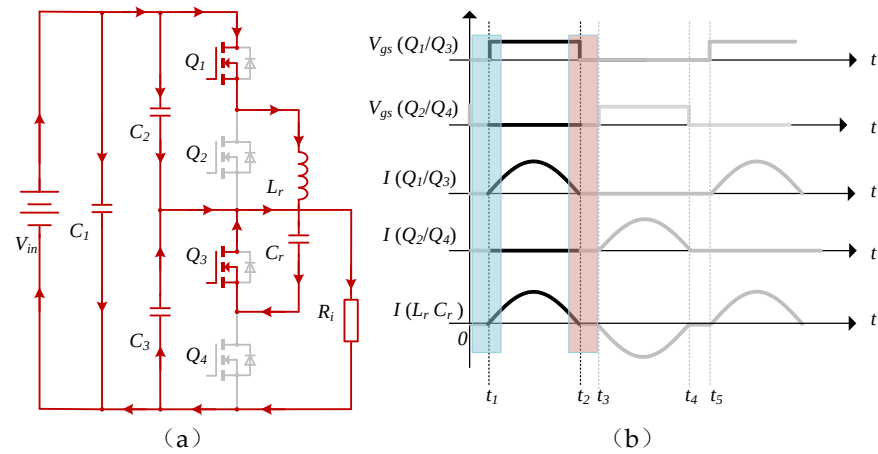


Figure 3. During t_1-t_2 time, Q_1 Q_3 is on, and Q_2 Q_4 is off, the circuit current direction and the waveform of Q_1 – Q_4 gate-source voltage (V_{gs}) and resonant inductor current (I_{Lr}): (a) diagram of current flow and (b) waveform diagram. The highlighted section shows the ZVS process (blue) and ZCS process (pink).

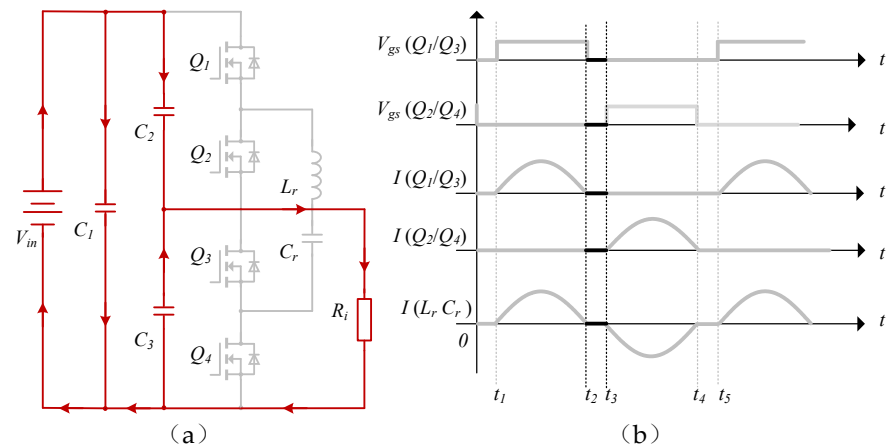


Figure 4. During the t_2-t_3 time, all MOSFETs are turned off, the circuit current direction and the working waveform of Q_1 – Q_4 gate-source voltage (V_{gs}) and current (I_{Qx}) and resonant inductor current: (a) diagram of current flow and (b) waveform diagram.

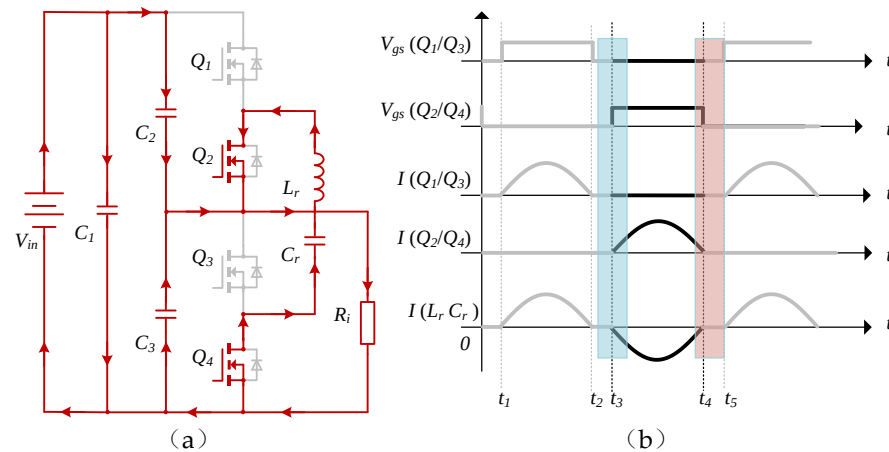


Figure 5. During t_3 – t_4 time, Q_1 Q_3 is turned off, Q_2 Q_4 is turned on, the circuit current direction and the working waveform of Q_1 – Q_4 gate-source voltage (V_{gs}) and current (I_{Qx}) and resonant inductor current: (a) diagram of current flow and (b) waveform diagram. The highlighted section shows the ZVS process (blue) and ZCS process (pink).

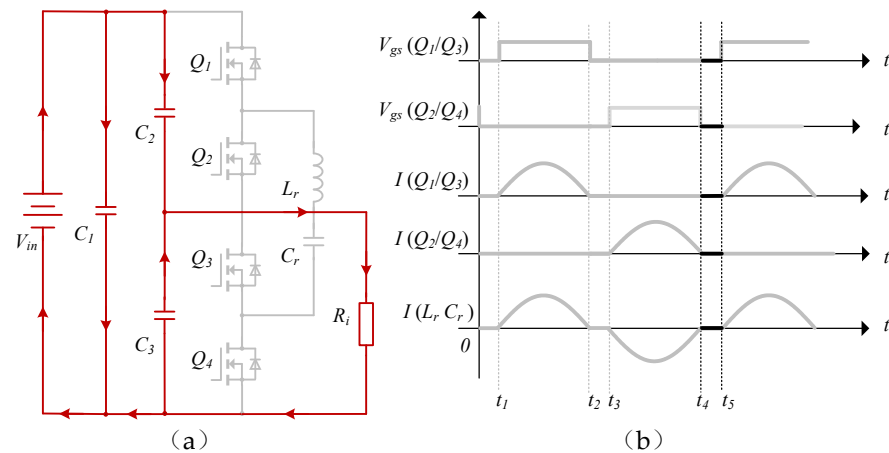


Figure 6. During the t_4 – t_5 time, all MOSFETs are turned off, the circuit current direction and the working waveform of Q_1 – Q_4 gate-source voltage (V_{gs}) and current (I_{Qx}) and resonant inductor current: (a) diagram of current flow and (b) waveform diagram.

2.3. Challenges

Due to the nonlinear properties of Class II dielectric materials, capacitance fluctuates sharply with its voltage changes. Figure 7 shows the DC bias characteristics of capacitors from various studies. Google initially used high-precision Class I capacitors in their 2018 STC circuit [5], but later opted for Class II capacitors with greater tolerances in 2022 [16]. Resonant Switched Capacitor Converter [6–10] research also predominantly employs Class II capacitors. Class II capacitors are broadly used in electronic circuits, including resonant switching circuits, for their high dielectric constant and broad temperature and capacitance ranges. However, their capacitance significantly varies with temperature and voltage, a drawback for high precision or stability needs. Class II capacitors, with their higher capacitance density, offer a significant advantage in miniaturization over Class I capacitors, making them ideal for compact power electronic applications where space is at a premium.

Figure 8 provides a comparative analysis of Class I (C0G) and Class II (X7R) capacitors under identical resonant capacitance and direct current bias conditions. It illustrates that the resonant capacitor composed of Class II (X7R) material occupies only 3.04% of the area and 2.24% of the volume compared to its Class I (C0G) counterpart. This stark contrast underscores the substantial reduction in both footprint and volumetric space achieved through the utilization of Class II capacitors, highlighting their potential for miniaturization

in power electronic applications while maintaining the same capacitance value. Although Class II capacitors may demonstrate reduced stability under DC bias, the innovative self-tracking frequency control strategy outlined in this manuscript effectively mitigates issues related to capacitor instability, thereby maintaining reliable system performance.

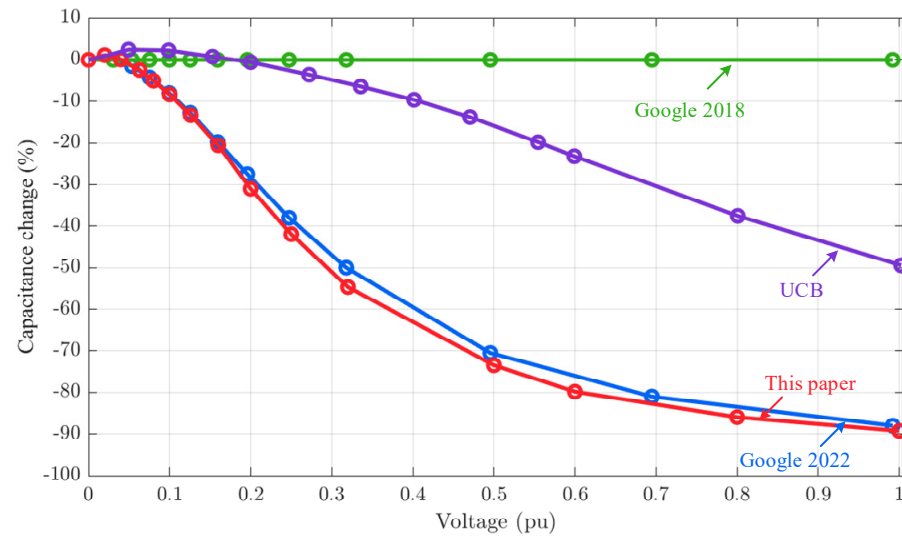


Figure 7. The DC bias characteristics of capacitors from various studies [5–10,16].

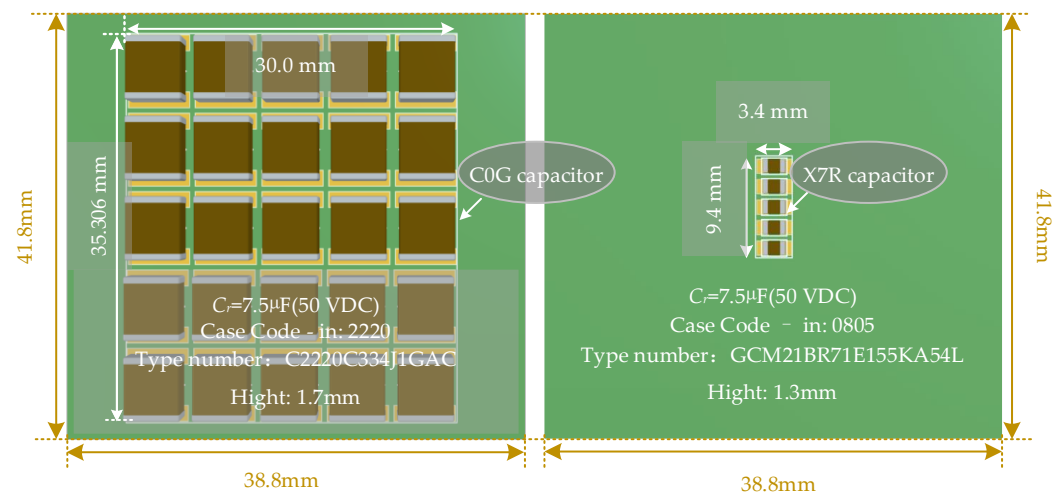


Figure 8. Dimensional Comparison of Class I and Class II Capacitors with Equivalent Capacitance and Rated Voltage.

An inductor serves to store energy via a magnetic field induced by current flow within a coil. The passage of current generates heat, elevating the coil's temperature. Such temperature increases impact the coil's resistance and inductance, consequently altering its output voltage and current characteristics. Figure 9 depicts the variability of MnZn's magnetic permeability with environmental conditions, demonstrating that inductance values fluctuate within $\pm 25\%$ across an ambient temperature range of -40°C to 85°C [15].

When $f_{sw} < f_r$, the system waveform diagram and diagram of current flow are shown in Figures 10 and 11. Within t_1 – t_2 time, Q_1 and Q_3 are switched on, the charging process of the resonant capacitor ends in advance, and the energy stored on the inductor begins to discharge and reverse charge the capacitor. The blue highlighted time in the waveform diagram is shown in Figure 10a, and the system current flow diagram is shown in Figure 10b. At this time, I_{Lr} , I_{Q-1} , and I_{Q-2} change direction, and the resonant capacitor is charged in reverse. At t_2 – t_3 , the system enters the dead time. Within the timeframe highlighted in

blue in the waveform diagram (Figure 10c), the flow current is depicted in Figure 10d. Q_1 – Q_4 is turned off, and the current passes through the MOSFET body diode to continue releasing the energy stored in the inductance. In t_3 – t_4 , Q_2 and Q_4 are switched on, the resonant inductor discharge process ends in advance, and the charging process begins. In the waveform diagram (Figure 11a), during the time highlighted in blue, the direction of system current flow is as shown in Figure 11b. At t_4 – t_5 , the system enters the dead time again. Within the timeframe highlighted in blue in the waveform diagram (Figure 11c), the flow current is depicted in Figure 11d. Q_1 – Q_4 is turned off and flow through the MOSFET body diode, and the capacitor continues to charge. When $f_{sw} > f_r$, the system waveform diagram and current direction diagram are shown in Figures 12 and 13. Comparing the two detuning states, although their waveform distortion is different, the current and voltage flowing through the MOSFET during the on-and-off process have overlapping regions. As a result, perfect ZVS/ZCS cannot be achieved in either detuning state, resulting in loss.

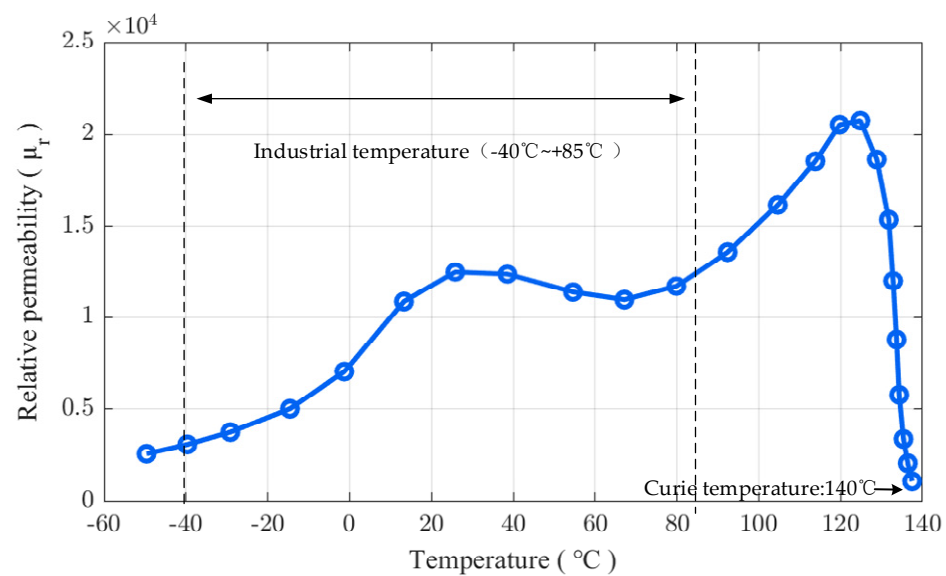


Figure 9. The change curve of the permeability of MnZn with environmental conditions mentioned in [15].

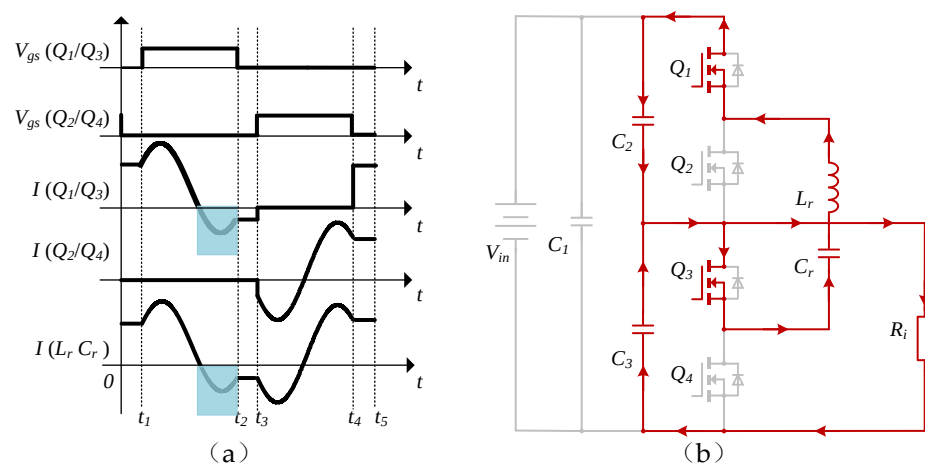


Figure 10. Cont.

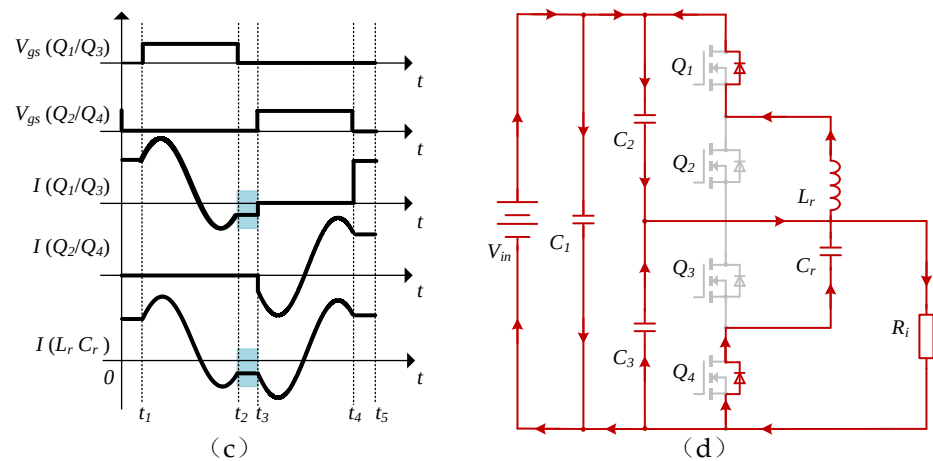


Figure 10. When $f_{sw} < f_r$, during t_1-t_3 time, the circuit current direction and the waveform: (a) During t_1-t_2 time, waveform distortion analysis (blue highlighted area in the figure). (b) The current flow diagram that works abnormally in t_1-t_2 time (blue highlighted area in the figure). (c) During t_1-t_2 time, waveform distortion analysis (blue highlighted area in the figure). (d) The current flow diagram that works abnormally in t_1-t_2 time [14–16].

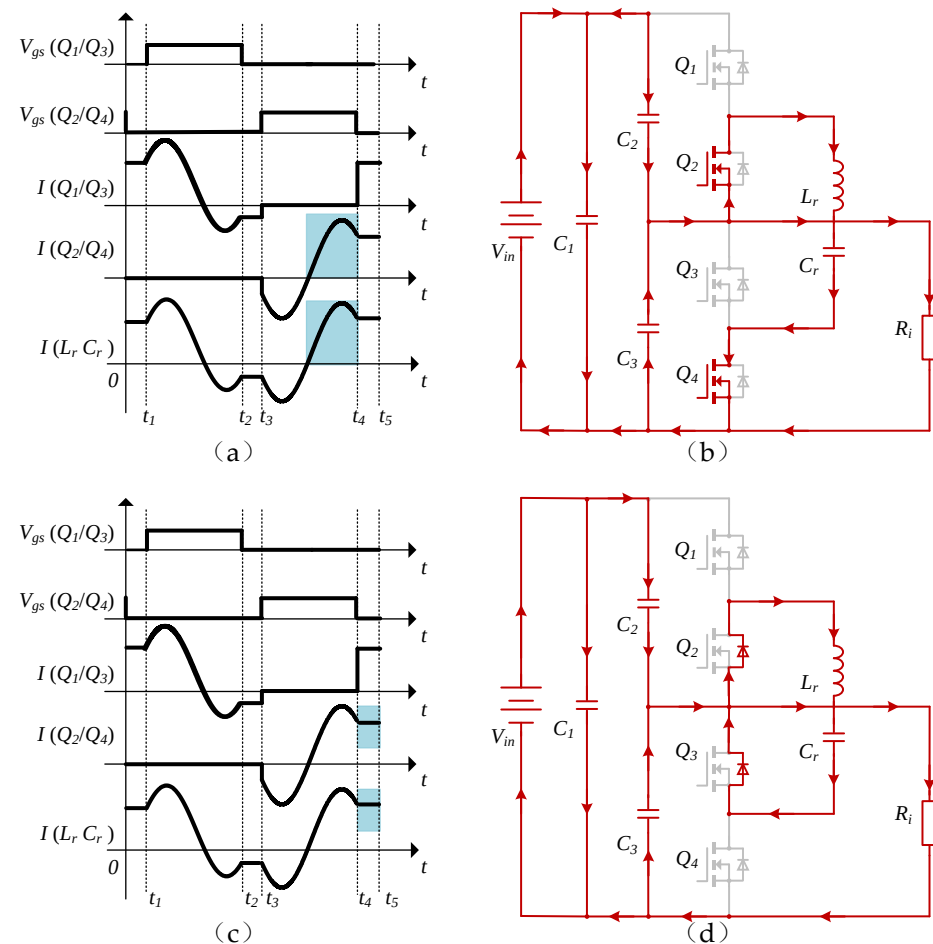


Figure 11. When $f_{sw} < f_r$, during t_3-t_5 time, the circuit current direction and the waveform: (a) During t_3-t_4 time, waveform distortion analysis (blue highlighted area in the figure). (b) The current flow diagram that works abnormally in t_3-t_4 time (blue highlighted area in the figure). (c) During t_4-t_5 time, waveform distortion analysis (blue highlighted area in the figure). (d) The current flow diagram that works abnormally in t_4-t_5 time [17–20].

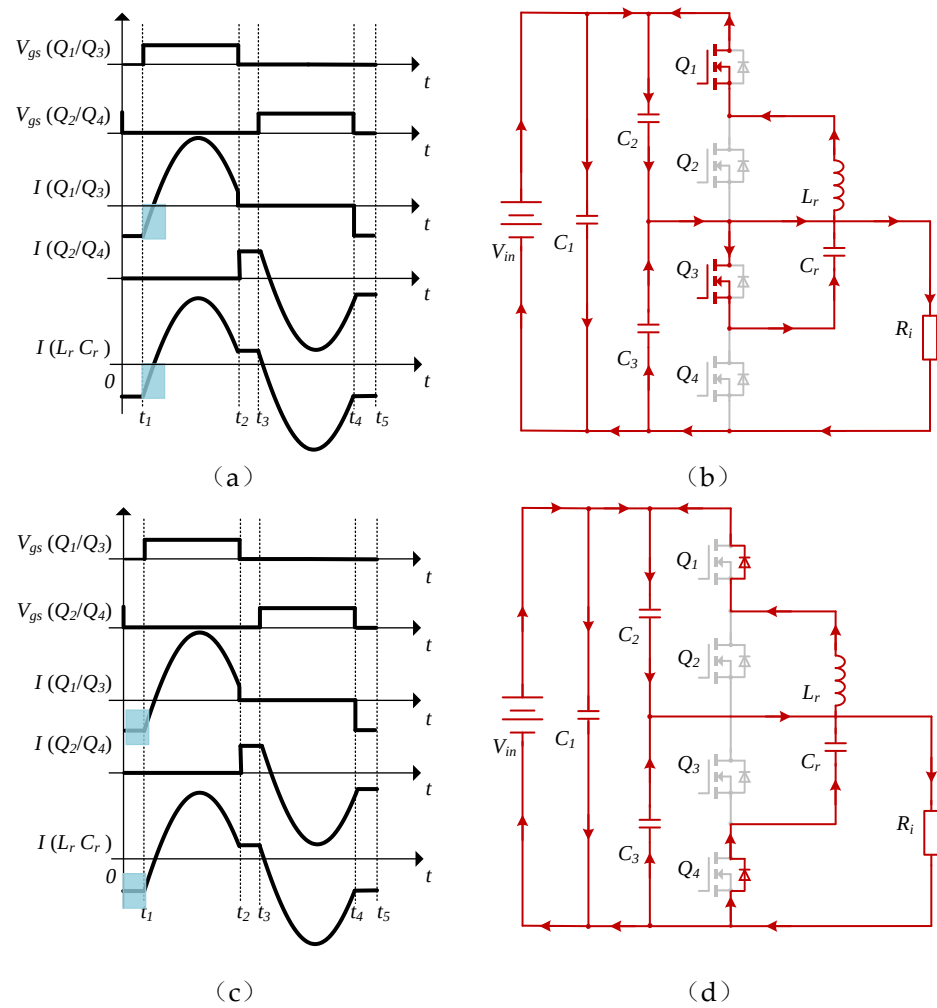


Figure 12. When $f_{sw} > f_r$, during t_1-t_3 time, the circuit current direction and the waveform: (a) During t_1-t_2 time, waveform distortion analysis (blue highlighted area in the figure). (b) The current flow diagram that works abnormally in t_1-t_2 time. (c) During $0-t_1$ time, waveform distortion analysis (blue highlighted area in the figure). (d) The current flow diagram that works abnormally in $0-t_1$ time [13].

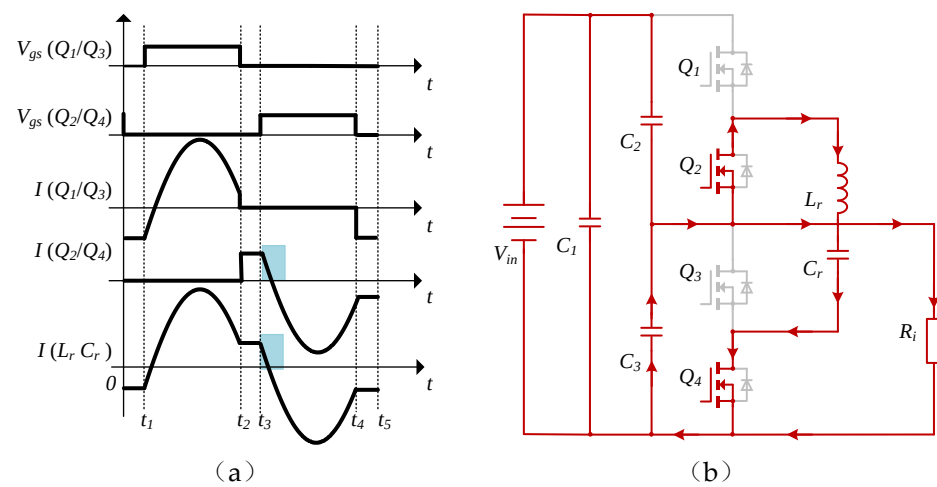


Figure 13. Cont.

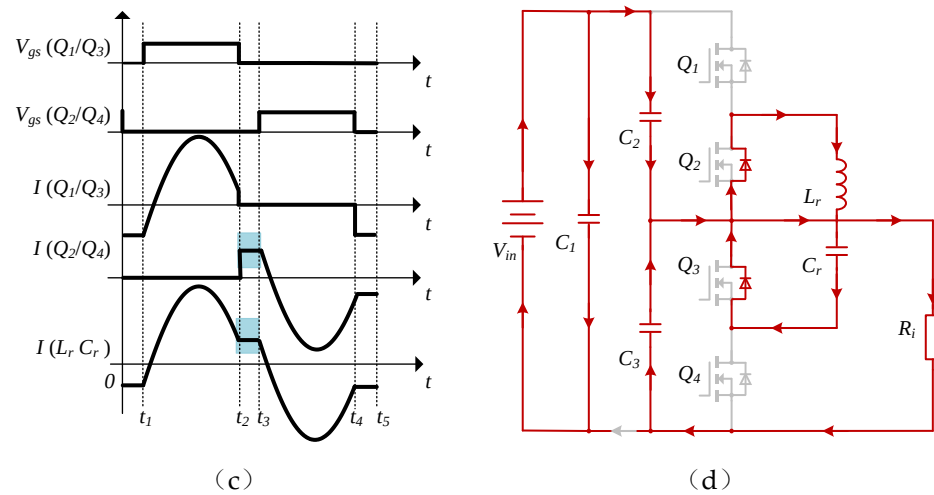


Figure 13. When $f_{sw} > f_r$, during t_3 – t_5 time, the circuit current direction and the waveform: (a) During t_2 – t_4 time, waveform distortion analysis (blue highlighted area in the figure). (b) The current flow diagram that works abnormally in t_3 – t_4 time. (c) During t_2 – t_3 time, waveform distortion analysis (blue highlighted area in the figure). (d) The current flow diagram that works abnormally in t_2 – t_3 time [16,17].

2.4. Algorithm

This manuscript introduces an algorithm designed to address disruptions stemming from variations in resonant frequency. Experimental data, as depicted in Figure 14, reveal that the converter's output voltage achieves its maximum when the switching frequency is synchronized with the resonant frequency. Consequently, the algorithm continuously modulates the switching frequency to maintain this maximum output voltage, thereby ensuring alignment between the switching and resonant frequencies to reduce system losses attributed to frequency deviation. A flowchart detailing the algorithm's methodology is provided in Figure 14.

V_{out} represents the system's output voltage, *direction* indicates the change in system switching cycles, and *period* denotes the number of switching cycles, with $period_{min}$ and $period_{max}$ signifying the minimum and maximum values of switching cycles, respectively. The algorithm initiates by comparing the output voltage values of two consecutive measurements. If the output voltage increases, the sign of *direction* remains unchanged; if the output voltage decreases, the sign of *direction* changes. The algorithm adjusts $period_k$ based on the change in $direction_k$. If $period_k$ falls within the threshold range of switching frequencies, the program proceeds to the next cycle; if $period_k < period_{min}$ or $period_k > period_{max}$, define $period_k$ as the boundary value for adjacent periods ($period_{min}$ or $period_{max}$), subsequently proceeding with the iterative process.

The algorithm optimizes the system's switching cycles by iteratively adjusting the period based on the output voltage's direction of change. It maintains the period within the specified minimum and maximum thresholds, ensuring stability and efficiency in the system's performance. The algorithm's start-up phase involves an initial measurement of the system's output voltage, V_{out} , which establishes a baseline for subsequent comparisons. This phase is critical as it sets the initial conditions for the direction indicator, $direction_k$, which will influence the adjustment of the switching cycles' period. By comparing the initial V_{out} with the following measurement, the algorithm determines the initial trend in voltage change, setting the stage for the iterative process that continuously adapts the system's response to achieve optimal performance within the defined thresholds. This start-up procedure ensures that the system begins its operation with a clear directive for maintaining voltage stability and efficiency.

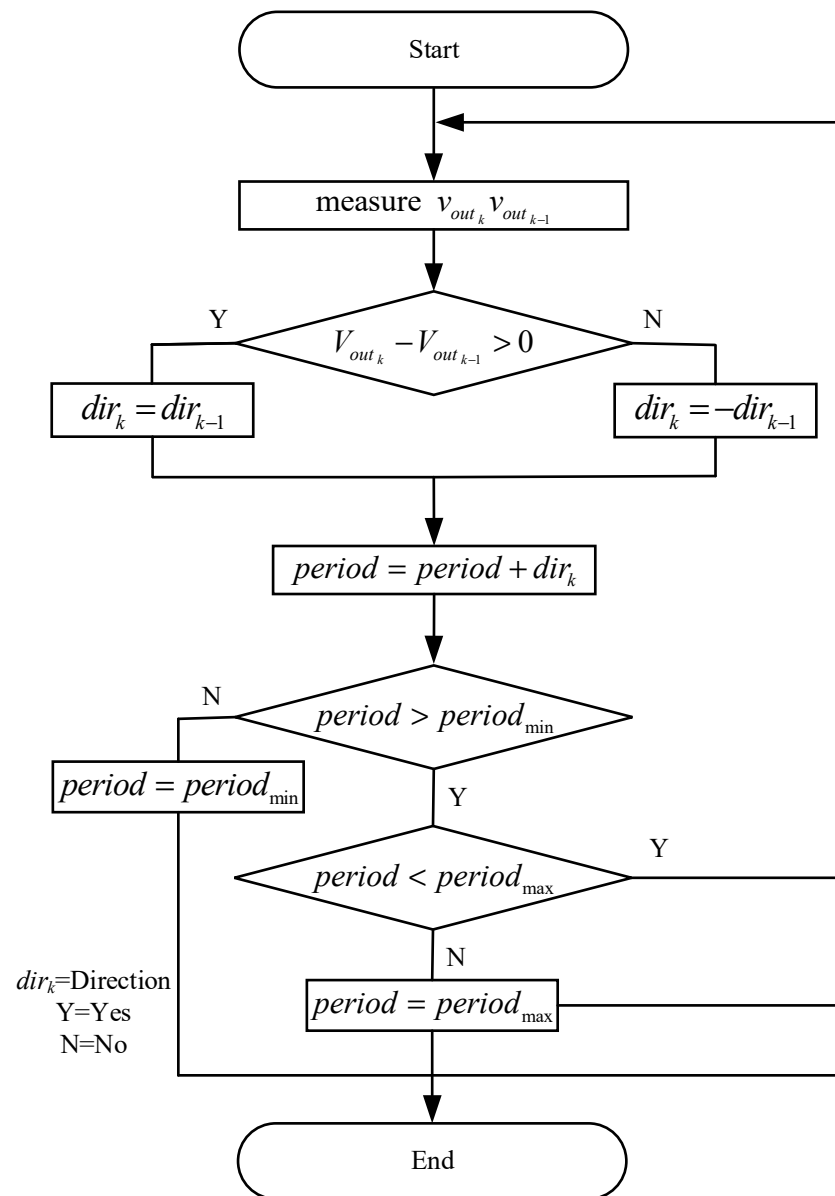


Figure 14. Flowchart of closed-loop control algorithm [18–28]. The related project, including the hardware design files and the software, is attached in the Supplementary Materials.

3. Simulation

Conducted Simulink simulations on the proposed circuit involved varying the switching frequency and recording the resultant changes in output voltage.

Data analysis, shown in Figure 15, reveals a relationship where output voltage increases with the switching frequency (f_{sw}) below the resonant frequency (f_r), decreases when f_{sw} exceeds f_r , and peaks at $f_{sw} = f_r$.

The voltage across the MOSFET's source and drain (V_{DS}) and the current through resonator L_r (I_{L_r}) were measured. At $f_{sw} = f_r$, Figure 16 shows the simulation waveform, indicating that the system operates at the resonant point with minimal circuit impedance, ensuring stable output voltage and current. This stability facilitates consistent output performance and parameter uniformity, even with fluctuating load conditions. When $f_{sw} < f_r$, the waveform is shown in Figure 17. The resonance current experiences over-resonance, leading to circuit resonance amplitudes significantly exceeding expectations and causing abnormal increases in voltage or current. This can result in component overheating or damage and circuit performance instability. When $f_{sw} > f_r$, the waveform is shown in

Figure 18. Significant voltage and current overlap impede the attainment of ideal Zero-Voltage Switching (ZVS) or Zero-Current Switching (ZCS), causing the switching device to operate under non-ideal conditions. This escalates switching losses and culminates in additional heat production.

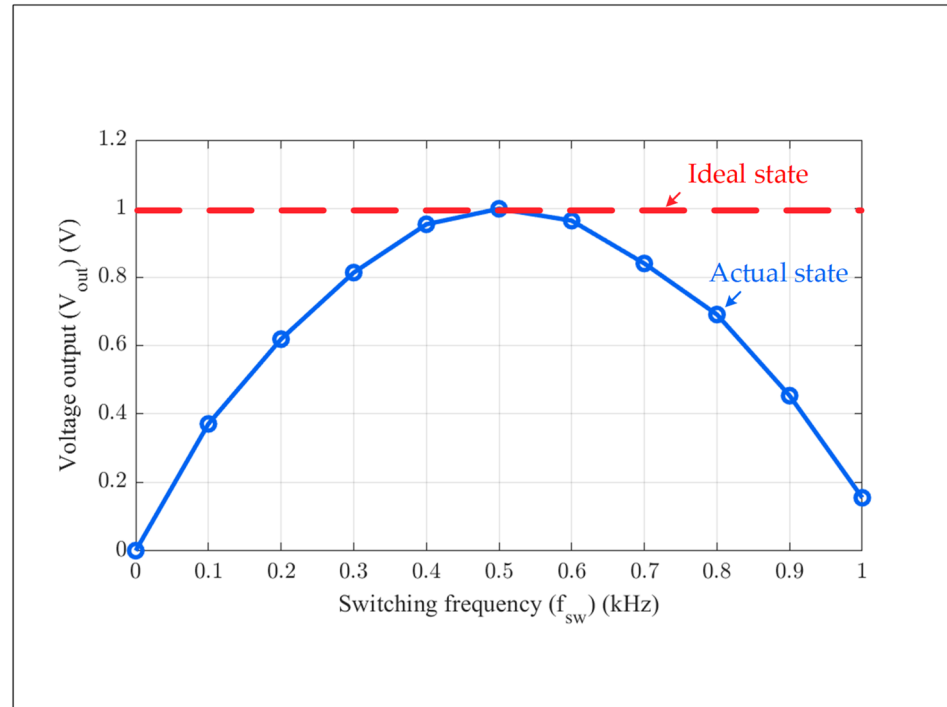


Figure 15. Curve of Output Voltage Gain as a Function of Switching Frequency with a Unique Maximum Value [29–32].

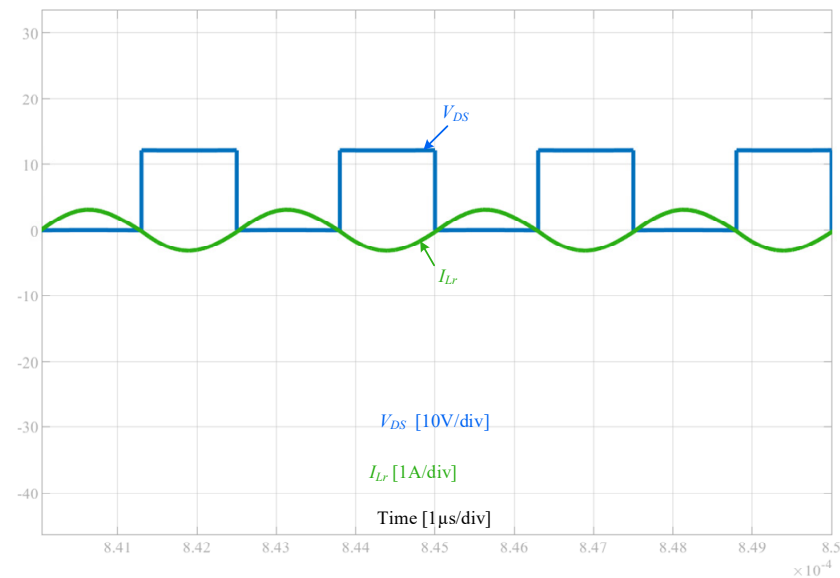


Figure 16. The simulation waveform of the current flowing in the resonant inductor and the voltage at both ends of Q_1 source and drain when $f_{sw} = f_r$.

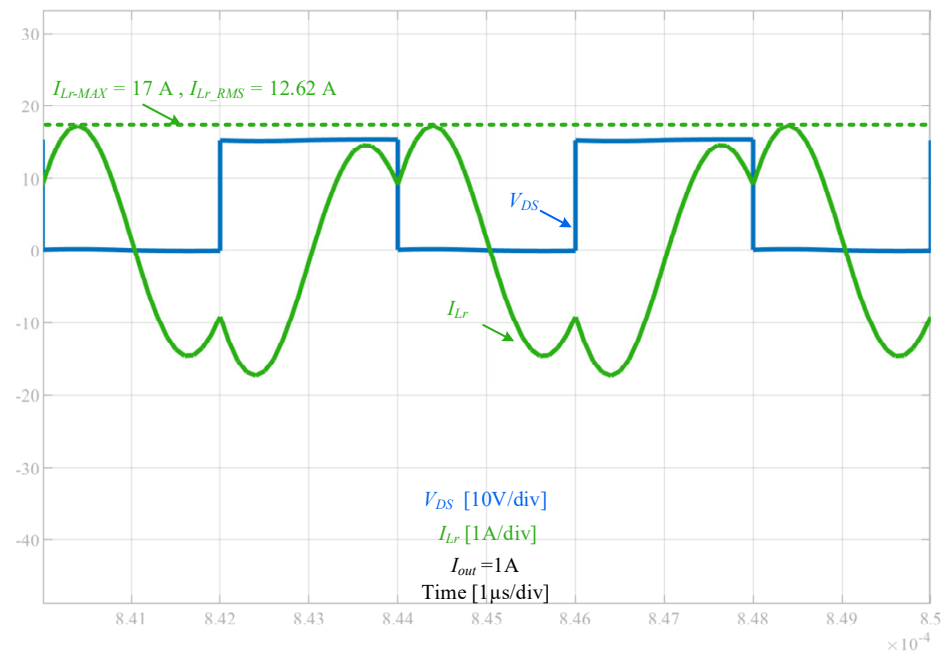


Figure 17. The simulation waveform of the current flowing in the resonant inductor and the voltage at both ends of Q_1 source and drain when $f_{sw} < f_r$.

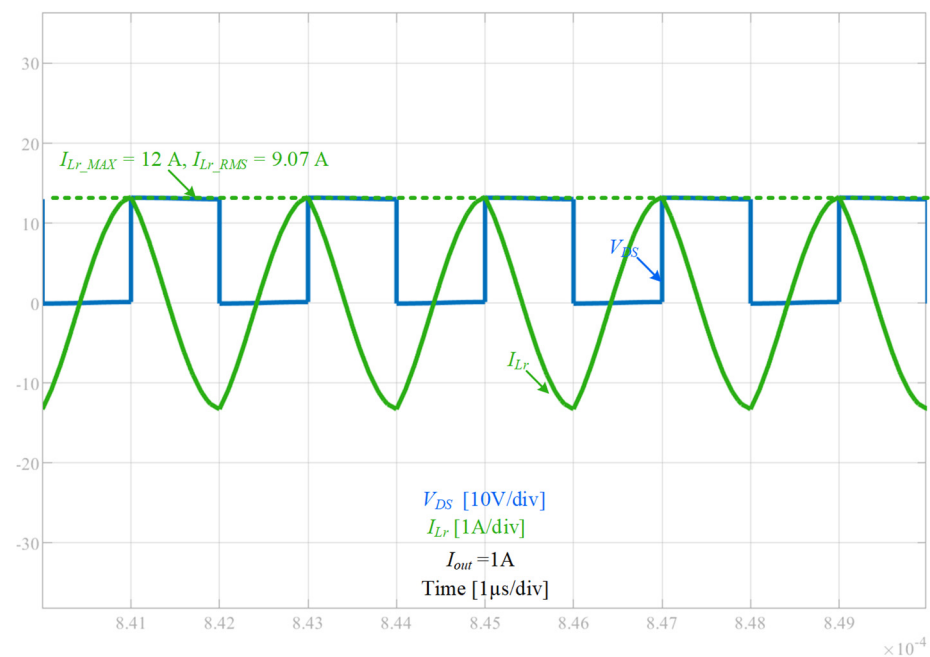


Figure 18. The simulation waveform of the current flowing in the resonant inductor and the voltage at both ends of Q_1 source and drain when $f_{sw} > f_r$.

The proposed methodology incorporates a self-tuning frequency mechanism that dynamically synchronizes the switching frequency with the resonant frequency. This strategy effectively addresses the issue of non-zero-voltage switching due to resonance inaccuracies, a technical challenge not adequately resolved by conventional technologies. In the simulation, the variations of the resonant inductor and resonant capacitor during actual operation are modeled. Utilizing the algorithm we proposed, the optimal point of the output voltage is determined to control the switching frequency of the system. This ensures that the system consistently produces the optimal output. Figure 19 illustrates the dynamic results of the simulation system, demonstrating that when a deviation in

the resonant frequency occurs, the system adjusts the switching frequency in a timely manner by monitoring the output voltage. Ultimately, this allows the system to return to an optimal state where zero-voltage turn-on and zero-current turn-off can be achieved. Table 2 contrasts Self-Frequency Tracking with Conventional Methods for ZVS achievement amidst resonance frequency shifts. It details their approaches to frequency adjustment, resonance accuracy, and technical application, highlighting Self-Frequency Tracking's adaptability and precision in maintaining system performance under varying conditions.

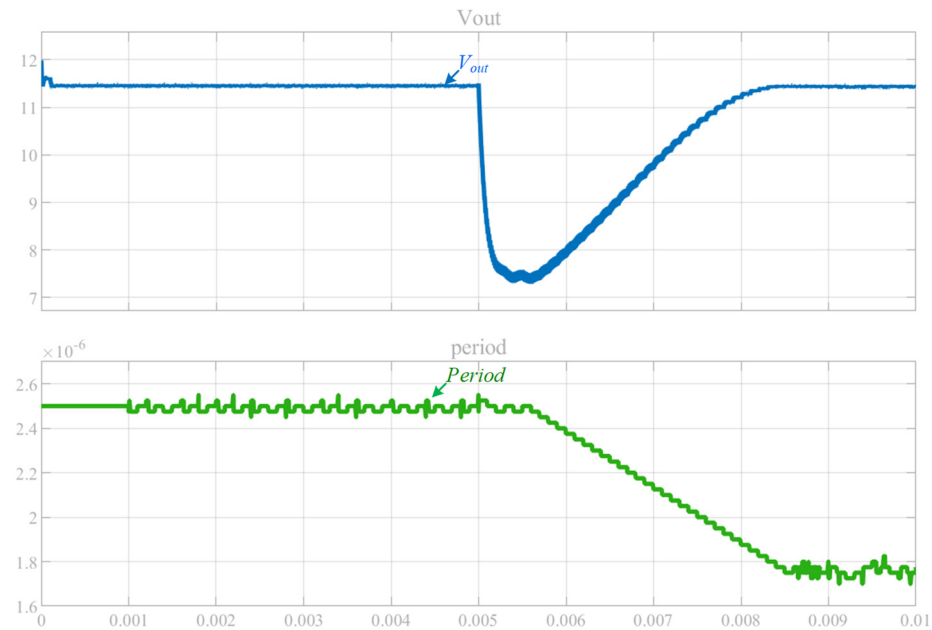


Figure 19. Dynamic Response of Self-Tracking Frequency System with Variable Resonant Components in Simulation.

Table 2. Resolving ZVS Challenges: A Comparative Study of Self-Frequency Tracking and Conventional Methods.

Feature	Self-Frequency Tracking	Other Studies
Switching Frequency Adjustment	Self-adjusting to maintain switching frequency approximately equal to the resonance frequency	Typical fixed switching frequency, does not adjust with changes in resonance frequency
Avoiding Resonance Inaccuracy	Effectively prevents non-zero-voltage switching caused by resonance inaccuracies	Resonance inaccuracies may lead to non-zero-voltage switching
Technical Implementation	Utilizes advanced frequency detection and automatic adjustment technology	Lacks effective frequency self-adaptation technology
Application Scenario	Suitable for high precision control requirements in power electronic systems	More suitable for applications with minor parameter changes
Literature Citation	Cites recent research demonstrating technological forefront	Often based on older theories, with fewer updates

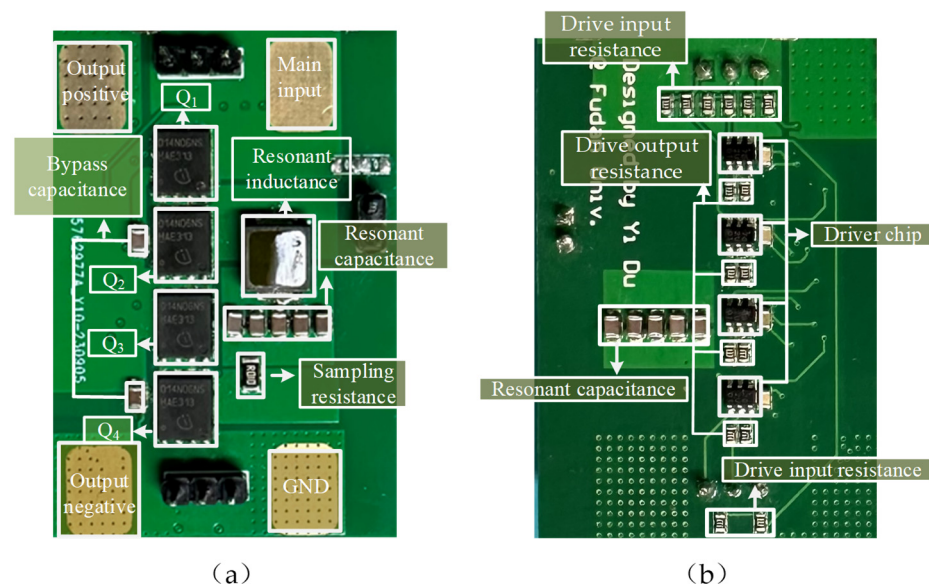
Table 3 lists the relevant parameters of the simulation system. Fundamentally, the resonant frequency exhibits a significant correlation with the switching frequency. The mismatch between the resonant frequency and the switching frequency results in decreased output voltage. Aligning the resonant frequency with the switching frequency is crucial for enhancing circuit performance and system reliability. Based on the relationship between the output voltage and the switching frequency, we believe that the proposed method is feasible.

Table 3. The modules and their parameters in the simulation system are listed.

Module	Parameter
MOSFET	FET resistance R_{on} (Ohms): 0.01 Snubber resistance R_{on} (Ohms): 100 k Internal diode resistance R_d (Ohms): 0.1
DC Voltage source	Amplitude (V): 24 V Internal resistance (Ohms): 0.01
PWM Generator	Timer period (s): $1/(f_{sw})$ Phase delay (s): 0 Sample time: 1×10^{-7}
Resonant capacitance	Capacitance (μ F): 1.5831 (24 V)
Resonant inductance	Inductance (nH): 100
Decoupling capacitance	Capacitance (μ F): 100 Capacitor initial voltage (V): 12 V
Resonant circuit-sampling resistance	Resistance (Ohms): 0.1
Output load	Resistance R_d (Ohms): 12

4. Discussion Results

The test prototype is shown in Figure 20. The device parameters utilized in the experimental setup are enumerated in Table 4. The circuit comprises four MOSFET switches, a sampling resistor for measuring I_{Lr} , decoupling capacitors, as well as resonant inductors and capacitors. The configuration features four inputs: two dedicated to driver signal inputs, one for VDD, and one for GND. Activation of the four MOSFETs is facilitated by a driver chip. The launchpad generates two complementary PWM drive signals, records the output voltage, and manages feedback control tasks.

**Figure 20.** Cont.

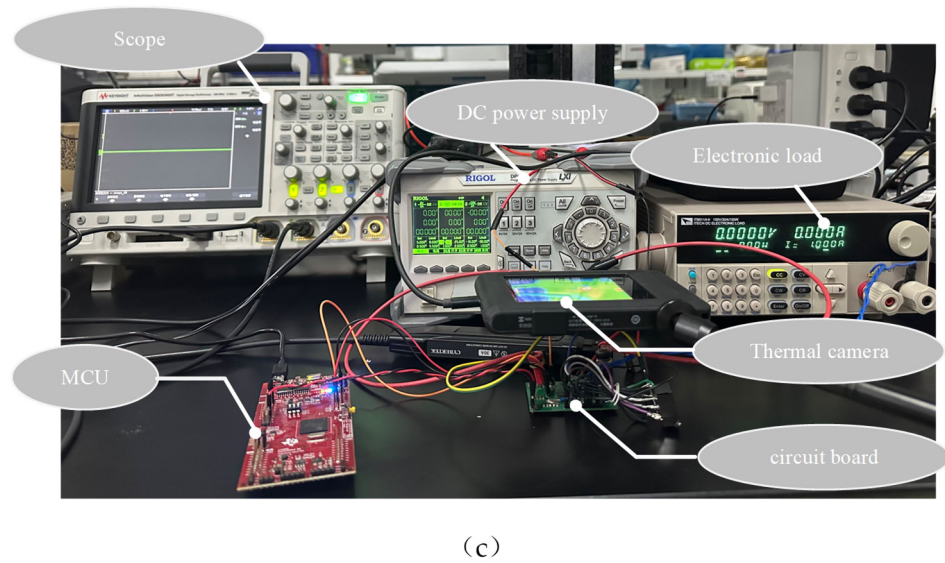


Figure 20. Converter prototype for PCB top view and up view, and test prototype: (a) PCB top view, (b) PCB up view, (c) Setup prototype.

Table 4. The parameters of the resonant converter are proposed.

Symbol	Parameters	Circuit Realization
f_{sw}	30~100 kHz	DSP 28379D
Q_1, Q_2, Q_3, Q_4	60 V, 240 A, 1.45 m Ω	BSC014N06NS
L_r	100 nH	SLC7250-101
C_r	10 μ F (Note)	GRM21BR61H106KE43L

Note: The rated capacitance is 10 μ F, but according to the data sheet When the DC voltage deviation is 24 V, the capacitance changes to -87% .

In an open-loop configuration, varying the switching frequency allows for recording the output voltage and establishing a relationship curve between the switching frequency and output voltage under different input voltages, as Figure 21 shows. The closed-loop system automatically adjusts the switching frequency to a stable state, identified as f_{sw-s} , where the output voltage reaches its maximum. Figure 22 displays the V_{DS} and I_{Lr} waveform. When operating in an open loop, if the switching frequency deviates from the specified f_{sw-s} , as illustrated in Figures 23 and 24, the waveform of I_{Lr} distorts. This distortion leads to an increase in current, which prevents the MOSFETs from turning off at zero current. Figures 25 and 26 show the experimental results of the system during open-loop operation and closed-loop operation respectively. In closed-loop mode, dynamic experimental results, as depicted in Figures 27 and 28, demonstrate that variations in the system's main voltage prompt instantaneous modifications in I_{Lr} . These modifications rapidly converge to the new steady state. Figure 29 displays the steady-state outcomes of the closed-loop system under varying input voltages. The system also continues to operate effectively with load changes, with results shown in Figure 30.

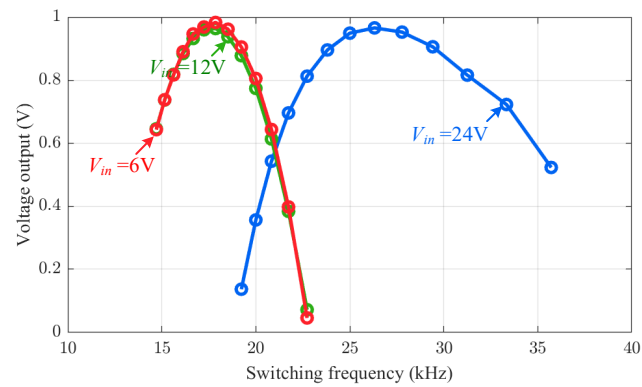


Figure 21. The output voltage varies with the switching frequency of the system. The red curve shows the relation between the output voltage and the switching frequency when the input voltage is 6 V; the green curve shows the relation between the output voltage and the switching frequency when the input voltage is 12 V; the blue curve shows the relation between the output voltage and the switching frequency when the input voltage is 24 V.

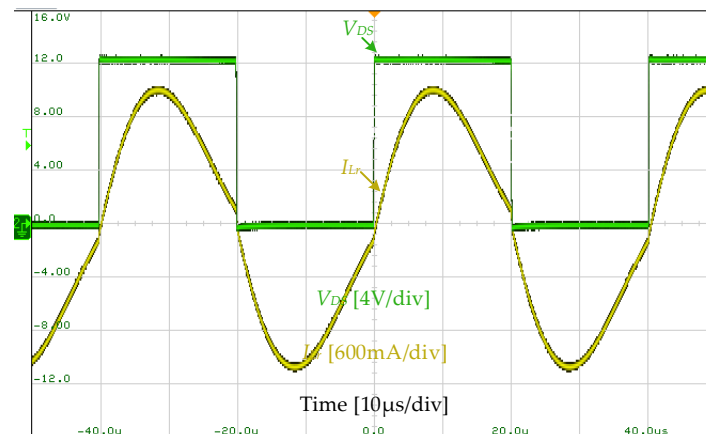


Figure 22. Experimental waveform of the current flowing in the resonant inductor (I_{Lr}) and the voltage at both ends of Q_1 source and drain (V_{DS}) when $f_{sw} = f_r$.

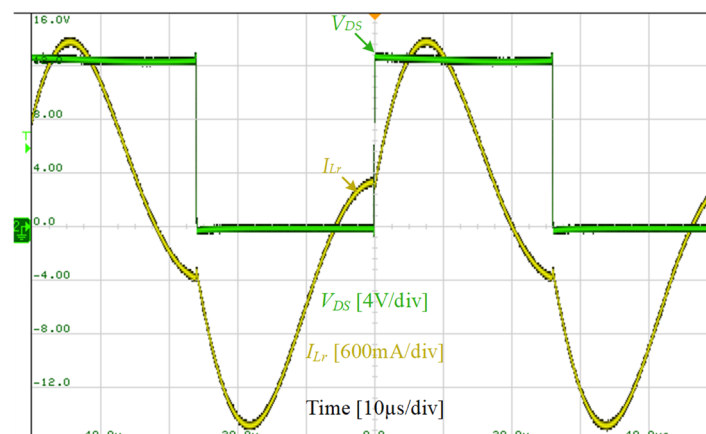


Figure 23. Experimental waveform of the current flowing in the resonant inductor (I_{Lr}) and the voltage at both ends of Q_1 source and drain (V_{DS}) when $f_{sw} < f_r$.

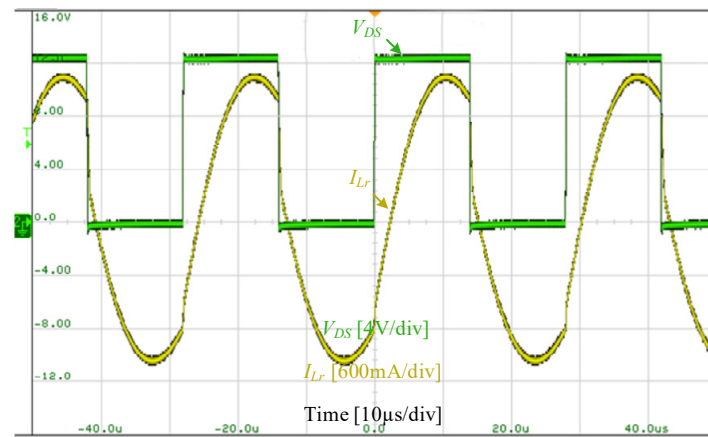


Figure 24. Experimental waveform of the current flowing through the resonant inductor and the voltage at both ends of Q_1 source and drain (V_{DS}) when $f_{sw} > f_r$.

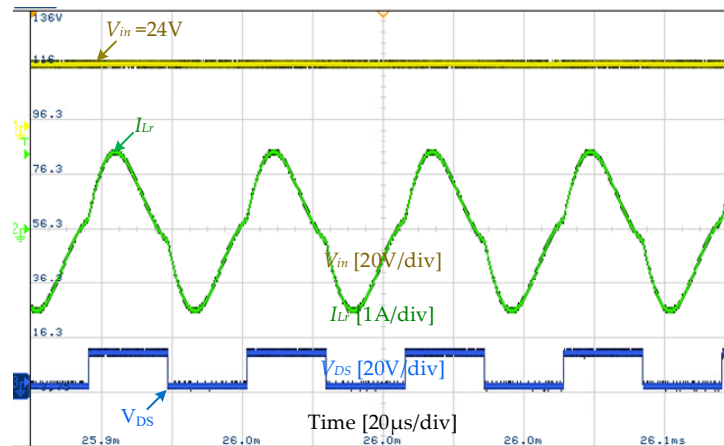


Figure 25. Experimental results of the system in open-loop operation.

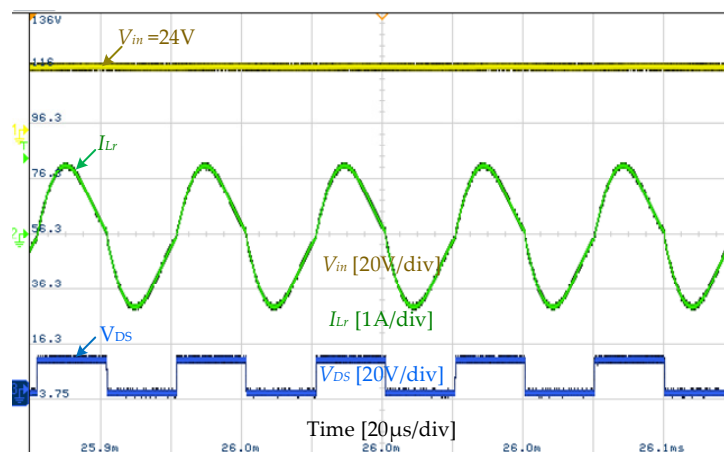


Figure 26. Experimental results of closed-loop operation of the system.

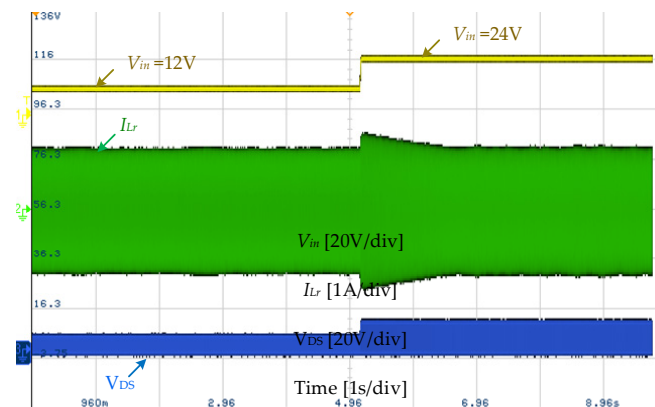


Figure 27. Dynamic test diagram: the input voltage from 12 V to 24 V capacitance value drops sharply, the resonant frequency drifts instantaneously, and the best advantage is obtained after about 1.2 s closed-loop control.

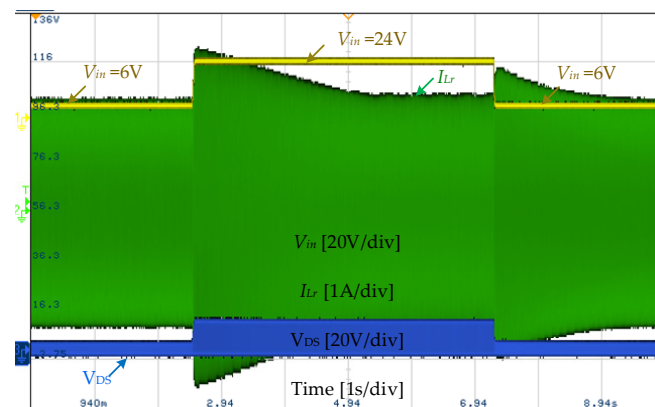


Figure 28. Dynamic experiment diagram: the input voltage from 6 V to 24 V capacitance value drops sharply, the resonant frequency shifts instantaneously, after about 2.4 s of closed-loop control to get the best advantage, and then the input voltage from 24 V to 6 V capacitance value increases, after about 2 s of closed-loop control back to the best advantage.

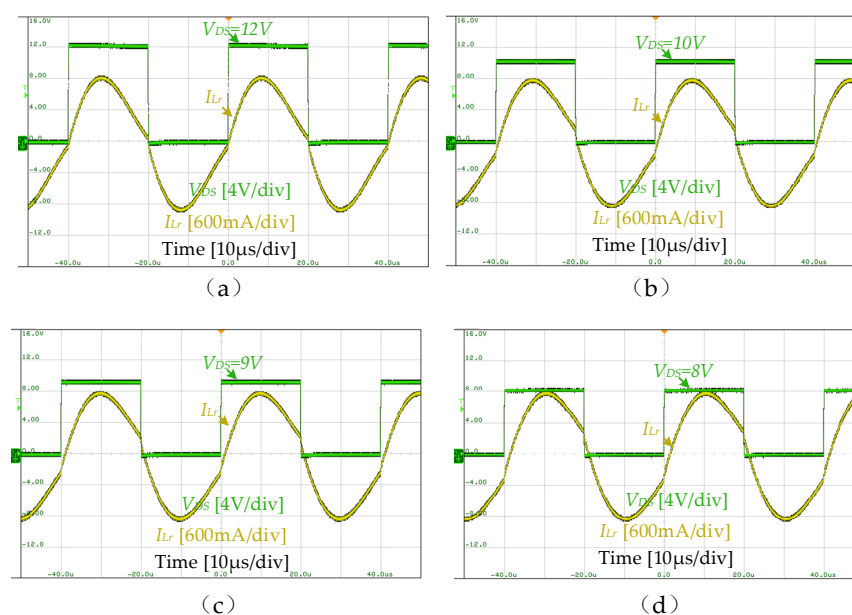


Figure 29. The variable input voltage changes the system waveform: (a) is the input voltage of 24 V, (b) is the input voltage of 20 V, (c) is the input voltage of 18 V, (d) is the input voltage of 16 V.

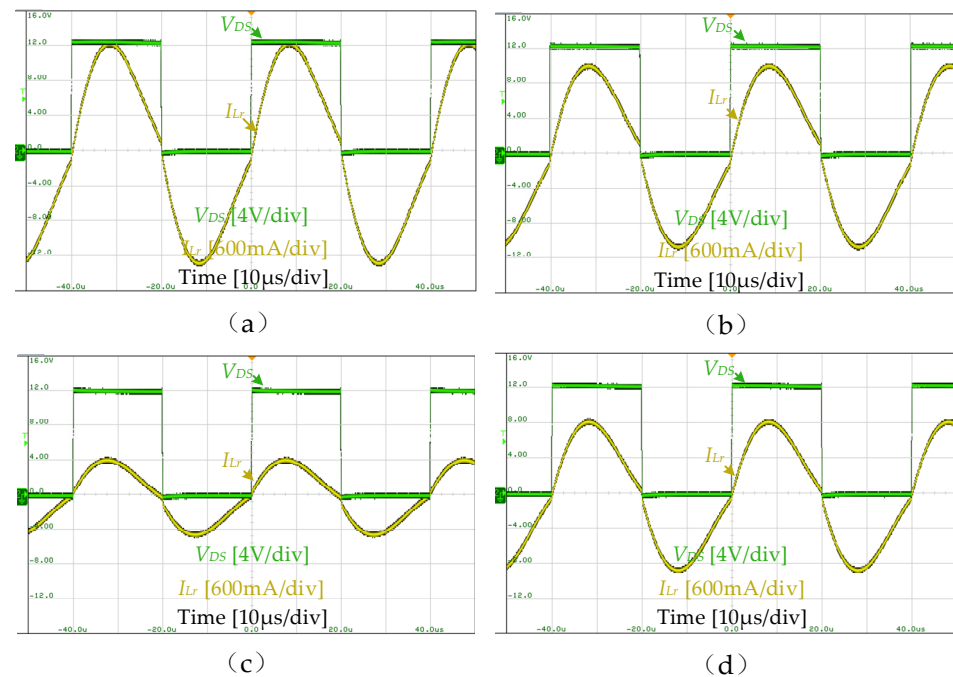


Figure 30. The system waveform changes under the changing load current: (a) the output current is 1.2 A, (b) the output current is 1 A, (c) the output current is 0.8 A, and (d) the output current is 0.4 A.

5. Conclusions

This research addresses resonant frequency instability in resonant capacitor converters by implementing a self-tracking frequency approach. The system's capability to synchronize the switching and resonant frequencies was experimentally validated, thereby reducing losses due to frequency misalignment. Our analysis revealed a critical correlation between output voltage and switching frequency. The proposed converter achieved stable operation with zero-voltage and zero-current switching, as evidenced by both simulation and experimental results. This research contributes to the field by offering a novel approach to addressing resonant frequency instability, enhancing the reliability and performance of resonant converters. It opens avenues for future investigations into the broader application and optimization of resonant conversion technologies.

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