

Review

CMOS IC Solutions for the 77 GHz Radar Sensor in Automotive Applications

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Abstract: This paper presents recent results on CMOS integrated circuits for automotive radar sensor applications in the 77 GHz frequency band. It is well demonstrated that nano-scale CMOS technologies are the best solution for the implementation of low-cost and high-performance mm-wave radar sensors since they provide high integration level besides supporting high-speed digital processing. The present work is mainly focused on the RF front-end and summarizes the most stringent requirements of both short/medium- and long-range radar applications. After a brief introduction of the adopted technology, the paper addresses the critical building blocks of the receiver and transmitter chain while discussing crucial design aspects to meet the final performance. Specifically, effective circuit topologies are presented, which concern mixer, variable-gain amplifier, and filter for the receiver, as well as frequency doubler and power amplifier for the transmitter. Moreover, a voltage-controlled oscillator for a PLL efficiently covering the two radar bands is described. Finally, the circuit description is accompanied by experimental results of an integrated implementation in a 28 nm fully depleted silicon-on-insulator CMOS technology.

Keywords: CMOS; radar sensor; mm-wave transmitter; mm-wave receiver; electromagnetic (EM) simulations; frequency doubler; transformer-based VCO; fully depleted (FD) silicon-on-insulator (SOI)



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1. Introduction

In the last decade, radar sensors have gained a lot of interest both in academic and industrial environments as the key technology for the implementation of next-generation autonomous driving systems [1,2]. Self-driving vehicles rely on a network of several different sensors, as shown in Figure 1 (i.e., lidar, radar, video, infrared, etc.), which collect data about the surrounding environment, thus allowing a microcontroller to properly manage their motion.

In this scenario, radar sensors are crucial devices since they guarantee high robustness over environmental interference (i.e., poor light, extreme temperature, bad weather conditions, etc.), and hence they can operate where other technologies could fail. According to their operating range, radar sensors can be grouped into two categories with specific requirements for the related RF front-end. Short/medium (S/MR) range radars provide a detection range of a few meters with a resolution of tens of centimeters. They call for a wide-tuning-range local oscillator (LO) as well as a very high-linear receiver. Conversely, long-range (LR) radars must guarantee a coverage area of more than 250 m, which translates into stringent requirements in terms of maximum transmitted power besides asking for a low-noise receiver [3]. W-band radar sensors can potentially support both applications thanks to the availability of a 5 GHz bandwidth, namely 76–77 GHz and 77–81 GHz bands,

which are used for LR and SM/R applications, respectively. The adoption of this band allows a substantial reduction in system size and cost, but it also enhances the design challenges of simultaneously fulfilling both S/MR and LR radar requirements.

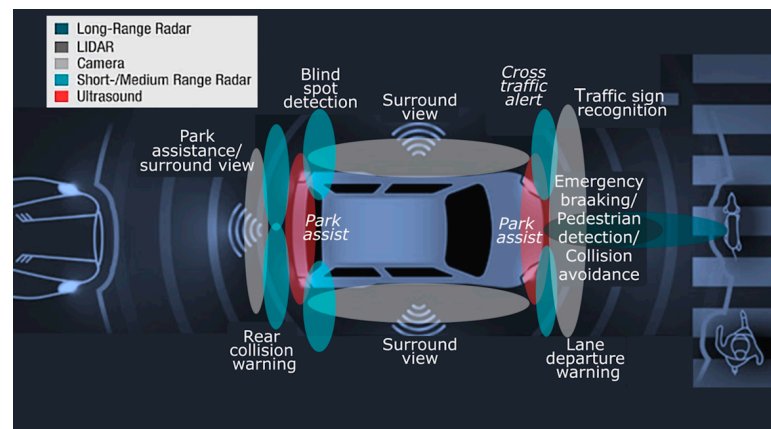


Figure 1. Typical sensor network architecture for autonomous driving systems.

Recent commercial radars exploit advanced SiGe BiCMOS technologies to embed on a single chip the mm-wave radio front-end and the digital interface [4–8]. However, modern nanometer CMOS technologies provide high-speed digital processing capabilities besides non-volatile memories, thus resulting in the most suitable solution for the implementation of low-cost and high-performance W-band sensors [9–14]. Unfortunately, the low-supply voltage, high flicker noise, and low-cost back-end-of-line (BEOL) of CMOS technologies strongly affect RF circuit design, especially at mm-wave frequencies, with respect to their SiGe BiCMOS counterpart [4,15].

In this paper, circuit topologies and design tradeoffs for both the RX and TX sections of a 77 GHz radar sensor are presented. The paper is organized as follows. Section 2 deals with the system analysis of a 77 GHz radar sensor and the related design challenges. Section 3 provides an overview of scaled CMOS technologies, with a special focus on the fully depleted (FD) silicon-on-insulator (SOI) CMOS platform. Section 4 discusses the implementation of a 77 GHz RX and TX front-end in a 28 nm FD-SOI CMOS. Finally, the main conclusions are drawn in Section 5.

2. System Analysis

Radar sensors properly exploit RF signals to detect objects located in the surrounding environment. Basically, they transmit an electromagnetic wave and receive the echo signal reflected by the target (i.e., any kind of obstacle) to determine its position and speed. Automotive radars usually adopt the FMCW scheme, which means they use a continuous wave (CW) frequency-modulated (FM) signal to provide the time reference suitable for target detection, as shown in Figure 2a.

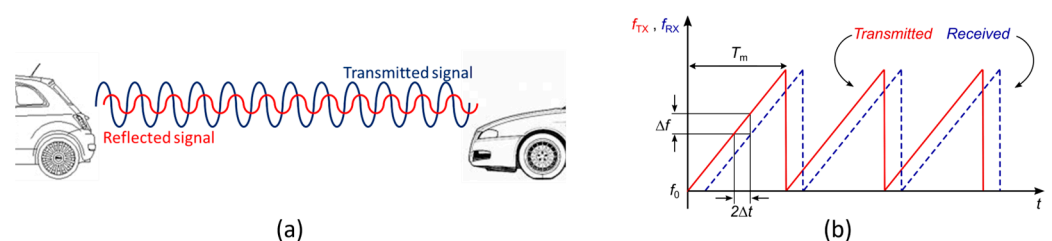


Figure 2. Automotive radar sensor: (a) operating principle, (b) target detection in FMCW radar systems.

Indeed, as depicted in Figure 2b, the time of flight of the transmitted signal Δt (i.e., the time it takes to get the target), and ultimately the distance d between sensor and target,

are linked to the frequency difference, Δf , between the transmitted and echo signals by the following equation:

$$d = \frac{cT_m}{2B}\Delta f \quad (1)$$

where c is the light speed, whereas B and T_m are the modulation bandwidth and period of the transmitted signal, respectively. It is worth noting that the radar resolution, i.e., the minimum detectable distance, $d_{\min}$, is set by B , given the minimum detectable Δf ($\Delta f_{\min}$). Therefore, a high resolution needs a wide-bandwidth transmitted signal. Next-generation automotive radar sensors will call for 10-cm resolution to accomplish the S/MR functionalities. This will lead to a modulation bandwidth requirement, and hence to a local oscillator tuning range (TR), as high as 4 GHz, assuming for T_m and $\Delta f_{\min}$ typical values of 10 μ s and 100 kHz, respectively. As far as the maximum detectable distance, $d_{\max}$, is concerned, it is dictated by a tradeoff between the receiver noise performance and the transmitted power, P_T . Indeed, the lower the P_T , the better should be the RX sensitivity, SRX, for a given detection distance. Specifically, the receiver input power, P_R , achieved with the echo signal is from the radar theory [16]:

$$P_R = \frac{\sigma G_T G_R \lambda^2}{(4\pi)^3 L_{ATM} d^4} P_T \quad (2)$$

where G_T and G_R , are the transmitter and receiver antenna gains, λ is the signal wavelength, L_{ATM} is the atmospheric propagation loss, and σ is the radar cross section of the target. For medium/long-range scenario in which d ranges from 250 m to 2 m, the echo signal power spans from about -110 dBm to -30 dBm. This input power range is evaluated by considering typical values for G_T/G_R , P_T (i.e., 20 dBi and 13 dBm, respectively), and the propagation loss and radar cross section (i.e., 0.3~0.5 dB/km and 30 m², respectively) [17,18]. This means that the receiver input signal can achieve a very low minimum level along with a wide range of variation (i.e., 80 dB). Furthermore, FMCW architecture suffers highly from TX-to-RX crosstalk [11,19,20], which leads to a blocking signal at the receiver input, whose power level is much higher than the received echo power level. Assuming a 20-dB attenuation between TX and RX, the blocking signal power is as high as -10 dBm [21]. Of course, detecting a signal with a large variation and an extremely low minimum level is a critical task, which turns out to be even more critical due to the RX-to-TX crosstalk. Consequently, severe constraints must be met both at the receiver level in terms of gain, noise, and linearity and at the local oscillator level in terms of phase noise (PN) and tuning range. Indeed, the RX sensitivity performance of -110 dBm calls for a local oscillator with a PN performance lower than 90 dBc/Hz at 1 MHz offset frequency [22], assuming a receiver NF of around 11 dB.

3. Overview of 28 nm FD-SOI Technology

The adoption of scaled CMOS technologies is crucial to allowing the implementation of system-on-chip (SoC) radars that feature a high-performance mm-wave front-end, a wide-band analog baseband, an analog-to-digital converter, and a high-speed digital processing interface. Although SoC implementations of 77 GHz radars using conventional bulk CMOS platforms [23–25] have already been reported, the FD-SOI CMOS technology provides a more suitable solution for analog/mm-wave designs thanks to better inherent transistor gain, lower flicker noise, and a higher transition frequency (f_T), along with a low threshold voltage (V_T), which enables low-voltage operation [12,26,27].

Figure 3a shows a simplified cross-section of the 28 nm FD-SOI CMOS technology by STMicroelectronics [12], which provides a low-cost standard back end of line (BEOL) with eight Cu-metal layers and a top aluminum one, and 5-fF/ μ m² metal-oxide-metal (MOM) capacitors. Transistors are fabricated in a 7 nm layer of silicon sitting over a 25 nm buried oxide (BOX). An ultra-thin body (UTB) provides an electrically isolated conduction channel between source and drain. The technology features flipped-well low-

V_T transistors, which use n-well and p-well bodies for n-MOS and p-MOS transistors, respectively, as shown in Figure 3a. In these devices, the buried oxide with the n-well and p-well body terminals (i.e., back-gate terminals) acts as a second transistor gate that allows the threshold voltage, V_T , to be properly varied. The body gain factor, namely the sensitivity of V_T over the body voltage variation, is around 90 mV/V, which is much higher than in conventional bulk technology (25 mV/V). The lower V_T of flipped-well devices is beneficial for low-voltage operation, whereas V_T tuning capabilities can be profitably exploited to compensate for process, voltage, and temperature variations (PVTs) [28–31]. However, the lack of dedicated thick-copper metal layers in the BEOL, typically available in SiGe BiCMOS technologies [6,32], makes crucial passive component design and layout arrangements (e.g., signal paths, power supply and ground interconnections, etc.), which greatly affect the performance of mm-wave ICs.

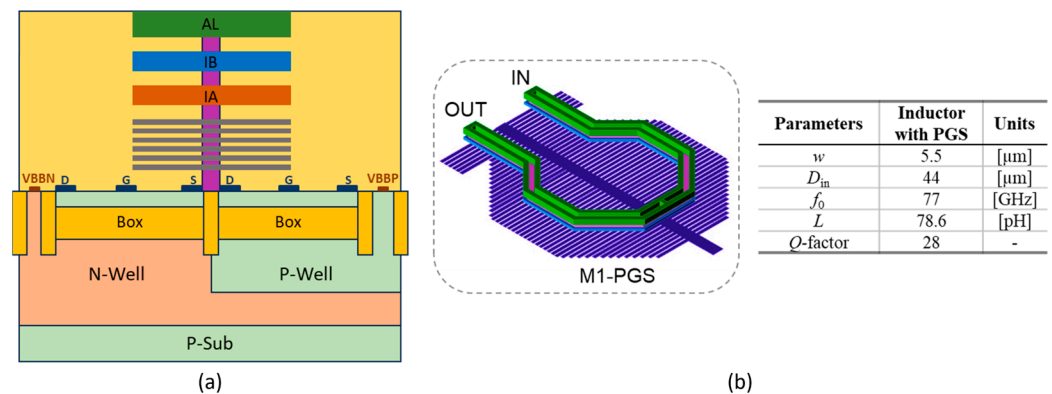


Figure 3. FD-SOI CMOS technology platform: (a) front-end and back-end cross-section, (b) multi-layer inductor and performance with and without PGS.

The inductive components (i.e., transformers and inductors) in this technology can take advantage of a multi-layer structure that exploits the last three-metal layers on top of the stack, i.e., aluminum top metal (LB), metal 8 (IB), and metal 7 (IA), which are the thickest available metal layers in the adopted technology. In this way, losses and parasitic capacitances are minimized [33]. A patterned ground shield (PGS) performed with the lowest metal layer (M1) could also be included beneath the inductor area, as shown in Figure 3b. However, substrate shielding in this technology is not effective since it increases substrate losses and reduces the self-resonant frequency (SRF) [34].

4. CMOS ICs for 77 GHz Automotive Radar

The mm-wave front-end of a 77 GHz CMOS radar sensor exploits a direct conversion scheme to achieve a high integration level along with low power consumption. However, this architecture suffers from LO pulling due to the high power transmitted by the power amplifier and the limited substrate isolation, especially at mm-wave, which may cause the PA signal to leak into the VCO, thus corrupting the LO spectrum. To overcome this limitation, a frequency-doubled architecture is used, which adopts an LO at half of the operating frequency (i.e., around 38 GHz), followed by a frequency doubler that drives the PA with the 77 GHz carrier. This avoids the VCO frequency pulling, thus improving PN performance and ultimately the receiver sensitivity [22,35,36].

4.1. Design of 77 GHz Receiver with TX Leakage Suppression

The design of a 77 GHz receiver for automotive radar sensors is very challenging. Indeed, there are stringent requirements in terms of noise figure, linearity, and gain, which are even more difficult to fulfill due to the voltage headroom limitations posed by a scaled CMOS technology. In this scenario, mixer-first direct-conversion architectures can be profitably exploited to achieve the best tradeoff between NF and linearity while providing high-gain performance. Of course, RF amplification before frequency down conversion

would greatly reduce the noise requirements of the mixer and simplify the achievement of high gain. However, this approach greatly impacts the linearity performance and can hardly achieve the required attenuation of the TX-to-RX blocker. Figure 4a displays the simplified block diagram of a 28 nm FD-SOI CMOS mixer-first receiver for 77 GHz automotive radar. It is made up of a 77 GHz down-converter, a VGA, and a 7th-order low-pass SC filter. The down-converter (see Figure 4b) consists of a voltage-to-current (V-I) converter and a current-driven double balanced passive quad with an IF active load performed by a transimpedance amplifier. The down-converter also embeds a leakage canceller to overcome the TX-to-RX crosstalk issue [37]. Specifically, the mm-wave V-I converter provides at its output a signal current proportional to the RF input voltage, which is fed to the passive quad for frequency down-conversion. The IF current at the down-converter output is injected into the virtual ground of the transimpedance amplifier, which performs a current-to-voltage (I-V) conversion with signal amplification. The leakage canceller is performed by a current-mode feedback loop operating at low frequency, which achieves leakage compensation by generating a proper replica of the leakage currents ($I_{IF,lkg}^+$ and $I_{IF,lkg}^-$) at the transimpedance amplifier inputs. In such a way, injection into the amplifier's virtual ground inputs of the leakage current is avoided, thus preventing down-converter saturation and allowing better RX linearity as well as higher gain performance to be achieved. Specifically, as displayed in Figure 4b, the V-I converter consists of a pseudo-differential common-source stage using transformer T_1 for 50- Ω input impedance matching and transformer T_2 as resonant load. The current density and size of transistors $M_{1,2}$ are set to simultaneously achieve low noise and impedance matching [38]. Accordingly, 28 nm transistors are used with a channel width of 36 μm and a bias current of around 5 mA.

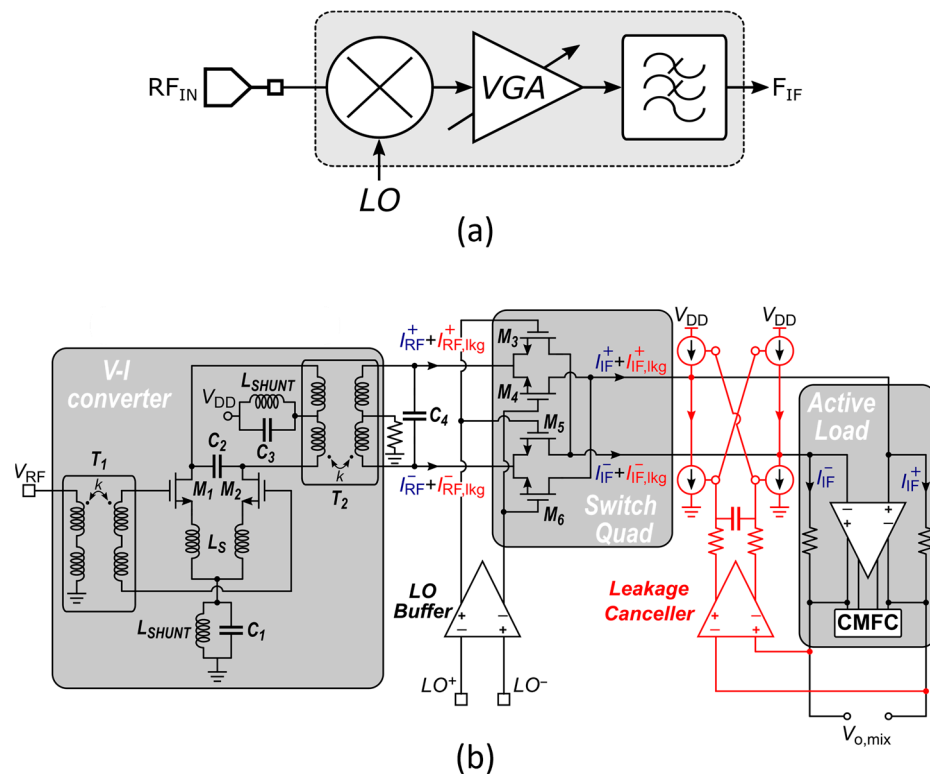


Figure 4. Simplified schematic of the 77 GHz receiver: (a) block diagram, (b) Simplified schematic of the down-converter [21].

The switch-based mixer quad guarantees low flicker noise with substantial power savings. Minimum channel length transistors are used for the quad transistors $M_{3,6}$ with a channel width of 36 μm to draw the high-level TX leakage current while keeping a relatively low drain–source voltage drop. The down-converter active load is implemented

by a three-stage transimpedance amplifier and includes the TX leakage canceller. The latter exploits voltage-controlled current sources, which are shunted to the transimpedance amplifier input and driven by an error amplifier that is connected to the down-converter output. A low-pass filter between the error amplifier and the current sources provides loop-gain frequency compensation and limits the canceller band properly to preserve the IF signal. Finally, an output common-mode feedback control loop (CMFC) stabilizes output bias voltage and guarantees maximum output swing. The down-converter provides a maximum voltage gain as high as 29 dB.

The mm-wave side layout is crucial for the down-converter noise and gain performance, especially for CMOS implementations using standard low-cost mm-wave BEOL. Figure 5a shows the layout of the 77 GHz V-I converter passive circuitry. Transformer T_1 adopts a stacked configuration, which achieves insertion loss as low as 1.9 dB, as displayed in Figure 5b. An interleaved structure is instead adopted for T_2 to increase the down-converter conversion gain by profitably exploiting the transformer turn ratio. Moreover, shunt LC resonators are used to increase isolation from ground and power supply disturbances. It is worth noting that both L_{SHUNT} and L_S adopt multilayer folded spirals to trade off quality factor and area while minimizing parasitic effects. The electrical parameters of inductors and transformers used in the down-converter design are given in Figure 5c.

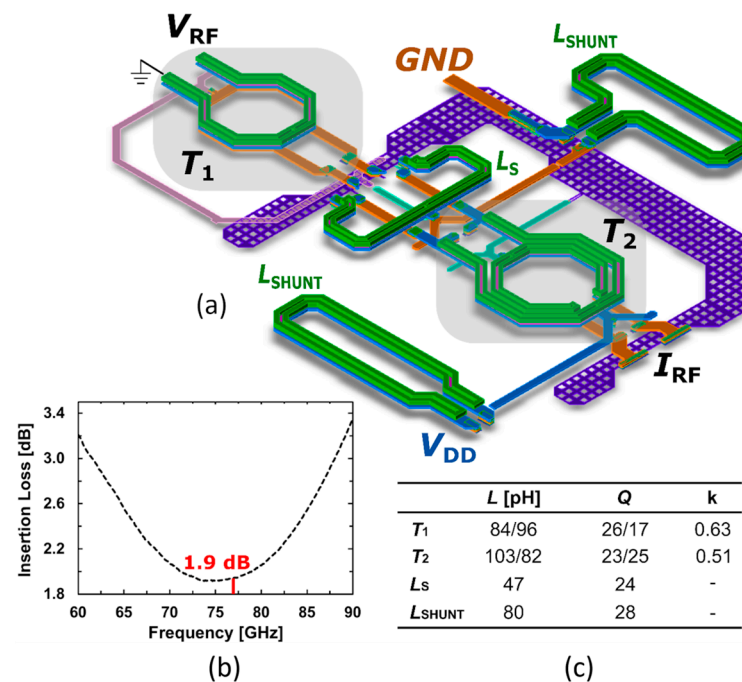


Figure 5. Down-converter passive circuitry: (a) layout view, (b) input insertion loss, (c) electrical characteristics of integrated transformers and inductors [21].

The VGA is made up of three dc-coupled gain stages and provides digitally controlled voltage amplification. It exploits the effective threshold voltage variation through the body terminal of the adopted technology to perform a control loop for the offset compensation. Specifically, a feedback error amplifier properly drives the body terminal of the input pair, $M_{1,2}$, thus forcing a threshold voltage difference that is equal to the offset value. A low-pass RC network provides frequency compensation and limits the loop band to preserve the signal's low-frequency components. It is worth noting that this approach achieves offset compensation without affecting the signal path and with negligible contribution to the VGA noise performance since the body transconductance is much lower than the input-stage transconductance [39]. An output CMFC sets the output bias voltage accurately and maximizes the output swing. The VGA guarantees a maximum gain of 44 dB with a gain range of 30 dB. Gain variation is achieved by controlling the resistive load and the input

pair transconductance of both the first and second gain stages. A further 12 dB gain step is provided on the down-converter side, thus achieving an overall gain variation of 42 dB for the RX chain.

Finally, the VGA is followed by a low-pass filter, which provides anti-aliasing feature, while rejecting out-of-band undesired signals. To reduce sampling frequency and hence power consumption in the external ADC, a 7th-order SC filter is used, which guarantees high linearity and accuracy against PVT variations with a negligible impact on the receiver NF thanks to the overall high gain achieved by the down-converter and VGA. The simplified schematic of the basic biquad cell of the SC filter is displayed in Figure 6b. The filter operates with a sampling frequency, f_s , up to 200 MHz and exploits a double sampling technique to reduce the current consumption. The filter provides a passband up to 20 MHz along with an out-of-band attenuation of around 40 dB at 2 MHz from the passband boundary [40]. The receiver core die is shown in Figure 7. Its silicon area occupation is $1.2 \times 0.8 \text{ mm}^2$ also including a 50Ω buffer for the 77 GHz LO signal. The receiver draws an overall quiescent current as low as 27 mA from a 1 V supply voltage and provides a maximum gain up to 75 dB with a linear-in-dB variation down to 33 dB with a 3 dB step. The noise figure is as low as 8.2 dB. Despite the low supply voltage, an excellent blocker immunity of -9.5 dBm is achieved, along with an output 1-dB compression point as high as -1.5 dB_V for all gain settings.

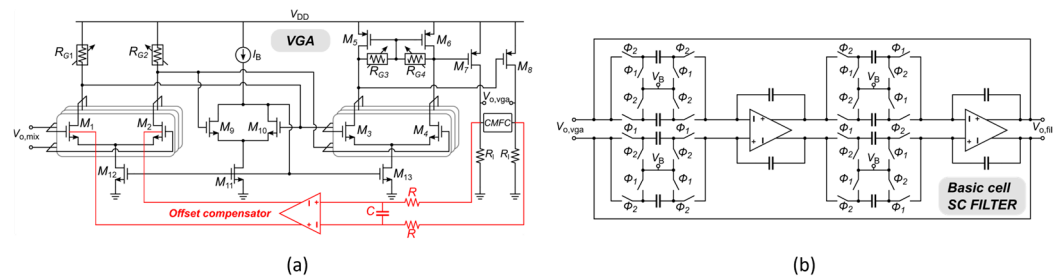


Figure 6. Schematic of the receiver baseband: (a) simplified schematic of the VGA [39], (b) SC filter basic cell [40].

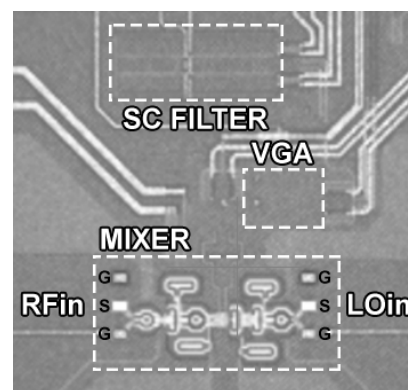


Figure 7. RX die micrograph [21].

Table 1 summarizes the measured receiver performance while comparing it with recent state-of-the-art works. The proposed receiver exhibits the best-in-class power consumption (i.e., 27 mW) and linear output swing (i.e., almost 1 V), along with very good noise performance. Better noise performance is achieved in [24], thanks to the use of an LNA, but at the cost of poor linearity performance.

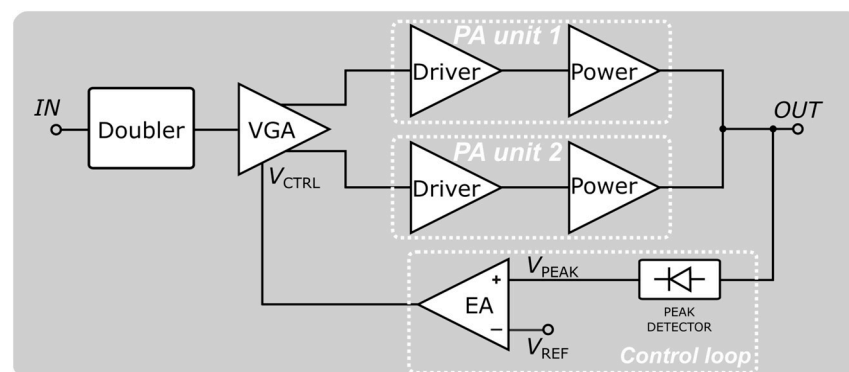
Table 1. Performance summary and comparison with the state-of-the-art RX.

	[23]	[24]	[25]	This Work
Technology	65 nm CMOS	65 nm CMOS	45 nm CMOS	28 nm SOI CMOS
Architecture	LNA-MIXER-VGA-LPF	LNA-MIXER	LNA-MIXER-VGA-LPF	MIXER-VGA-LPF
Operating frequency [GHz]	77	77	77	77
Power supply [V]	1 (Down-converter) 1.2 (IF Baseband)	1	1.3 (Down-converter) 1.8 (IF Baseband)	1
Power consumption [mW]	30 ^(a)	60	-	27 ^{(a)(b)}
Max gain [dB]	101	32	48	75
Gain variation [dB]	53	-	24	42
Gain step [dB]	6	-	2	3
IF bandwidth	5 MHz	300 MHz	175 kHz ÷ 15 MHz	50 kHz ÷ 20 MHz
Noise figure [dB]	8 (@3 MHz)	5.8 (@10 MHz)	14 (@1 MHz)	10.5 (@1 MHz) 8.2 (@10 MHz)
OP1dB [dBV]	-	−16 (IP _{1dB} = −37 dBm)	−9 (IP _{1dB} = −22 dBm)	−1.5 (IP _{1dB} = −23.5 dBm)
Blocker immunity [dBm]	-	-	−8	−9.5

^(a) Excluding LO buffer current consumption; ^(b) 20 MHz IF bandwidth.

4.2. Design of 77 GHz Transmitter for Automotive Radar Sensors

The transmitter is a key component of the radar sensor since it constrains the sensitivity performance as well as the overall power consumption. The transmitter design at mm-wave takes advantage of stacked-cascode gain stages with a doubled supply voltage with respect to its nominal value. This approach guarantees the best tradeoff among gain, output power performance, and current consumption since a higher output resistance and a transistor optimum bias condition (namely, optimum current density and maximum drain source voltage) are achieved [22,41,42]. To this end, the bias voltage of the common-gate transistor is set to equally share the supply voltage between the drain-source voltages of the stacked transistors. This condition also guarantees safe operation for the cascode amplifying stage. The block diagram of the transmitter is shown in Figure 8. It consists of a frequency doubler driving a two-way power amplifier arranged in a current-combining scheme to increase the power delivered to the load.

**Figure 8.** Block diagram of the 77 GHz transmitter.

As mentioned above, frequency doubling is a core feature of the TX since it allows preventing VCO pulling thus improving the PN performance of the local oscillator. Push-push topologies based on single-ended common-source V-I converter are widely used to implement frequency doublers at mm-wave due to their high performance in terms of

output signal magnitude and very low power consumption [43]. However, mm-wave single-ended circuits suffer from high sensitivity over the impedance of the supply paths, namely the routing paths used to locally provide VDD and GND to the circuitry. Actually, an equivalent impedance as low as $20\ \Omega$, which could come from a parasitic inductance in the supply lines of 40 pH, can drastically reduce the output signal amplitude at 77 GHz [22]. Unfortunately, controlling such impedances is not a trivial task at 77 GHz, especially in highly complex systems such as radar sensors. To overcome this issue, the AC-isolated push-push frequency doubler displayed in Figure 9a was proposed [44], which exploits a cascode V-I converter, $M_{1,4}$, driving a load resonant transformer, T_1 . The minimum channel length is set for $M_{1,4}$ to guarantee optimum frequency response, whereas a channel width of $12\ \mu\text{m}$ is used for a fair trade-off between conversion gain and power consumption. Transformer T_1 adopts a stacked configuration to achieve the highest magnetic coupling, k , thus increasing the power transfer to the load. Shunt resonators, $L_{\text{SHUNT}}\text{-}C_{\text{SHUNT}}$, and series resonators, $L_0\text{-}C_0$, are profitably used to guarantee AC-decoupling of the inner circuitry from the supply paths while providing the output current, i_{RF} , with a low impedance path. This prevents i_{RF} from being injected into the parasitic supply impedances. The 3-D view of the passive circuitry of the frequency doubler is shown in Figure 9b, along with the electrical parameters of the related inductive components.

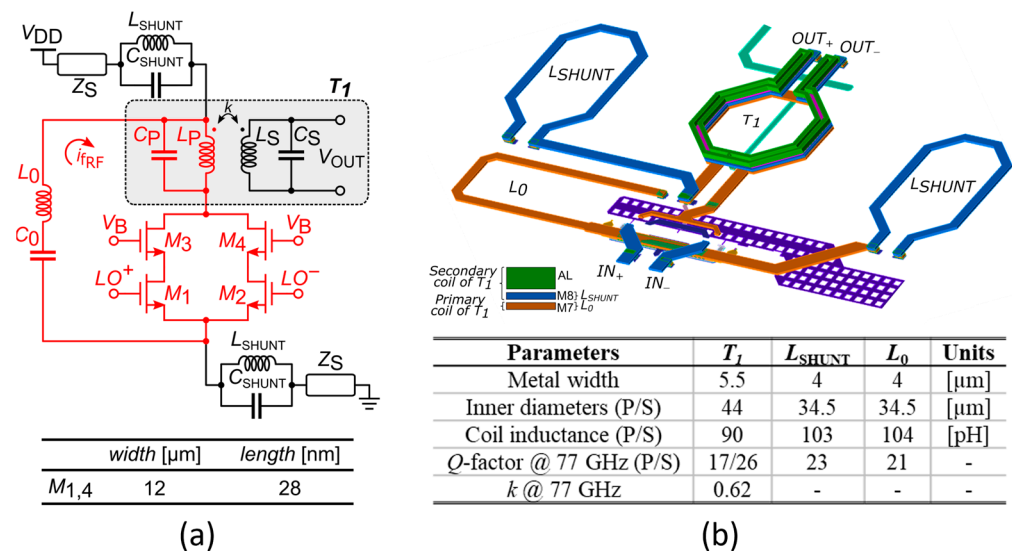


Figure 9. Frequency doubler: (a) simplified schematic, (b) layout and electrical parameters of inductive components [22].

The power amplifier is crucial for the achievement of the maximum operating range in radar sensors. Indeed, next-generation self-driving systems call for PA maximum power levels as high as 13 dBm, as mentioned in Section 2. However, the PA performance is affected by the package insertion loss and PVT variations, which cause a reduction in the output power of around 1 and 3 dB, respectively. Therefore, the PA should be able to deliver an output power of around 17 dBm to guarantee the requirement of 13 dBm at the antenna. To meet such a high output power requirement, a 2 V two-way PA was exploited [22]. It consists of two PA units arranged in a current-combining scheme, which are driven by a VGA that performs a feedback loop to properly set the PA output power according to the targeted application (i.e., S/MR or LR applications). A simplified schematic of the PA is displayed in Figure 10a. It comprises a driver and a power stage. The two driver stages exploit a common-source pair, $M_{1,2}$, with neutralization capacitors, C_n , for improved stability performance. They take advantage of a transformer-based current reusing arrangement to reduce current consumption and then boost PA efficiency. The power units adopt a stacked cascode stage, M_{3-6} , with series inductors L_N between the common-source and common-gate stages to compensate for the parasitic capacitance in the

interstage node, thus increasing the power delivered to the load. Figure 10b gives a 3-D view of the passive circuitry of the PA along with the electrical parameters of the adopted inductive components.

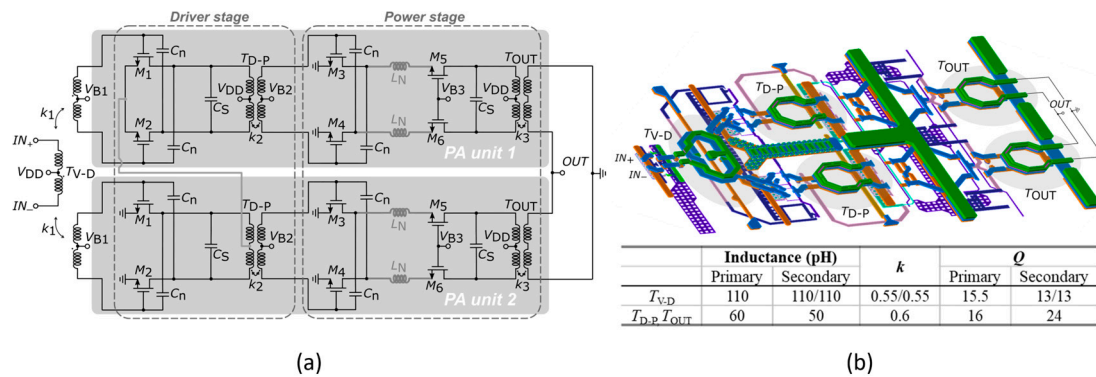


Figure 10. PA power stage: (a) simplified schematic, (b) PA layout and electrical parameters of inductive components [22].

A simplified schematic of the VGA is shown in Figure 11a. It is made up of a cascode differential amplifier with the common-gate stage implemented with a pair of source-coupled transistors, $M_{2,3}$, which allows partitioning the signal current between the three-coil load transformer, T_{V-D} , and the supply voltage thanks to the control signal, V_{CTRL} . The load transformer is made up of a primary coil and two secondary coils, which split the VGA output signal into the inputs of two PA units. V_{CTRL} is properly set by the feedback loop according to the reference voltage, V_{REF} (see Figure 8). The feedback path is mainly composed of a peak detector and an error amplifier (EA). Specifically, the peak detector provides the error amplifier with a dc voltage, V_{PEAK} , that is strictly related to the PA output power. The high-gain control loop sets V_{PEAK} equal to V_{REF} , thus forcing the PA to deliver the desired power to the output load. This allows adjusting the PA output power according to the addressed application by merely changing V_{REF} . Loop stability is achieved by a dominant pole compensation performed by the capacitor C_C . Figure 11b shows a simplified schematic of the peak detector. It uses an AC-coupled common-drain stage, M_1 , to perform peak detection of the PA output voltage at its source node. The transistor replica, M_2 , is used as a level shifter for V_{REF} to provide the EA with a differential input voltage that is compensated against process and temperature variations. Indeed, such variations appear as common-mode signals at the input of the error amplifier, and hence they are rejected.

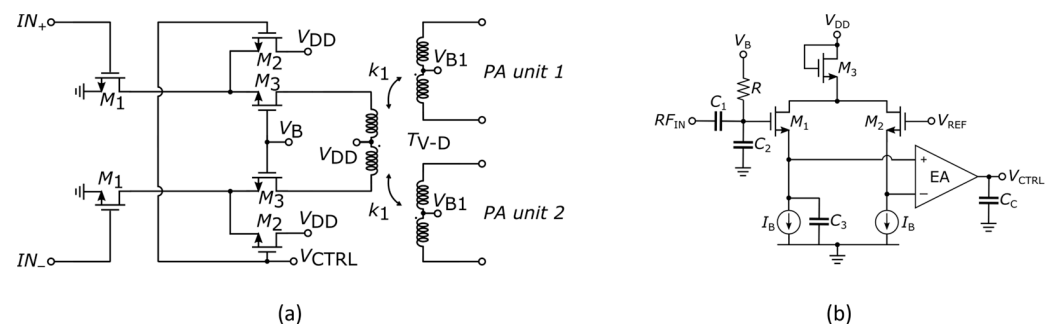


Figure 11. Circuitry of the PA power control loop: simplified schematics of the (a) VGA with the load transformer and (b) peak detector [22].

The transmitter silicon core area is $0.5 \times 0.3 \text{ mm}^2$ and is shown in Figure 12. It operates with a 2 V supply voltage and can deliver a maximum output power as high as 17.5 dBm with a control range of around 13 dB. The overall power consumption is around 336 mW.

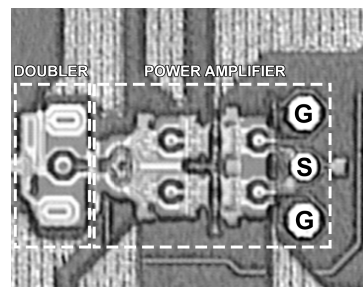


Figure 12. TX die micrograph.

Moreover, the output power is almost flat over a wide frequency range. Specifically, it exhibits a variation of around 2 dB in the band of interest, ranging from 76 GHz to 81 GHz [22].

Table 2 summarizes the TX experimental results while comparing them with the state-of-the-art of 77 GHz CMOS works. The proposed TX exhibits the highest saturated output power along with the best drain efficiency performance ($P_{\text{sat}}/P_{\text{dc}}$).

Table 2. Performance summary and comparison with the state-of-the-art TX at 77 GHz.

Reference	Technology	Features	P_{out} [dBm]	P_{dc} [mW]	$P_{\text{sat}}/P_{\text{dc}}$ [%]
[2]	65 nm CMOS	1-TX 1-RX	13	-	-
[9]	40 nm CMOS	3-TX 8-RX	14.1	-	-
[23]	65 nm CMOS	1-TX 1-RX	13	175	11.4
[24]	65 nm CMOS	2-TX 6-RX	13.7	381	6
[45]	65 nm CMOS	1-TX	8.9	117 ⁽¹⁾	6.8
This work	28 nm CMOS	1-TX	17.5	336	16.7

⁽¹⁾ TX + PLL.

4.3. Transformer-Based VCO

Simultaneously fulfilling both S/MR and LR applications calls for VCOs with a low PN and a wide TR, whose design is very challenging due to the relatively low Q-factor of the LC resonators at mm-wave and the high parasitic capacitance of large transistors required to sustain the oscillation. Moreover, the high conversion gain (k_{VCO}) in wide-band VCOs [46,47] reduces the VCO PN performance due to a high AM-to-PM conversion [48] and makes it very difficult to address both LR and S/MR applications with the same local oscillator. However, wide TR and low PN are not simultaneously required. Indeed, the stringent PN requirement is demanded only by the LR application in the narrow frequency band ranging from 76 to 77 GHz. Consequently, a dual-band VCO is the most viable option to meet the requirements of both S/MR and LR applications. Several dual-band VCOs based on switched components have been proposed, such as switched inductors (SL) [49] and switched capacitors (SC) [45]. These solutions rely on a shunt switch, SW , embedded in the VCO tank to enable/disable either a capacitor or an inductor, thus properly shifting the VCO tuning curve, as shown in Figure 13.

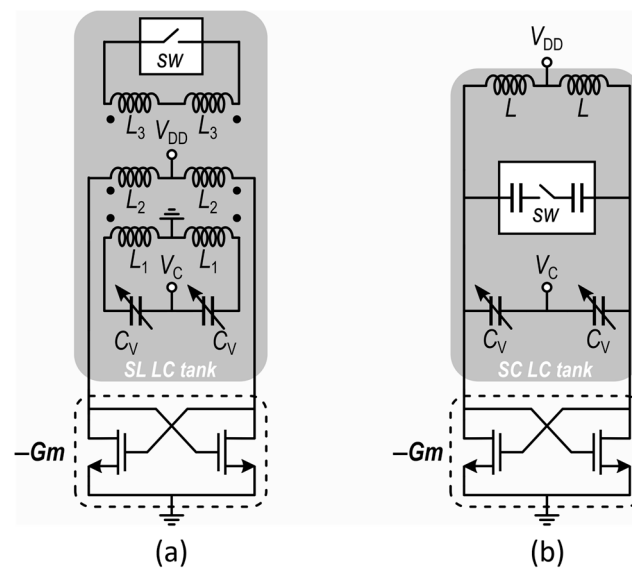


Figure 13. Dual-band VCO: (a) switched-inductor solution, (b) switched-capacitor solution.

However, SW considerably increases both resistive losses and parasitic capacitances of the VCO tank, thus affecting PN and limiting the maximum VCO operating frequency and TR. To overcome this issue, the switched core solution proposed in [50] can be used, which takes advantage of two different VCOs, each one operated with an LC-tank that is designed to address a specific application (i.e., LR or S/MR applications). This allows both SM/R and LR requirements to be fulfilled at the cost of a larger silicon area occupation and higher system complexity. These limitations can be overcome with the dual-band VCO tank structure shown in Figure 14 [51].

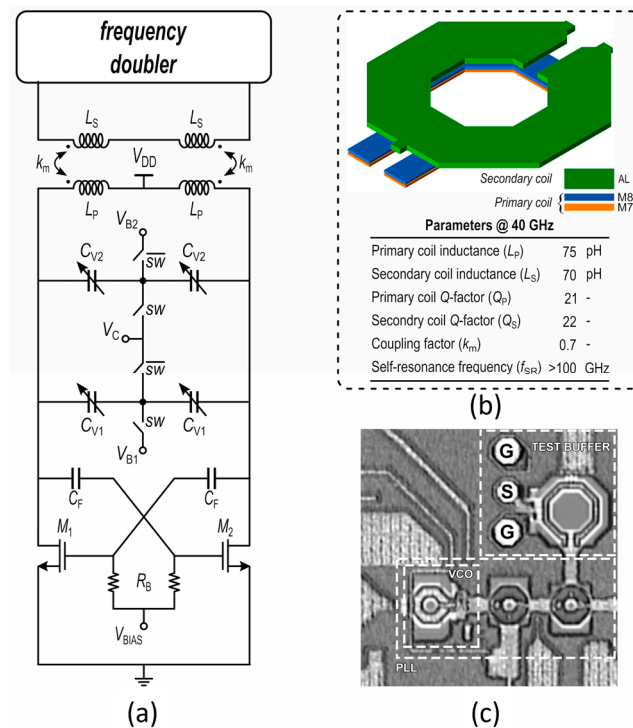


Figure 14. Transformer-based dual-band VCO [22]: (a) simplified schematic, (b) transformer layout and electrical parameters, (c) die micrograph.

The VCO adopts a single-core cross-coupled topology operated at a 1 V supply voltage to reduce power consumption. It exploits a dual-band tank that takes advantage of a

couple of varactors, C_{V1} and C_{V2} , which are alternatively enabled by means of the band selector switches, SW and $\overline{SW}$, which are placed in the common-mode terminal of the VCO tank. This allows dual-band operation to be achieved without affecting both VCO maximum operating frequency and TR and with a negligible impact on PN performance. The basic idea is to use the enabled varactor C_{V1} (C_{V2}) to cover the LR (S/MR) band, whereas the disabled varactor C_{V2} (C_{V1}) acts as a fixed capacitor, allowing the tuning curve to be properly shifted. To this end, a control voltage, V_C , is applied to the enabled varactor, whereas the disabled varactor is connected to a bias voltage (i.e., V_{B1} or V_{B2}) to provide a proper fixed capacitance according to the addressed sub-band. The VCO core is based on an NMOS topology with a transformer-coupled tank. It uses a cross-coupled differential pair, $M_{1,2}$, which is operated in the class-D way with the aim of improving PN performance by maximizing oscillation amplitude [22]. To this end, the transistor channel width and length are set to 28 μm and 45 nm, respectively. AC-coupling is used to implement the feedback path in the VCO active core. This allows setting the bias voltage, V_{BIAS} , to achieve a fair trade-off between the start-up condition and power consumption. The use of a tank transformer simplifies the interconnection of the VCO with the frequency doubler and avoids the parasitic capacitances of an ac-coupling approach based on capacitors [52,53]. It adopts a stacked configuration with octagonal windings, as shown in Figure 14b. The VCO operates at a 1 V supply voltage and exhibits a power consumption as low as 15 mW. It provides a TR spanning from 37.7 to 38.6 GHz and from 38.3 to 40.7 GHz in the LR and S/MR band, respectively, while the varactor control voltage is swept from 0 to 1 V. The PN performance is about -99 dBc/Hz and -94 dBc/Hz at 1 MHz offset frequency from the 38 GHz carrier, which translates into a PN performance of -93 dBc/Hz and -88 dBc/Hz at 1-MHz offset frequency from the 77 GHz carrier for the LR and S/MR bands, respectively. The VCO silicon core photo is shown in Figure 14c.

Table 3 summarizes the VCO experimental results while comparing them with the state of the art. As apparent, the proposed VCO exhibits best-in-class PN performance while guaranteeing a 6 GHz bandwidth.

Table 3. Performance summary and comparison with the state-of-the-art VCO.

Reference	Technology	Frequency [GHz]	77 GHz PN @1 MHz [dBc/Hz]
[2]	65 nm CMOS	$77 \div 81$	-91
[9]	40 nm CMOS	$76 \div 77$	-91
[23]	65 nm CMOS	$76.9 \div 78.8$	-81
[45]	65 nm CMOS	$76.8 \div 78$	-91.2
This work	28 nm CMOS	$75.5 \div 81.5$	-93

5. Conclusions

Nanoscale CMOS technologies promise to lower the implementation costs of the next generation of automotive radar sensors, thus boosting the development of future self-driving systems. This is mainly due to the higher integration level and high-speed processing capabilities that can be achieved with CMOS implementations over their conventional SiGe BiCMOS counterparts. Specifically, 28 nm FD-SOI CMOS has proven to be a very promising option for the implementation of high-performance mm-wave front-end able to cope with both short/medium- and long-range applications. Actually, as detailed in this paper, excellent performance in terms of gain, linearity, noise, and good PN and TR

performance, along with very high output power, have been achieved for a 77 GHz radar receiver and transmitter, respectively.

Future trends in automotive radar sensors envisage the adoption of phased array systems. Research efforts are currently focused on the design of high-precision phase shifters that set the signal phase in each element of the phased array, thus allowing better localization of the target and finally enabling autonomous driving systems to be developed.

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