

Article

A High-Voltage Pulse Modulator Composed of SiC MOSFETs/IGBTs in a Hybrid Connecting State

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Abstract: In order to solve problems such as a slow switching speed, a high switching power, a loss of pure IGBT modulators, and the weak withstanding load short-circuit ability of pure SiC MOSFET modulators used for vacuum loads, this paper proposes a new scheme for high-voltage pulse modulators based on SiC MOSFET/IGBT hybrid connecting circuits. It has a low power loss like the pure SiC MOSFET modulator and a strong withstanding load short-circuit ability like the pure IGBT modulator. Firstly, the principle circuit of the hybrid connecting modulator are discussed and chosen. And the basic working processes of the hybrid parallel-series modulator is described in detail. Secondly, three key points in this new scheme are analyzed and designed as follows: the static and dynamic voltage sharing; the actualizing of the ZVS process for IGBTs; the improvement of short-circuit protection for SiC MOSFETs. A modulator consisting of 16-stage 1200 V-SiC MOSFETs and 1200 V-IGBTs in hybrid parallel-series states is tested. Based on the sample circuit, the working data, such as high-voltage pulse waveforms of 10 kV/2 KHz/10 μ s, static and dynamic voltage sharing, the driving control sequence, the U/I sequence of the IGBT, the short-circuit protection waveform, and the calculation, are obtained and discussed.

Keywords: high-voltage pulse modulator; SiC MOSFET/IGBT hybrid connecting circuit; short-circuit protection; ZVS



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1. Introduction

The high-voltage pulse modulator is a key unit in a circuit with a vacuum load [1–4]. Its main function is to convert high-voltage DC energy into the pulse output. The pulsed high-voltage electric field with specific parameters is used to accelerate particles to a high-energy state.

Many vacuum loads always need high-voltage pulses of 10–50 kV and a high repetition frequency of 500–100 kHz [5–8]. Also, these vacuum loads have the disadvantage of high short-circuit probability when working at high pulsed voltages [9,10]. Therefore, it is valuable to study a pulse modulator with a low power loss, fast rising time, and strong withstanding load short-circuit ability.

Researchers in the field of pulse power originally designed a high-voltage pulse modulator using a vacuum tube switch or thyatron. The two kinds of switches have certain limitations, such as a complicated auxiliary power supply circuit, a large volume, low power efficiency (about 60~70%), and the poor stability and adjustability of the pulse width and repetition. They are not particularly beneficial to the high-voltage pulse modulator.

With the rapid development of solid-state switches such as the GTO, IGBT, and MOSFET, the power consumption and volume are much lower and the circuit control is more flexible. Over the past decade in particular, silicon carbide (SiC) with a wide band gap, high electron drift rate, and high-voltage withstanding strength has emerged. This represents an advancement in the development bottleneck of solid-state switching devices at higher temperatures, voltages, and switching frequencies [11,12]. It is becoming a development trend of power semiconductor devices in the future.

Figure 1 shows a classic pulse power circuit schematic as follows: S is a series high-voltage modulator switch assembly controlled by a driving control unit; C is an energy storage capacitor; R_1 is a current limiting resistor for C; R_L is a load resistor; and R_2 is an over-current limiting resistor for S when R_L is sparking too short. It works as follows: the high-voltage capacitor C is charged to the required high voltage, and the pulsed high voltage can be obtained at the load R_L via controlling the opening and closing of S. When the load is sparking, R_2 can suppress the transient over-current and protect the solid switches in S from degrading or being damaged. Inevitably, there is a large amount of power loss in R_2 in the case of a big duty cycle. The driving control unit is designed to output the synchronized switch drive signals. It is a key point for maintaining the series switch voltage evenness in a large body of the literature. As an example, the magnetic isolation drive is a passive and economic one, which can be used to easily obtain synchronized switch drive signals. Its principle is transmitting signals to S with two channel transformers, one for opening and the other for closing. The time delay between the “Open signal” and “Close signal” is the pulse width τ . It is shown at the bottom of Figure 1.

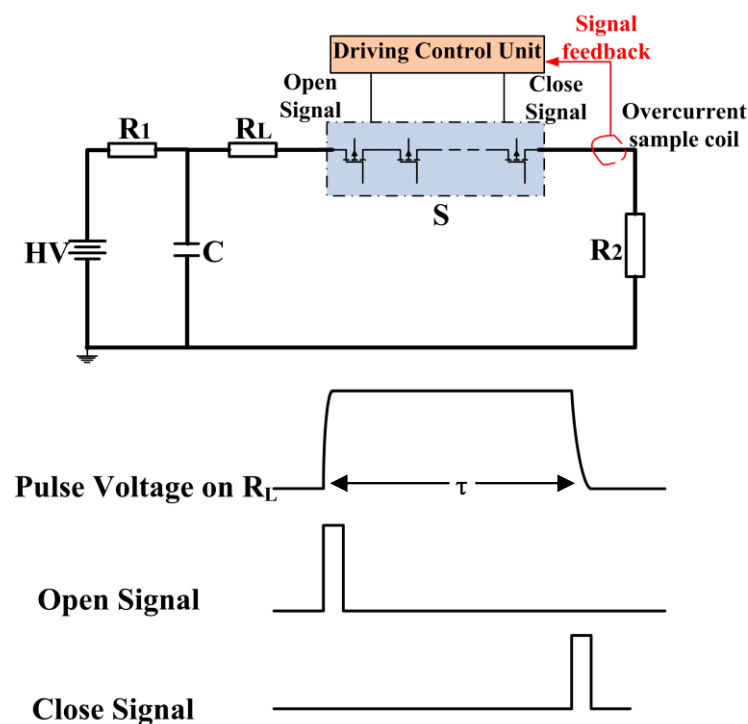


Figure 1. Schematic diagram of the pulse power circuit and control sequence.

When compared with a vacuum tube switch or thyatron, the high-voltage pulse modulators using solid state switches [13–17] such as IGBTs have outstanding advantages, including flexible parameter adjustments, low power consumption, small sizes, and strong withstanding load short-circuit ability. However, due to the switching loss of IGBTs when working at kHz, it is necessary to assemble heat sinks for each switch to ensure that the internal junction heat is conducted to the outside. Especially for switches with 1700 V and above, with tens of ampere, the fins on the heat sinks are wide. The distance between the high-voltage components must be increased to avoid high-voltage breakdown. Therefore, when designing high-voltage pulse modulators with a high repetition frequency, it is a common choice to choose a large number of 800–1700 V IGBTs in the series.

The control method of SiC MOSFETs is similar to IGBTs, based on Figure 1. At present, the rated voltage of commercial discrete SiC MOSFETs is mostly 800–3300 V, and the switching power consumption is about 10–30% of IGBTs with the same voltage level and package volume. For example, 3300 V SiC MOSFET discrete devices can be used in high-repetition frequency high-voltage modulators with much lower power loss levels than

in IGBTs. At kHz repetition frequency, the required heat sink structure is simple, and could even be ignored. And the series number is half of that of a modulator with a 1200 V IGBT [18].

Although the SiC MOSFET has many outstanding advantages when compared with IGBTs, its disadvantages are also obvious, as follows: SiC MOSFETs with the same rated voltage can withstand lower over-currents than IGBTs, and its price is 5–10 times that for IGBTs [19]. Because the vacuum load sparks frequently, the over-current will flow through the series switches in the modulator. The SiC MOSFETs could be degraded or even be damaged after many short circuits [20–22]. One method for limiting over-currents is increasing R_2 in Figure 1. However, the power loss and volume of R_2 will increase to a huge value. So, a pure series SiC MOSFET pulse modulator scheme is an expensive and time-consuming method, and is not a better design than series IGBT pulse modulators.

In order to make full use of the advantages of SiC MOSFETs and IGBTs, this paper proposes a high-voltage pulse modulator based on SiC MOSFETs/IGBTs in hybrid connecting states. The two branches of SiC MOSFETs and IGBTs are independently controlled using magnetic coupling driving signals.

There are three designing key points in this new scheme being analyzed and verified as follows:

1. The static and dynamic voltage sharing:

The static and dynamic voltage calculating formulas of the series switches are applied to this kind of hybrid connecting modulator, and the design parameters for the circuit are obtained;

2. Delay parameter design and ZVS actualizing of IGBTs:

According to the calculation and test results of the abovementioned key point, the time-delay parameters of the drive voltage are analyzed and given. The discharge time of the IGBT junction capacitor is analyzed, and the driving delays of the SiC MOSFET branch and IGBT branch are adjusted to ensure the realization of the ZVS process of the IGBT.

3. The short-circuit protection for SiC MOSFETs:

Factors causing internal core heating are analyzed according to the short-circuit waveform process of SiC MOSFETs. As a new scheme, the improvement for the short-circuit protection of SiC MOSFETs in hybrid connecting modulators are discussed, including a reduced short-circuit current, shortened protection time, and soft turning off. The influence of parasitic inductance on the short-circuit current distribution is analyzed, and the impedance isolation method is proposed to ensure the constant current distribution when load short circuiting happens.

2. Basic Principle of the Main Circuit

To correspond with the basic functions of high-voltage pulse modulators, two different hybrid connecting basic circuits are shown in Figures 2 and 3.

Figure 2 shows the hybrid parallel-series mode. Q_M (Q_{M1} , Q_{M2} ...) are SiC MOSFETs, and Q_I (Q_{I1} , Q_{I2} ...) are IGBTs. Two kinds of switches are connected in parallel and then connected in series. This circuit form is consistent with the working process of pure switch modulators in normal operations, which accords with the design purpose of the hybrid series-parallel scheme. There are many other components, like R, C, and D paralleling with SiC MOSFETs and IGBTs. They are very important for the security of the switches; C_S (C_{S1} , C_{S2} ...) are dynamic voltage sharing capacitors, R_S (R_{S1} , R_{S2} ...) are static voltage sharing resistors, D_S (D_{S1} , D_{S2} ...) are transient current channels for C_S , and R_P (R_{P1} , R_{P2} ...) are suppressing resistors for the pulsed discharge current of C_S .

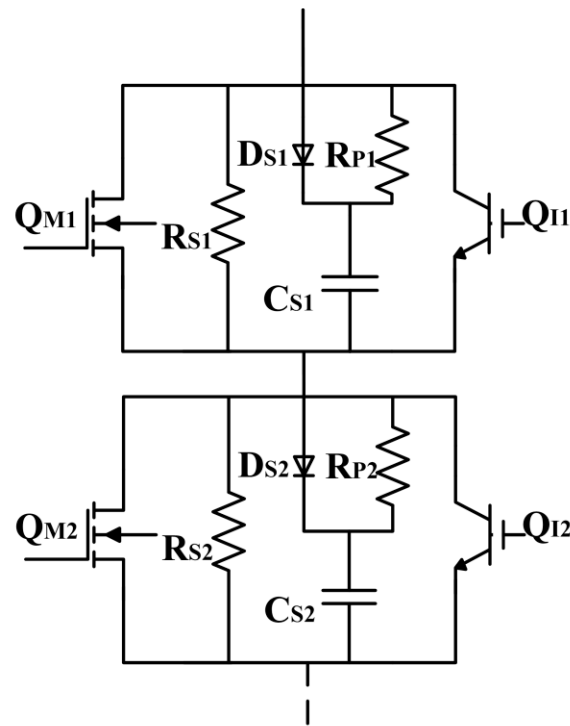


Figure 2. The hybrid parallel-series mode circuit.

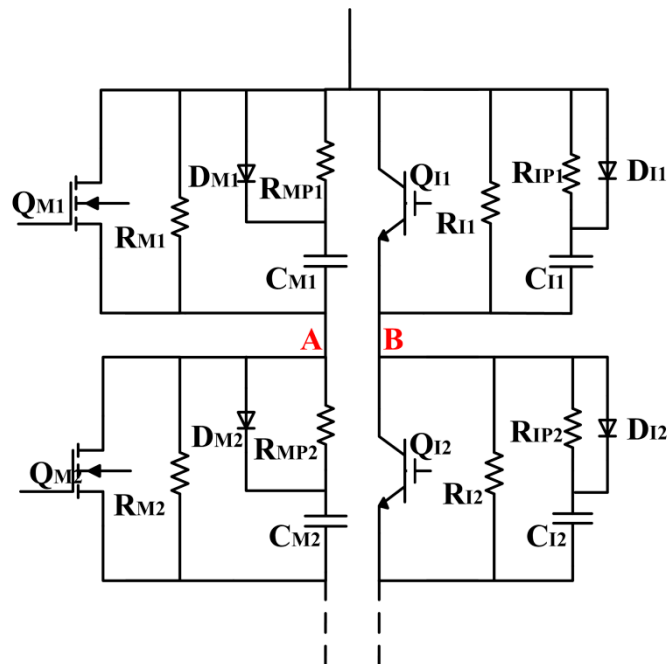


Figure 3. The hybrid series-parallel mode circuit. (“A” is point on series SiC MOSFETs branch, “B” is point on series IGBTs branch).

Figure 3 shows the hybrid series-parallel mode. Two kinds of switches are, respectively, connected in series and then connected in parallel. In principle, the circuit can modulate DC high-voltage pulses, but each switch needs to be equipped with a dynamic and static voltage sharing circuit. In addition, when one branch is “off” and the other is “on”, the transient potential difference will occur at two points, such as A and B. In the actual circuit sample PCB, the two points A and B are adjacent for compact design, which results in

a great risk of high-voltage breakdown occurring. Obviously, this is a complicated and unreliable design.

Therefore, according to the above analysis, the hybrid parallel-series mode circuit in Figure 2 is adopted as the basic scheme of the high-voltage pulse modulator. The detailed control sequence logic is shown in Figure 4.

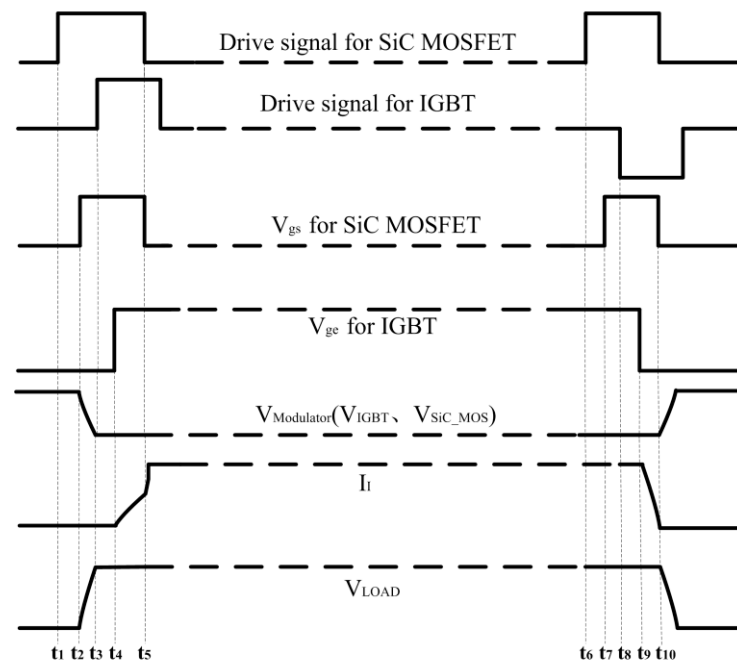


Figure 4. Control sequence logic for the hybrid parallel-series mode modulator.

A. The generation of the high-voltage pulse front edge:

Figure 5 shows the high-voltage pulse front edge operating modes of a single stage module, which can be divided into four stages as follows:

- (a) $t_1 \sim t_2$: SiC MOSFET switch Q_{M1} and IGBT switch Q_{I1} are all in the “off” state. The leakage current mainly passes through the static voltage sharing resistor R_{S1} . The trigger-generating circuit sends a pulsed drive signal to Q_{M1} and the grid-source voltage (V_{gs}) begins to rise to V_{gs_th} .
- (b) $t_2 \sim t_3$: Q_{M1} has been driven to the “on” state. Obviously, it is a hard switch process. At the same time, the paralleled capacitors, including the dynamic voltage sharing capacitors C_{S1} , C_{ds} of the Q_{M1} , and C_{ce} of Q_{I1} , are discharged to 0 V, and the voltage of the modulator (V_{IGBT}) begins to decline to 0 V. The modulator begins to output the pulse voltage to the load.
- (c) $t_3 \sim t_4$: The trigger-generating circuit starts sending pulsed drive signals to Q_{I1} . Before the grid-emitter voltage (V_{ge}) of Q_{I1} rises to V_{ge_th} , the currents are all passed through Q_{M1} .
- (d) $t_4 \sim t_5$: Q_{I1} is driven to the “on” state, and the current flowing through the IGBT (I_I) will reach a value lower than that of the load current. It is a ZVS process as the voltage of the modulator (V_{IGBT}) has declined to 0 V. At the time of t_5 , the pulse signal for Q_{M1} begins to end. It is a ZVS process in which Q_{M1} is turned to the “off” state, and with the V_{ds} remaining at a voltage of zero.

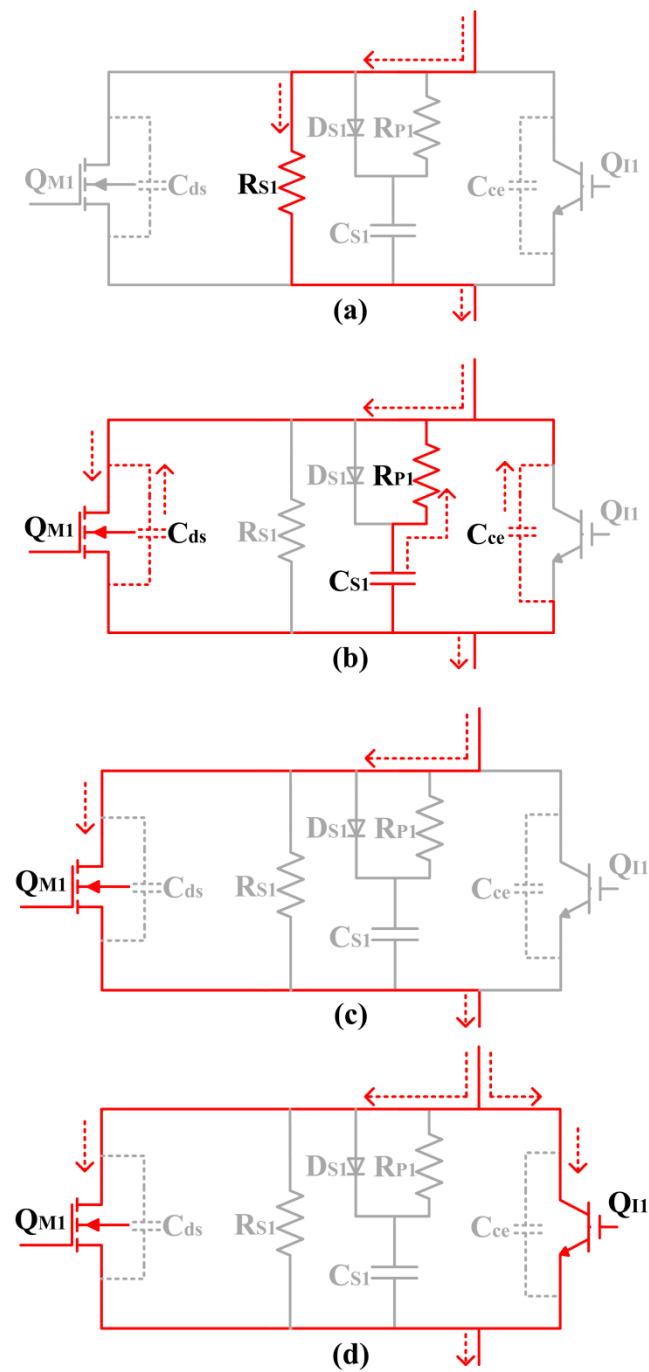


Figure 5. High-voltage pulse front edge operating modes of a single stage module.

B. Generation of the high-voltage pulse back edge:

Figure 6 shows the high-voltage pulse back edge operating modes of a single stage module, which can be divided into four stages as follows:

- (a) $t_6 \sim t_7$: The trigger-generating circuit starts sending a pulsed drive signal to the SiC MOSFET switch Q_{M1} . The grid-emitter voltage (V_{ge}) of Q_{M1} is beginning to rise to V_{gs_th} . At this time, the current all pass through the IGBT switch Q_{I1} .
- (b) $t_7 \sim t_8$: Q_{M1} has been driven to the “on” state. The current begins to pass through Q_{M1} .
- (c) $t_8 \sim t_9$: The trigger-generating circuit starts sending an “off” signal to the IGBTs. The working state is the same as $t_7 \sim t_8$.
- (d) $t_9 \sim t_{10}$: The grid-emitter voltage (V_{ge}) of Q_{I1} is beginning to decline to 0 V. As the paralleled Q_{M1} has been driven to the “on” state, the IGBTs’ would turn off with V_{IGBT}

= 0 V. It is a ZVS process for the IGBT. At t_{10} , the pulse signal for SiC MOSFETs is ending. At this moment, the pulse voltage begins to decline.

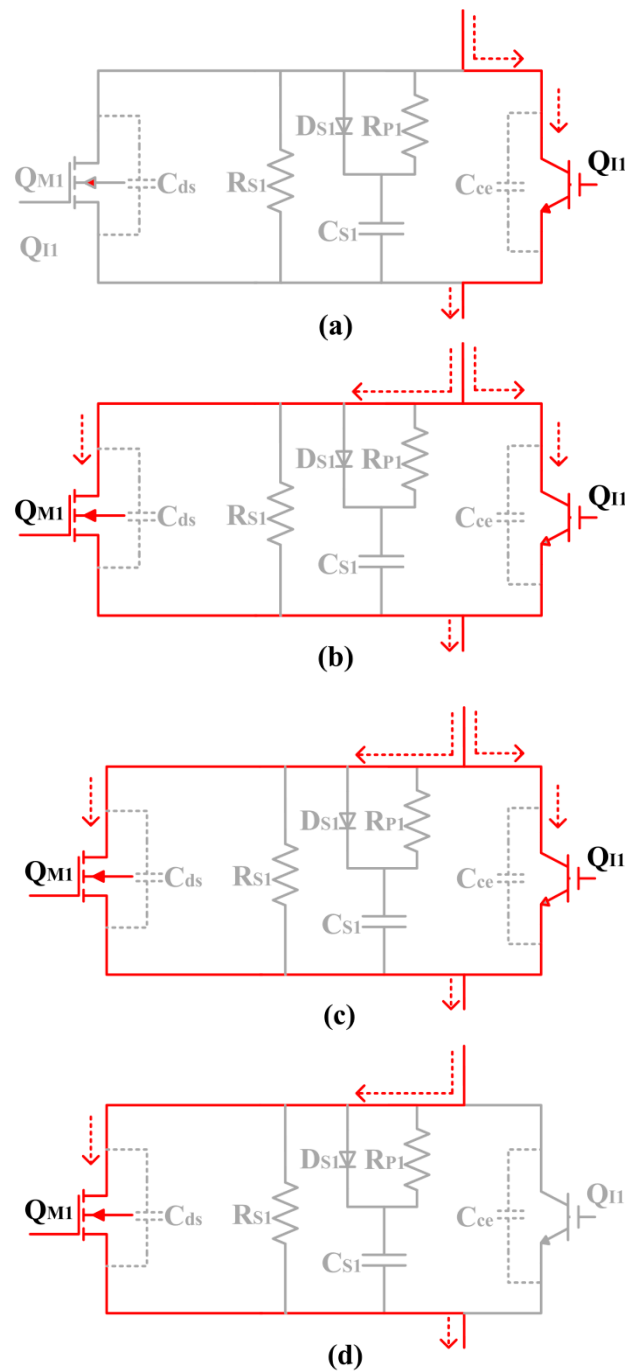


Figure 6. High-voltage pulse back edge operating modes of a single stage module.

3. Design and Discussion of the Key Parameters

3.1. Dynamic and Static Voltage Sharing

In the circuit of Figure 2, R_S (R_{S1} , R_{S2} ...) plays the role of the static voltage sharing resistor when the dU/dt is small, and C_S (C_{S1} , C_{S2} ...) plays the role of the dynamic voltage sharing capacitor when the dU/dt is large.

When the resistor R_S is much smaller than the leakage resistance of the SiC MOSFET and IGBT in parallel, the voltage distribution on the series components depends on the value of the resistor R_S , so R_S can ensure the static voltage sharing of the series switches.

The larger the leakage current of the SiC MOSFET and IGBT in parallel, the smaller the leakage resistance. According to the calculation regarding the “RCD” snubber circuit of series solid switches [18], R_S should satisfy Formula (1) as follows:

$$R_S \leq \frac{nU_D - U_N}{(n-1)(I_{LM} + I_{LI})} \quad (1)$$

where n is the number of series switching stages, which is always bigger than 10, U_D is the rated voltage of a single switching device, U_N is the working voltage of the modulator, I_{LM} is the leakage current of the SiC MOSFET, and I_{LI} is the leakage current of the IGBT. To ensure the safe working-voltage allowance, the working voltage for each switch generally takes the value of $1/2 \sim 2/3$ of U_D , meaning $U_N/n = 0.5U_D \sim 0.67U_D$.

In practical applications, the selection of R_S can be simplified through the use of Formula (1), then becoming an empirical formula, as follows:

$$R_S = (0.3 \sim 0.5) \frac{U_D}{I_{LM} + I_{LI}} \quad (2)$$

Due to the difference in the switching characteristics and transmission delay of the driving circuit, the switching action will not synchronize perfectly. Obviously, the devices with slow opening and fast closing rates will withstand higher voltages. Therefore, the function of the capacitor C_S is a voltage snubbing capacitor within the delay time, preventing the switching devices from overvoltage. According to the principle of the charge balance,

$$I_L \Delta t = C_{smin} \left(U_D - \frac{U_N}{n} \right) \quad (3)$$

Its calculation formula can be found in Equation (4) as follows:

$$C_S \geq C_{smin} = \frac{I_L \Delta t}{U_D - \frac{U_N}{n}} \quad (4)$$

C_{smin} is the minimum value of the voltage sharing capacitance. I_L is the load current at the time of conduction. Δt is the maximum switching delay time of each series switch, generally taking $0.1 \mu s$ as the maximum value.

D_S is where a low impedance current path to C_S is formed when the switch is turned off. R_P is where a limited discharge current path is formed and the thermal absorbing resistor for C_S when the switch is turned on. It should be much bigger than the conduction resistor R_M of the SiC MOSFET, but small enough to ensure the discharging of C_S when the SiC MOSFET is turned on. In the actual design, the general value of R_P is as shown in Equation (5).

$$10R_M \leq R_P \leq \frac{\tau_{min}}{5C_S} \quad (5)$$

τ_{min} is the minimum pulse width.

To verify the reliability of the principle circuit, a schematic prototype was designed. Its main working parameters are shown in Table 1.

Table 1. Main working parameters.

Symbol	Quantity	Value
U_N	input voltage	10 kV
n	series stages	16
R_L	load resistance	$500 \Omega \sim 1 \text{ k}\Omega$
Δt	switching delay time	$0.1 \mu s$
τ_{min}	minimum pulse width	$10 \mu s$

Based on the above equation and the electrical characteristics of the switch, the main device parameters are selected and calculated as shown in Table 2.

Table 2. Main device parameters.

Symbol	Quantity	Value
U_{MD}	rated voltage of SiC MOSFET	1200 V
U_{ID}	rated voltage of SiC MOSFET	1200 V
I_{LM}	leakage current of SiC MOSFET	100 μ A–1 mA
I_{LI}	leakage current of IGBT	250 μ A
R_s	static voltage sharing resistor	470 k Ω
C_s	dynamic voltage sharing capacitor	10 nF
R_P	thermal absorbing resistor	5 Ω

As is shown in Figure 7, each PCB board is arranged with two hybrid 1200 V-switches in series as follows: two series IGBTs on one surface and two series SiC MOSFETs on the other surface. Then, eight PCB boards (sixteen stage series switches) are connected in a straight line, as shown in Figure 8.

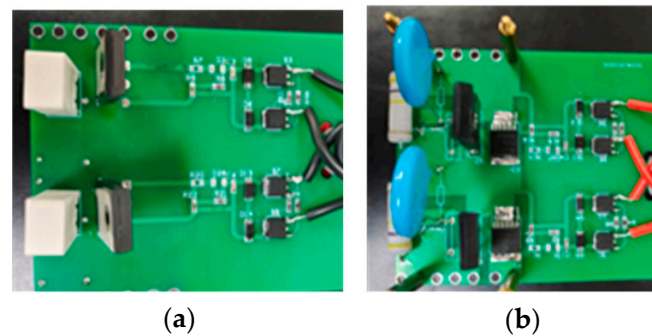


Figure 7. The single PCB sample type (a) surface of the IGBT branch (b) and the surface of the SiC MOSFET branch.

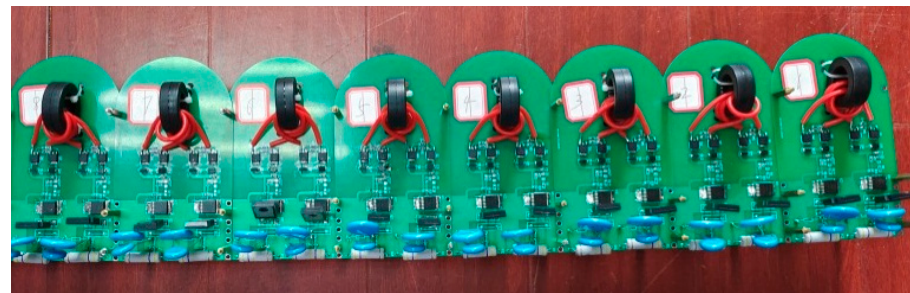


Figure 8. Eight PCB boards connected in a straight line.

Under the working condition of a 2 kHz repetition frequency, the output voltage of the modulator can reach 10 kV, and its pulse width is adjustable within 15 μ s. The repeated high-voltage pulse operation waveform is shown in Figure 9. To test the static and dynamic voltage sharing, four high-voltage pulse probes are used to monitor the voltages of the 4th, 8th, 12th, and 16th switches, respectively, in the experiment. The test for the voltage sharing at 10 kV, 2 kHz, 10 μ s, and a 500 Ω resistance load is shown in Figure 10. It shows that every stage of the modulator works in a voltage balance state.

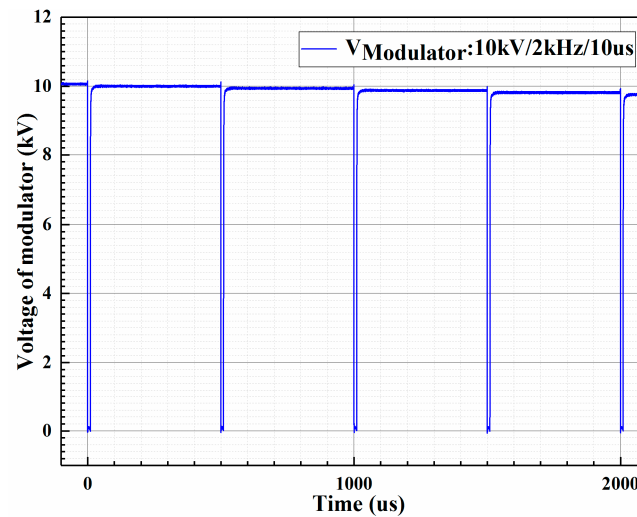


Figure 9. The high-voltage working waveform of the modulator at 10 kV, 2 kHz, 10 μ s, and a 500 Ω resistance load.

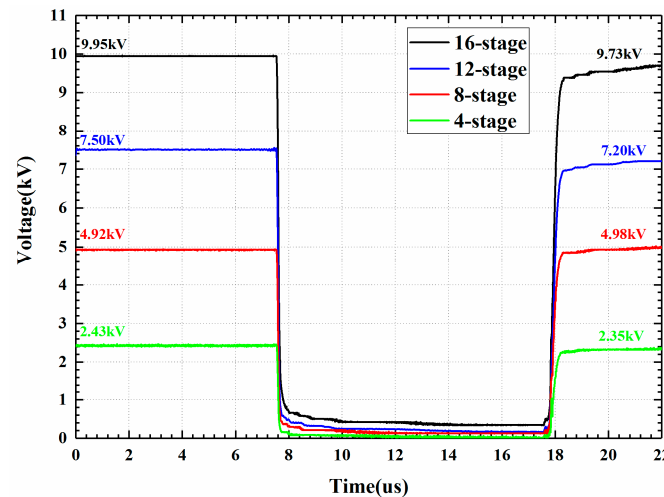


Figure 10. Test for the voltage sharing at 10 kV, 2 kHz, 10 μ s, and a 500 Ω resistance load.

3.2. Delay Parameter Design and ZVS Implementation of the IGBT

According to the description in Figure 4, the following conditions need to be met for the ZVS actualizing of the IGBT:

1. Period $t_2 \sim t_4$: All kinds of capacitors, C_{ce} , C_{ds} , and C_s , connected in parallel with the IGBT need to be discharged to 0 V through the SiC MOSFET, so that the V_{IGBT} (voltage of the modulator) is always kept at 0 V when the IGBT is turned on. According to the parameters, the maximum delay value is $3(R_M + R_P)(C_s + C_{ce} + C_{ds}) \approx 3 \times (0.2 \Omega + 5 \Omega) \times 10 \text{ nf} = 156 \text{ ns}$, that is, $t_4 - t_2 > 156 \text{ ns}$.
2. Period $t_7 \sim t_9$: There is a delay of 20 ns from the gate. The voltage of the SiC MOSFET is 5 V for the flowing of the current; $t_9 - t_7 > T_{d(\text{on})-\text{MOS}} = 20 \text{ ns}$, $V_{ce} = 0 \text{ V}$ when the IGBT is turned off.
3. Period $t_4 \sim t_5$ and $t_9 \sim t_{10}$: To ensure V_{ce} is always kept at 0 V before the SiC MOSFET turns off, we choose $(t_5 - t_4)$ and $(t_{10} - t_9)$, which are bigger than $T_{d(\text{on})-\text{IGBT}}$ and $T_{d(\text{off})-\text{IGBT}}$.

After the above discussion about the control time sequence of the two branches, it is determined that the control signal is shown in Figure 11 below. The green line is the control signal of the SiC MOSFET with a conduction threshold voltage of 5 V, and the blue line is the IGBT control signal with a conduction threshold voltage of 8 V.

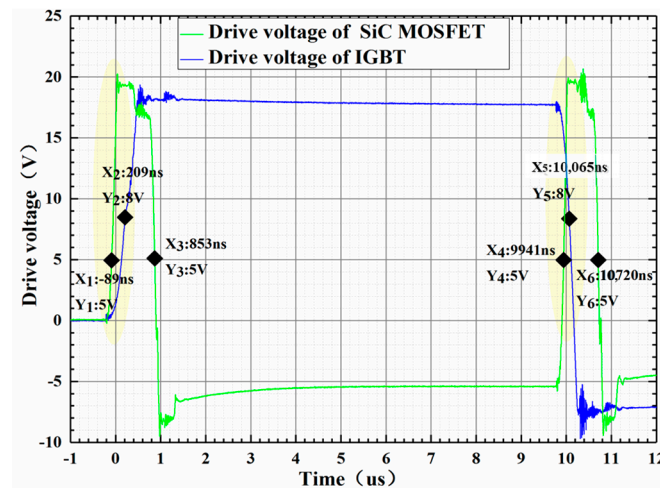


Figure 11. Time sequence and waveform of the driving pulse.

In the yellow area of Figure 11, key points have been marked at the curve of the drive signals.

At the front edge of the high-voltage pulse, the SiC MOSFET is turned on from $X_1 = t_2 = -89$ ns, and the IGBT is turned on from $X_2 = t_4 = 209$ ns, $X_2 - X_1 = 298$ ns = $t_4 - t_2 > 156$ ns.

And then the SiC MOSFET is turned off from $X_3 = t_5 = 853$ ns, $X_3 - X_2 = 644$ ns = $t_5 - t_4 > T_{d(on)-IGBT}$.

At the back edge of the high-voltage pulse, the SiC MOSFET is turned off from $X_4 = t_7 = 9941$ ns, and the IGBT is turned on from $X_5 = t_9 = 10,065$ ns, $X_5 - X_4 = 124$ ns = $t_9 - t_7 > 45$ ns.

And then the SiC MOSFET is turned off from $X_6 = t_{10} = 10,720$ ns, $X_6 - X_5 = 655$ ns = $t_{10} - t_9 > T_{d(off)-IGBT}$.

The voltage across the modulator (equal to the voltage across the IGBT, the blue line) and the timing of the current flowing through the IGBT branch (the orange line) are tested for this drive signal, as shown in Figure 12. As one of the most important characters, the ZVS process of IGBTs are proven as follows: the current begins ascending (time point X_2) or descending (time point X_4) when $V_{IGBT} = V_{Modulator} = 0$ V. It almost synchronizes with the drive voltage of the IGBT in Figure 11.

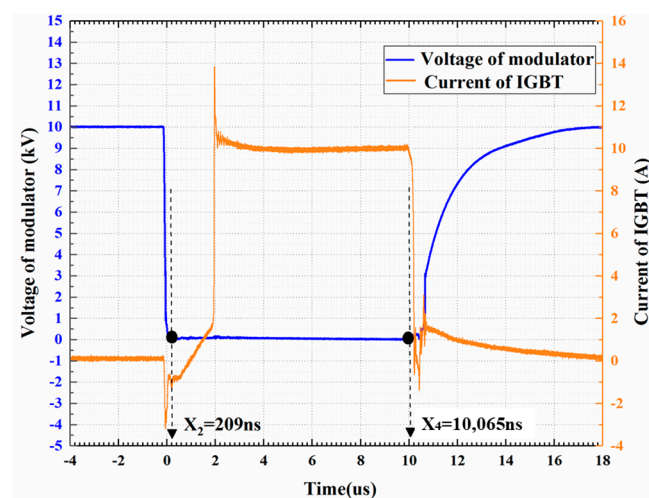


Figure 12. Voltage and current waveform of the ZVS process for IGBTs at 10 kV, a 10~15 μ s pulse width, and a 1 k Ω resistance load.

The miller plateau of the IGBT in $T_{d(on)}$ and $T_{d(off)}$ has been eliminated as $V_{IGBT} = V_{Modulator} = 0$ V. So, the $X_3 - X_2$ and $X_6 - X_5$ can still be shortened to smaller than 300 ns without affecting the ZVS process of the IGBT. It will be an improvement for the short-circuit protection of the SiC MOSFET in later research.

Apart from the power loss produced by the distributed capacitance's charging and discharging, the power loss produced by the switches of the hybrid SiC MOSFET/IGBT modulator is expressed as Equation (6).

$$P_{Hys-loss} = P_{SiC-on-loss} + P_{SiC-off-loss} + P_{IGBT-cond-loss} + P_{SiC-cond-loss} \quad (6)$$

In contrast to Equation (6), the power loss produced by the switches of the modulator based on pure SiC MOSFETs or IGBTs can be expressed as Equations (7) and (8).

$$P_{SiC-loss} = P_{SiC-on-loss} + P_{SiC-off-loss} + P_{SiC-cond-loss} \quad (7)$$

$$P_{IGBT-loss} = P_{IGBT-on-loss} + P_{IGBT-off-loss} + P_{IGBT-cond-loss} \quad (8)$$

Through researching commercial discrete SiC MOSFETs and IGBTs, the SiC MOSFETs' switch loss is commonly 10~30% of the IGBTs' at the same rated parameters. So, when the pulse modulator works at a high repetition frequency, such as 2 kHz, $P_{Hys-loss} \approx P_{SiC-loss} \approx (10\sim30\%) P_{IGBT-loss}$.

3.3. The Short-Circuit Protection of SiC MOSFET

3.3.1. The Short-Circuit Protection Analysis of the Pure SiC MOSFET Modulator

We fabricated the short-circuit fault with a 16-stage pure SiC MOSFET modulator. To protect SiC MOSFETs from damaging by short-circuit current, 8 kV input voltage and 80 Ω load resistor are set. The voltage and current waveforms during protection are shown in Figure 13.

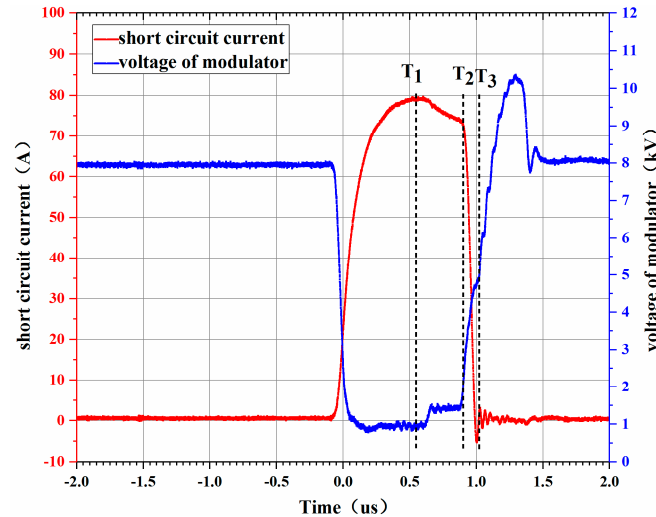


Figure 13. Voltage and current waveforms of pure SiC MOSFET modulator during protection at 8 kV, 80 Ω load resistor.

The short-circuit current ascends to 79 A peak value at T_1 and then descends as increasing inner resistance of modulator. The conductive energy loss ($T_1 \sim T_2$, $E_{SiC-cond-loss}$) and the turning-off energy loss ($T_2 \sim T_3$, $E_{SiC-off-loss}$) of each SiC MOSFET in modulator are estimated 2.68 mJ as reference data according to Equation (9):

$$E_{SiC-cond-loss} + E_{SiC-off-loss} = \frac{\int_{T_1}^{T_3} V_{ds} * I_d * dt}{16} \quad (9)$$

From Equation (9), the effective methods to decrease $E_{SiC-cond-loss}$ and $E_{SiC-off-loss}$ are reducing the I_d and V_{ds} and shortening the protection time. The traditional improvement

method is increasing the current limiting resistance and speeding up the sampling judgment degree to shorten the protection time. However, increasing the current limiting resistance will cause huge power losses, and speeding up the sampling–feedback–judgment is easy to be interfered and misjudged.

The characteristic of the hybrid connecting modulator is that SiC MOSFETs are only conductive at the front and back edges. The drive voltage pulse can be shortened to 0.5 μ s and the paralleled IGBT branch will share the short-circuit current.

3.3.2. Transient Current Distribution Consistent Researching for Hybrid Connecting Modulator

The short-circuit current will be shared by the SiC MOSFET and IGBT, so that both devices will bear a lower short-circuit current than a single switch. However, the sharing of this transient current is not only determined by the parameter ratio of the SiC MOSFET and IGBT, but also will be affected by parasitic inductance parameters, as shown in Figure 14.

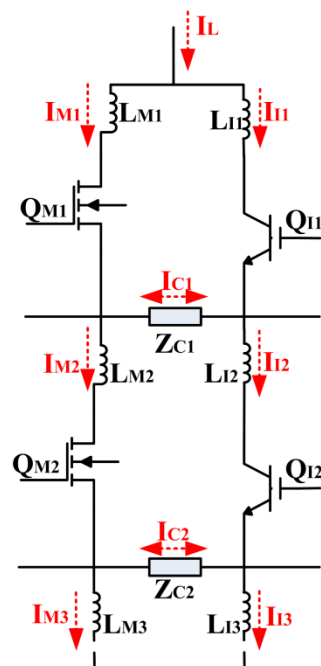


Figure 14. Simplified schematic diagram of the hybrid connecting modulator with stray inductance parameters.

Because the assembly and production will inevitably lead to the discreteness of parasitic impedance, as shown in Figure 14, the parasitic inductance L_M (L_{M1} , L_{M2} , L_{M3} ...) or L_I (L_{I1} , L_{I2} , L_{I3} ...) of each stage will not be exactly the same. It will cause transient coupling currents I_C (I_{C1} , I_{C2} ...).

Taking the empirical data range of PCB parasitic inductance designed by the modulator as simulation parameters leads to the following: 150 A short-circuit current, $L_{M1} = L_{M2} = 4$ nH, $L_{I1} = 6$ nH, $Z_{C1} = 0$. Taking L_{I2} as a variable, increasing from 3 nH to 45 nH and stepping 3 nH, the curve of the I_{C1} peak increases with L_{I2} , as shown in Figure 15. It can be seen from the following simulation results:

1. $L_{I2} = 3$ nH < $L_{I1} = 6$ nH, $I_{C1} = -58$ A; this means that I_{C1} flows from the SiC MOSFET branch to the IGBT branch.
2. $L_{I2} > L_{I1} = 6$ nH, $I_{C1} > 0$ A; this means that I_{C1} flows from the IGBT branch to the SiC MOSFET branch.
3. $L_{I2} = L_{I1} = 6$ nH, $I_{C1} = 0$ A; this means that there is no coupling between the IGBT branch and the SiC MOSFET branch.

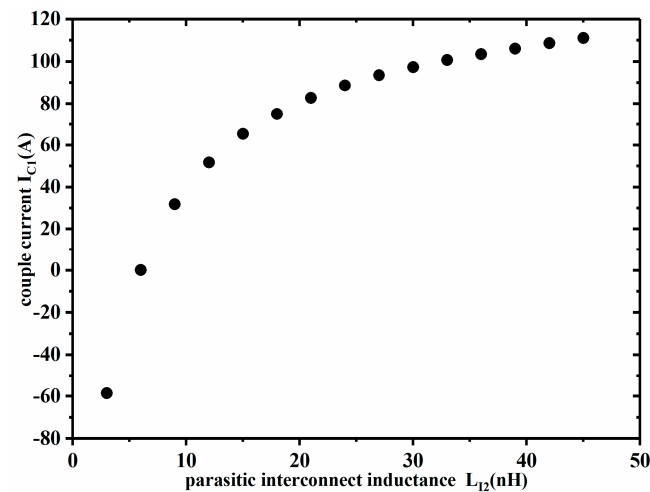


Figure 15. Simulation of the peak value of the couple current I_{C1} with parasitic inductance L_{I2} (150 A short-circuit current, $L_{M1} = L_{M2} = 4$ nH, $L_{I1} = 6$ nH, L_{I2} as variables, increasing from 3 nH to 45 nH and stepping 3 nH).

As can be seen from Figure 15, and as can be seen from the simulation results, L_{I2} has a large dispersion when compared with L_{I1} . With the increase in L_{I2} , the SiC MOSFET connected in parallel will be distributed at a higher short-circuit current I_{M2} , so it is necessary to decouple the IGBT branch and SiC MOSFET branch.

We set Z_{C1} in Figure 15 as the inductance or resistance. And two decoupling methods are simulated and analyzed as follows: The peak value of the couple current I_{C1} with decouple inductance Z_{C1} is shown in Figure 16, and the peak value of the couple current I_{C1} with decouple resistance Z_{C1} is shown in Figure 17.

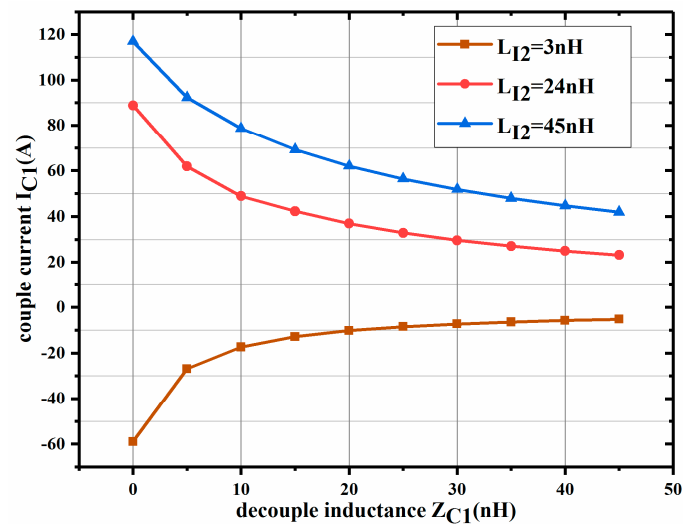


Figure 16. The peak value of the couple current I_{C1} with decouple inductance Z_{C1} (2 stages of SiC MOSFETs/IGBTs at a short-circuit current of 150 A, parasitic inductance $L_{M1} = L_{M2} = 4$ nH, $L_{I1} = 6$ nH, $L_{I2} = 3$ nH, 24 nH, 45 nH).

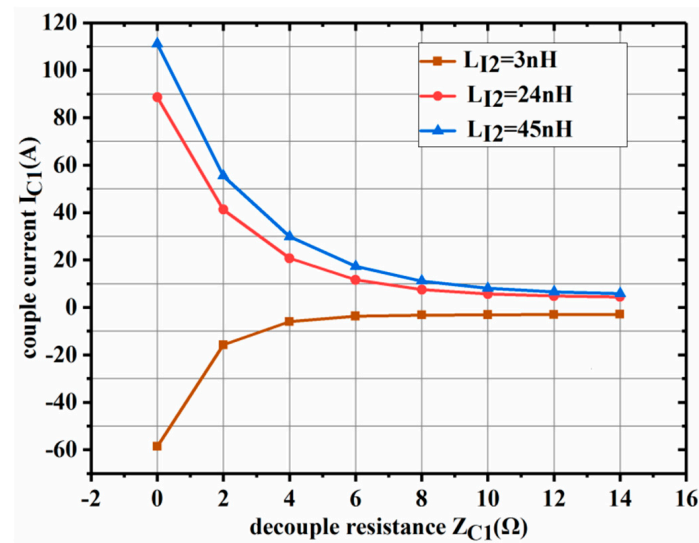


Figure 17. The peak value of the couple current I_{C1} with decouple resistance Z_{C1} (2 stages of SiC MOSFETs/IGBTs at a short-circuit current of 150 A, parasitic inductance $L_{M1} = L_{M2} = 4$ nH, $L_{I1} = 6$ nH, $L_{I2} = 3$ nH, 24 nH, 45 nH).

It can be summarized that both methods are effective for couple current suppression due to the following:

1. When $Z_{C1} = 0$, the value of I_{C1} is consistent with Figure 15 at $L_{I1} = 3$ nH, 24 nH, 45 nH.
2. When Z_{C1} is growing, the peak value of the couple current I_{C1} will obviously gradually descend to a stable trend.
3. Due to the extra power loss caused by the decouple resistance Z_{C1} , we chose to design a narrow PCB line between the source electrode of the SiC MOSFET and the emitter electrode of the IGBT in order to achieve a relatively larger decoupling inductance value. Each board connection is connected by copper terminals and bolts to reduce the parasitic inductance and discreteness.

3.3.3. The Short-Circuit Current Protection at the Front Edge for the SiC MOSFET Hybrid Connect Modulator

The short-circuit protection time of the sampling–feedback–judgment loop for the IGBT should be designed longer than the SiC MOSFET’s drive pulse time width. When short-circuit fault happens at the front edge, the SiC MOSFET will be turned off before the IGBT. This is a zero voltage turning-off process for the SiC MOSFET.

Based on the design discussion, we fabricated the short-circuit fault with a 16-stage SiC MOSFET/IGBT hybrid connecting modulator and with 8 kV of input voltage and an 80 Ω load resistor. The voltage and current waveforms during protection are shown in Figure 18.

The short-circuit current flowing through the SiC MOSFET branch ascends to a 55 A peak value at T_1 , and then descends as the current sharing of the IGBT branch increases. It is approximately a zero voltage turning-off process. The conductive energy loss ($T_1 \sim T_2$, $E_{\text{SiC-cond-loss}}$) and the turning-off energy loss ($T_2 \sim T_3$, $E_{\text{SiC-off-loss}}$) of each SiC MOSFET in the modulator is estimated at 0.71 mJ according to Equation (9). It is only 26.1% of the pure SiC MOSFET modulator’s 2.68 mJ.

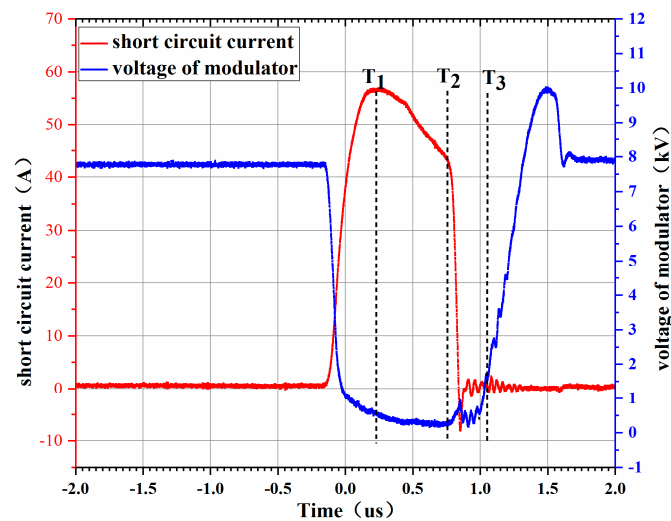


Figure 18. Voltage and current waveforms of the hybrid connecting modulator during protection at 8 kV and with a 100 Ω current load resistor.

3.3.4. The Short-Circuit Current Protection at the Back Edge for the SiC MOSFET Hybrid Connect Modulator

According to the research results of the ZVS process of the IGBT, the SiC MOSFET's drive pulse width could be shortened within 500 ns. That means shorter ($T_2 - T_1$) and fewer $E_{\text{SiC-cond-loss}}$ than Figure 13. Despite it being a difficult turning-off process for the SiC MOSFET, the sum of $E_{\text{SiC-cond-loss}}$ and $E_{\text{SiC-off-loss}}$ would still be reduced to much lower than a pure SiC MOSFET modulator.

4. Conclusions

In this paper, a modulator composed of a hybrid connecting SiC MOSFET/IGBT is designed, and its working schematic is expatiated. The theory analyses and measurements demonstrate that the modulator can work based on hybrid connecting switches. The control sequences of the driving signal for the SiC MOSFET, including the pulse front edge and back edge, is studied.

To verify the reliability of the principle, 16-stage hybrid 1200 V SiC MOSFET/1200 V IGBT modulators are assembled and tested.

1. The main power circuit achieves a repetition pulse output of 10 kV/10 A/10 μs /2 kHz and good dynamic voltage sharing.
2. The experiment proves that the hybrid connecting modulator can achieve low switch losses, approaching all SiC MOSFET modulators when the IGBT works with the ZVS process in periods.
3. Factors causing internal core heating are analyzed according to the short-circuit waveform of the SiC MOSFET. As a new scheme, the improvement, including the transient current decouple methods between the MOSEFT branch and the IGBT branch, the soft turning-off process of the SiC MOSFET, and the very short conduction time (less than 500 ns) of the SiC MOSFET, are discussed. A surprised decrease is verified through a short-circuit simulation experiment: the turning-off energy loss ($E_{\text{SiC-off-loss}}$) of the short-circuit protection for each SiC MOSFET in the hybrid connecting modulator is estimated at 0.71 mJ, which is only 26.1% of the pure SiC MOSFET modulator's 2.68 mJ.

Apart from these advantages, the following issues are worthy of further consideration:

1. The control sequence in this paper is not unique for hybrid switch components. There are multiple choices for different occasions.

2. To exert the miniature application potential in the pulse power area of this design method, discrete components, such as SiC MOSFETs and IGBTs with higher rated voltages (3.3 kV, 6.5 kV, 10 kV), could be used in the circuit design.

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