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Collaborative Design of Pulsed-Power Generator Based on SiC Drift Step Recovery Diode

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Abstract: Despite the extensively researched physical principles, numerous published simulations on SiC drift step recovery diodes (SiC DSRD) and the practical implementation of SiC DSRD-based pulses, there are few kinds of research focusing on collaborative design between a SiC DSRD and its driving circuit. In this paper, a collaborative design method of a SiC DSRD and its driving circuit are presented. In addition, a detailed simulation is conducted to verify design considerations and to analyze the impact of driving parameter changes on the output pulse waveform. A pulse generator prototype with a self-developed SiC DSRD is implemented. The experimental results show that the circuit can output a peak voltage of 790 V on a matching load of 50 Ω, with a rise time of 520 ps (20%~80%), and can work at a 1 MHz repetition frequency rate with good stability.

Keywords: SiC; pulsed power circuit; drift step recovery diodes; sub-nanosecond

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1. Introduction

Pulsed power technology is a method that compresses energy from milli- or microseconds to nano- or picoseconds on the time scale and brings several orders of magnitude increase in the power level. This technology finds extensive applications across various industries such as food processing, nitric oxide production, water and exhaust gas treatment, and ion implantation, among others [1]. Numerous experiments have demonstrated that nanosecond pulses are particularly advantageous for these applications [2–4]. While conventional semiconductor switches like IGBTs, MOSFETs, and thyristors can effectively generate microsecond power pulses in such scenarios, they are not suitable for generating high-voltage nanosecond pulses. To address this issue, drift step recovery diodes (DSRDs) can be employed [5].

Drift step recovery diodes (DSRDs), as a new type of semiconductor opening switch, can generate a nanosecond pulse on the load through a matching external trigger circuit. However, the DSRD has strict requirements for circuit matching. The unmatched driving circuits will lead to a decrease in the output peak, the slowdown of the pulse front, and an increase in power loss owing to the appearance of pre-pulse.

Based on DSRD devices, a number of scholars have reported extensive research. The Russian Ioffe Physical-Technical Institute developed a pulsed generator with a front edge of 600 ps and an amplitude of 2 kV [6]. Israel's Soreq Nuclear Laboratory presented a solid-state pulsed generator with a front edge of less than 1 ns and an amplitude of 6 kV [7]. The American SLAC National Accelerator Laboratory reported a pulsed power supply. The rise time was less than 2 ns and the amplitude was 15 kV based on the DSRD front-end pump circuit [8,9]. The Northwest Institute of Nuclear Technology in China developed a pulsed generator with a pulse front of 700 ps and an amplitude of 2 kV [10]. In 2016, V.A. Ilyin et al. reported the circuit test results of an eight-diode-stacked 4H-SiC DSRD device with the P+PN+ structure. The rise time of the output pulse was 900 ps with an amplitude of 10.5 kV and verified the possibility of stacking 4H-SiC DSRD devices for the first time [11].

In the same year, B.V. Ivanov et al. reported the results of the repetition frequency operation test of a single diode P+PN+ structure. The rise time of the output pulse was 500 ps with an amplitude of 1.8 kV and a maximum repetition frequency of 500 kHz [12]. In 2018, T Goto et al. from Tsukuba University of Japan prepared a SiC DSRD with a P+PNN+ structure. It is different from the conventional P+PNN+ structure. In conventional P+PNN+ structure, the P-type base region stores plasma, and the N-type base region bears pressure. However, based on the result of the simulation, T Goto et al. found that the 9 μm thick P-type base region matches the 8 μm thick N-type base region when the pulse generator output voltage is the largest and the rise time is shorter. After stacking five diodes, the rise time of the output pulse was 2.3 ns with an amplitude of 11 kV [13]. In addition, V.A. Ilyin et al. reported the test results of 15 diodes stacked with a 4H-SiC DSRD, with an output pulse rise time of 1.6 ns and an amplitude of 30.5 kV [14]. In the same year, Wang Yajie et al. reported a pulse generator with an output pulse amplitude of 2 kV and a pulse front of 680 ps (20%~90%). Based on the equivalent model of DSRD, the simulation model of the forward-and-reverse pump circuit is established. According to the requirements of output voltage, the values of energy storage inductance are simulated and analyzed. Finally, optimal values of the component parameters in the circuit are obtained [15]. In 2020, Sun Ruize et al. reported a SiC DSRD device with the P+PNN+ structure, in which the breakdown voltage was above 10.9 kV. The measured output pulse rise time was 1.75 ns with an amplitude of 10.56 kV, and the maximum repetition frequency was 1 MHz [16]. In 2021, Liang Lin et al., from Huazhong University of Science and Technology of China, reported the testing results of a SiC DSRD circuit using four-way parallel triggering. The measured rise time of the output pulse was 1.011 ns, and the amplitude was 2.302 kV. By adjusting the DC bias voltage of the input circuit, they found that the amplitude and rise time of the output voltage of the device increase with the increase in the DC bias voltage [17].

Although the match between a DSRD and its driving circuits is an important issue, little research pays attention to the collaborative design of DSRD and its driving circuits. In this paper, a collaborative design method of a SiC DSRD and its driving circuit are presented. In addition, a detailed simulation is conducted to verify design considerations and to analyze the impact of driving parameter changes on the output pulse waveform. A pulse generator prototype with self-developed SiC DSRD is implemented.

2. Design of SiC DSRD Device

2.1. Operation Principle of SiC DSRD

A simplified operating circuit is shown in Figure 1a. The DSRD is connected in parallel to the load. The waveform of input current I_{in} is shown in Figure 1b. I_d and I_{out} are the currents flowing through the DSRD and the load, respectively. When the DSRD is turned off, I_{in} is switched from the the DSRD loop to the load loop, then forms a high-voltage fast pulse on the load (R_L).

Figure 1c shows the carrier concentration and electric field distributions at different times. Initially, the DSRD is in the blocking state due to the existence of the space charge region (SCR). Before t_0, the hole concentration and doping concentration are basically the same in the base region, whereas the electron concentration can be ignored. Then, I_{in} provides a forward current to the DSRD. Electrons and holes, from the N^+ region and P^+ region, are injected into the base region. It decreases the resistance of the base region. During the t_1-t_2 process, the current I_{in} changes direction into reverse to extract the plasma in the base area. The resistance of the base region is still low due to the existence of high-concentration plasma. At time t_2, the plasma is completely extracted, and the reverse current reaches the maximum. At this moment, the majority of carriers are extracted by the reverse current I_{in} and move with the saturated velocity. Meanwhile, the space charge region forms at the PN^+ junction and expands with the speed of saturated velocity. As a result, the resistance of the base region sharply increases, and the current switches from the

DSRD to the parallel connected load with the output pulse. At time t_3, the space charge region is completely established, and the output pulse reaches its maximum voltage.

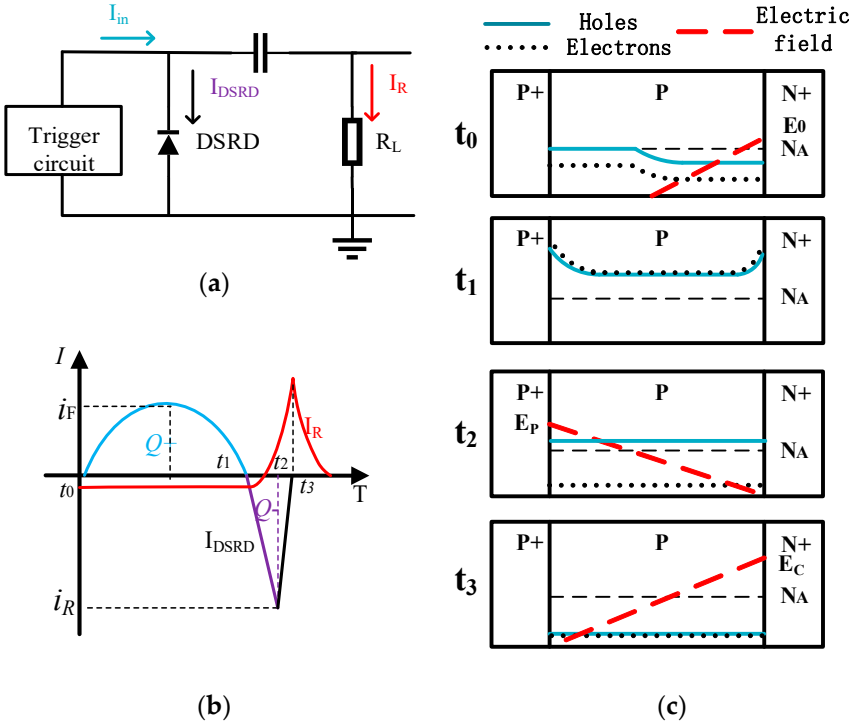


Figure 1. The working principle of DSRD: (**a**) the simplified working circuit of DSRD; (**b**) switching characteristics of DSRD; (**c**) the carrier concentration and electric field distributions at different times.

In addition, for SiC DSRDs, vast loss of injected charge is a general issue [18,19] which may lead to a decrease in DSRD energy efficiency. The charge loss rate is defined as Q-/Q+. The extracted non-equilibrium charge Q- and injected charge Q+ are defined by the areas under current transient response at different stages of the recovery process of the DSRD [20].

2.2. Parameter Selection and Optimization of SiC DSRD

It is worth noting that, in the process of plasma extraction, if the carrier concentration at the base region cannot sustain the reverse current, major carriers will accumulate at the border of the P+P junction [21]. In this case, the voltage drop on the base will occur before the cutoff, resulting in the appearance of pre-pulse. It increases the power loss of the DSRD. To avoid the appearance of the pre-pulse, in terms of the DSRD design, the maximum reverse current (I_{max}) must satisfy the following:

$$I_{max} \leq qN_A v_s S \quad (1)$$

In Equation (1), q is the elementary charge quantity; N_A is the base doping concentration; v_s is the carrier-saturated drift velocity of the base region; and S is the active area of the DSRD.

In addition, the breakdown voltage (V_{BV}) of the DSRD is the main parameter that restricts the output peak voltage (V_{max}) of the pulse generator. In other words, V_{BV} puts an upper limitation on the output peak current. The DSRD breakdown voltage V_{BV} can be expressed as

$$V_{BV} \propto {N_A}^{-1} W \quad (2)$$

The output peak voltage V_{max} is

$$V_{max} = I_{max}R_L \quad (3)$$

The relation between V_{BV} and V_{max} is

$$V_{max} \approx V_{BV} \quad (4)$$

Therefore, the I_{max} is limited by N_A and W, as shown in Equation (6):

$$I_{max} = \frac{V_{max}}{R_L} \quad (5)$$

$$I_{max} \propto {N_A}^{-1}W \quad (6)$$

In Equations (2) and (3), W is the base width; R_L is the load resistance which is usually 50 Ω.

Then, the suitable structure parameter of DSRD can be determined. At first, the I_{max} value or V_{max} value will be given in advance according to practical requirements. Next, the value of the W, $N_{A,}$ and S can be chosen based on Equations (1) and (6). That is to say, when one of the three parameters is given, the other two parameters will also be obtained. For example, in this paper, the given V_{max} value is 800 V. Based on the given design method, a SiC DSRD is designed. The thicknesses of the p+ and p-base layers are 2 μm and 6 μm, with accepted concentrations of 1×10^{19} and 2×10^{16} cm^{-3}, respectively; the n+ layer has a thickness of 5 μm and a doping concentration of 1×10^{19} cm^{-3}. The active area S is 0.28 mm^2.

3. Collaborative Design of DSRD-Based Pulse Generator

3.1. Working Principle of Driving Circuit

The schematic diagram of the driving circuit of the DSRD is illustrated in Figure 2. which consists of two DC power supplies with voltage V_1 and V_2, the primary switch of SiC MOSFET(MOS), energy storage inductances L_1 and L_2, the decoupling capacitance C_1, the resonant capacitance C_2, the dc-blocking capacitance C_3, the decoupling capacitance C_4, the DSRD device, and the load R_L.

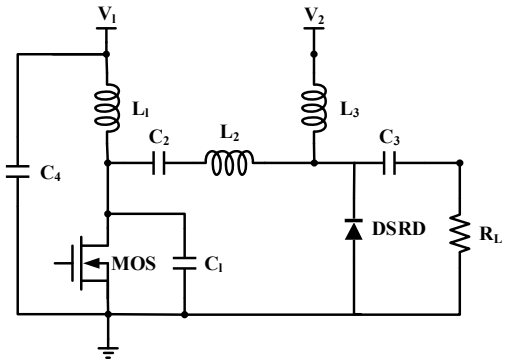


Figure 2. Schematic diagram of DSRD-based pulse generator.

The working process can be divided into four intervals, which are shown in Figure 3. Figure 4 shows the current waveforms during the operation.

Interval 1: Initially, the MOS is off-state, and the resonant capacitance C_2 is charged by V_1 and V_2 to the initial voltage $\Delta V = V_1 - V_2$.

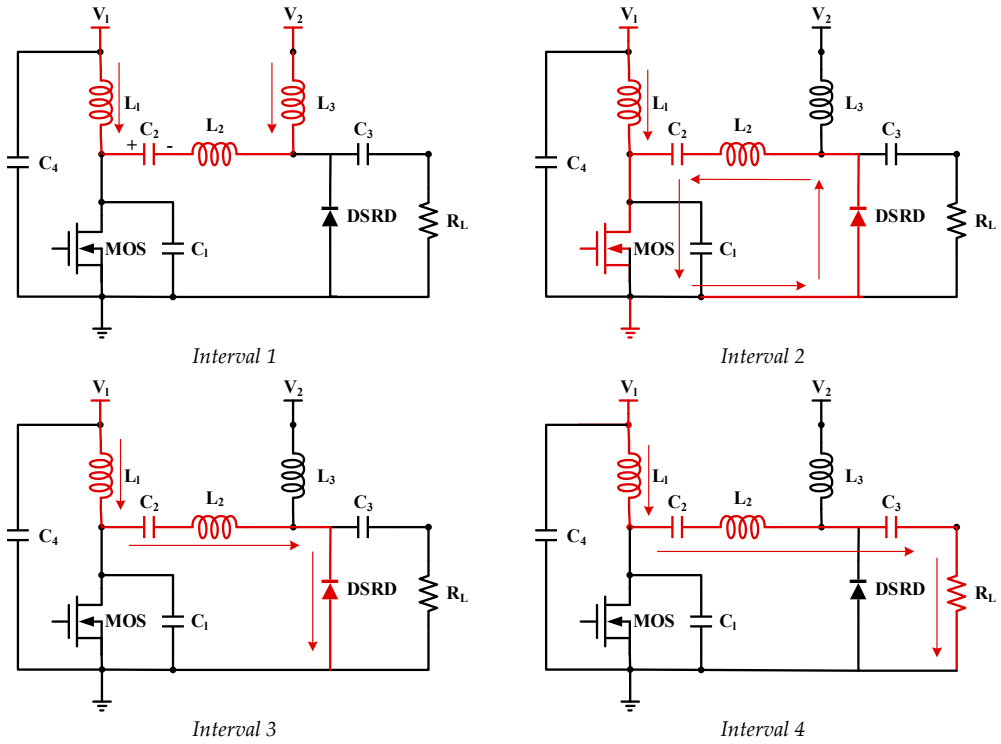


Figure 3. Equivalent circuit of pulse generator.

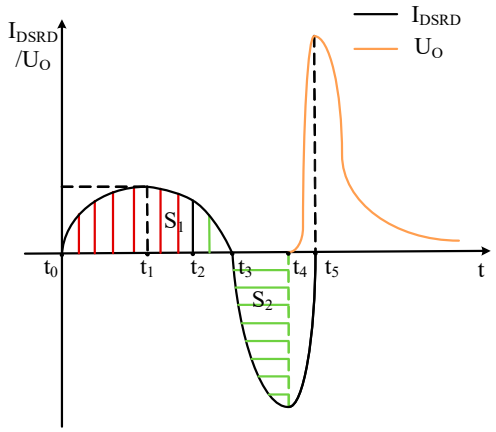


Figure 4. Theoretical waveforms in the circuit shown in Figure 3.

Interval 2: At t_0, the MOSFET is turned on; then, the circuit can be divided into two loops, which are V_1-L_1-*MOSFET(loop1)* and C_2-*MOSFET-DSRD-*L_2*(loop2)*. In loop1, the inductor L_1 stores the energy from V_1, and the current of L_1 can be expressed as

$$i_{L_1} = \frac{V_1}{L_1} t \tag{7}$$

In loop2, the inductor L_2 and capacitor C_2 begin to resonate, and at t_1 the resonant current reaches its peak value, then it begins to decrease. The resonant current which can be considered as the forward current accumulates charge carriers in the DSRD; the resonant current can be expressed as

$$i_{L_2} = \frac{\Delta V}{\omega_2 L_2} \sin(\omega_2 t),\ \omega_2 = 1/\sqrt{L_2 C_2} \tag{8}$$

Interval 3: At t_2, the MOSFET turns off. The energy stored in L_1 needs to be released through C_2, L_2, and DSRD. Then, the resonant current decreases rapidly. At t_3, the resonant current reverses. During the interval, the resonant current extracts charged plasma which has been accumulated in interval 2.

Interval 4: At t_4, the plasma in the DSRD base region is depleted by the extracting process, and the DSRD is rapidly turned off. Then, the high current through the DSRD is swiftly switched to the load R_L, generating a high-voltage pulse.

3.2. Conduction Time of the MOSFET

In order to weaken the effect of carrier recombination, the charge carrier's accumulation process in DSRD should satisfy the following equation:

$$\Delta T + (t_4 - t_2) \leq \tau \tag{9}$$

where ΔT represents the conduction time of the MOSFET, τ represents the carrier lifetime of the SiC DSRD, which equals 40 ns. Therefore, the conduction time ΔT is selected as 25 ns.

3.3. Inductance Design

The inductors used in power pulse technology often require a wide frequency response. Due to the easy saturation and large inductance deviation under different frequencies of the magnetic core inductor, the hollow inductor is selected in this design.

Based on the working principle illustrated above, the high-voltage pulse is generated by the high current through the DSRD swiftly switched to the load R_L. During the voltage pulse output, the current of L_2 can be expressed as

$$I_{L_2} = I_{peak} e^{\left(-\frac{t}{L_2/R_L}\right)} \tag{10}$$

The energy stored in the inductor L_2 can be expressed as

$$W_{\max} = \frac{1}{2} L_2 I_{L_2}^2 = \frac{1}{2} L_2 I_{\text{peak}}^2 e^{\left(\frac{2t}{L_2/R_L}\right)} \tag{11}$$

Based on (11), the relationship between the value of L_2 and its stored energy is shown in Figure 5.

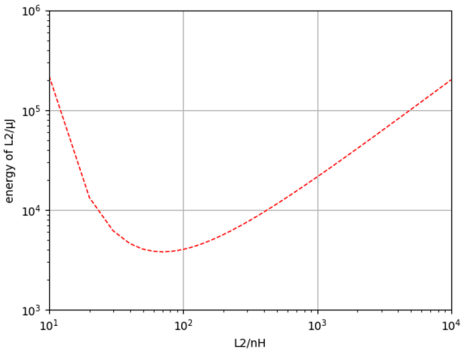


Figure 5. Energy varies with the value of L2.

It can be seen that when the L_2 equals 75 nH, the energy stored in L_2 reaches its maximum value. In practice, the L_2 is selected as 100 nH.

In order to ensure that the designed inductance works in the linear region, the maximum current of L_1 is selected as $i_{\text{L1-max}}$ = 9.5 A. Therefore, the inductance of L_1 can be calculated as

$$L_1 = \frac{V_1}{i_{L1-MAX}} \Delta T \tag{12}$$

Based on (12), when ΔT = 25 ns, V_1 = 120 V, and $i_{L1\text{-}max}$ = 9.5 A, L_1 = 320 nH is selected. Table 1 shows the selected circuit parameters.

Table 1. Pulse generator parameters.

Parameters	Values
L_1	320 nH
L_2	100 nH
C_1	1 nF
C_2	15 nF
ΔT	25 ns

3.4. Capacitance Design

During the interval2, in circuit loop2, the on-resistance of MOSFET (R_{DSon}), the on-resistance of the DSRD (R_{DSRD}), the capacitance C_2, and the inductance L_2 begin to resonate and the equation can be achieved as

$$L_2C_2\frac{d^2u_{C_2}}{dt^2} + RC_2\frac{du_{C_2}}{dt} + u_{C_2} = 0 \tag{13}$$

Assuming that the MOSFET is turned off when the resonant current of L_2 and C_2 reaches its peak value, the following equation can be achieved as

$$C_2 = \frac{4\Delta T^2}{\pi^2 L_2} \tag{14}$$

where the R represents the sum of the $R_{DS(on)}$ and R_{DSRD}. Based on (13) and (14), when ΔT = 25 ns and L_2=100 nH, C_2 = 15 nF is achieved.

3.5. MOSFET and Driver Design

In the pulse generator, the MOSFET is used to switch between forward-carrier injection and reverse-carrier extraction. In order to achieve an ultra-fast edge of the output pulse, the MOSFET needs to have a fast turn-off speed. Therefore, the RF MOSFET (DE475-102N21A) with 8 ns turn-off time is selected. To match the RF MOSFET (DE475-102N21A), the driver chip (IXRFD630) which is recommended by the device manufacturer is selected. The device parameters are listed in Table 2.

Table 2. MOSFET and driver parameters.

DE475-102N21A	IXRFD630
V_{DS} = 1000 V	V_{cc} = 30 V
I_{D25} = 24 A	I_{in} = 10 μA
I_{DM} = 144 A	I_{peak} = 28 A
$R_{DS(on)}$ < 0.45 Ω	V_{OH} = 30 V
T_{on} = 5 ns	T_r = 4 ns
T_{off} = 8 ns	T_f = 4 ns

4. Simulation Analysis

In order to analyze the impact of the parameter changes on the waveform of the output pulse, the simulation based on the software Pspice (https://www.pspice.com/ (accessed on 26 January 2024)) is conducted. Figure 6a shows the simulation output pulse waveform with a different conduction time ΔT, which is changed from 10 ns to 90 ns with an interval of 20 ns. It can be seen that when ΔT = 10 ns, the output pulse is relatively low due to the MOS being turned off at a small current in circuit loop1. When the ΔT changes from 30 ns

to 70 ns, the pulse amplitude increases slightly, and the energy of each power pulse also improves. As energy increases, electromagnetic interference becomes more serious, which brings a larger secondary pulse. When ΔT = 90 ns, the output pulse disappears due to the large recombination of carriers in the DSRD base region. Figure 6b shows the simulation output pulse waveform with a different conductor, L_2, which is changed from 40 nH to 130 nH with an interval of 30 nH. It can be seen that when L_2 = 70 nH, the pulse amplitude reaches its peak value. As the L_2 increases, both the pulse delay and pulse discharge time are prolonged. Figure 6c shows the simulation output pulse waveform with a different conductor, L_1, which is changed from 40 nH to 160 nH with an interval of 30 nH. It can be seen that a smaller L_1 should make the output pulse appear unexpectedly flat-topped, and a larger L_1 should make the pulse amplitude reduce. Figure 6d shows the simulation output pulse waveform with a different capacitor C_1, which is changed from 40 pF to 1640 pF with an interval of 400 pF. It can be seen that when C_1 = 440 pF, the pulse amplitude reaches its highest value. Figure 6e shows the simulation output pulse waveform with a different ΔV by adjusting V_1, which is changed from 30 V to 150 V with an interval of 30 V. It can be seen that the pulse amplitude does not change significantly, but the pulse width increases which means the pulse energy is related to the ΔV. Figure 6f shows the simulation output pulse waveform with different V_1 and V_2 while maintaining a constant ΔT. When V_1 increases to 150 V, the pulse amplitude no longer changes. However, considering that the energy storage of the inductor L_1 is small when the V_1 is low, the pulse amplitude is decreased due to insufficient energy storage. For trade-offs, V_1 = 210 V is optimal.

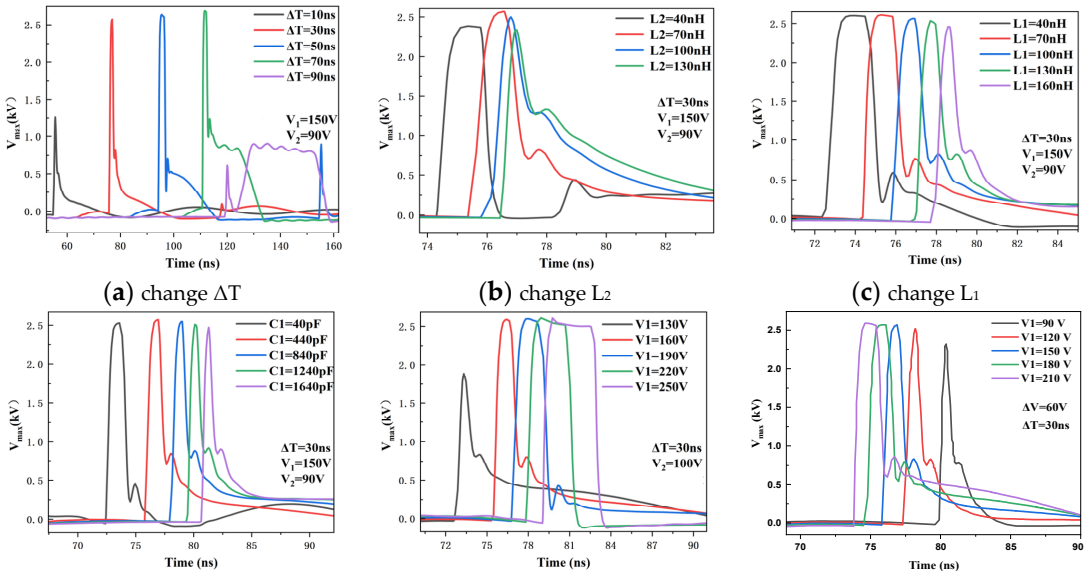


Figure 6. Changing circuit parameters; the output peak V_{max} change curve.

5. Experimental Result

According to the parameters obtained in Table 1, a pulse generator prototype was built based on a self-developed SiC DSRD, as shown in Figure 7a. We selected the IXRFD630 driver from IXYS company and the DE475-102N21A RF MOSFET as a switch. Figure 7b shows that the Tektronix MSO64B Oscilloscope captures the output waveform. The output load uses two 30 dB attenuators connected to the oscilloscope via coaxial lines. The SDN-414-05 current divider from T&M Germany was used to obtain the current flowing through the DSRD.

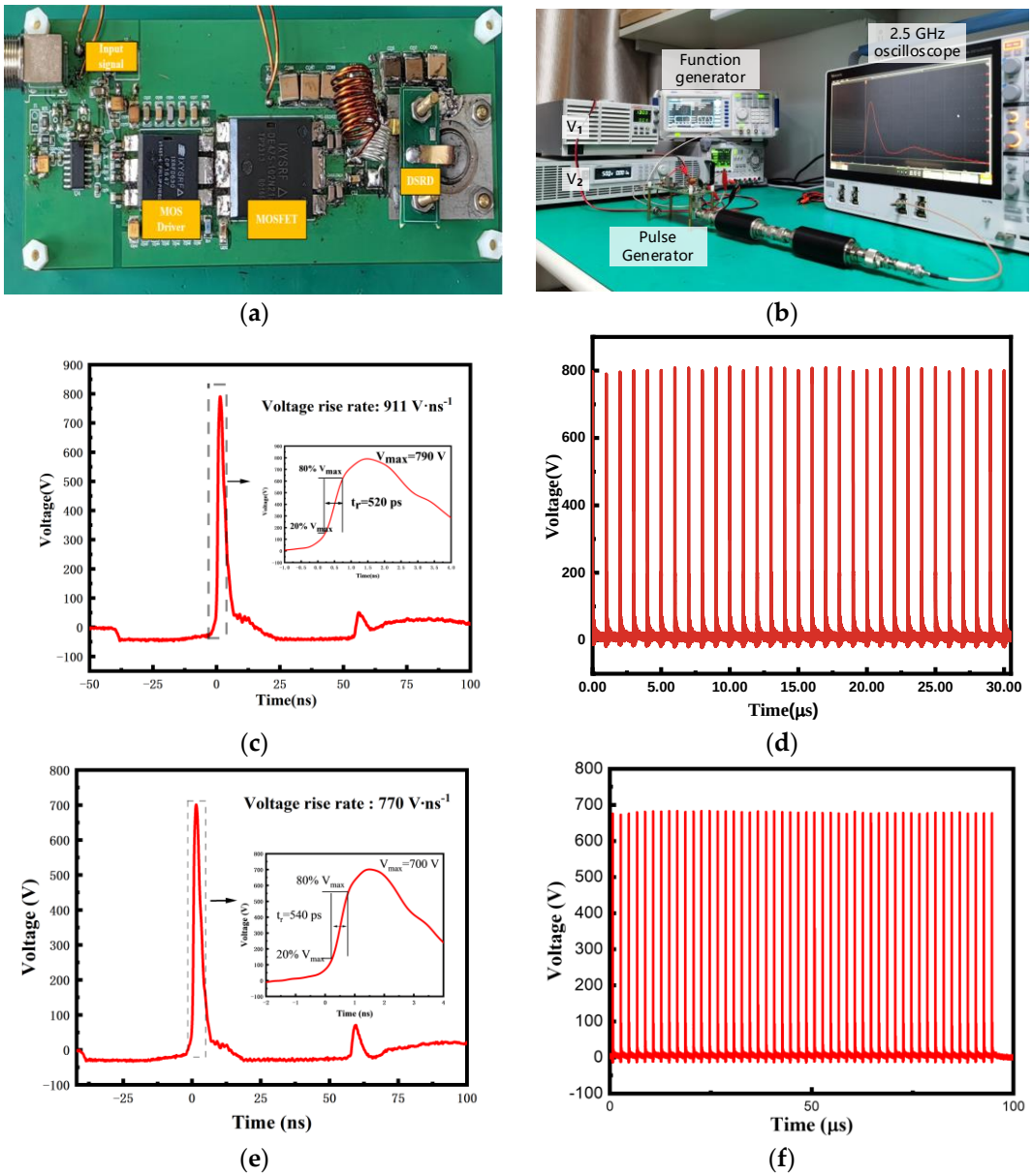


Figure 7. The pulse generator and output waveforms of the pulse generator are based on SiC DSRD. (**a**) Pulse generator based on self-developed SiC DSRD; (**b**) the test platform; (**c**) output voltage waveform of pulse generator with 790V; (**d**) output voltage waveform of pulse generator with peak amplitude 790 V and 1 MHz repetition rate under V_1 = 120 V, V_2 = 40 V; (**e**) output voltage waveform of pulse generator with peak amplitude 700 V under V_1 = 90 V, V_2 = 30 V; (**f**) output voltage waveform of pulse generator with peak amplitude 700 V and 500kHz repetition rate under V_1 = 90 V, V_2 = 30 V.

Figure 7c shows the waveform of a single power pulse. It can be seen that there is no pre-pulse in the output waveform. The peak voltage is 790 V, and the pulse rise time is 520 ps, which meets the design requirements (820 V) of the pulse generator. In addition, there is a slight secondary pulse observed in the waveform. Figure 7d shows the test result of the pulsed generator with a repetition rate of 1 MHz under V_1 = 120 V, V_2 = 40 V. Figure 7e,f show the output voltage waveform of the pulse generator with 700 V and 500 kHz repetition rate under V_1 = 90 V, V_2 = 30 V. The stable output pulse indicates the excellent stability of the pulsed generator.

6. Conclusions

According to the operating principle of DSRDs, this paper presents a collaborative design method of a SiC DSRD and the pulse generator based on it. An optimal method of DSRD parameters is proposed from the viewpoint of driving circuit requirements. In addition, a detailed simulation is conducted to verify design considerations and to analyze the impact of driving parameter changes on the output pulse waveform. A pulse generator based on a SiC DSRD was developed. The experimental results show that the generator can output a peak voltage of 790 V on a matching load of 50 Ω, with a pulse rise time of 520 ps. The pulse front is in the sub-nanosecond level with good stability and can be applied in miniaturized ultra-wideband electromagnetic pulse generators.

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Data Availability Statement: The authors confirm that the data supporting the findings of this study are available within this article.

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