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A 2.0–3.0 GHz GaN HEMT-Based High-Efficiency Rectifier Using Class-EFJ Operating Mode

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Abstract: In this paper, a CGH40010F GaN-based wideband RF rectifier with high rectification efficiency is presented. A novel continuous class-EFJ-mode rectifier is constructed by combining a continuous class-J-mode rectifier and class-EF-mode rectifier under specific impedance conditions. This novel continuous class-EFJ-mode rectifier has high rectification efficiency and wide bandwidth at the same time. For validation, a wideband high-efficiency class-EFJ-mode rectifier functioning within the 2.0–3.0 GHz range is designed, fabricated, and measured. The measurements indicate that, with an input power of 40 dBm and a resistance of 72 Ω on the dc load, the implemented rectifier sustains a rectification efficiency exceeding 60% across its entire operational frequency band. Meanwhile, the dimensions of the circuits are only 3 cm × 3.1 cm.

Keywords: wide band; class-EFJ; GaN transistor; high efficiency; rectifier

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1. Introduction

Recently, the scenario that can provide a high-capacity wireless power supply for vehicles and drones has gradually attracted much attention with the development of wireless power transmission technologies [1]. In the context of a wireless energy transmission system, the radio frequency (RF)-DC rectifier stands as a pivotal circuit module, and its performance is absolutely critical to the efficient operation of the entire system [2]. In order to obtain the optimum energy density and efficiency of the wireless power transmission, the rectifier needs to maintain high efficiency across a wide frequency band [3]. Conventional diode-based rectifiers have realized wide-bandwidth and high-efficiency operation [4–7]. In [4], a BAT15-03W Schottky diode-based broadband rectifier with a rectification efficiency of over 70% is implemented in the frequency band from 1.77 GHz to 2.85 GHz at the input power level of 11.5-dBm. In [5], an ultra-wideband high-efficiency rectifier is designed with an input power capacity of 23 dBm using a diode MAE1347B. In [6,7], a broadband radio frequency (RF) energy harvester is presented using a Schottky HSMS-2862 diode, which can work efficiently in a wide frequency band. The state-of-the-art performance of diode-based rectifiers is listed in Table 1. Table 1 indicates that the power capacity of diode-based rectifiers is typically less than 1 W. Although diode-based rectifiers can achieve good bandwidth and rectification efficiency, diode-based rectifiers' power capacity is low, which fails to satisfy the requirements of application situations with high performance capacity (at least 10 W).

Table 1. The state-of-the-art performance of diode-based rectifiers.

Ref.	Device	Frequency (GHz)	Input Power (dBm)	Efficiency (%)
[5]	Diode BAT15-03W	1.77–2.85	11.5	>70
[8]	Diode HSMS2860	2.0–3.05	10	>70
[9]	Diode HSMS2860	2.1–3.3	14	>70
[10]	Diode HSMS2860	1.7–2.8	12	>70
[8]	Diode HSMS2860	2.0–3.0	14	>70
[11]	Diode HSMS286F	2.08–2.58	15.5	>70
[12]	Diode HSMS2860	1.47–1.77	10	>70

In order to meet the requirements of high-power-capacity applications, transistor-based rectifiers have recently become promising solutions due to their high power capacity. Using the concept of the time-reversal duality, transistor-based rectifiers are evolved from the original power amplifiers [13]. Several transistor-based rectifiers with high efficiency, such as class-F [14], class-F^{-1} [15], and our recent work, class-GF [16], have been investigated. However, these rectifiers are narrowband, while high-efficiency transistor-based rectifiers with wide bandwidth are rarely reported. Most of the existing bandwidth enhancement methods for transistor-based rectifiers are achieved by the introduction of broadband phase shift networks [17,18]. The theoretical studies on the operation modes of rectifiers with wide bandwidth and high efficiency are inadequate.

Therefore, different from the presented technology, this paper investigates the operation mode of the rectifier itself. Through the analysis of the impedance characteristics of conventional class-EF rectifiers and continuous class-J rectifiers, it is found that class-EF rectifiers and continuous class-J rectifiers can be effectively merged under certain conditions. As a result, a rectifier called continuous class-EFJ-mode is constructed, which incorporates the high-efficiency characteristics of the class-EF with the broadband characteristics of the continuous class-J mode. The load impedance of the novel class-EFJ rectifier is theoretically derived. The introduction of the continuous-mode parameter has resulted in the fundamental and second-harmonic impedances of the continuous class-EFJ rectifier becoming a dynamic range rather than a fixed value. This extended impedance space provides convenience for the design of the broadband matching network. This flexibility is advantageous in widening the operating bandwidth of the rectifier. To substantiate the efficacy of the proposed approach, a continuous class-EFJ rectifier utilizing a GaN HEMT is designed and fabricated.

2. Analysis of the Proposed Rectifier

Figure 1 presents the GaN HEMT-based rectifier topology, which is converted from a power amplifier according to the principle of the time-reversal duality [19]. In the architecture of the transistor-based rectifier, the RF output terminal and DC drain bias of the original power amplifier are used as the RF input terminal and DC output terminal of the rectifier, respectively. As illustrated in Figure 1, the rectifier mainly consists of four parts: the input matching network (with a phase θ_{IMN}), the output matching network (with a phase θ_{OMN}), the gate bias line and the phase shift network, and θ_{PS} is the phase shift imparted by the phase shifter network. θ_{IN} represents the phase of the input power, $\theta_{\mathrm{I\text{-}OMN}}$ is the phase shift from the input to output matching network, and $\theta_{\mathrm{I\text{-}PS}}$ refers to the phase shift from the input to phase shift network.

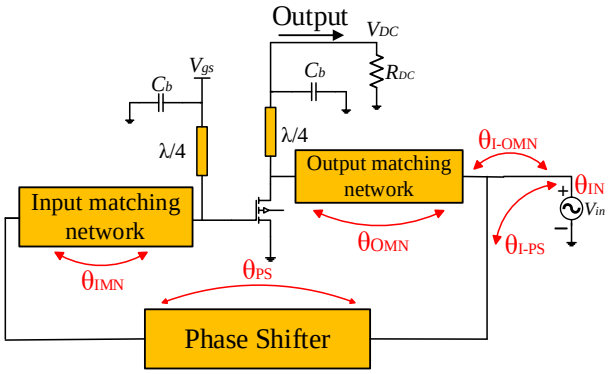


Figure 1. Topology diagram of the synchronous transistor-based rectifier.

Utilizing the principle of time-reversal duality, the designed rectifier can be achieved via the conversion of the power amplifier. Therefore, using the conventional class-EF-mode PA described in [20] as a reference, the corresponding fundamental and harmonic load impedance, $Z_{1,EF}$, $Z_{2,EF}$, and $Z_{3,EF}$, of the conventional class-EF-mode rectifier are delineated as follows.

$$Z_{1,EF} = (1 + j * A) * R \tag{1}$$

$$A = \frac{\tau_D - 0.5sin(2\tau_D)}{sin\tau_D * sin\tau_D}, R = \frac{2(1 + cos\tau_D)^2}{\pi^2}\frac{V_{DC}^2}{P_o} \tag{2}$$

$$\begin{cases} Z_{2,EF} = 0 \\ Z_{3,EF} = \infty \end{cases} \tag{3}$$

where τ_D denotes the turn-off time of the transistor (in radians). P_o denotes the output power, and V_{DC} represents the dc bias voltage. Based on (1)–(3), Figure 2a plots the load impedance space of the class-EF mode. The load impedance of the EF mode is limited to a fixed value. Although it can achieve high efficiency through the switch operation harmonious control, it is obvious that its working bandwidth is very narrow.

Accordingly, drawing upon the theory of the continuous class-J-mode PA in [21], the corresponding fundamental load impedance $Z_{1\text{-}CJ}$ and second-harmonic load impedances $Z_{2\text{-}CJ}$ of the continuous class-J-mode rectifier are formulated as

$$Z_{1-CJ} = (1 + j * \gamma)R_{opt} \tag{4}$$

$$Z_{2-CJ} = -j\frac{3\pi\gamma}{8}R_{opt} \tag{5}$$

where γ represents the continuous-mode parameter, the value of which falls within the range of -1 and 1. Additionally, R_{opt} signifies the optimal load impedance for the device being utilized, computable as follows:

$$R_{opt} = \frac{2(V_{DC} - V_K)}{I_{max}} \tag{6}$$

where V_K is the knee voltage of the transistor. I_{max} signifies the maximum current. Based on (4)–(6), Figure 2b shows the load impedance space of the continuous class-J mode. It can be observed from the figure that, compared with the class-EF mode, due to the introduction of continuous-mode parameter γ, the impedance space of the J mode has expanded. This extended impedance space can be used to achieve large bandwidth. However, the expansion of impedance is exchanged at the cost of reducing efficiency. Therefore, compared with the EF mode's ideal 100% efficiency, the efficiency of continuous J mode can usually only reach about 78.5%.

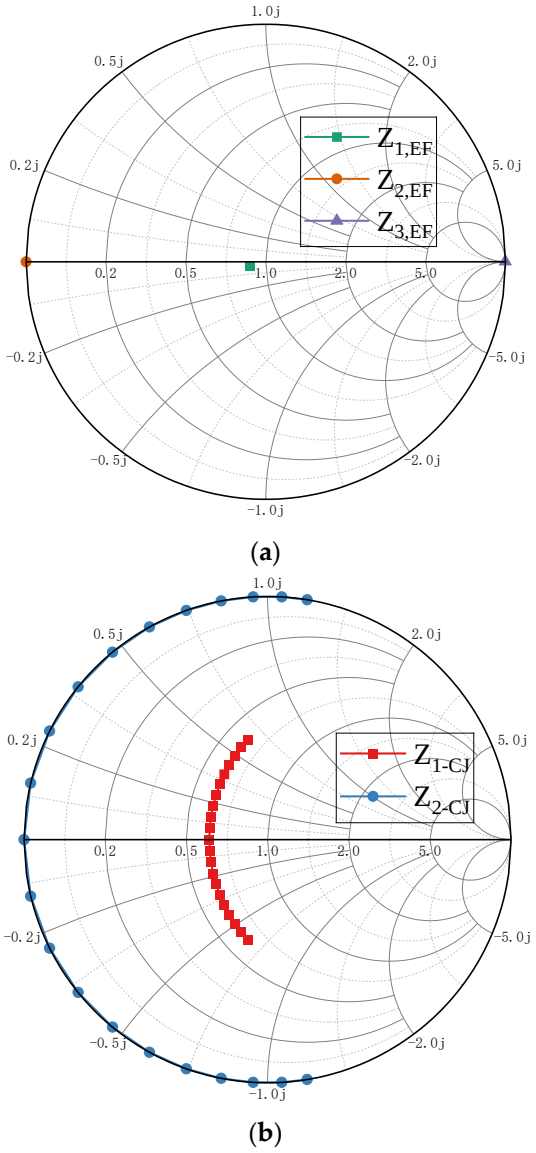


Figure 2. Load impedance space of the class-EF and continuous class-J modes: (**a**) class-EF mode; (**b**) continuous class-J.

Based on the above descriptions of the EF mode and continuous J mode, it can be concluded that they have their own advantages and deficiencies; that is, the EF mode has high efficiency but narrow bandwidth, and the continuous J mode has a wide bandwidth but low efficiency. Therefore, how to combine the advantages of the two to realize a working model with both bandwidth and high efficiency is worth further exploring.

Next, by analyzing the impedance expression of the two modes, we look for the possibility of integrating the two modes. Upon comparing (1) with (4), it becomes apparent that the load impedance formulations for class-EF and continuous class-J bear similarities. To facilitate the integration of these two operational modes, the following relationships need to be met:

$$\begin{cases} (1 + j * \gamma)R_{opt} = (1 + j * A)R \\ A = \gamma \\ R = R_{opt} \end{cases} \tag{7}$$

By utilizing (2) and (7), the τ_D can be determined to fall within the range of -1.20601 to 1.20601, provided that γ remains between -1 and 1. The correlation between τ_D and γ is graphically represented in Figure 3a.

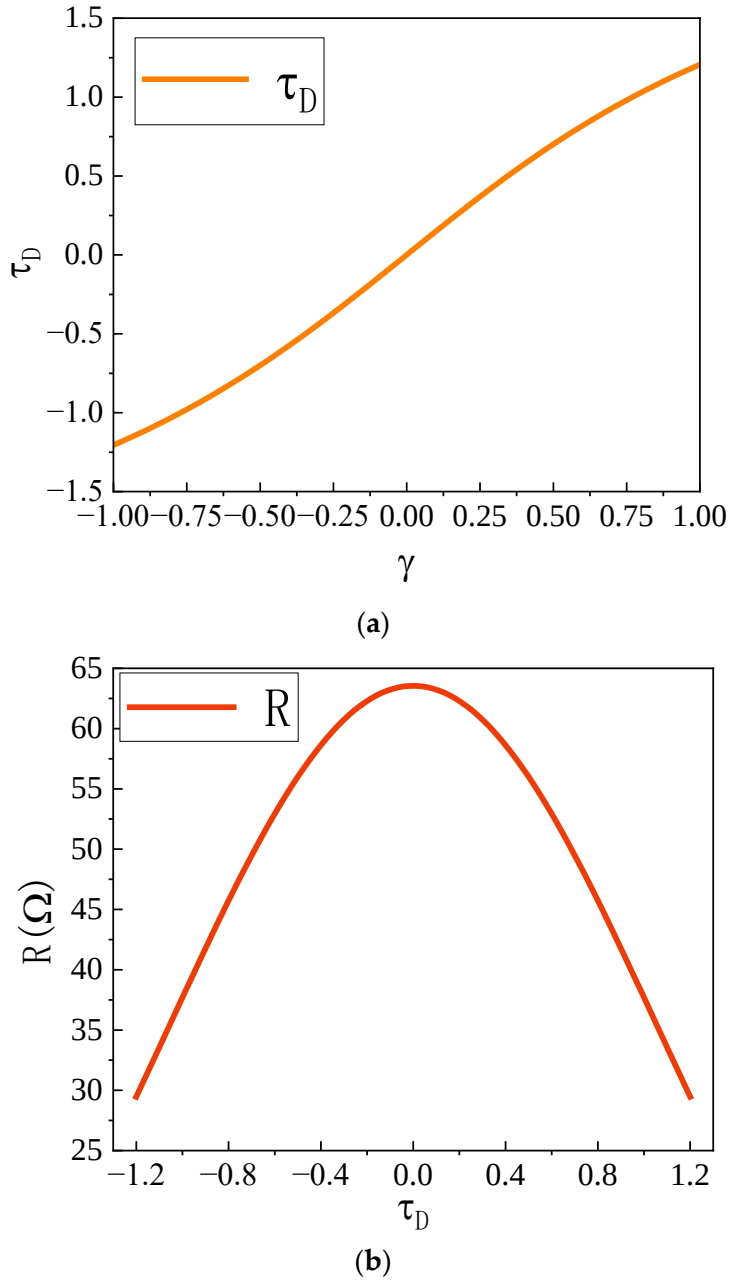


Figure 3. (**a**) Relationship between τ_D and γ; (**b**) relationship between R and τ_D.

This paper utilizes the Cree CGH40010F as the primary active device. Given that V_K is approximately 5 V, V_{DC} is set as 28 V, and I_{max} stands at 1.5 A. Then, the optimum load R_{opt} can be determined using (6) and is calculated to be 30.7 Ω. Furthermore, (2) can be used to calculate the value of R, provided that the condition of $-1.20601 \leq \tau_D \leq 1.20601$, P_o = 10 W, V_{DC} = 28 V. Figure 3b illustrates the value of R versus τ_D. As depicted in Figure 3b, the value of R ranges from 29.24 Ω to 63.55 Ω. Evidently, the value of R_{opt} falls within this range, thus confirming the validity of (7). It is indicated that the class-EF-mode rectifier and the continuous class-J-mode rectifier can be combined when certain impedance conditions are satisfied. Then, the fundamental and harmonic load impedances of the continuous class-EFJ-mode rectifier can be expressed as

$$Z_{1-EFJ} = (1 + j * \gamma)R \tag{8}$$

$$Z_{2-EFJ} = -j\frac{3\pi\gamma}{8}R,\ Z_{3-EFJ} = \infty \tag{9}$$

where R is between 29.24 Ω and 63.55 Ω.

The load impedances of the proposed continuous class-EFJ-mode rectifier expressed in (8) and (9) are illustrated in Figure 4. From Figure 4, it is evident that, when $\gamma = 0$, the fundamental load impedance of the continuous class-EFJ-mode-rectifier conforms to the expression of the fundamental load impedance of the traditional class-EF-mode rectifier. Additionally, the conditions for a shortened circuit at the second harmonic and an open circuit at the third harmonic are satisfied. When γ assumes other values, the class-EFJ-mode rectifier operates as the continuous class-J-mode rectifier, leading to expanded impedance ranges as parameter γ varies. Further, in comparison to the traditional continuous class-J, the introduction of the additional variable parameter R offers an expanded resistive impedance space. This broadened impedance design space subsequently enables a wider operational bandwidth.

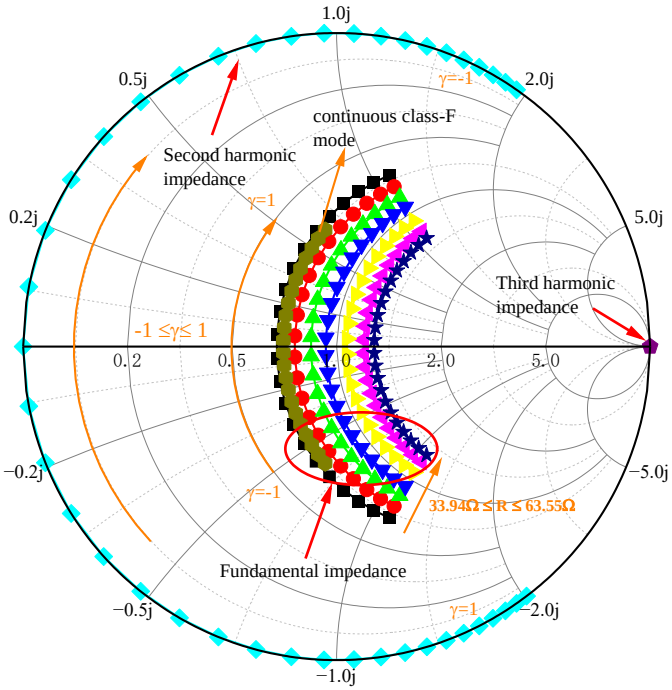


Figure 4. Impedance space of the class-EFJ-mode rectifier.

3. Design of the Rectifier

For validation, a wideband high-efficiency class-EFJ-mode rectifier operational within the 2.0–3.0 GHz frequency range is designed based on Rogers 4350B substrate ($\varepsilon_r = 3.66$, $h = 30$ mil) using a CGH40010F GaN HEMT, which is modeled in [22].

The gate voltage V_{gs} is set to −3.2 V based on the previously derived τ_D. R_{opt} is taken as 30.7 Ω. For the continuous class-EFJ-mode rectifier, the theoretical second-harmonic impedance is purely reactive, and the theoretical third-harmonic impedance approaches infinity. The designed harmonic control network, depicted in Figure 5a, employs transmission lines TL1 and TL2 to meet the second-harmonic impedance requirements. Transmission lines TL1, TL3, and TL4 are used to satisfy the third-harmonic impedances expressed in (9). The output matching network is designed in 2.0–3.0 GHz using the stepped impedance matching technology. The package parameters of this device are integrated into the output network after undergoing minor optimization in ADS 2022 software. The simulated impedance at the output is shown in Figure 5b. It is observable that the load impedance lies within the theoretical impedance space, as expressed in (8) and (9).

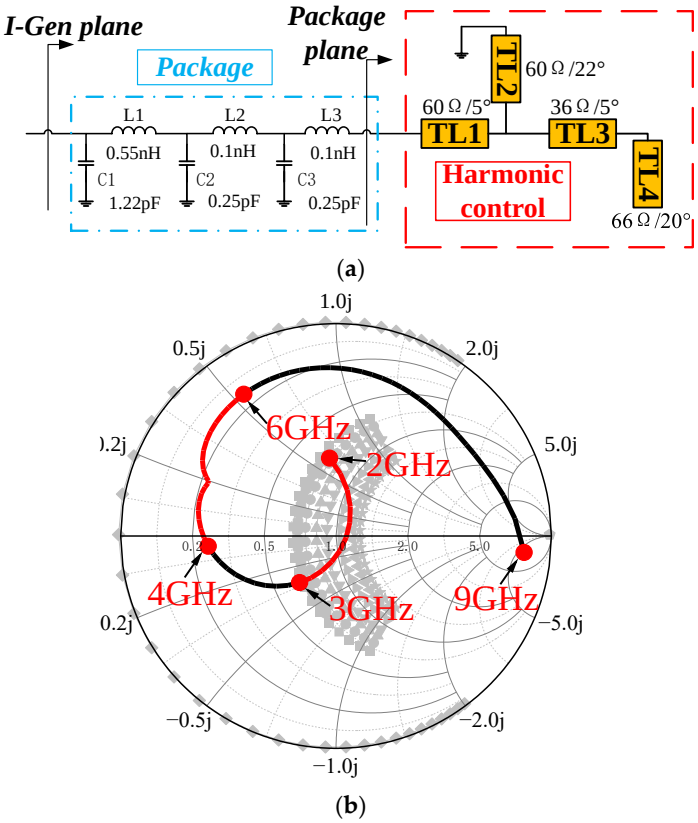


Figure 5. (**a**) Harmonic tuning network; (**b**) simulated impedance versus operating frequency.

The necessary phase disparity between the gate and the drain (θ_{DG}) terminals is 180° or an odd multiple of 180° according to [15]. As shown in Figure 1, the phase difference is expressed as

$$\theta_{DG} = (\theta_{I-OMN} + \theta_{OMN}) - (\theta_{I-PS} + \theta_{PS} + \theta_{IMN}) = (2n+1)\pi\ (rad) \quad (10)$$

A wideband phase-shift network needs to be designed to satisfy the desired phase difference θ_{DG}. As shown in Figure 6a, transmission lines TL5–TL10 are employed to realize the desired phase conversion. The phase θ_{DG} between the gate and drain nodes and the phase θ_{PS} of the shift network are illustrated in Figure 6b. As depicted in Figure 6b, the θ_{PS} values exhibit a range of −157.8° to −177.6° within the frequency band of 2.0–2.4 GHz, whereas they span from 179.9° to 151.8° within 2.45–3.0 GHz. The value of θ_{DG} is between 180.5° and 184.7° in 2.0–3.0 GHz, which is approximately equal to 180° defined in (10). Meanwhile, the stepped impedance matching technology is utilized to match the source impedance to the standard terminal impedance. Then, the phase shift network and the input and output networks are combined into a completed rectifier circuit that is shown in Figure 7.

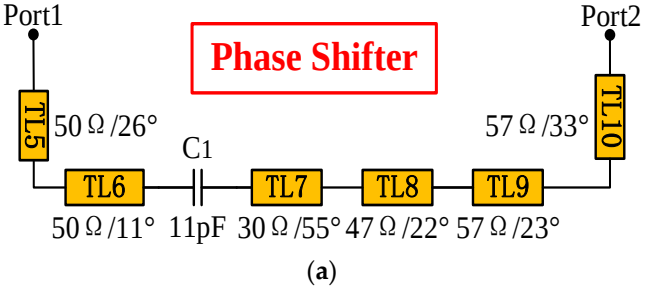


Figure 6. *Cont.*

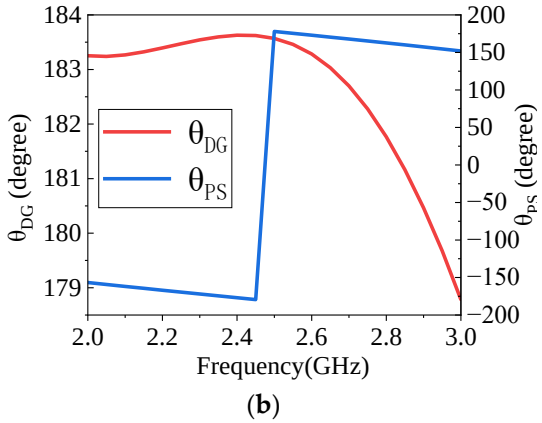


Figure 6. (**a**) Phase shift network; (**b**) simulated phase of drain-gate and phase of phase shift network.

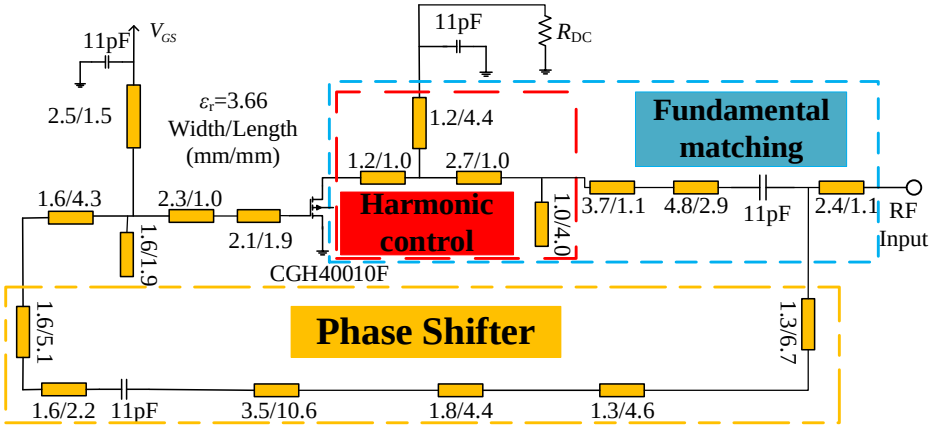


Figure 7. Complete schematic of the designed rectifier.

The waveforms for voltage and current at the drain are simulated with RF input power levels ranging from 20 to 40 dBm. The simulated waveforms are shown in Figure 8, in which the voltage (blue) is negative and the current (red) is positive. As presented in [23], transistor-based rectifiers have positive and negative operating polarities. The class-EFJ-mode rectifier, designed as such, depicts a negative polarity in operation. A photograph depicting the fabricated rectifier, measuring 3 cm × 3.1 cm in size, is presented in Figure 9.

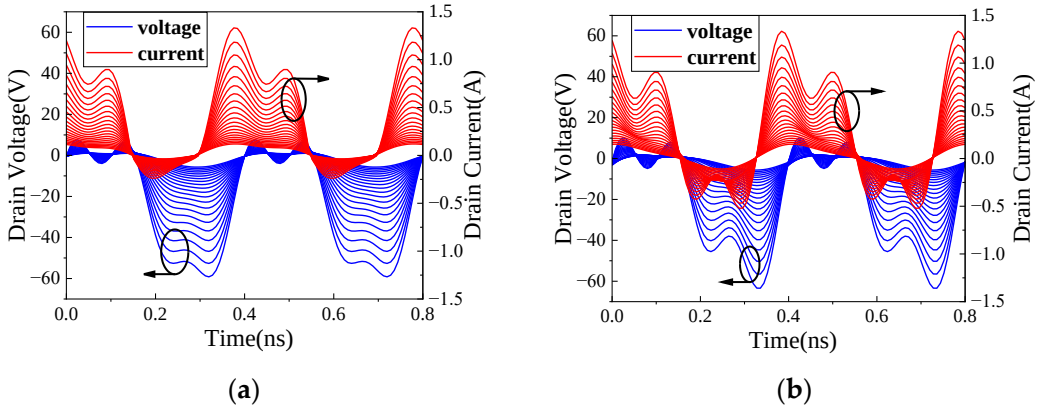


Figure 8. Simulated drain voltage and current waveforms at several frequencies (sweeping RF input power from 20 to 40 dBm): (**a**) 2.5 GHz; (**b**) 2.7 GHz.

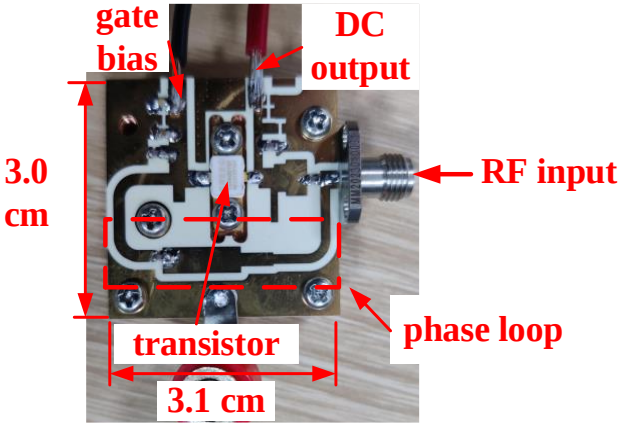
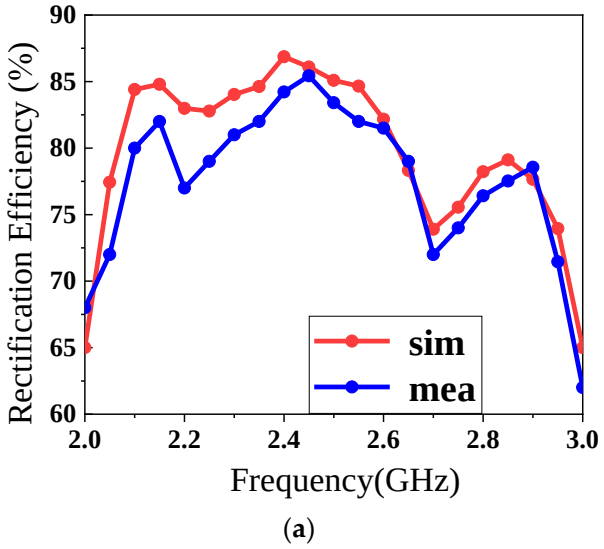


Figure 9. Photograph of the fabricated rectifier.

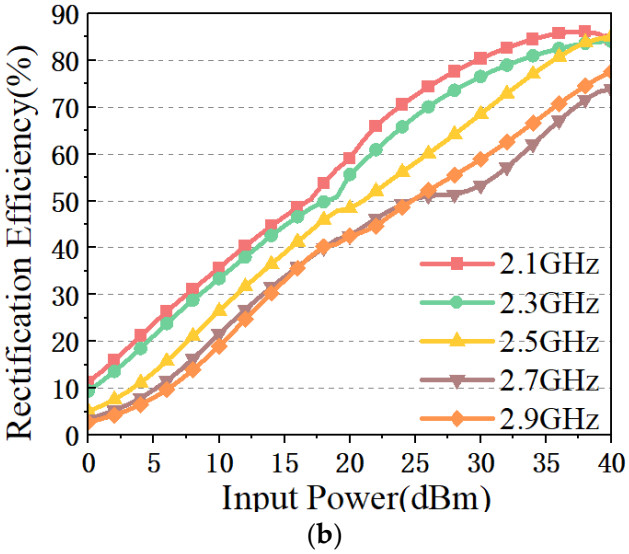
Testing has been conducted on the fabricated rectifier, and the measurements are presented in Figure 10a. With an RF input power at 40 dBm and a dc load at 72 Ω, the measured rectification efficiency of the rectifier ranges from 60% to 87% across the 2.0–3.0 GHz range. In particular, as shown in Figure 8b, at 2.7 GHz, the voltage and current have more overlapping portions, which increases the losses. This leads to a significantly lower efficiency than that of other frequencies. Figure 10b shows the dynamic profiles of rectification efficiency versus RF input power at several representative frequencies. With an increase in the RF input power ranging from 20 dBm to 40 dBm, the rectification efficiency experiences a significant rise from 40% to 85%. Figure 10c,d illustrate the rectification efficiency profiles for different RF input power levels under varying conditions at 2.45 GHz, including the gate bias voltages (V_{gs}) and DC loads (R_{dc}). Furthermore, as shown in Figure 10b,c, the rectification efficiency profiles exhibit distinct patterns due to changes in the dc load and gate bias voltages.

Table 2 presents some of the relevant rectifier works. As shown in Table 1, the class-EFJ-mode rectifier presented exhibits excellent operating bandwidth and rectification efficiency among GaN HEMT-based broadband rectifiers. Meanwhile, the proposed rectifier boasts a greater input power capability when compared to rectifiers that utilize diodes.



(**a**)

Figure 10. *Cont.*



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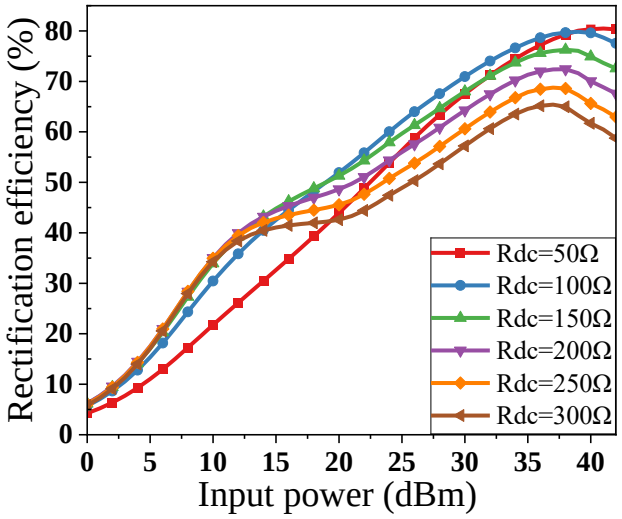
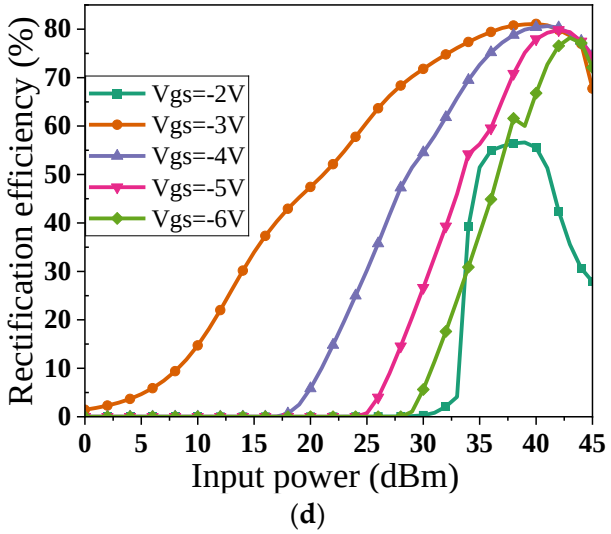


(**c**)



(**d**)

Figure 10. (**a**) Simulated and measured efficiency versus frequency; (**b**) measured efficiency versus input power; (**c**) measured efficiency versus DC load when V_{gs} = −3.2 V at 2.45 GHz; (**d**) measured efficiency versus gate bias voltage when R_{dc} = 72 Ω at 2.45 GHz.

Table 2. Comparison of performance with other rectifiers.

Ref.	Device	Frequency (GHz)	Pin (W)	Efficiency (%)	Mode/Class of Operation	Size (cm × cm)
[4]	diode	1.77–2.85	0.015	70–82.3	none	2.25 × 2.28
[5]	diode	0.04–6.74	0.2	50–74.8	none	4.3 × 7.4
[16]	GAN HEMT	2.45	10	90.7	Class-GF	3.4 × 2.6
[18]	GAN HEMT	2.65–2.95	10	60–84.9	none	10.89 × 6.65
[24]	GAN HEMT	0.6–1.15	10	60–80.1	Class-F^{-1}	5 × 5.2
[25]	GAN HEMT	1.17/2.4	10	77/75	Class-F/F^{-1}	5.2 × 5
This Work	**GAN HEMT**	**2.0–3.0**	**10**	**60–87**	**Class-EFJ**	**3 × 3.1**

4. Conclusions

This paper proposes a high-efficiency GaN-based wideband RF rectifier. The integration of the class-EF rectifier mode and the continuous class-J rectifier mode serves to notably broaden the operating bandwidth of the class-EFJ rectifier. For validation, a continuous class-EFJ rectifier is fabricated, operable within the frequency range of 2.0–3.0 GHz. The rectification efficiency ranging from 60% to 87% can be realized over the entire operating frequency band when the input power is set to 40 dBm and the DC load is 72 Ω. In comparison to the related rectifiers, the class-EFJ rectifier implemented in this paper demonstrates strong competitiveness in terms of both efficiency and bandwidth.

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