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A Pseudo-Differential LNA with Noise Improvement Techniques for Concurrent Multi-Band GNSS Applications

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Abstract: A low-noise amplifier (LNA) design with the operation of concurrent dual-band for Global Navigation Satellite System (GNSS) receivers with single channel is presented in this work. This LNA structure has an inductively degenerated cascode architecture and is pseudo-differential, operating at two frequencies simultaneously (1.2 GHz and 1.57 GHz). Two noise reduction/cancellation techniques, using load capacitor and feedforward path, respectively, are proposed resulting in an excellent improvement in the noise figure (*NF*). The input matching circuit uses both series and parallel resonant components to enable concurrency. The adopted pseudo-differential structure results in input balun elimination. Inductively degenerated cascode topology provides both input impedance and optimum noise impedance matching. The soundness of the proposed approach has been demonstrated in a 0.18- μ m CMOS technology by TSMC. Simulation results show that at 1.2 GHz and 1.57 GHz the LNA achieves -13 dB and -11 dB of input matching, 24.6 dB and 24.7 dB of gain, 1.47 dB and 1.43 dB of *NF*, respectively. The input-referred 1-dB compression point (IP_{1dB}) is around -16 dBm, while the input-referred third-order intercept point (IIP_3) achieves -2.2 dBm at 1.2 GHz and -0.6 dBm at 1.57 GHz. The LNA draws about 13 mA from a 1.8-V supply voltage.

Keywords: concurrent dual-band; LNA; feedforward path; multi-band single-channel; GNSS; noise cancellation



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1. Introduction

The Global Navigation Satellite System (GNSS) covers the entire world with its precise positioning information for electronic devices. The information is transmitted through the radio frequency signals that are in the line of sight of the satellites. On the other hand, providing detailed location, time, and speed data allows GNSS systems to perform management, navigation and monitoring [1–4].

Different countries have been encouraged to develop their own GNSS systems because of increasing demand and widespread use in electronic devices and smartphones. The Global Positioning System (GPS), which was developed in 1970 by the United States of America, was the first GNSS system [5]. The main application of GPS at its infancy days was for the military, but it quickly moved on to non-military use. After that, Russia introduced the GLONASS system in 1982. China and European nations have also developed their own systems in 2000 and 2011, named COMPASS (BeiDou-2 (BD-2)) and Galileo. The standard frequency bands recognized for these systems are 1.2 GHz and 1.57 GHz.

The main weakness of GPS is its imprecision, particularly in multipath and jamming circumstances. Places covered by trees or inside apartments, tunnels, and noisy places are instances that highlight the GPS's low sensitivity issues, as a simple one-band GNSS receiver cannot provide sufficient availability and accuracy of navigation [6]. This encourages designers to move toward multi-band GNSS systems to overcome these problems [7].

An integrated Galileo and GPS receiver can deal with the abovementioned problems and provide more precise navigation regarding non-military GPS. Supporting alternative navigation bands and systems became a more interesting topic since these systems' reliability was likewise unable to satisfy the highest sensitivity requirements. It is consequently worthwhile to explore GNSS receiver design with multi-band capability.

Multi-band receivers are categorized into two main groups [8], including concurrent and non-concurrent receivers. Regarding the non-concurrent receivers, their high area consumption due to their adjustable capacitors and inductors for each band makes them less attractive in portable equipment [8–15]. On the other hand, multi-band concurrent structures can be also divided into two different categories as follows:

- (1) Multi-channel [5–7,16–20];
- (2) Single-channel [4,21,22].

In multi-band multi-channel concurrent receivers, one physical channel is assigned to each band. Therefore, like non-concurrent multi-band structures, this architecture suffers from a very high area consumption. However, single-channel receivers use only one physical channel for simultaneous reception in different bands, which makes them an optimum choice for GNSS applications due to their lower area and power consumption. Receiving concurrent signals through just one channel requires a proper LNA structure and a frequency plan.

In this paper, an LNA for a concurrent multi-band single-channel GNSS receiver is proposed. The main purpose of the adopted LNA topology is to operate in multi-bands, along with the lowest possible noise figure (NF). Since GNSS signals are so weak and their power lies beneath the thermal noise level [6], the NF is crucial in the LNA design for GNSS receivers, especially in concurrent operation. To this aim, two different noise improvement strategies have been exploited for multi-band operation, which allows achieving a significant reduction of the NF with respect to the previous work in [23], with a consequent improvement of the receiver sensitivity performance. The proposed design strategies in this work are based on adding a load capacitor for noise improvement and a feedforward path as a noise cancellation technique. Compared to the earlier work in [23], the NF is significantly improved by the employed design strategies, with reductions of roughly 0.9 dB for both frequency bands, 1.2 GHz and 1.57 GHz. In dual-band operation, this enhancement has been made possible by upholding a better tradeoff between the other design parameters (i.e., input matching, gain, linearity, and power consumption).

The paper is arranged as follows. In Section 2, the proposed concurrent dual-band LNA topology is introduced and discussed. Section 3 presents the design of the LNA by means of a full analysis based on simulations. Section 4 draws the main conclusions and describes the advantages of the proposed structure in comparison with the state of the art.

2. LNA Architecture

Figure 1 depicts the basic LNA topology for an initial design, which is a pseudo-differential amplifier with concurrent dual-band performance based on [23]. The amplifier is based on inductively degenerated cascode topology. Indeed, this topology can provide simultaneous input impedance and optimum noise impedance matching to achieve the maximum gain and minimum NF [22] when operated in narrowband modes, as in GNSS receivers. The following sub-sections discuss the main design parameters of the LNA.

2.1. Concurrent Dual-Band Input–Noise Matching

Input matching guarantees the optimum power transmission, and therefore it is crucial in the LNA design. As shown in Figure 1, the adopted input-matching network consists of a parallel resonant network (i.e., L_1C_1) along with a series one (i.e., L_2C_T and L_S , with $C_T = C_{ex} \parallel C_{gs1}$). To achieve concurrent dual-band performance, the input-matching network is designed to resonate in two bands simultaneously. Thus, parallel and series resonant parts enable the circuit for simultaneous matching in both GNSS frequency bands.

$$i_{left-side} = i_1 \left(1 + \frac{j\omega C_T}{g_{m1}} \right) \quad (4)$$

where i_1 is the drain current of M_1 and g_{m1} is the transconductance of transistor M_1 . Finally, the value of C_C is determined as follows:

$$C_C = \frac{(1-P)(C_{gs3}^2\omega^2 - g_{m1}^2)}{g_{m1}^2 + (1-P)(g_{m1}^2 - C_{gs3}^2\omega^2)} C_{gs2} \quad (5)$$

Equation (5) indicates that the value of C_C can be set by the transconductance of input transistor g_{m1} , the gate-source capacitor $C_{gs2,3}$ of transistor $M_{2,3}$, and the parasitics at the M_5 drain node. Thus, the imbalance of the LNA, which is a result of unequal current signals at the right and left sides of the amplifier, can be compensated by choosing the proper value of the compensation capacitor C_C based on (5).

2.3. Noise

Due to the position of the LNA in the receiver chain (i.e., immediately after the antenna), it plays a key role in the noise performance of the system. Besides the input noise-matching approach described in Section 2.1, the overall noise of the LNA can be reduced by means of proper techniques. In this work, two techniques for noise reduction and noise cancellation have been exploited, i.e., by means of a load capacitor and a feedforward path, respectively. The adopted techniques are detailed in the following.

2.3.1. Noise Figure Improvement by Means of a Load Capacitor

Figure 2 shows the amplifier with the current source, i_{n1} , that models the channel thermal noise of the input transistor M_1 . Indeed, it plays an important role in the overall NF performance of the LNA. The output noise voltages (i.e., $V_{o1,n}$ and $V_{o2,n}$) due to the noise current i_{n1} are calculated as follows, where Z_X is the impedance of node X and R_L is the load resistor.

$$V_{o1,n} = -\frac{R_L Z_X g_{m3}}{2} i_{n1} \quad (6)$$

$$V_{o2,n} = \frac{R_L g_{m4}}{g_{m4} + j\omega C_{gs4}} \left[\frac{Z_X C_C g_{m2}}{2(C_{gs2} + C_C)} \right] i_{n1} \quad (7)$$

$$Z_X = \frac{1}{g_{m3}} \left\| \frac{1}{j\omega C_{gs3}} \right\| \left(\frac{1}{j\omega C_C} + \frac{1}{j\omega C_{gs2}} \right) \quad (8)$$

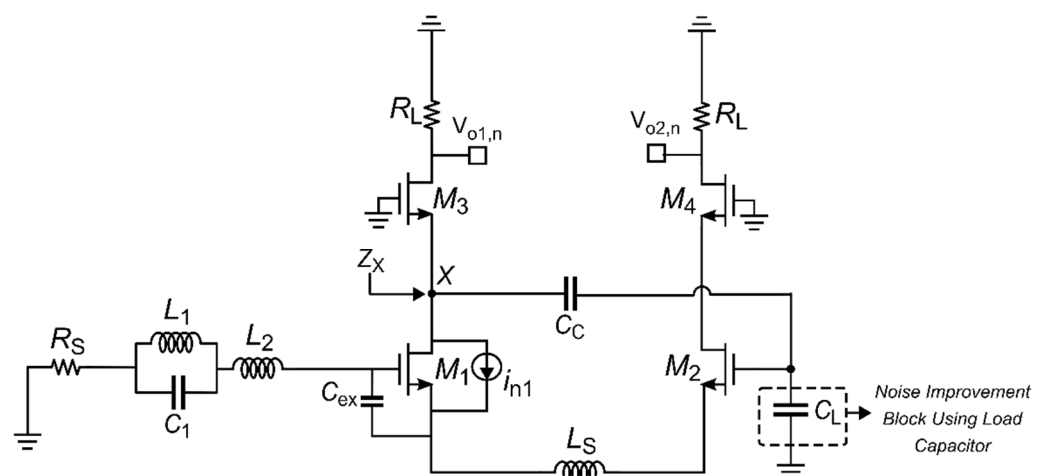


Figure 2. *NF* improvement by using a load capacitor.

As shown in Figure 2, the compensation capacitor C_C allows the input noise to flow to the right-hand side of the circuit, causing an increment of the noise figure. For this reason, it is effective to reduce the noise effect on the right-hand side of the amplifier. Equation (7) states that $V_{o2,n}$ is related to the ratio $C_C/(C_{gs2} + C_C)$, which has to be reduced to improve the NF. Since capacitor C_C has already been set for the balance condition between the two sides of the circuit by means of equation (5), C_{gs2} should inevitably be increased by means of an additional load capacitor, C_L , in the right-hand side of the circuit, as shown in Figure 2. The load capacitor, C_L , also results in a lower value of Z_X , which, based on (6) and (8), decreases the left-hand side noise.

On the other hand, the load capacitor influences the input matching through the M_1 gate-drain capacitor, C_{gd1} . To analyze the load capacitor effect on the input matching, the admittance Y_{in} seen from the gate of M_1 is calculated considering the capacitance C_{gd1} , while assuming L_S to be very small.

$$Y_{in} = j\omega \left[C_T + C_{gd1} + \frac{g_{m1}g_{m3}C_{gd1} - \omega^2 C_{gd1}^2 C_{eq}}{g_{m3}^2 + C_{eq}^2 \omega^2} \right] + \frac{C_{gd1}\omega^2 (g_{m3}C_{gd1} + C_{eq}g_{m1})}{g_{m3}^2 + \omega^2 C_{eq}^2} \quad (9)$$

$$C_{eq} = \frac{(C_L + C_{gs2})C_C}{C_C + C_L + C_{gs2}} + C_{gs3} + C_{gd1} \quad (10)$$

Based on (9), the equivalent impedance seen from the gate of the input transistor consists of a parallel RC according to (11) and (12).

$$C_{in} = C_T + C_{gd1} + \frac{g_{m1}g_{m3}C_{gd1} - \omega^2 C_{gd1}^2 C_{eq}}{g_{m3}^2 + C_{eq}^2 \omega^2} \quad (11)$$

$$R_{in} = \frac{g_{m3}^2 + \omega^2 C_{eq}^2}{C_{gd1}\omega^2 (g_{m3}C_{gd1} + C_{eq}g_{m1})} \quad (12)$$

The resistive contribution, R_{in} , is quite high and can be considered as an open circuit. As shown in (11), C_{in} , which is the input capacitive contribution, consists of three parallel capacitors. Thus, including the load capacitor, C_L , will result in adding two parallel capacitors to C_T , i.e., C_{gd1} and $(g_{m1}g_{m3}C_{gd1} - \omega^2 C_{gd1}^2 C_{eq})/(g_{m3}^2 + C_{eq}^2 \omega^2)$. In other terms, these two extra capacitors increase the effectiveness of C_T . To achieve input matching, C_T has to meet the following equation:

$$\frac{1}{C_T} = \omega^2 \left(\frac{L_1}{1 - \omega^2 L_1 C_1} + L_2 \right) \quad (13)$$

Since adding C_L would increase the amount of C_T , from (13), smaller L_1 and L_2 are needed for input matching. On the other hand, L_1 and L_2 are both gate inductances, and smaller values will turn in smaller resistive losses and a better noise figure. Therefore, apart from reducing the channel thermal noise of the input transistor, the addition of the load capacitor C_L would improve the noise through a smaller amount of input inductances.

2.3.2. Noise Cancellation Using a Feedforward Path

The basic idea for noise cancellation exploits an additional amplifier, which senses the input noise. The combination of the outputs of the additional and main amplifier results in noise cancellation of the input transistor [24].

As shown in Figure 3, the M_1 gate and source signals have the same signs, but the noise signs are opposite. Therefore, connecting the left-hand side of the circuit through an extra path could cancel the effect of i_{n1} on the right-hand side. In this approach, both the gate noise and the signal of M_1 are transferred to the right-hand side of the circuit through a negative gain amplifier (A_f).

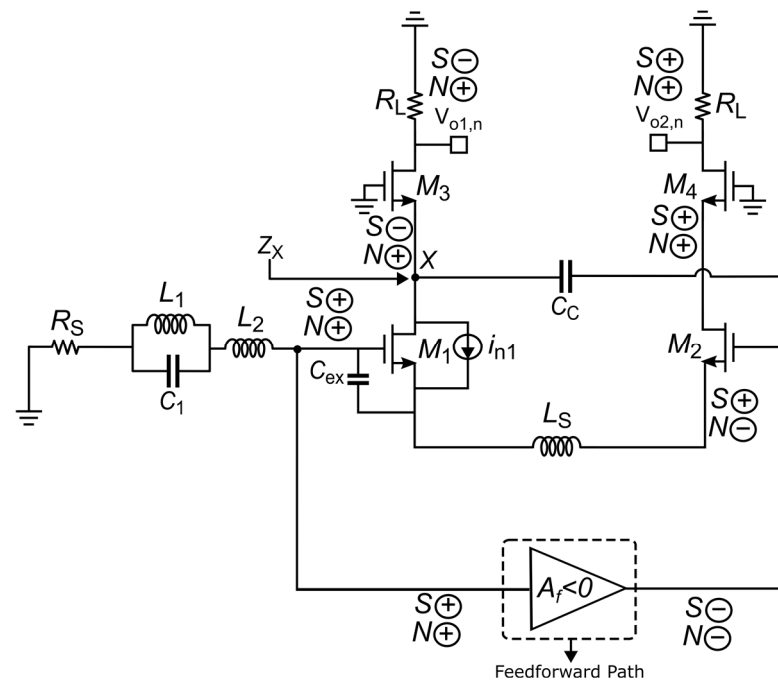


Figure 3. Noise cancellation technique by means of a feedforward path.

On the one hand, since the noise signs in the M_2 gate and source are the same, V_{gs2} and therefore the output noise current of the right-hand side would be cancelled. On the other hand, since the signal signs are opposite, the output current signal would be increased simultaneously, thus resulting in a higher gain.

The i_{n1} noise cancellation condition in the right-hand side of the circuit is as follows:

$$A_f V_{g1,n} = V_{s2,n} \quad (14)$$

where $V_{g1,n}$ is the M_1 gate noise voltage, $V_{s2,n}$ is the M_2 source noise voltage, and A_f is the voltage gain of the feedforward path. Additionally, the output noise voltage in the left-hand side, $V_{o1,n}$, can be cancelled through the differential output, which is equal in sign to the right-hand side output noise voltage, $V_{o2,n}$. To achieve perfect noise cancellation, the following conditions must be met and A_f should be determined based on (18), where $V_{o,n}$ is the differential output noise voltage and L_S is the source degeneration inductance:

$$V_{o,n} = V_{o1,n} - V_{o2,n} = V_{o1,n} + R_L A_f g_{m2} V_{g1,n} = 0 \quad (15)$$

$$V_{o1,n} = \frac{R_L g_{m3}}{g_{m3} + C_C S} \left(-\frac{i_{n1}}{2} + j\omega A_f V_{g1,n} C_C \right) \quad (16)$$

$$V_{g1,n} = \frac{i_{n1}}{2} \left[L_S S - \frac{1}{g_{m1}} (1 - \omega^2 L_S C_T) \right] \quad (17)$$

$$A_f = \frac{1}{(g_{m3} + 2j\omega C_C) \left[j\omega L_S - \frac{1}{g_{m1}} (1 - \omega^2 L_S C_T) \right]} \quad (18)$$

As shown in Figure 4, the feedforward path provides 0.31 dB and 0.52 dB NF improvements at 1.2 GHz and 1.57 GHz, respectively. It should be noticed that a proper setting of A_f is important to avoid introducing further noise into the amplifier, as calculated in (19), where the feedforward path noise is modeled as the voltage source V_{nf} .

$$V_{o,n} = -R_L g_m A_f \left[1 + \frac{j\omega C_C}{g_{m3} + j\omega C_C} \right] V_{nf} \quad (19)$$

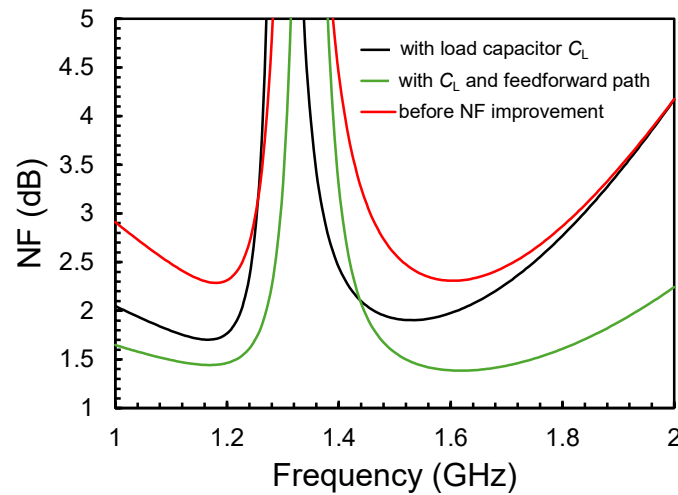


Figure 4. NF versus frequency before and after noise improvement/cancellation techniques.

The final schematic of the proposed LNA, including both noise reduction/cancellation approaches, is shown in Figure 5. The feedforward path is provided through a common-source transistor, M_f .

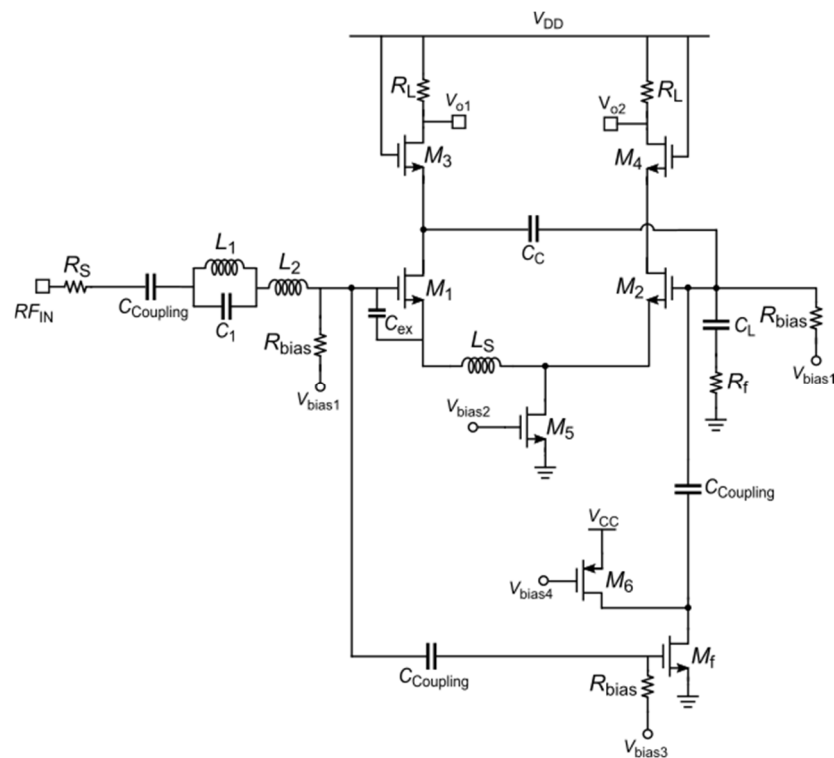


Figure 5. Final structure of the proposed LNA with improving/cancelling noise techniques.

The overall NF including all the noise sources of the LNA shown in Figure 5 is given in (20). They include the M_1 , M_2 , and M_f transistor-induced gate and channel thermal noise and the thermal noise of R_S

$$NF = 1 + \frac{1}{R_S |A_V|^2} \left(r_g + \frac{\delta}{5g_{d0}} \right) \cdot \left[\frac{|R_L g_{m2} g_{mf} + j\omega A_V (C_C + C_L)|^2}{(C_C + C_L)^2 \omega^2} + R_L^2 g_{m2}^2 + R_L^2 g_{mf}^2 A_f^2 \left(\frac{g_{m3}^2 + 4C_C^2 \omega^2}{g_{m3}^2 + C_C^2 \omega^2} \right) \right] + \frac{\gamma_{g_{d0}}}{R_S} \times \frac{R_L^2}{|A_V|^2} \times \left[1 + \frac{C_C^2}{4(C_C + C_L)^2} + \frac{g_m^2 (g_{m3}^2 + 4C_C^2 \omega^2)}{C_C^2 C_L^2 \omega^4 + g_{m3}^2 \omega^2 (C_L + C_C)^2} \right] \quad (20)$$

where g_{mf} is the transconductance of transistor M_f , A_V is the overall voltage gain of the LNA, r_g is the intrinsic gate resistance, δ is the induced gate noise current factor, γ is channel noise coefficient, and g_{d0} is drain-source channel conductivity, when the DC voltage of the drain source is zero. As shown in (20), increasing C_L and g_{mf} (because of the dependency of A_V on g_{mf}) results in a lower NF , thus confirming the soundness of the proposed noise-reduction techniques.

2.4. Gain

The proposed LNA shown in Figure 5 exploits a resistive load, R_L , instead of a resonant LC load. Despite the higher impedance provided by a resonant LC load, it is not suited to a concurrent dual-band operation due to its narrow-band operation. The sizing of R_L is crucial to achieve high gain. R_L is upper-limited by both DC biasing constraints and the maximum voltage swing, since transistors could be pushed outside the saturation region during operation. In the proposed design, R_L has been set to have a voltage drop that is lower than the threshold, thus guaranteeing that transistors $M_{3,4}$ are biased in the saturated region. The main advantage of using a resistive load is that the frequency behavior of the LNA is essentially set by the input matching network. On the other hand, the maximum gain that can be achieved by a resistive load is lower compared to a resonant LC load due to the abovementioned limitations through the voltage overhead and parasitic capacitors. Apart from that, the adopted single-ended-to-differential conversion provides a 6 dB extra gain that in part compensates for this gain reduction.

The voltage gain, A_V , of the LNA in Figure 5 is given in (21), while the proportion with the voltage gain, A_{V1} , of the initial topology in Figure 1 is provided in (22) for comparison.

$$|A_V| = \frac{2R_L g_{m1}}{R_S C_T (C_C + C_L) \omega} \sqrt{\left(C_C + L_S g_{mf} g_{m2} \right)^2 + \frac{g_{mf}^2}{\omega^2} (1 - L_S C_T \omega^2)^2} \cong \frac{2R_L g_{m1} g_{mf}}{R_S C_T (C_C + C_L) \omega^2} \quad (21)$$

$$\frac{|A_V|}{|A_{V1}|} = \frac{C_C + C_{gs2}}{(C_C + C_L) C_C} \sqrt{\left(C_C + L_S g_{mf} g_{m2} \right)^2 + \frac{g_{mf}^2}{\omega^2} (1 - L_S C_T \omega^2)^2} \cong \frac{(C_C + C_{gs2}) g_{mf}}{(C_C + C_L) C_C \omega} \quad (22)$$

Equation (22) clearly indicates that the transconductance of feedforward path transistor, g_{mf} , produces a gain improvement, while the load capacitor C_L decreases the gain. To compensate for that detrimental effect of C_L , a series resistor, R_f , has also been included, as shown in Figure 5. Indeed, such a resistor increases the output impedance of the feedforward path, which results in a higher gain of M_f and, and therefore a higher overall gain.

3. Expected Performance and Comparisons

The soundness of the proposed concurrent dual-band LNA topology has been evaluated by using a low-cost 0.18 μm CMOS technology by TSMC. The LNA draws less than 13 mA from a 1.8 V supply voltage. The main LNA design parameters are reported in Table 1 for the sake of completeness. L_1 , L_2 , and C_1 are off-chip components, since high-quality factor values are required.

Table 1. Circuit design parameters of the LNA.

$M_{1,2}$	$M_{3,4}$	M_5	M_{6f}	L_1	C_1	L_2	L_S	C_{ex}	C_C	C_L	$C_{Coupling}$	R_f	R_L	R_{bias}
160 μm 0.18 μm	160 μm 0.18 μm	350 μm 1 μm	100 μm 0.18 μm	1.4 nH	10 pF	14 nH	0.6 nH	190 fF	640 fF	5 pF	100 pF	50 Ω	50 Ω	7 K Ω

Figure 6 shows the input matching, S_{11} , and the voltage gain of the amplifier. Thanks to the adopted input network, the LNA is adequately matched to the source at 1.2 GHz and 1.57 GHz, which also results in a 24 dB voltage gain in both frequency bands. Thanks to the notch between the two bands, the LNA provides good rejection for out-band signals with a maximum attenuation of 33 dB.

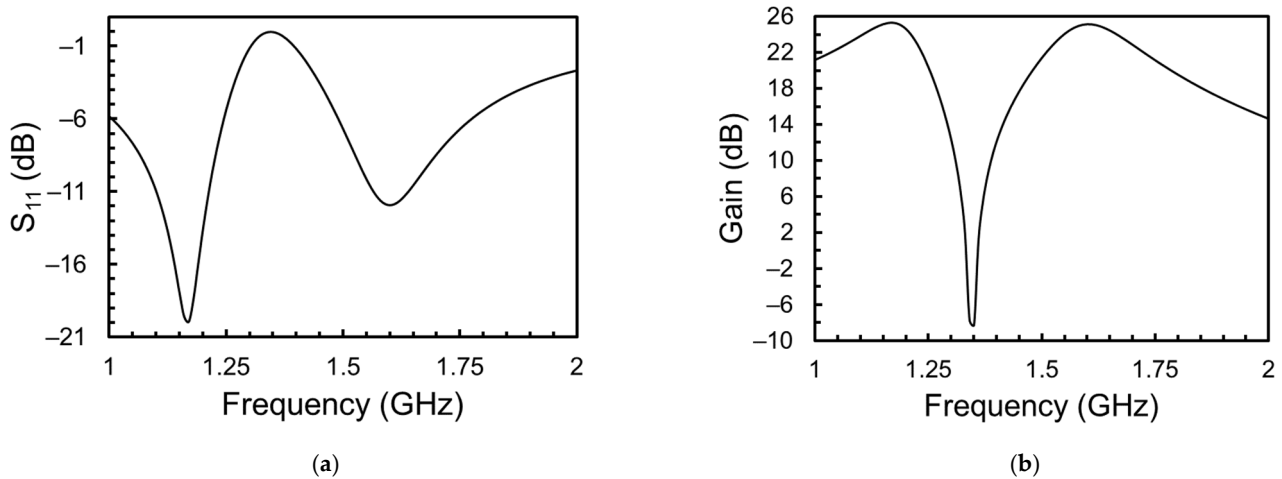


Figure 6. (a) Input matching; (b) voltage gain.

The NF performance over the frequency range is depicted in Figure 7a. The LNA has an NF that is lower than 1.5 dB in both frequency bands, thus validating the adopted simultaneous input–noise matching at the given power constraint. The combination of the two adopted noise cancellation techniques, i.e., a feedforward path and a load capacitor, reduced the NF by about 0.8 dB and 0.9 dB at 1.2 GHz and 1.57 GHz, respectively. The S_{22} is also reported in Figure 7b. An output matching of around -10 dB was achieved.

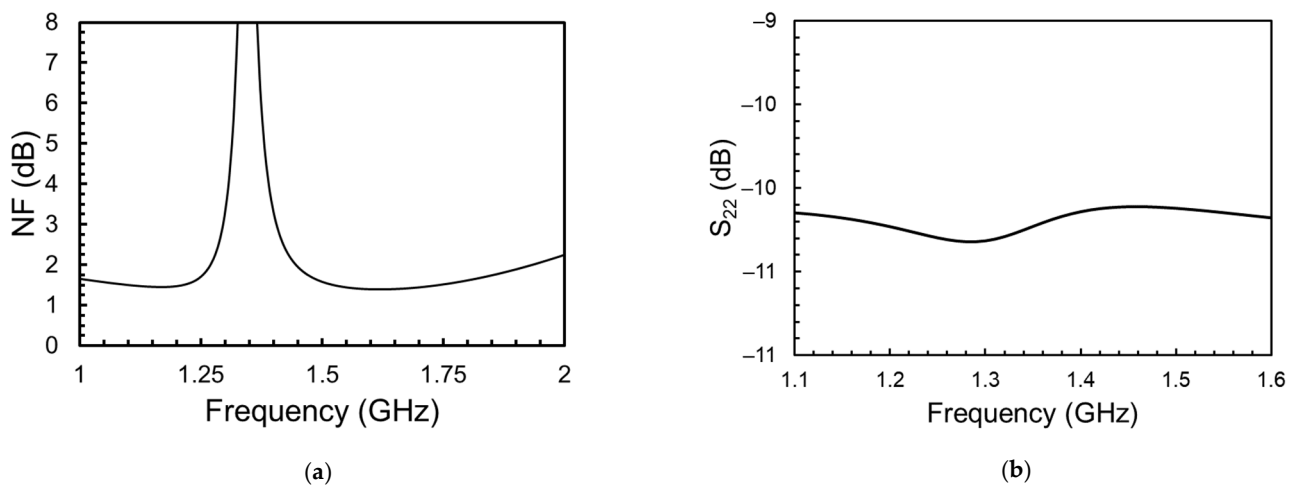


Figure 7. (a) NF versus frequency; (b) output matching.

Linearity is crucial in a two-band concurrent reception. It has been evaluated by means of a 1 dB input compression point (IP_{1dB}) and an input third-order intermodulation product (IIP_3) for both operative frequency bands in Figures 8 and 9, respectively. The IP_{1dB} performance is almost equal for both operative frequency bands (i.e., about -16 dBm) while the IIP_3 is -2.2 dBm and -0.6 dBm at 1.2 GHz and 1.57 GHz, respectively. Such high linearity of the LNA is mainly due to the adoption of pseudo-differential topology along with the compensation capacitor used to balance the outputs.

As far as stability is concerned, the proposed LNA is unconditionally stable since it fulfills Rollett's conditions. For the sake of completeness, Figure 10a–c report the corner simulations for the input matching, gain, and NF , respectively. The slow corner is the most critical for the concurrent operation of the LNA, since the higher C_{gs} capacitance produces an upper shift of the two resonance frequencies. It is worth mentioning that such an effect can be partially compensated for by means of a proper tuning of the off-chip components L_1 , L_2 , and C_1 .

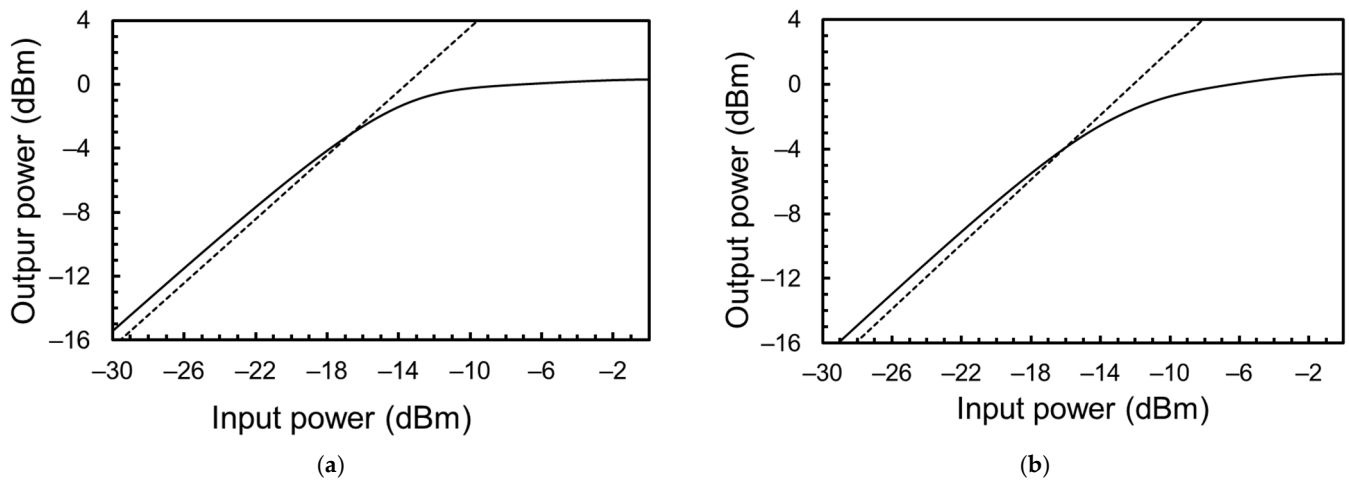


Figure 8. IP_{1dB} at (a) 1.2 GHz and (b) 1.57 GHz.

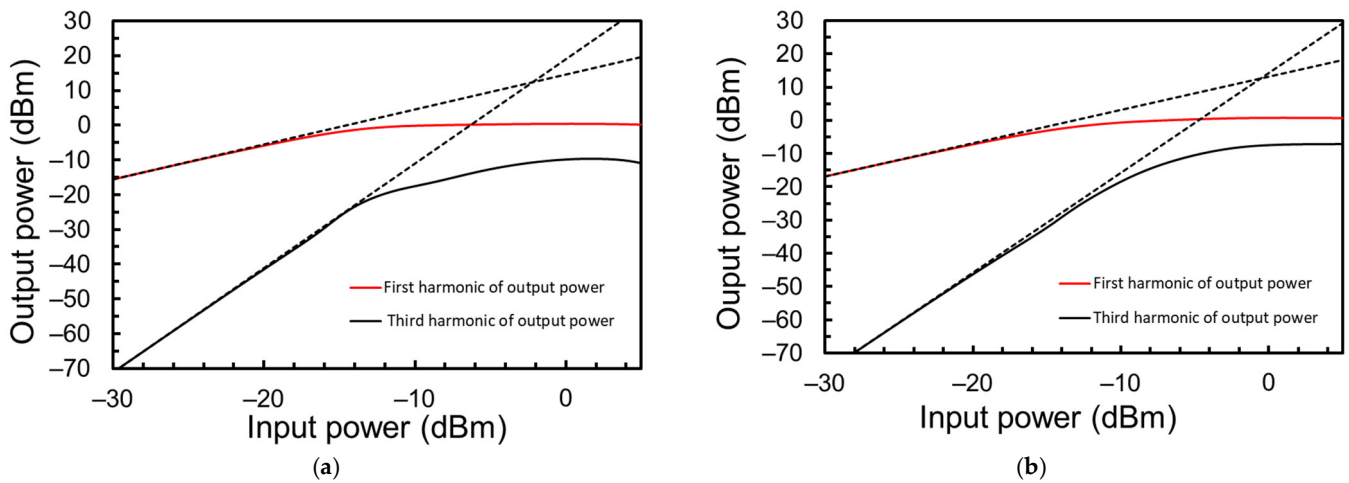


Figure 9. IIP_3 at (a) 1.2 GHz and (b) 1.57 GHz.

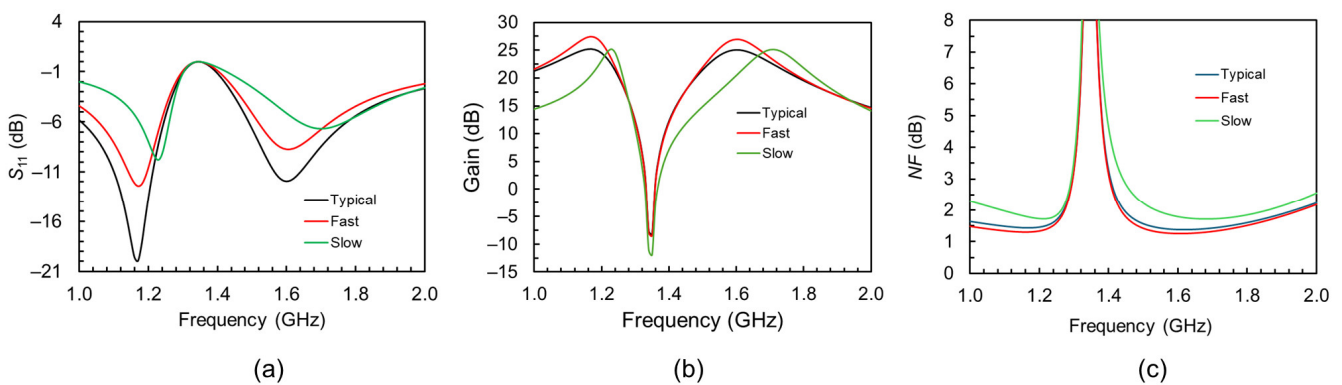


Figure 10. Process corner simulations for input matching (a), gain (b), and NF (c).

Table 2 provides the main LNA performance along with a comparison to related recent publications. While using differential structure and noise improvement techniques, the suggested LNA exhibits an optimal trade-off between gain, linearity, NF , and power consumption in single-channel concurrent dual-band operation, as demonstrated by the reported Figure of Merit (FoM). Finally, with respect to the previous work in the same CMOS technology [23], the proposed LNA exhibits a 0.9 dB lower NF , which demonstrates the effectiveness of the adopted noise reduction/cancellation strategies described in Section 2.

Moreover, such an improvement has been achieved without considerably affecting the other performance parameters.

Table 2. Summarized performance of the LNA and comparison with the state of the art.

	[25] (S)	[26] (S)	[27] (S)	[28] (PLS)	[29] (M)	[23] (S)	This Work (S)	Unit
Structure	SC/C/MB	SC/C/MB	SC/C/MB	SC/C/WB	NC/MB	SC/C/MB	SC/C/MB	-
Frequency	2.4/5.2	2.4/5.2	1.7/3.5	0.7–2.5 ⁽¹⁾	1.2/1.7/2.2	1.2/1.57	1.2/1.57	GHz
S_{11}	−15.6/−13.8	−13/−21.9	−15.8/−12.6	<−11	−25/−35/−11	−11/−13.1	−13.6/−11.2	dB
Gain	17.1/8.5	20.6/20.4	17.3/17.7	24	18/19/15	27/27.6	24.6/24.7	dB
NF	3.6/3.3	2.1/3.1	2.33/2.72	3.3 ⁽²⁾	3.5/3.6/5.8	2.3	1.5/1.4	dB
IP_{1dB}	−16.5/−9.5	−30/−30	−14.3/−7.4	−14.4	−26.1/−27.1/−24.1 ⁽³⁾	−15.3/−13	−16.5/−16	dBm
IIP_3	−6.87/0.13 ⁽³⁾	−15/−7	−4.67/2.23 ⁽³⁾	1.3	−16.5/−17.5/−14.5	−0.9/2.2	−2.2/−0.6	dBm
V_{DD}	1.2	1.2	1.8	1.1	1.2	1.8	1.8	V
Power, P_{DC}	9.8	7.3	14	19	7	15	23.4	mW
CMOS	130	90	180	28	130	180	180	nm
FoM [30]	0.27/1.24	0.17/1.43	0.38/3.68	1.37	0.02/0.03/0.03	2/6.1	1.27/2.73	-

S = circuit simulations; PLS = post-layout simulations; M = measurements; SC = single-channel; C = concurrent; NC = non-concurrent; MB = multi-band; WB = wide-band; ⁽¹⁾ GNSS is included; ⁽²⁾ for GNSS mode; ⁽³⁾ $IIP_3 \cong 9.63 \text{ dB} + P_{1dB}$; $FoM = \text{Gain}[\text{lin}] \cdot \text{frequency}[\text{GHz}] \cdot IIP_3[\text{mW}] / (NF[\text{lin}] - 1) \cdot P_{DC} [\text{mW}]$.

4. Conclusions

This paper has presented a concurrent dual-band LNA of a GNSS receiver design with two proposed noise reduction/cancellation techniques. The noise figure is significantly improved by these methods with around a 0.9 dB reduction for both frequency bands of 1.2 GHz and 1.57 GHz. A pseudo-differential topology allows for no input balun to be required. Simultaneous noise–input matching with a power constraint has been obtained in the two frequency bands by means of parallel and series resonant networks. The LNA has been designed using a low-cost 0.18 μm CMOS technology and achieves excellent performance in terms of input matching, voltage gain, NF, and linearity at two GNSS bands simultaneously.

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