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Design and Characterization of a Digitally Tunable Gm-C Filter for Multi-Standard Receivers

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Abstract: This paper presents the design, simulation, prototyping, and measurement results of a digitally tunable fourth order Gm-C low-pass filter (LPF) for multi-standard radio receivers. The LPF cut-off frequency can be tuned by digitally selecting the transconductance of the basic reconfigurable operational transconductance amplifiers (OTAs) that compose the circuit. Four operation modes allow for control of the OTA transconductances and, consequently, the scaling of power consumption. The filter was designed and prototyped in a 1.8 V 180 nm CMOS process. The measurement results indicate that the configurability provides a cutoff frequency of 1.90/3.56/6.07/8.15 MHz with a power consumption ranging from 9.9 to 13.1 mW. The designed filter achieves an IIP3 of 8.17 dBm for a signal bandwidth of 8.15 MHz. The performance, in terms of power dissipation, noise, and cut-off frequency, is at the same order of magnitude compared to recent related works reported in the literature. The advantages are a compact area, small sensitivity to component mismatches, and low design complexity. The proposed filter presents electrical characteristics suitable for the application in radio receivers for multi-carrier WCDMA signals.

Keywords: Gm-C filter; multistandard radio receiver; analog design



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1. Introduction

The ever-increasing demand for high transmission rates and portability motivated enormous advances in wireless communication systems. This has led to the development of several wireless communication standards, with the need for high bandwidth and low power consumption increasing.

CMOS technology follows the same path. Reducing the minimum dimensions of MOS transistors enables operation at higher frequencies and reduces the power consumption and silicon area occupied by the integrated circuit. These features are critical for low power budget receiver circuits that are powered by low capacity batteries (e.g., wireless embedded systems).

The use of configurable analog blocks is a good alternative to support multiple standards on a single chip [1]. In this case, the power consumption must be proportional to the required performance level. It is necessary to adjust the different power consumption levels in each operating mode, such as in software-defined radio (SDR) devices [2]. The specification of the analog blocks must be reduced when the system is switched from a hard standard to a softer standard so that the front-end circuit can meet the performance requirements of each standard while having lower power consumption, similar to a single-mode device specifically designed for this application.

The homodyne (zero-IF) receiver architecture is widely used in multistandard wireless transceivers as it allows for direct conversion of the incoming radio signal with advantages

in terms of circuit complexity and power consumption, despite the degradation of the dynamic range [3,4]. These receivers convert the signal directly to the baseband without the need for an intermediate frequency. An important component in this case is the continuous-time active low-pass filter (LPF), which is important for generating the demodulated baseband output [5]. For multiple communication standards, an array of channel selection filters would be required. However, a more energy-efficient approach is to design a single tunable LPF that can adapt to the local operating frequency and allows for reconfiguration of the circuit at the architectural and circuit levels [1].

Designing an integrated low-pass filter that operates in the MHz frequency range while providing a high dynamic range and making efficient use of CMOS technology in terms of power and area remains a major challenge in analog circuit design. To meet all of these performance requirements simultaneously, new techniques and strategies need to be developed [6]. A fully integrated solution is important to avoid using external components to perform frequency tuning, which would demand an increase in both area and power consumption [7].

This paper presents the design, physical implementation, and characterization of a digitally tunable Gm-C low-pass filter for multistandard radio receivers. The tunability is achieved by varying the filter transconductance (g_m) using a digitally programmable transconductance operational amplifier (OTA). This technique allows the cut-off frequency of the filter to be adjusted while providing proportional scalability of the power consumption. Previous simulation results were presented in Oliveira et al. [8]. The measurement results described here confirm the practical applicability of the proposed methodology, suitable for most communication standards.

The reconfigurable filter was built in TSMC 180 nm CMOS technology. Post-layout simulations and electrical measurements of a prototype chip show that its characteristics are suitable for use in radio receivers for multi-carrier WCDMA signals [9]. Furthermore, this technique can be extended to the design of various communication protocols such as IEEE 802.15.4 g and Bluetooth Low Energy 5.0.

The remaining sections of this paper are organized as follows: Section 2 presents the architecture of the tunable gm-C filter and the implementation of the circuit; post-layout simulation results of the designed filter are presented in Section 3; measurements of a prototype version of the filter and a comparison with related works are presented in Section 4; finally, conclusions are drawn in Section 5.

2. Reconfigurable Gm-C Filter

There are two common implementations for an integrated active low-pass filter: Gm-C [10], and active-RC [1]. Both can be tuned to adapt the transfer function to a specific application. Although active RC filters can be tuned using digitally configurable resistor and capacitor banks, the absolute values of integrated resistors are very sensitive to process variations and can vary up to 20% in a typical IC manufacturing process. In addition, the operational amplifiers in an active-RC filter must meet stringent specifications, such as high DC voltage gain and a high gain-bandwidth product (GBW). On the other hand, the Gm-C filter can be tuned by changing the values of capacitances and transconductances. The reconfigurability of the transconductance has advantages as it is less sensitive to component mismatch and also allows for scaling of power consumption [8]. In addition, the GBW of the transconductance amplifier only needs to be slightly higher than the cut-off frequency of the filter [5].

In this work, a fourth-order Gm-C filter topology was used to design a tunable LPF, where the cutoff frequency was controlled by changing the OTA transconductance [8]. The circuit diagram is shown in Figure 1 [11]. The order of the filter was determined in accordance with related multimode LPFs for radio receivers presented in the literature [12]. The transfer function of the filter can be divided into two terms related to two biquad filters:

$$F(s) = \frac{\frac{gm_{11} \cdot gm_{14}}{C_{11} \cdot C_{12}}}{s^2 + \frac{gm_{12}}{C_{11}}s + \frac{gm_{13} \cdot gm_{14}}{C_{11} \cdot C_{12}}} \cdot \frac{\frac{gm_{21} \cdot gm_{24}}{C_{21} \cdot C_{22}}}{s^2 + \frac{gm_{22}}{C_{21}}s + \frac{gm_{23} \cdot gm_{24}}{C_{21} \cdot C_{22}}} \quad (1)$$

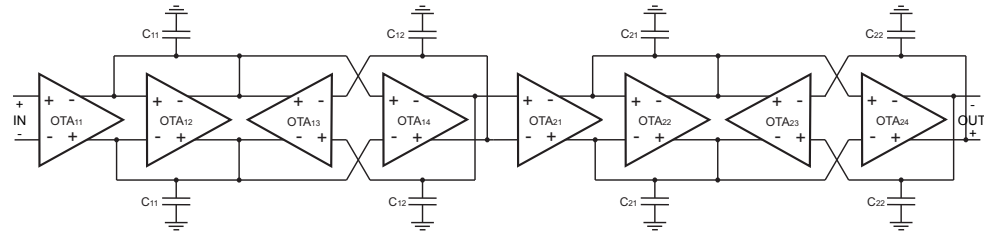


Figure 1. Schematic of the fourth-order reconfigurable Gm-C filter.

Here, gm_{ij} is the transconductance of OTA_{ij} , i is the biquad index, and j is the OTA number. The cut-off frequency (f_c) is controlled by gm_{i3} and gm_{i4} , as shown in Equation (2). In addition, the quality factor (Q_i) of each biquad is defined according to Equation (3).

$$f_{ci} = \frac{1}{2\pi} \sqrt{\frac{gm_{i3} \cdot gm_{i4}}{C_{i1} \cdot C_{i2}}} \quad (2)$$

$$Q_i = \sqrt{\frac{C_{i1} \cdot gm_{i3} \cdot gm_{i4}}{C_{i2} \cdot gm_{i2}^2}} \quad (3)$$

Capacitors C_{i1} and C_{i2} are defined to have the same value. To reduce the complexity of the design, only one reconfigurable OTA is designed and replicated in the filter. Thus, each biquad in the designed filter has a quality factor of one, resulting in a frequency response similar to the transfer function of a Butterworth filter.

This reconfigurable fourth-order Gm-C filter is developed in a 180 nm CMOS process with a 1.8 V power supply and uses only standard transistors and metal–insulator–metal (MiM) capacitors. The reconfiguration approach is based on a reconfigurable operational transconductance amplifier (OTA), while the values of the filter capacitors are kept constant.

2.1. Reconfigurable OTA

Reconfigurable operational transconductance amplifiers are fundamental building blocks for multi-mode analog baseband circuits of radio receivers, such as integrated analog filters and analog-to-digital converters (ADCs). In addition, these reconfigurable OTAs are designed to meet the requirements for flexibility and energy efficiency [13].

The reconfigurable OTA used in this work is shown in Figure 2 and is based on the implementation presented in Giannini et al. [1]. Its architecture essentially consists of an array of multiple switchable parallel operational amplifiers that are controlled via digital inputs. The main amplifier is always active and has a transconductance gm_0 , while the other amplifiers are programmatically activated by digital inputs to change the reconfigurable OTA transconductance. All amplifiers are the same, which reduces the overall complexity of the design. By selecting n amplifiers in parallel, the transconductance gm_0 is multiplied by n times while the DC gain of the reconfigurable amplifier is kept constant.

This configuration strategy is based on the relationship between GBW and the transconductance shown in Equation (4), where C_L represents the load capacitance. It is possible to change the GBW of the OTA by increasing n , enabling control of the filter cut-off frequency, at the cost of higher power consumption.

$$GBW = \frac{n \cdot gm_0}{2 \cdot \pi \cdot C_L} \quad (4)$$

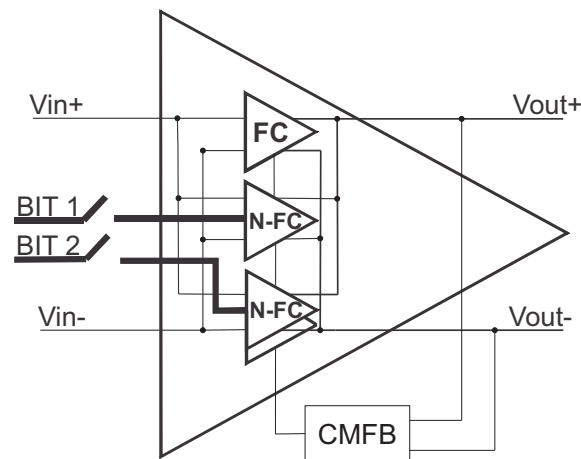


Figure 2. Reconfigurable OTA architecture.

We used four amplifiers in the reconfigurable OTA. The first, whose schematic is shown in Figure 3, is the main amplifier. It is a conventional fully-differential folded cascode (FC) amplifier with features such as a high DC voltage gain, wide input common-mode range (ICMR), and self-compensation [14]. This amplifier is always switched on in the reconfigurable OTA. The others are switchable amplifiers, which are referred to as N-FC in this paper, as they are also fully differential folded-cascode amplifiers. The circuit diagram is shown in Figure 4. The difference is the presence of switches that control the gate voltage of the transistors to turn them on or off. These switches are built with minimum size transistors in the transmission gate configuration, as shown in Figure 5.

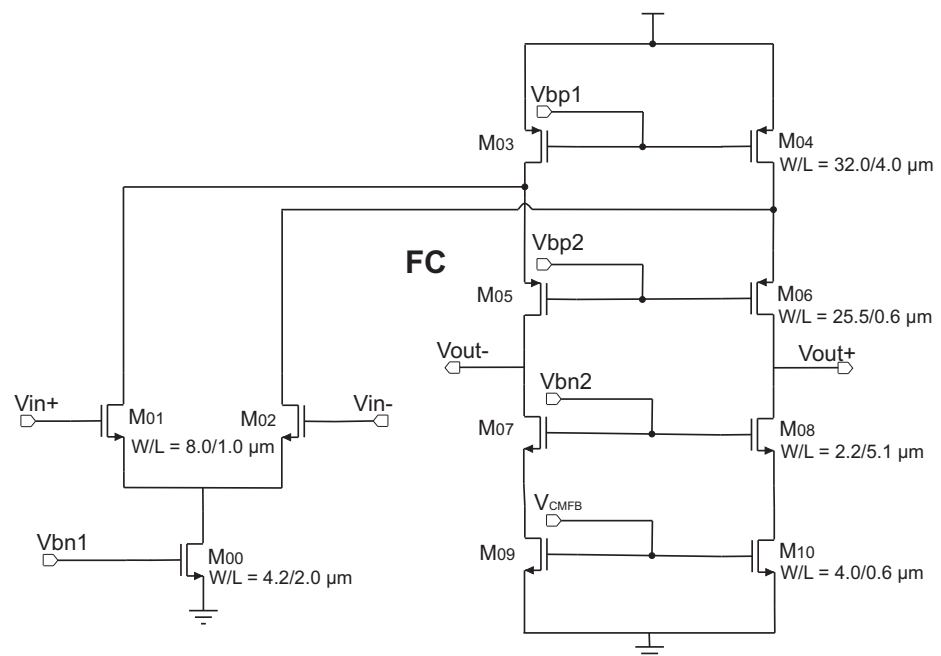


Figure 3. Schematics of the folded-cascode amplifier (FC).

In the “off” state, the switches at nodes Vbp1, Vbp2, Vbn1, Vbn2, and V_{CMFB} are open. The others are closed, whereby the NMOS and PMOS gate nodes are connected to the ground and to VDD, respectively [1]. In this state, the static power consumption is

minimized as the switchable amplifier is electrically isolated from the main circuit. In the “on” state, all switches connecting the supply sources are activated. The same happens with the gate nodes of transistors M_{01} and M_{02} , which are connected to inputs V_{in+} and V_{in-} , respectively.

Four modes of operation are provided by two control bits associated with the following digital words: “00”, “01”, “10”, and “11”. Configuration “00” represents the minimum operating mode in which only the non-switchable amplifier is active. This configuration offers a lower transconductance and also has the lowest GBW and power consumption. On the other hand, configuration “11” provides the maximum transconductance and also has the highest GBW and power consumption, as all switchable amplifiers are switched on.

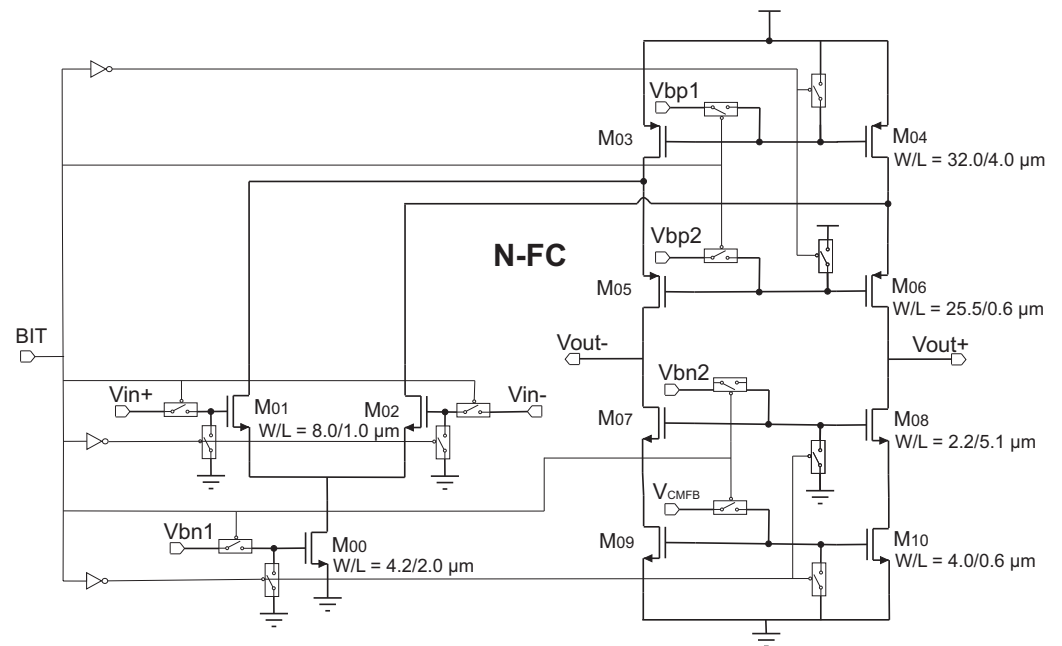


Figure 4. Switchable OTA schematic (N-FC).

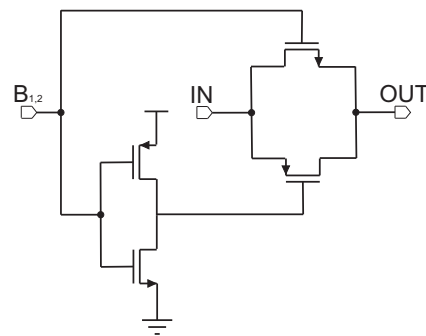


Figure 5. Switch implementation with minimum-sized transistors in the transmission gate configuration.

The common-mode feedback (CMFB) circuit used in the reconfigurable OTA is a PMOS differential-difference CMFB [15] and its schematic is depicted in Figure 6. In this topology, only CMOS transistors are used, avoiding the use of passive components to reduce the area. The common-mode reference voltage V_{CM} is 0.9 V. Only a single CMFB unit is employed for all unit amplifiers as they are connected in parallel. This allows for a large saving in silicon area. Note that M_{18} is connected as a diode to improve the stability of the circuit.

value is 15.78 V/ μ s for configuration “00” and the highest SR value is 37.22 V/ μ s for configuration “11”.

Table 1. Summarized post-layout simulation results for the reconfigurable OTA cell.

Specification	Control Bits			
	00	01	10	11
OTAs	1	2	3	4
Av0 (dB)	69.18	69.96	68.85	68.75
PM (°)	85.28	79.51	74.14	69.28
GBW (MHz)	22.07	44.04	65.85	87.46
gm (μ S)	192.77	385.54	578.31	771.08
Power (mW)	1.28	1.39	1.51	1.62
OS (V)	1.50	1.53	1.54	1.54
SR (V/ μ s)	15.78	26.16	32.79	37.22

A Monte Carlo (MC) simulation with 1000 runs was performed and the results for the frequency response parameters are summarized in Table 2.

It can be observed that the mean values (μ) of Av, PM, and GBW are very similar to the nominal results for all operating modes. Based on the values obtained for the standard deviation (σ), it can also be seen that the circuit has a low sensitivity to process variations, as the parameters are within a narrow range.

Table 2. Monte Carlo simulation results for the frequency response of the reconfigurable OTA cell.

Control Bits	Av (dB)		PM (°)		GBW (MHz)	
	μ	σ	μ	σ	μ	σ
00	68.69	3.52	85.3	0.13	22.34	0.99
01	68.44	3.37	79.55	0.33	44.59	1.98
10	68.29	3.28	74.19	0.48	66.69	2.95
11	68.20	3.23	69.29	0.65	88.58	3.90

3. Fourth Order Filter Post-Layout Simulation Results

This section describes post-layout electrical simulation results for the designed tunable Gm-C low-pass filter. The circuit layout is shown in Figure 8 and occupies a total silicon area of 0.23 mm². The filter capacitors C_{i1} and C_{i2} have a capacitance of 12.58 pF. A load consisting of a 1 pF capacitor connected to each output node (inverting and non-inverting) was used in the filter evaluation. Figure 9 shows the frequency response of the filter. The DC voltage gain is 0 dB in the passband and has a small peak near the cut-off frequency, which is due to the filter’s quality factor. The four configurable cut-off frequencies, which are selected by tuning the reconfigurable OTA transconductance values, are 2.55, 5.11, 7.68, and 10.29 MHz. The total power consumption for each operating mode is 10.27, 11.18, 12.06, and 12.96 mW. The power consumption is not linear with the cut-off frequency because the reconfigurable OTAs use a power hungry CMFB that always remains active.

The input referred third-order intercept points (IIP3s) were estimated by the two-tone test as −2.59/1.11/2.96/4.14 dBm for the 00/01/10/11 configuration. The noise power estimate ranged from 58.1 (“00” configuration) to 27.88 nV/ $\sqrt{\text{Hz}}$ (“11” configuration).



Figure 8. Layout of the designed fourth-order reconfigurable Gm-C filter, with a occupied silicon area of $1137 \mu\text{m} \times 199 \mu\text{m}$ (0.23 mm^2).

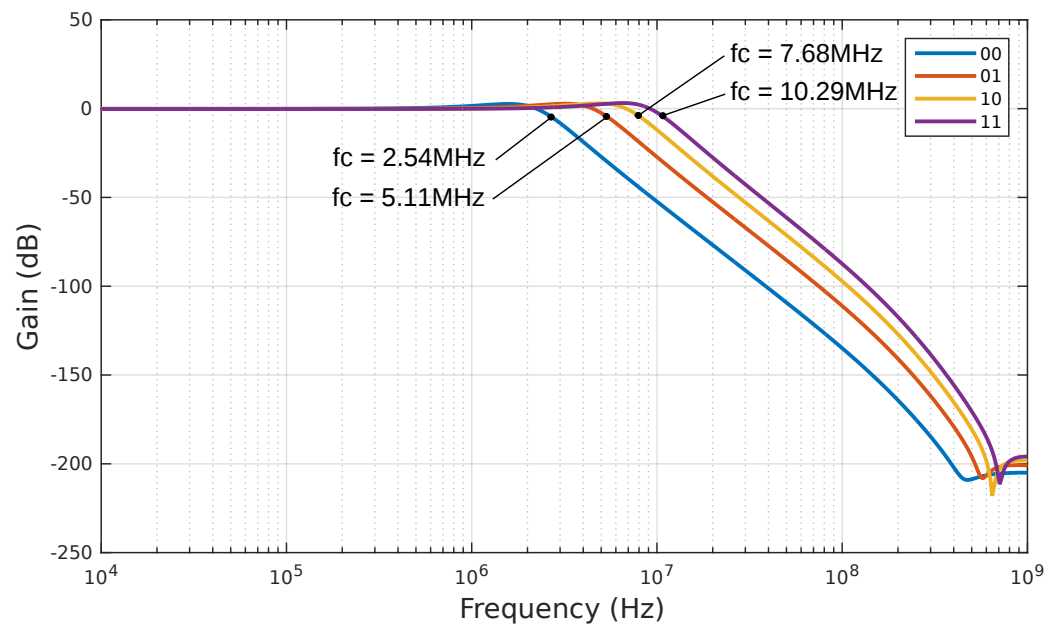


Figure 9. Post-layout simulated frequency response of the fourth-order reconfigurable filter.

4. Prototyping and Measurement Results

The Gm-C filter was manufactured in a CMOS 180 nm process with a supply voltage of 1.8 V. Figure 10 shows the photomicrograph of the prototype chip. The filter occupies an area of $1137 \times 199 \mu\text{m}$ (0.23 mm^2) and nine pins of the 48-pin DIP package: VDD, VSS, CM, BIT1, BIT2, INP, INN, OUTP, and OUTN.

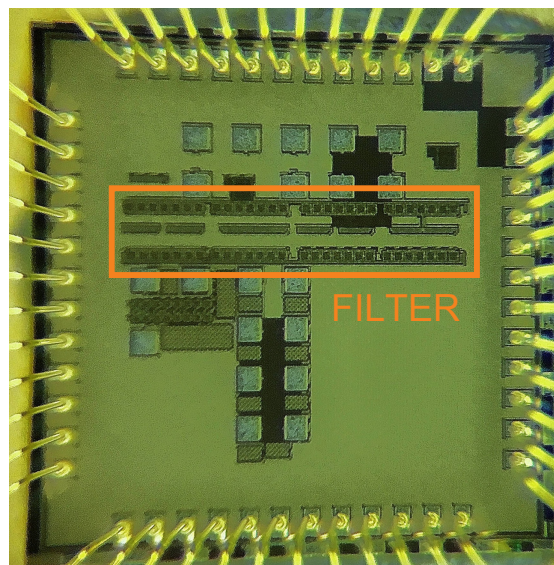


Figure 10. Microphotography of the prototyped chip containing the Gm-C reconfigurable filter.

The filter was measured using a test setup depicted in the diagram of Figure 11. The common-mode voltage was set to 0 V, as we used a symmetrical supply voltage of ± 0.9 V. As the filter was fully differential, elements had to be used to convert single signals into differential signals and vice versa. For this purpose, a Coilcraft WB1-6T transformer was used at the input, as it had an attenuation of less than 1 dB in the range of 100 kHz to 90 MHz. The output was measured with a model 701922 differential probe from the Yokogawa DLM2054 oscilloscope. This probe had an input resistance of 500 k Ω and an input capacitance of 7 pF. Figure 12 shows the printed circuit board produced for the test setup.

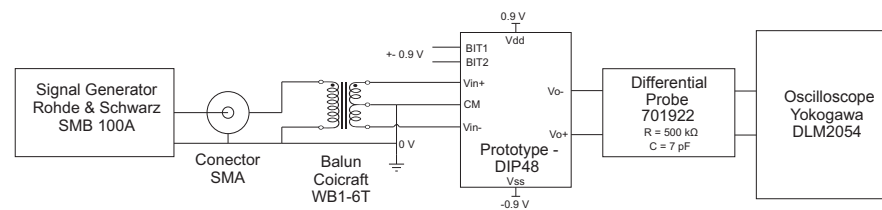


Figure 11. Test setup for electrical characterization of the prototyped filter.



Figure 12. Test PCB for filter measurements.

As no buffer for impedance matching was integrated at the filter output, the additional load caused by the probe and chip package could influence the measurement results. To estimate this influence, we performed an electrical simulation of the filter with an output load of 10 pF (7 pF from the probe and 3 pF from the pads and PCB routing) in parallel with an output resistance of 500 k Ω . A decrease in the cut-off frequency could be observed in all operating modes. This behavior could be explained by the fact that the output load was parallel to the capacitor C_{22} (Figure 1). According to the relationship given by Equation (2), the higher the value of the capacitance C_{22} , the lower the cut-off frequency of the filter. In addition, according to Equation (3), the quality factor also decreased.

The power consumption was measured as 9.9/11.52/12.83/13.10 mW for the operating modes 00/01/10/11. It was very close to the value predicted by the electrical simulation.

To measure the frequency response of the filter for the four available configurations, we applied a 100 mV signal to the input of the transformer and recorded the amplitude of the filter output signal, varying the input frequency with a step of 100 kHz. Figure 13 shows the results obtained. It can be seen that the additional load contributed to lowering the cut-off frequency, as indicated in the simulation.

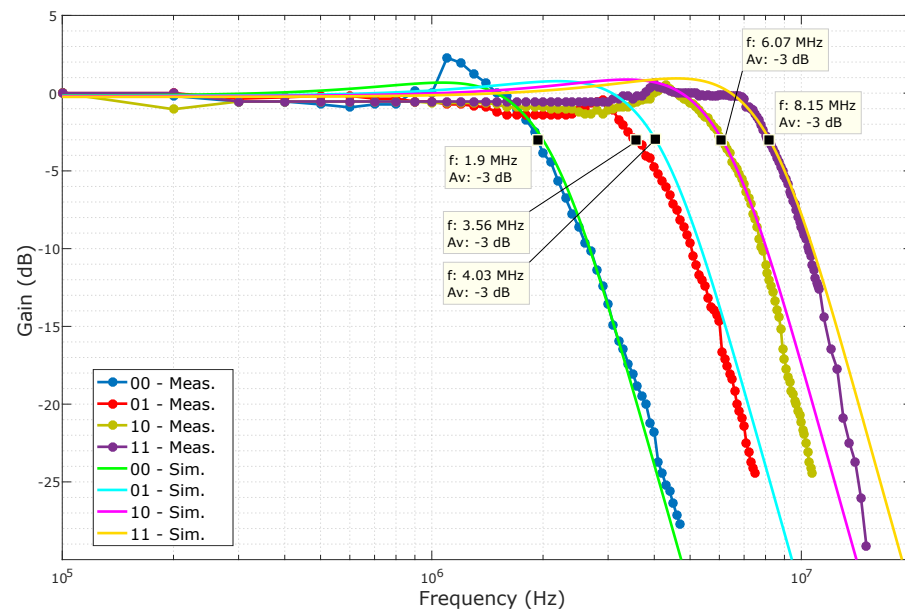


Figure 13. Electrical simulation and measurement of the Gm-C filter frequency response for an output load of 10 pF.

The measurement results confirmed the simulated values for the four operating modes and provided a reconfigurable filter with a cut-off frequency of 1.9 to 8.1 MHz.

The measurement of in-band linearity was evaluated using a two-tone test. We combined two input signals, with differential a peak amplitude of 40 mV and frequencies of 1.0 and 1.1 MHz so that the third order intermodulation distortion (IM3) remained in the bandpass. Figure 14 shows the power spectrum density (PSD) of the filter output.

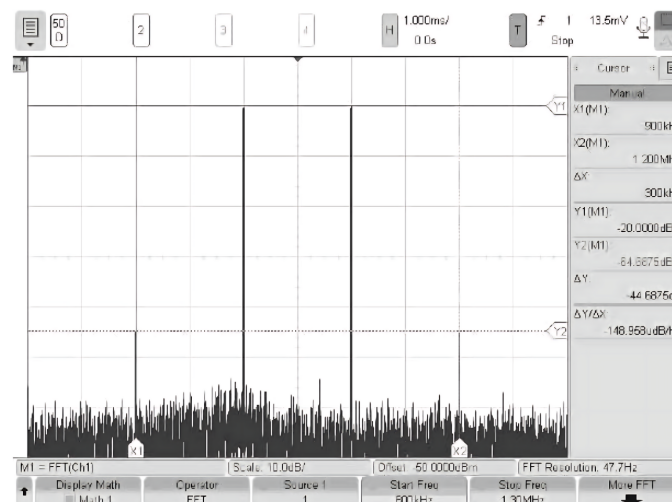


Figure 14. Measured PSD of the filter output for a two-tone test (“11” operation mode).

The IIP3 was also evaluated for each operating mode according to Lo et al. [4]. As the reconfigurable OTA used in the filter had a high output impedance, the IIP3 analysis was performed by applying a power signal to the filter input and measuring a voltage signal at the output instead of a power signal. However, for comparison purposes, the input and IIP3 voltage signal values were expressed as power signals referred to a 50 Ω load. Figure 15 shows the measured input power versus the IM3 output power of the filter for each operating operation mode. Two input tones with frequencies of 0.5 and 0.6 MHz and an initial power of -40 dBm were applied to the filter input. The values of IIP3

were estimated by extrapolating these points and reached 0.13/4.63/7.75/8.17 dBm for configuration modes 00/01/10/11.

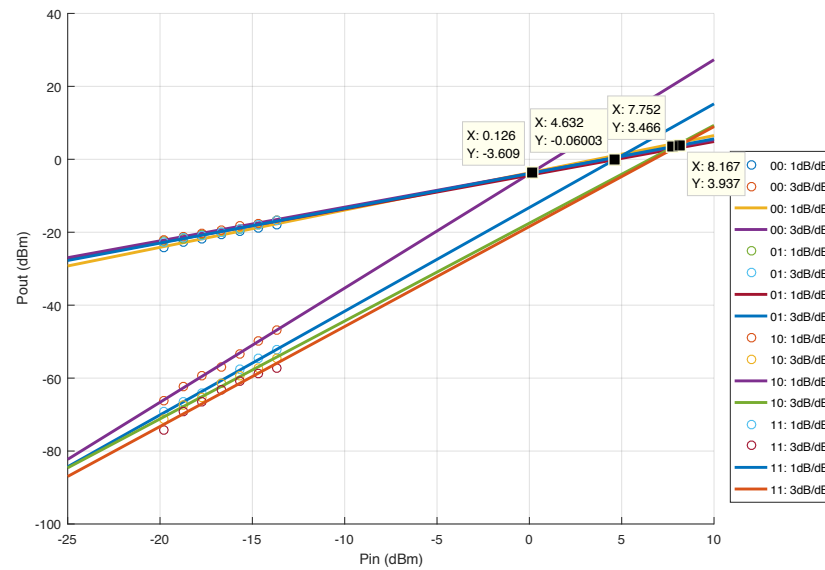


Figure 15. Measured in-band IIP3 for each filter operation mode.

The noise density was measured in a spectrum analyzer from 100 kHz to 20 MHz with a span of 2 MHz and a resolution bandwidth (RBW) of 100 Hz. The RBW and span needed be set so that the DC trace was not integrated by the bandpass filter. The results obtained were 162/239/61.2/49.7 nV/ $\sqrt{\text{Hz}}$ for the operating modes 00/01/10/11, according to Figure 16.

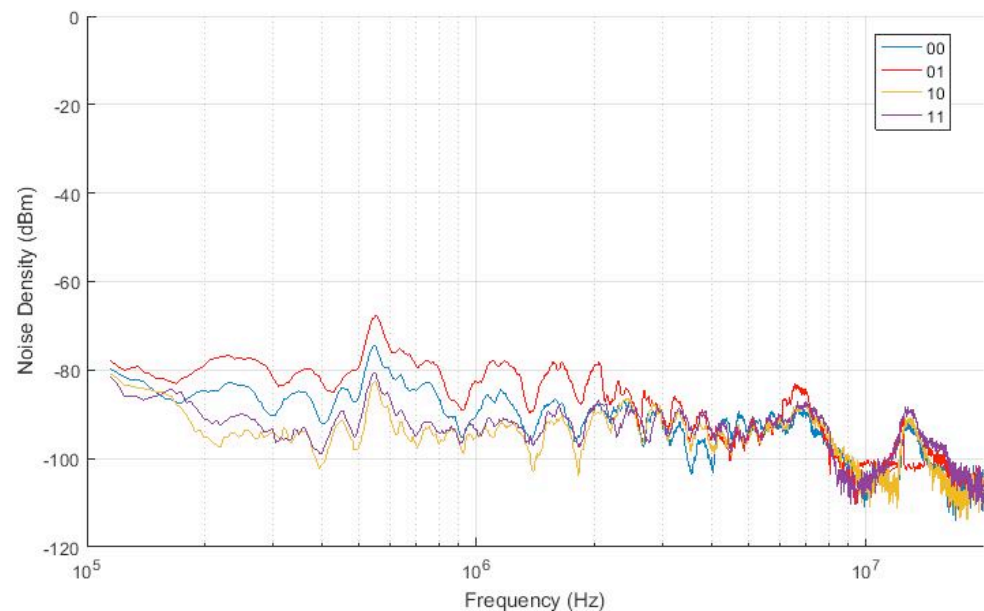


Figure 16. Measured filter noise density.

In order to compare this work with previous work in the literature, the following figure of merit (FoM) was evaluated [16]:

$$\text{FoM} = \frac{P_{\text{tot}}/N}{f_c \cdot (\text{SFDR} \cdot N^{\frac{4}{3}})} \quad (5)$$

Here, P_{tot} is the total power consumption of the LPF, N is the number of poles and zeros, f_c is the cut-off frequency, and SFDR is the spurious-free dynamic range expressed by:

$$\text{SFDR} = \left(\frac{\text{IIP3}}{P_N} \right)^{2/3} \quad (6)$$

In this case, P_N is the noise power evaluated at the filter input.

Table 3 summarizes the filter performance results including the FoM (expressed in fJ) and Table 4 presents a performance comparison with related works reported in recent years. It is possible to verify that our tunable filter had a low noise power and reduced silicon area. It achieved a comparable Figure of Merit (FoM) for the cutoff frequency of 8.1 MHz, but it suffered from high power consumption. We should highlight that the main source of power consumption was the common-mode feedback (CMFB) circuit, which was not optimized and accounted for about 80% of the filter total power consumption. If not considering the power consumed by the CMFB circuit, the FoM reduced from a range of 0.99 to 20.07 fJ to a range of 0.12 to 2.60 fJ.

Our tunable filter also featured a competitively small microchip area of 0.23 mm² compared with the other designs compared in Table 4, which had areas ranging from 0.125 mm² to 2.9 mm². The exception is [17], which presented a silicon area of 9 μm², achieved with a first order passive RC filter.

It is worth noting that the work in [11] showed a tunable gm-C filter, where the tuning range was achieved without the need for array configuration, as it used triode-biased input MOSFETs with transconductance tuned by adjusting the drain bias current. Our work adopted the same filter architecture, but the tuning was achieved by the reconfigurable OTA. Our work consumed more power, but this was due to the oversized CMFB circuit in our filter. It could be improved and scaled in future implementations. As for [11], the reconfiguration implemented the reconfiguration in our work did not rely on a precise voltage to set the filter bandwidth, but only digital signals were used to increase the OTA transconductance. A wider tuning range could be achieved by increasing the number of switchable OTAs. In addition, the work presented in [18] introduced a complex-pole filter implemented with switched capacitors, where tunability was achieved using a capacitor bank. Our work was a low-pass gm-C filter where tunability was achieved by reconfiguring the OTA transconductance, with the advantage of power scaling. In [18], the overall performance was superior but the silicon area was 2.9 mm², while the proposed filter occupied only 0.23 mm².

The achieved IIP3 was lower than in related works, indicating lower linearity of the filter. However, as the objective was to present a reconfigurable Gm-C filter based on switched OTAs with a digital control, there was an expected impact on linearity, increasing the FoM for cases with a smaller cutoff frequency.

This drawback in linearity could be compensated by the fact that the filter can be easily implemented in CMOS technologies, offering simplicity and cost-effectiveness in manufacturing. Moreover, the reconfigurable OTA can be reused for the design of active RC analog filters, providing greater versatility and efficiency in the development of other analog circuits.

Table 3. LPF Performance summary.

Technology	180 nm CMOS							
Supply Voltage	1.8 V							
Filter Type	Biquad (Q = 1)							
Order	4							
Silicon area	0.23 mm ²							
Reference	Post layout Simulation				Measurements			
Operation mode	00	01	10	11	00	01	10	11
Cutoff Frequency (MHz)	2.55	5.11	7.68	10.29	1.90	3.56	6.07	8.15
IIP3 (dBm)	−2.59	1.11	2.96	4.14	0.13	4.63	7.75	8.17
Noise (nV/√Hz)	58.1	42.66	34.88	27.88	162	239	61.2	49.7
Power (mW)	10.27	11.18	12.06	12.96	9.90	11.52	12.83	13.10
FOM (fj)	7.30	2.37	1.28	0.77	20.07	15.95	1.55	0.98

Table 4. LPF measurement performance comparison with previously reported works.

Parameter	This Work	[1]	[19]	[18]	[20]	[11]	[21]	[17]
Tech. (nm)	180	130	180	180	90	180	22	45
VDD (V)	1.8	1.2	1.8	1.8	1.0	1.8	1	1.8
Filter Type	2 × Bi (Q = 1)	But.	Cheb.	LPF	But.	But.	Papoulis	Passive RC
Order	4	2-4-6	3	4	6	4	10	1
f_c (MHz)	1.9–8.1	0.3–23.5	48–200	0.49–13.3	8.1–13.5	0.3–12.0	700–1500	0.02–0.2
Tuning ratio	4	67	4	N/A	N/A	40	2.1	N/A
IIP3 (dBm)	0.13–8.17	22.97	26.27–32.47	8.07–22.41	21.7–22.1	8.7–18.0	N/A	N/A
Noise ($\frac{nV}{\sqrt{Hz}}$)	162–49.7	83.35–163	5.1	6.54	75	112–4780	N/A	11,313–35,777
Power (mW)	1.28–1.62 * 9.9–13.1 **	0.72–21.6	23.4	4.3	4.35	1.08–4.68	3.3	6×10^{-7}
Area (mm ²)	0.23	0.52	0.24	2.9	0.24	0.125	0.1815	9×10^{-6}
FOM (fj)	2.60–0.12 * 20.07–0.99 **	0.003–0.57	0.005–0.001	0.056–0.002	0.03–0.02	0.66–30.13	-	10.34–1.03

* not considering CMFB; ** considering CMFB.

5. Conclusions

This paper presents the complete design, post-layout simulation results, and silicon measurements for a tunable fourth-order Gm-C filter in a 180 nm CMOS process. Four modes of operation are achieved, covering cut-off frequencies for multi-carrier radio receivers from 1.9 to 8.1 MHz. Tunability is achieved through digitally reconfigurable OTAs, which also allow for scaling of power consumption. The filter offers FoM in terms of power dissipation, noise, and cut-off frequency comparable to recent work published in the literature, but with advantages such as a small area and low sensitivity to component mismatch. The complexity of the design is also reduced as only a single reconfigurable OTA needs to be dimensioned. The measurement results on a prototype chip confirm the functionality of the filter. The configurable strategy is suitable for application in multi-standard receivers for wireless circuits, with advantages in integration due to the smaller silicon area.

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Abbreviations

The following abbreviations are used in this manuscript:

ADC	Analog to digital converter
CMOS	Complementary Metal Oxide Semiconductor
FC	Folded cascode
FoM	Figure of merit
GBW	Gain bandwidth product
ICMR	Input common-mode range
IIP3	Third-order input interception point
LPF	Low pass filter
MiM	Metal insulator metal
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PM	Phase margin
RBW	Resolution bandwidth
SDR	Software defined radio
SFDR	Spurious free dynamic range
SR	Slew rate
WCDMA	Wide-Band code-division multiple access

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