

Article

Synergistic Effects of Total Ionizing Dose and Single-Event Upset in 130 nm 7T Silicon-on-Insulator Static Random Access Memory

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Abstract: The exposure of spaceborne devices to high-energy charged particles in space results in the occurrence of both a total ionizing dose (TID) and the single-event effect (SEE). These phenomena present significant challenges for the reliable operation of spacecraft and satellites. The rapid advancement of semiconductor fabrication processes and the continuous reduction in device feature size have led to an increase in the significance of the synergistic effects of TID and SEE in static random access memory (SRAM). In order to elucidate the involved physical mechanisms, the synergistic effects of TID and single-event upset (SEU) in a new kind of 130 nm 7T silicon-on-insulator (SOI) SRAM were investigated by means of cobalt-60 gamma-ray and heavy ion irradiation experiments. The findings demonstrate that 7T SOI SRAM is capable of maintaining normal reading and writing functionality when subjected to TID irradiation at a total dose of up to 750 krad(Si). In general, the TID was observed to reduce the SEU cross-section of the 7T SOI SRAM. However, the extent of this reduction was influenced by the heavy ion LET value and the specific writing data pattern employed. Based on the available evidence, it can be proposed that TID preirradiation represents a promising avenue for enhancing the resilience of 7T SOI SRAMs to SEU.

Keywords: total ionizing dose; single-event effect; single-event upset; synergistic effects; static random access memory



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1. Introduction

SRAM's advantages of high reading and writing speeds and low power consumption have led to its widespread use in spacecraft and satellites. The space environment is replete with high-energy charged particles, which deposit energy in the SRAM, resulting in radiation effects and ultimately leading to SRAM function errors and mission failure for the spacecraft. Two significant radiation effects that spaceborne SRAM frequently encounter are the TID and SEE. Consequently, research in this area has garnered increasing attention [1]. Since the launch of the first human-made satellite, a certain percentage of spacecraft and satellites have exhibited functional errors or even mission failures as a result of a SEE or the TID [2,3]. The rapid development of semiconductor technology has resulted in a reduction in the feature size of SRAMs to the order of ten nanometers, accompanied by a reduction in the critical charge of the SEU to one-tenth of the femtocoulombs [4]. The cross-section of the SEU in an SRAM with a smaller feature size is greater than that of an SRAM with a larger feature size when subjected to the same radiation conditions. In recent years, the synergistic effects of the TID and SEE in SRAMs with a nanometer feature

size have become increasingly significant. However, the underlying physical mechanisms remain unclear.

In SRAM, the generation of additional electron–hole pairs is achieved through the direct ionization of heavy ions. Given that electrons exhibit considerably higher mobility than holes, the latter are prone to forming trapped charges within the oxide layer [5]. Once trap charges are formed, the threshold voltage of the transistors begins to drift, and the off-state leakage current increases [6,7]. The SRAM region that is susceptible to SEUs is the drain region of the transistors in the off-state [8]. An increase in the transistor off-state leakage current results in a change in the potential of the storage nodes. Furthermore, threshold voltage drift leads to a change in the critical charge required for SEU, which affects the SEU sensitivity of the memory cell. Therefore, the SEU sensitivity of SRAM is affected by the TID. Furthermore, if the transistor is in the on state during TID irradiation, the effects of the TID on SEU of SRAM are more pronounced.

Since the 1980s, a number of research groups have conducted studies into the effects of the TID on SEU in SRAM with feature sizes ranging from microns to sub-microns, particularly in the context of advanced processes [9–12]. In light of the findings of relevant research, the guidance for SEE evaluation proposed by the Sandia National Laboratory explicitly requires the performance of the SEE test on an SRAM without a TID and with an 80% expected TID [13]. This is in order to determine the impact of the TID on the SEE of the SRAMs. Given the disparate internal structures and production processes of the various types of SRAMs, the impact of the TID on SEU resistance has been observed to vary. Some studies have indicated that the TID can diminish SEU resistance, while others have demonstrated that the TID can markedly increase the SEU cross-section [14]. Others have found no significant influence of the TID on SEU cross-section [15]. The influence of the feature size and the test data patterns during irradiation experiments on the synergistic effects of the TID and SEU in SRAM is considerable. The sensitivity of SRAM to SEU is dependent on the writing data pattern employed during both the TID and SEU experiments. This phenomenon, which is associated with the data patterns employed during the experimental process, is known as the “imprinting effect” [10,16]. The application of varying gate voltages to the transistor during the TID experiments is postulated to result in disparate degrees of radiation-induced damage, which is believed to be the primary mechanism underlying the “imprinting effect”. The “imprinting effect” in SRAM appears to dissipate as the feature size of the SRAM diminishes to the depths of the submicron and subnanometer ranges.

The physical isolation between the channel region and the substrate inherent to the SOI process serves to markedly diminish the charge collected at the source and drain electrodes during heavy ion irradiation, thereby conferring a substantial enhancement in the SEU resistance of SRAM [17–19]. The single-event latch-up (SEL) [20] and tunneling effects [21] are two common phenomena observed in bulk silicon devices subjected to heavy ion irradiation. However, these effects are absent in SRAM that employs the SOI process. It is hypothesized that SOI SRAM will prove resistant to the space radiation environment and thus have a broad range of applications in such conditions. Raine et al. observed that a single heavy ion incident in 45 and 28 nm SOI SRAMs with an oblique angle would result in a four-bit upset [22]. Additionally, they found that the charge sharing effect is not the primary cause of multibit upsets under positive incidence conditions [23]. In experiments involving protons and heavy ions, Liu et al. observed that SEU in SOI SRAM occurs exclusively when the delay transistor and the off-state NMOS transistor in the same memory cell are simultaneously irradiated by heavy ions or secondary ions produced by protons [24]. The synergistic effects of the TID and SEE in SOI SRAM are subject to variation depending on the material preparation process and device structure employed. As a result, there is currently no unified understanding of the synergistic effects. Studies examining the synergistic effects of the TID and SEU in 7T SOI SRAM are relatively limited, and the underlying physical mechanisms remain poorly understood. In this study, a broader range of heavy ion LET values was employed in an SEU irradiation experiment,

and a greater number of dose points were set for the TID experiment, with the aim of obtaining more general experimental results. Based on these results, an investigation was conducted into the physical mechanisms of the synergistic effects in 7T SOI SRAM.

2. Experimental Details

To enhance the SEE resistance of SRAM during the course of a space mission, a team of scientists from the Institute of Microelectronics, Chinese Academy of Sciences, devised a 130 nm 7T SOI SRAM based on a CMOS process. The 7T SOI SRAM is formed by the addition of a delay transistor, N5, to the conventional 6T SOI SRAM layout, as illustrated in Figure 1. In the 7T SOI SRAM, the memory cells are organized in an $8\text{ k} \times 8\text{ bit}$ configuration, resulting in a total memory capacity of 64 kbits. During operation, the 7T SOI SRAM is powered by two sources: a 3.3 V source for the input and output circuit and a 1.5 V source for the memory array. The memory cell comprises four N-type metal-oxide semiconductor (NMOS) transistors, two P-type metal-oxide-semiconductor (PMOS) transistors, and a delay transistor. The feature size of the memory cell is $3.9\text{ }\mu\text{m} \times 3.4\text{ }\mu\text{m}$. The access transistors N3 and N4 share drains with their pull-down transistors N1 and N2, and the gate electrode of the access transistors N3 and N4 is connected to the gate electrode of the delay transistor N5. During the reading and writing of data, the delay transistor N5 is activated, resulting in a notable reduction in its resistance. Once data are written to the cell, the delay transistor N5 is deactivated, resulting in a high resistance value. This effectively mitigates the impact of single-event transients (SETs), enhancing the resilience of the 7T SOI SRAM in a space radiation environment. Figure 2a illustrates the configuration of the NMOS transistors (N1, N2, N3, N4) and PMOS transistors (P1, P2) within a memory cell, which can be described as a body under source field effect transistor (BUSFET). Figure 2b depicts the internal structure of the delay transistor N5.

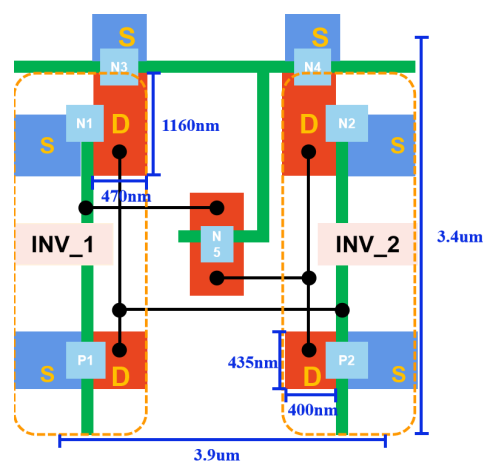


Figure 1. Schematic diagram of memory cell structure in of 7T SOI SRAM.

The TID experiment of the 7T SOI SRAM was conducted in the cobalt-60 gamma-ray irradiation chamber at the China Institute of Atomic Energy (CIAE), as illustrated in Figure 3. The dose rate was set to 90 krad(Si)/h. The 7T SOI SRAMs undergoing evaluation were partitioned into three categories, with each category comprising two 7T SOI SRAMs, resulting in a total of six 7T SOI SRAMs being utilized. The total dose imparted to the three groups of 7T SOI SRAM was set at 300 krad(Si), 500 krad(Si), and 750 krad(Si), separately. All 7T SOI SRAMs were mounted on a test board and removed from the board when the prescribed dose was reached. To ascertain whether a “imprinting effect” was present in the synergistic effects of the TID and SEU, a data pattern of “55” was written into one 7T SOI SRAM in each group prior to the TID experiment. This involved writing data “0” and “1” into the memory cell in the form of a checkerboard. Following the TID experiment, the irradiated 7T SOI SRAMs were maintained in a dry ice bucket until the

commencement of the SEU experiment. During this interval, the 7T SOI SRAM was in the dry ice bucket, with the exception of the postirradiation performance test.

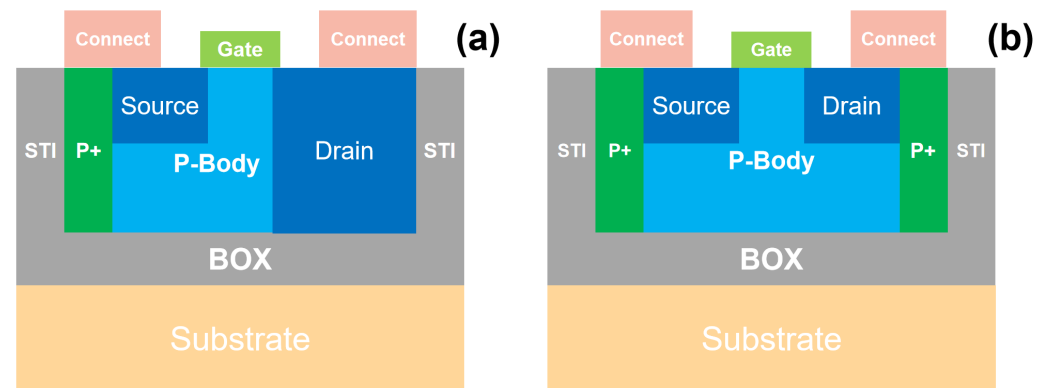


Figure 2. Schematic diagram of transistors N1, N2, N3, N4, P1, P2 (a) and delay transistor N5 (b).



Figure 3. The irradiation platform (a) and the 7T SOI SRAMs under test (b) of the TID experiment.

The SEU experiment of the 7T SOI SRAMs was conducted at the SEE experimental terminal of the HI-13 heavy ion tandem accelerator, which is operated by the CIAE. Figure 4 illustrates the configuration of the 7T SOI SRAM on the test board. Table 1 presents the principal parameters of the heavy ions employed in the SEU experiment, together with the LET value and projection range of the heavy ions within the 7T SOI SRAM, which were calculated by SRIM 2013. The LET values ranged from 5.0 MeV·cm²/mg to 37.4 MeV·cm²/mg. To determine the synergistic effects of the TID and SEU cross-section in the 7T SOI SRAM, two 7T SOI SRAMs devoid of TID irradiation were incorporated into the SEU experiment. The SEU experiment was terminated when the SEU count exceeded 100 or the heavy ion fluence reached 1.0×10^7 ions/cm². Two SEU experiments were conducted on each 7T SOI SRAM, utilizing data patterns “55” and “AA”, separately.

Table 1. The key parameters of the heavy ions used in this work.

Ion Species	Energy (MeV)	LET (MeV·cm ² /mg)	Range in Si (μm)
F	80	5.0	54.35
Si	143	9.3	50.69
Cl	138	13.9	38.99
Ti	169	21.8	34.66
Ge	205	37.4	29.95

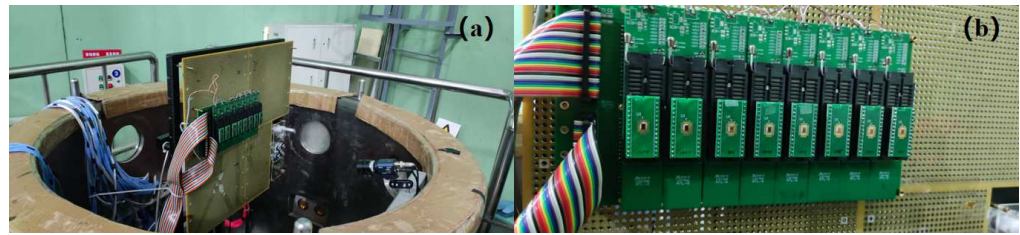


Figure 4. The irradiation platform (a) and the 7T SOI SRAMs under test (b) of the SEU experiment.

3. Results and Discussion

In the TID experiment, three groups of 7T SOI SRAMs were subjected to total doses of 300 krad(Si), 500 krad(Si), or 750 krad(Si) by a cobalt-60 gamma-ray. Following the TID experiment, a test was conducted to assess the functionality of the 7T SOI SRAM. The results demonstrated that the 7T SOI SRAM exhibited no errors following the TID experiment. Figure 5 illustrates the integrated circuit quiescent current (IDD) of the 7T SOI SRAM following the TID experiment, with all memory cells written to a value of “0” or “1”. The IDD of the 7T SOI SRAM in the absence of TID irradiation was 0.0024 mA. Following the TID experiment, the IDD increased to 1.26 mA when all the memory cells were written to data “0” and to 2.92 mA when all the memory cells were written to a value of “1”. Changes in IDD are associated with the generation of trap charges in the shallow trench isolation (STI) region. Following the TID experiment, the trap charges captured in the STI region resulted in the formation of a weak leakage channel between the source and drain regions, thereby increasing the IDD. In the case of all memory cells written to a value of “1”, transistors N1 and P2 were in the on state, while in the case of all memory cells written to a value of “0”, transistors P1 and N2 were in the on state. Consequently, the IDD leakage current flowed through the NMOS N1 and PMOS P2 when the memory cell stored the value “1”, while the IDD leakage current flowed through the PMOS P1 and NMOS N2 when the memory cell stored the value “0”. Two factors are of particular consequence with regard to the TID in 7T SOI SRAM: the trap charges density in the SiO₂ layer and the trap density of the SiO₂/Si interfacial state. Following the TID experiment, the threshold voltages of the transistors underwent alteration, as did the internal electric fields, due to the differing mobilities of the carriers. This resulted in an increase in the IDD of the 7T SOI SRAM.

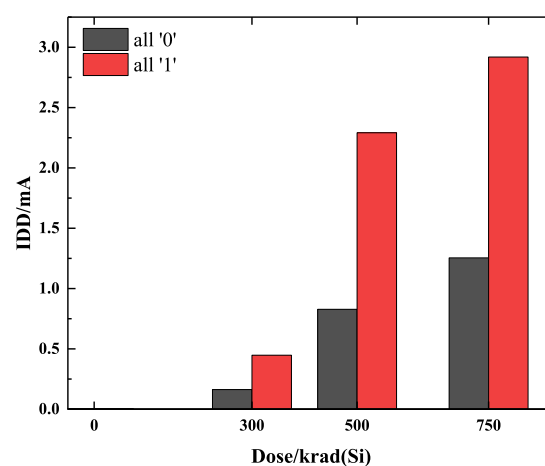


Figure 5. The IDD of the 7T SOI SRAMs after TID irradiation.

Figure 6 illustrates the SEU cross-section of the 7T SOI SRAM subjected to irradiation with and without a total dose of 750 krad(Si) as a function of the heavy ion LET value. The data pattern that can be observed in the 7T SOI SRAM is “55”. The SEU cross-section of the 7T SOI SRAM without the TID demonstrated a positive correlation with the heavy ion LET value. The minimum SEU cross-section of the 7T SOI SRAM without the TID was

$1.56 \times 10^{-11} \text{ cm}^2/\text{bit}$, which was larger than the average area, $1.33 \times 10^{-11} \text{ cm}^2/\text{bit}$, of the memory cell. This indicates that multicell upsets occurred during the SEU experiment. The minimum SEU cross-section of the 7T SOI SRAM with a total dose of 750 krad(Si) was $2.81 \times 10^{-11} \text{ cm}^2/\text{bit}$, which indicated that the probability of multicell upsets was increased by the TID. When the heavy ions LET value was less than $13.9 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, the TID was observed to increase the SEU cross-section by approximately 80%. In comparison to the SEU cross-section of the 7T SOI SRAM in the absence of the TID, the SEU cross-section was observed to decrease by a factor of 63.4%, 60.0% and 51.8% following the TID irradiation when the heavy ion LET values were 13.9, 21.8, and $37.4 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. The observed trend in the SEU cross-section of the 7T SOI SRAM employed in this study differs from that of the conventional 6T SOI SRAM in response to TID irradiation [25]. The 6T SOI SRAM has the same design layout, manufacturing process, feature size, and storage capacity as the 7T SOI SRAM. The 7T SOI SRAM is formed by the addition of a delay transistor, N5, to the 6T SOI SRAM layout. Once the data are stored, the delay transistor N5 is in the off state, with a high resistance value that effectively suppresses the transmission of SET pulses between the nodes in the memory cell. The reduction in the SEU cross-section caused by the TID is attributed to the alteration in the internal structure of the memory cell, specifically the change in the role of delay transistor N5, in the 6T and 7T SOI SRAMs.

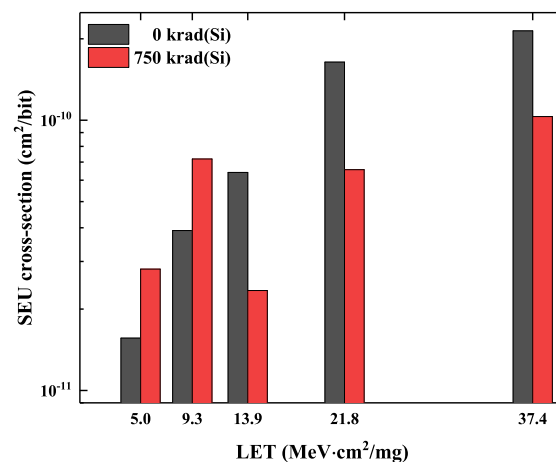


Figure 6. SEU cross-section of the 7T SOI SRAMs before and after the TID irradiation versus the heavy ion LET value.

Figure 7 illustrates the SEU cross-section of the 7T SOI SRAM with total doses of 300 krad(Si), 500 krad(Si), and 750 krad(Si) versus the heavy ion LET value. The left and right panels depict the SEU cross-section of the 7T SOI SRAM with a data pattern of “55” and “AA”, respectively. In general, the impact of the TID on the SEU cross-section is not solely contingent on the total dose but also on the heavy ion LET value. For the “55” data pattern, the TID was observed to increase the SEU cross-section when the heavy ion LET value was lower than $13.9 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ and to decrease the SEU cross-section when the heavy ion LET value was higher than $13.9 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. The impact of the TID on the SEU cross-section exhibited a contrasting trend between the “AA” and “55” data patterns. When the heavy ion LET value was $5.0 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ and the 7T SOI SRAM was irradiated with doses of 300 krad(Si), 500 krad(Si), and 750 krad(Si), the SEU cross-section increased by 20% (“55”), 120% (“55”), and 80% (“55”), respectively. When the heavy ion LET value was $13.9 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, the TID was observed to decrease the SEU cross-section by 12.2% (“55”), 63.4% (“55”), and 63.4% (“55”), respectively. The SEU cross-section of the 7T SOI SRAM with data pattern “55” was also observed to decrease as a result of the TID when the heavy ion LET values were 21.8 and $37.4 \text{ MeV}\cdot\text{cm}^2/\text{mg}$. In the case of the “AA” data pattern and the heavy ion LET value of $37.4 \text{ MeV}\cdot\text{cm}^2/\text{mg}$, the SEU cross-section was observed to increase as a result of the TID. Conversely, when the heavy ion LET values

were 13.9 and 21.8 MeV·cm²/mg, the TID was seen to decrease in the SEU cross-section of the 7T SOI SRAM.

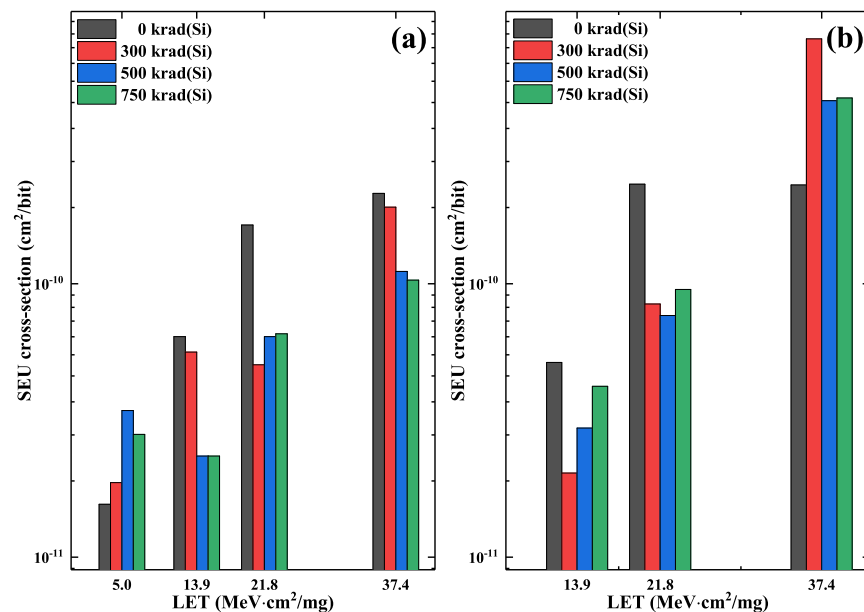


Figure 7. SEU cross-section of the 7T SOI SRAM with data patterns “55” (a) and “AA” (b) versus the heavy ion LET value.

To ascertain the impact of the TID on the SEU cross-section of the 7T SOI SRAM, the variation in the SEU cross-section with the total dose was determined, as illustrated in Figure 8. The SEU cross-section of the 7T SOI SRAM exhibited an increase with the heavy ion LET value. However, the SEU cross-section did not demonstrate a consistent, monotonic variation with the total dose. When the heavy ion LET values were 13.9 and 37.4 MeV·cm²/mg and the data pattern was “55”, a monotonic decrease in the SEU cross-section with the total dose was observed. When the heavy ion LET value was 13.9 MeV·cm²/mg and the data pattern was “AA”, the SEU cross-section demonstrated a monotonic increase with the total dose. In other instances, the SEU cross-section exhibited fluctuations in response to the total dose. When the heavy ion LET value was 5.0 MeV·cm²/mg, the SEU cross-section initially increased and subsequently decreased with the total dose. In the case of a heavy ion LET value of 21.8 MeV·cm²/mg and a data pattern of “55”, the SEU cross-section demonstrated an initial decrease, followed by an increase, with increasing total dose. In the case when the heavy ion LET value was 21.8 MeV·cm²/mg and the data pattern was “AA”, the SEU cross-section initially decreased and subsequently increased with increasing total dose. When the heavy ion LET value was 37.4 MeV·cm²/mg and the data pattern was “AA”, the SEU cross-section exhibited an initial increase followed by a subsequent decrease with increasing total dose. In general, the TID reduces the probability of SEU occurring in the 7T SOI SRAM. In other words, TID preirradiation prior to a space mission can enhance the SEU resistance of 7T SOI SRAM.

To ascertain whether an “imprinting effect” could be observed in the synergistic effects of the TID and the SEU, the data pattern “55” was written to one of the 7T SOI SRAMs in each test group prior to the TID experiment. Figure 9 illustrates the SEU cross-section of the 7T SOI SRAM with and without the data pattern “55” prior to the TID experiment. When the data pattern written to the 7T SOI SRAM prior to TID and SEU experiments was identical, namely, “55”, the SEU cross-section was markedly elevated in comparison to that observed with the data pattern “AA” prior to the SEU experiment. The data pattern “55” written prior to TID experiment was observed to reduce the SEU cross-section of 7T SOI SRAM with a data pattern of “AA” prior to the SEU experiment. The results demonstrate that the data pattern written before the TID experiment affected the SEU cross-section of the 7T SOI SRAM. This indicates that the “imprint effect” is present in the synergistic

effects of the TID and the SEU in 7T SOI SRAM. It can thus be concluded that the SEU cross-section is larger if the same data pattern is written to the 7T SOI SRAM before TID and SEU experiments.

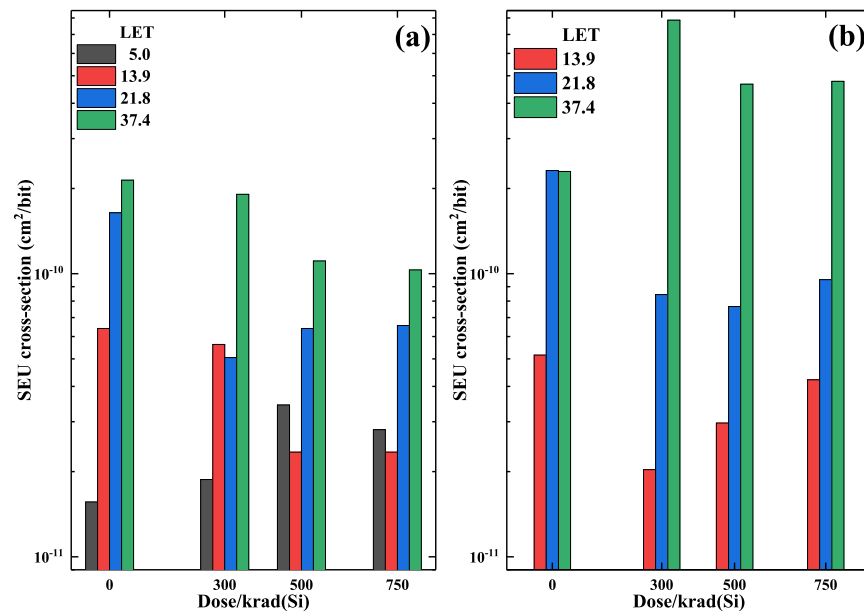


Figure 8. SEU cross-section of the 7T SOI SRAM with data patterns “55” (a) and “AA” (b) versus the total dose.

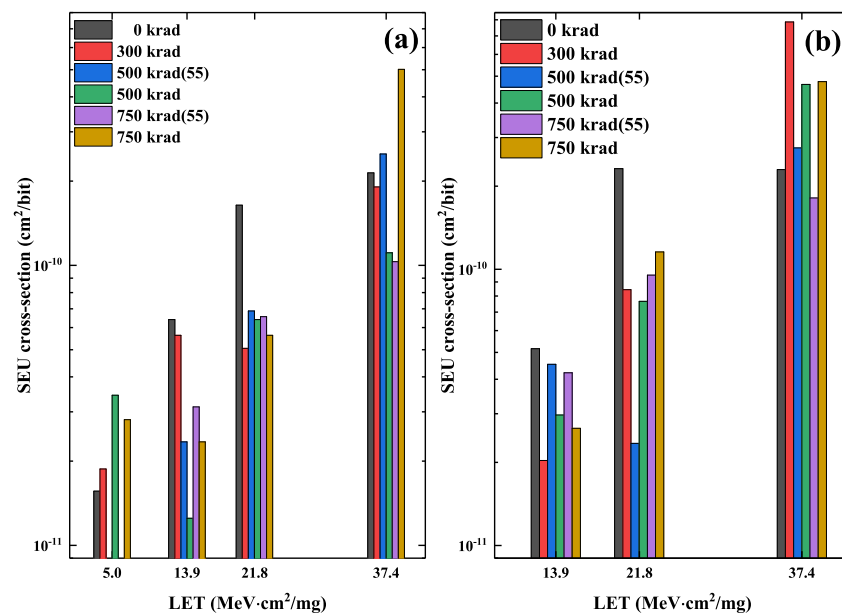


Figure 9. SEU cross-section of the 7T SOI SRAMs with data pattern “55” (a) and “AA” (b), and one of the SOI SRAMs in each test group was written with data pattern “55” before the TID irradiation.

To reveal the reason for the SEU cross-section change in the 7T SOI SRAM following TID irradiation, the alteration of upset models (including “0→1” upset and “1→0” upset) under varying irradiation conditions was examined, as illustrated in Figures 10 and 11. The proportion of the “0→1” upset and “1→0” upset models was altered by the TID, and the results were not only dependent on the total dose but also on the data pattern and heavy ion LET value. In certain instances, the “0→1” upset constituted the majority of the SEU, with a subsequent decrease in its proportion following TID irradiation. In other instances, the TID was observed to increase the proportion of the “0→1” upset. Following TID irradiation, the

reduction in the “0→1” upset cross-section was greater than that observed for the “1→0” cross-section. It can be concluded that the reduction in the SEU cross-section was primarily attributable to the decline in the “0→1” upset.

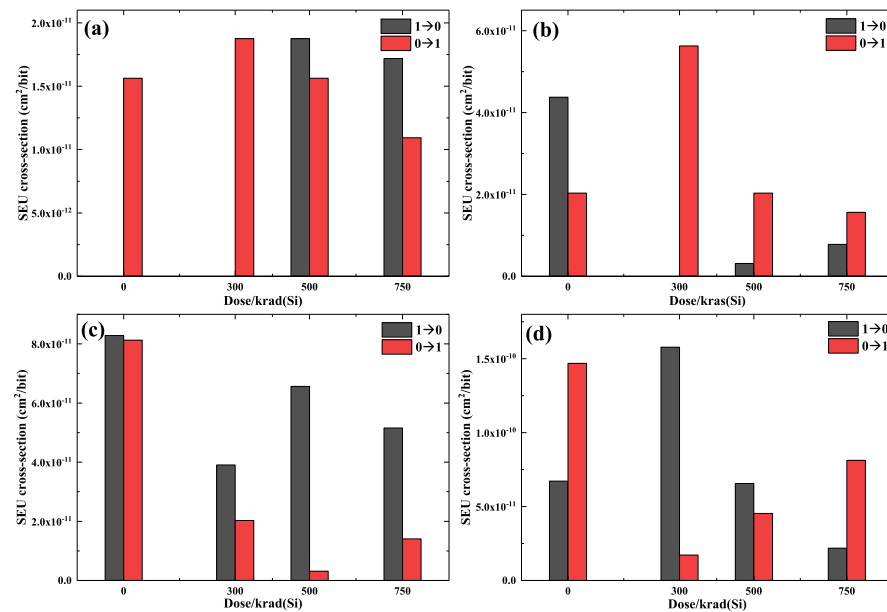


Figure 10. SEU cross-section of the upset models “0→1” and “1→0” in the 7T SOI SRAMs with data pattern “55” under heavy ion irradiation with LET of 5.0 (a), 13.9 (b), 21.8 (c), and 37.4 (d) MeV·cm²/mg after TID irradiation.

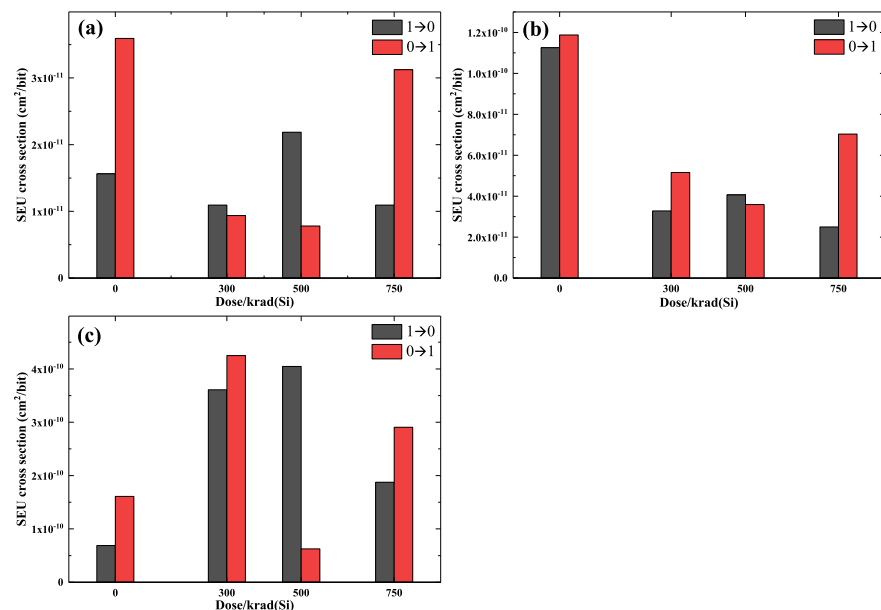


Figure 11. SEU cross-section of the upset models “0→1” and “1→0” in the 7T SOI SRAMs with data pattern “AA” under heavy ion irradiation with LET of 13.9 (a), 21.8 (b), and 37.4 (c) MeV·cm²/mg after TID irradiation.

The greater mobility of electrons in silicon compared to holes results in the rapid collection of electrons by a drain, driven by the electric field. It can thus be concluded that the SEU cross-section of 7T SOI SRAM is dependent on the pull-down NMOS transistor in the off state. Figure 12 illustrates the simplified equivalent circuits of the upset models “0→1” and “1→0” in a memory cell, including the SET pulse propagation. When the Q node stores a value of “0”, the pull-down transistor N1 is in the off state, maintaining a low

potential at the Q node. The generation of SET pulses is achieved through the bombardment of the transistor N1 with heavy ions, resulting in the collection of charge at the drain of transistor N1. The subsequent effect of the SET pulse on the gate of inverter 2 is an increase in the potential of the Q node. Given that delay transistor N5 is in an off state following the completion of the write and read operations, the potential perturbation in the Q node via the delay transistor N5 cannot affect the gate state of inverter 1. Consequently, the potential of the $\bar{Q}$ node is reduced gradually. The feedback signal of the SET pulse is suppressed and latched in the memory cell affected by heavy ion irradiation, resulting in a high “0→1” upset cross-section.

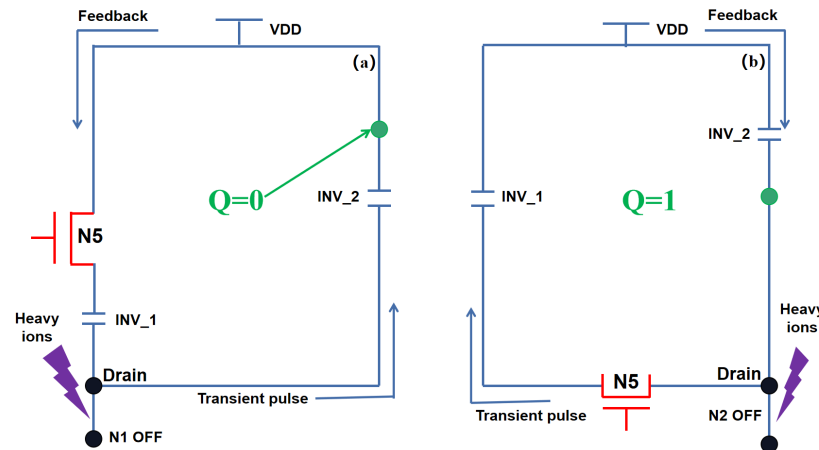


Figure 12. The equivalent circuits of SET pulse propagation corresponding to “0→1” upset (a) and “1→0” upset (b) in 7T SOI SRAMs.

Pull-down transistor N2 is in an off state when the Q node stores a value of “1”. This is indicated by the high potential of the Q node, as illustrated in Figure 12b. Transistor N2 generates SET pulses as a result of heavy ions striking it, with the charge subsequently collected by the drain of transistor N2. The potential perturbation generated in the Q node well is fed back to the gate of inverter 2 through delay transistor N5, resulting in a gradual decrease in the potential of the Q node. As a consequence of the delay transistor N5 being in the off state following the completion of the write and read operations, the SET pulses are unable to be transmitted to the gate of inverter 1 by the delay transistor N5. This results in the potential of the $\bar{Q}$ node being very difficult to affect. Consequently, the SET pulse is delayed and suppressed, becoming latched to the memory cell affected by heavy ions. The “1→0” upset cross-section is smaller than that of the “0→1” upset in 7T SOI SRAM.

Previous research has demonstrated that carrier mobility is subject to alteration as a consequence of the TID [26–28]. The carrier mobility in the transistor can be calculated using the following equation:

$$\frac{1}{\mu_n} = \frac{1}{\mu_1} (E_{eff})^{|\alpha_1|} + \frac{1}{\mu_2} (E_{eff})^{|\alpha_2|} + \frac{1}{\mu_3} Q_{ot} \left(\frac{1}{N_i} \right)^{\alpha_3} \quad (1)$$

where μ_i , E_{eff} , α_i , Q_{ot} , and N_i are the fitting parameters, the effective vertical electric field intensity, the oxide trap charge density, and the charge density of inversion layer, respectively.

The carrier mobility is primarily influenced by three key factors: charged impurity scattering, surface scattering, and phonon scattering. The rate of charged impurity scattering is seldom affected by TID; rather, it is contingent upon the specific preparation methodology employed for the device in question. The intensity of the electric field perpendicular to the channel direction determines the rate of phonon scattering and surface scattering. The vertical electric field component is strongly dependent on the density of trap charges generated in the oxide. The rate of surface scattering and phonon scattering in the transistor is increased by TID. As a consequence of TID irradiation, a considerable number of radiation-induced trap charges are created in the STI and BOX regions of delay

transistor N5 [27,29]. This results in the generation of an electric field perpendicular to the channel region. Following TID irradiation, the vertical electric field results in increases in both phonon and surface scattering. The reduction in the carrier mobility rate results in an increase in the off-state resistance of delay transistor N5, while simultaneously enhancing the memory cell's ability to withstand SET perturbations. Ultimately, the SEU cross-section of 7T SOI SRAM is reduced as a consequence of TID.

4. Conclusions

This work investigated the synergistic effects of TID and SEU in a new kind of 130 nm 7T SOI SRAM through the use of cobalt-60 gamma-ray and heavy ion irradiation experiments. The results demonstrated that the SEU cross-section of the 7T SOI SRAM is reduced by the TID. However, the trend of the variation is dependent on the heavy ion LET value and the test data pattern. No monotone linear relationship was observed between the reduction in the SEU cross-section and the total dose. The SEU cross-section of the 7T SOI SRAM is influenced by the data pattern. It was observed that the SEU cross-section was higher when the 7T SOI SRAM was written with the same data pattern prior to the TID and SEU experiments. This suggests the presence of an “imprinting effect”. The trapped charges in the STI and BOX region are generated by the TID, which enhances the surface scattering and phonon scattering of the carriers and reduces the carrier mobility in delay transistor N5. Therefore, the resistance of delay transistor N5 is increased by the TID. The increase in resistance enhances the ability of delay transistor N5 to suppress the SET pulses and the feedback signals. Consequently, the SEU cross-section of 7T SOI SRAM is decreased by the TID. Furthermore, our research demonstrates that TID irradiation prior to a space mission can improve the SEU resistance of 7T SOI SRAM.

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Abbreviations

The following abbreviations are used in this manuscript:

TID	Total Ionizing Dose
SEE	Single-Event Effect
SRAM	Static Random Access Memory
SEU	Single-Event Upset
SOI	Silicon-on-Insulator
LET	Linear Energy Transfer
SET	Single-Event Transient
IDC	Integrated Circuit Quiescent Current

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