A 14-Bit Digital to Analog Converter for a Topmetal-CEE Pixel Readout Chip

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Abstract: The Lanzhou Heavy Ion Research Facility (LIRF) is the largest heavy ion research facility in China, providing a substantial volume of experimental data for fundamental research in nuclear physics. The Topmetal-CEE is a pixel readout chip specifically designed for tracking detectors. Within the Topmetal-CEE framework, the front-end amplifier and comparator necessitate precisely adjustable bias voltages. Hence, in this paper, a 14-bit resolution DAC with an R-2R resistor network structure is designed, along with an amplifier featuring high driving capabilities as the DAC driver, thus preventing potential impedance issues when driving large pixel arrays. Test results demonstrate that the DAC module, operating under a 3.3 V supply voltage, can consistently output voltages ranging from 0 to 1.8 V. Furthermore, the differential non-linearity error is less than 1.07 LSB, and the integral non-linearity error is less than 1.57 LSB.

Keywords: DAC; R-2R; bandgap; ACBC AMP

1. Introduction

With the progress of science and technology, the instruments utilized in physics experiments continuously undergo enhancements and refinements. The establishment of the Heavy Ion Research Facility in Lanzhou (HIRFL) represents a significant milestone in the realm of particle physics in China [1]. This facility has the capability to accelerate heavy ions up to a medium energy of 110 MeV, facilitating research on various fronts, including the synthesis of new nuclides located far from the stabilization line, collisions involving low- and medium-energy heavy ions with thermonuclear properties, as well as the utilization of heavy ion beams.

The collisions between these high-energy particles result in a diverse range of charged entities. In the vicinity of the heavy ion accelerator, an array of detectors is responsible for capturing the trajectories, positions, and temporal signatures of these resulting ions. And the Heavy Ion Research Facility in Lanzhou consists of two integral systems along with a versatile cooling storage ring (CSR): the sector-focused cyclotron (SFC) and the separated sector cyclotron (SSC) [2].

To advance research in particle physics, a groundbreaking scientific instrument is set to be established on the CSR platform. The CSR external-target experiment (CEE) is a low-temperature, high-density nuclear matter detection spectrometer [3]. It is used to explore the properties of nuclear matter in the region of elevated baryon density through heavy ion collision experiments. At the heart of the CEE is the time projection chamber (TPC) [4], which primarily captures the three-dimensional trajectory information of particles...
The DAC is required to provide bias voltages for 256 pixel units while considering factors such as routing capacitance and parasitic capacitance. Consequently, the DAC must possess ample driving capability to handle around a 10 pF load in total. To meet the stringent demands of precise and stable threshold and bias voltages within the Topmetal-CEE chip, a DAC with at least 12-bit of accuracy and minimal power consumption is essential. Ref. [7] presents a 12-bit digitally calibrated D/A converter that uses digital calibration to bring the design to a high level of accuracy, but its power consumption is high. The design proposed in [8] consumes less power, but its accuracy is only 4-bit. This work, tailored to the specific application requirements, incorporates Cadence tools for design and simulation. A DAC has been designed and fabricated, guaranteeing a stable output voltage with a precision of 14-bit over a range of 0–1.8 V, where the least significant bit (LSB) is a mere 101 µV.

The initial chip design of the Topmetal-CEE, depicted in Figure 1, can be divided into two main areas [6]: the pixel array and the peripheral circuitry. The pixel configuration consists of a single column and an array of 256 rows. To streamline the readout process for the entire pixel array, the pixels are divided into two distinct sections, each managed by its own dedicated priority logic circuitry. The peripheral circuitry includes essential components such as the DAC, SPI, four ADCs, and high-speed data transmission circuitry. The SPI controls the DAC, providing threshold and bias voltage to the individual pixel units. Meanwhile, the ADCs undertake the conversion of information containing both energy and temporal data into digital code, facilitated by a high-speed data link.

![Figure 1. Topmetal-CEE chip architecture block diagram.](image-url)
2. Design of Key Modules

The DAC designed in this paper is required to bias the pixel unit. The types of DAC can be categorized into a switched-capacitor DAC, a delta-sigma DAC, and a resistive DAC. Switched-capacitor DACs have low-power characteristics, but in order to reduce the area of the DAC, their unit capacitance is generally in the fF order of magnitude, and small capacitance is difficult to match in tape-out, resulting in large errors. A delta-sigma DAC [9] is used as an oversampling DAC to achieve higher DAC accuracy by oversampling. Its internal structure contains an interpolation filter, a noise rectifier circuit, a DAC, and a low-pass filter. In order to ensure the quality of the over-sampled signal, the interpolation filter uses multiple filters to achieve a high sampling rate, and the increase in the number of bits of the quantizer also improves the accuracy of the DAC, which will increase power consumption and area. The resistive DAC includes a resistive network and an output amplifier, which is easier to guarantee the mismatch of the network and also can achieve a low power consumption. In summary, the resistive DAC is more suitable for this application. The typical structure of a binary-weighted resistive DAC is depicted in Figure 2. While this structure can be utilized in high-sampling-rate circuits due to its minimal susceptibility to the overall sampling caused by parasitic capacitance, it presents challenges during manufacture due to the significant impedance mismatch between the highest and lowest bits, reaching a ratio of 1:16384. This makes resistance matching difficult, whereby any mismatch introduced during layout design and production will undermine the performance of the DAC as data converters [10].

![Figure 2. Binary-weighted resistive DAC diagram.](image)

The circuit suffers not only from the difficulty of matching the resistors, but also from the noise, and the one-sided spectral density of the thermal noise of the resistors can be expressed as

\[ S_v(f) = 4KTR, f \geq 0 \]

(1)

where \( S_v(f) \) is the thermal noise spectrum of the resistor, \( K \) is Boltzmann constant, \( T \) is the temperature in Kelvins, and \( R \) is the resistance value of the resistor. For the integrating noise \( P \) over 0–100 kHz at a temperature of 300 K, the noise can be expressed as

\[ P = \int_0^{100k} 4KTR = 1.656 \times 10^{-15} \times RV^2 \]

(2)

To achieve a high accuracy, the thermal noise should be kept below half of the least significant bit (LSB) value:

\[ \sqrt{P} = 5.5 \times 10^{-5}, R = 18,260 \Omega, r = \frac{R}{2^{13}} = 2.23 \Omega \]

(3)

where \( R \) is the maximum resistance value in the resistive network and \( r \) is the minimum resistance value. Obviously, the smallest \( r \) is only 2.23 ohms, making it difficult to match the circuit during layout design. To solve this problem, the binary resistive DAC shown...
in Figure 3 has an improved structure, where the high and low bits are segmented by weighting the series resistors.

![Segmented DAC Structure Diagram](image)

Figure 3. The segmented DAC structure diagram.

In the following, we have analyzed the weight of the segmented resistors; when only the lowest bit is connected to the VREF, the higher six resistors are connected to the ground. The current of the feedback resistor R can be expressed as

$$I = \frac{V_{\text{ref}}}{8R + (8R//4R//2R//R)} = \frac{15 \times V_{\text{ref}}}{128R} \quad (4)$$

The potential of $V_x$ can be expressed as

$$V_x = V_{\text{ref}} - I \times 8R = \frac{V_{\text{ref}}}{16} \quad (5)$$

The output voltage $V_{\text{out}}$ can be expressed as

$$V_{\text{out}} = \frac{V_x}{8R} \times R = \frac{V_{\text{ref}}}{2^7} \quad (6)$$

Similarly, other weighting bits can be obtained, and the total output expression can be expressed as

$$V_{\text{out}} = V_{\text{ref}} \times \left[ \frac{D_7}{2^0} + \frac{D_6}{2^1} + \frac{D_5}{2^2} + \frac{D_4}{2^3} + \frac{1}{2^4} \left( \frac{D_3}{2^1} + \frac{D_2}{2^2} + \frac{D_1}{2^3} + \frac{D_0}{2^4} \right) \right] \quad (7)$$

The above formula indicates that this method can reduce the resistance value from $2^7$ to $2^3$. However, if we want to achieve a resolution above a 14-bit DAC, this improvement still makes it difficult to match the design resistor network in the layout, resulting in relatively large errors. So, for this design, we have chosen an R-2R resistor network [11] to achieve a 14-bit voltage-type DAC, as illustrated in Figure 4. This R-2R structure exclusively uses two resistance values, R and 2R, significantly reducing the resistance values compared to the basic binary DAC architecture [12–14].

It comprises a bandgap reference, a 14-bit R-2R resistor network, and a differential operational amplifier working as a source follower. The bandgap reference operates at 3.3 V to produce a constant DC reference voltage of 1.8 V. The input code controls the switches within the R-2R resistor network to produce an output voltage at the terminal of the R-2R resistor network. The voltage is then buffered out by the source follower which is Vout, corresponding to the input code. The output voltage Vout of the DAC can be expressed as

$$V_{\text{out}} = V_{\text{REF}} \left( \frac{1}{2^1} D_1 + \frac{1}{2^2} D_2 + \cdots + \frac{1}{2^{10}} D_{13} + \frac{1}{2^{11}} D_{14} \right) \quad (8)$$
2.1. Bandgap Reference Design

For an R-2R-type DAC, a stable voltage reference is imperative to ensure the precision and decide the full-scale range of the output voltage [15]. The low-voltage bandgap structure depicted in Figure 5 is the approach adopted in this study. This structure utilizes the technique of current summation at the positive and negative input nodes of the operational amplifier [16].

Figure 4. The schematic of the proposed DAC overall structure diagram.

Figure 5. The schematic of the proposed bandgap.

The voltage of the resistor $R_2$ corresponds to the base and emitter of the bipolar transistor Q1 and is inversely proportional to temperature. Assuming that the resistors have zero-temperature resistance, the current flowing through $R_2$ exhibits a negative temperature characteristic [17].

The output of the amplifier is connected to the gates of M4 and M5. There are two branches of positive and negative feedback in the BandGap loop, and the strength of negative feedback in the circuit should be greater than the strength of positive feedback to ensure the stability of the circuit [18].

The voltage formula across the terminals of $R_1$ in Figure 5 is as follows:

$$\Delta V_{EB} = \Delta V_{EB1} - \Delta V_{EB2}$$

(9)

Hence, the current flowing through resistor $R_1$ is directly proportional to temperature. PMOS transistor M3, in conjunction with transistors M1 and M2, collectively forms a current mirror. M3 mirrors a current with two opposite temperature coefficients. By selecting the appropriate resistor ratio in the design process, a temperature-independent bandgap reference voltage is generated [19]. The pertinent derivation process is as follows:

$$I_{R2} = \frac{V_{EB1}}{R_2}$$

(10)
\[ I_{R1} = \frac{V_{EB1} - V_{EB2}}{R_1} = \frac{\Delta V_{EB}}{R_1} = V_T \frac{\ln N}{R_1} \]  
\[ I = I_{R1} + I_{R2} \]  
\( \text{(11)} \)

where \( N \) is the ratio of the number of Q2 and Q1 transistors; \( V_T = KT/q \) is a positive temperature coefficient voltage. The current flowing through resistor \( R_4 \) is equal to the current flowing through \( M3 \), so the output voltage \( V_{\text{REF}} \) of the bandgap is

\[ V_{\text{REF}} = R_4 I = R_4 \left( \frac{V_{EB1}}{R_2} + \frac{V_T \ln N}{R_1} \right) \]
\[ \text{(12)} \]

Organize the above equation into the following:

\[ V_{\text{REF}} = \frac{R_4}{R_2} \left( \frac{V_{EB1}}{R_2} + V_T \frac{\ln N}{R_1} \right) \]
\[ \text{(13)} \]

The temperature drift coefficient \( (T_c) \) is as follows:

\[ T_c = \frac{V_{\text{max}} - V_{\text{min}}}{V_{\text{mean}}(T_{\text{max}} - T_{\text{min}})} \times 10^6 \text{ ppm/}^{\circ}\text{C} \]
\[ \text{(14)} \]

In the equation, \( V_{\text{max}}, V_{\text{min}}, \) and \( V_{\text{mean}} \) represent the maximum, minimum, and mean values of the reference voltage, respectively, while \( T_{\text{max}} \) and \( T_{\text{min}} \) denote the maximum and minimum temperature variations. A smaller temperature coefficient for the bandgap implies higher precision of the reference voltage, resulting in a better stable output voltage.

### 2.2. Circuit Design of the R-2R Resistor Network

The structure of an R-2R digital-to-analog converter inherently dictates that its precision is highly contingent upon the matching of the resistor network and switch matching. In other words, the actual resistance values of the vertical resistors and cross-bridge resistors are maintained at a two-fold relationship. In practical circuitry, linear-range-working NMOS transistors are used as the switch devices, and their on-resistance is given by

\[ R_s = \frac{1}{\mu_n C_{\text{OX}}(V_{GS} - V_{TH})} \]
\[ \text{(15)} \]

where \( R_s \) is the conductive resistance of the switch. For high-precision DAC, a large number of resistors and switches are required, and the increase in the number of resistors increases the chance of resistor mismatch, leading to a decrease in DAC accuracy [20]. Figure 6 illustrates the structure of a 14-bit analog-to-digital converter utilizing the R-2R resistor network design with offset switches for conduction resistance. Assuming that the resistance value of the resistor connected to the lowest switch \( D14 \) has changed to \( 2R + 2kR \) due to process deviation, the output voltage \( V_o \) of the DAC can be expressed as

\[ V_o = V_{\text{REF}} \left( \frac{1}{2} D_1 + \frac{1}{2^2} D_2 + \cdots + \frac{1}{2^{13}} D_{13} + \frac{1}{2^{14}}(2 + k) D_{14} \right) \]
\[ \text{(16)} \]

This binary relationship is no longer established because of the switch resistance, thus reducing the resolution. All MOS switch transistors are set to the same dimensions, and the resistance values connected to the switches in the R-2R resistor network are reduced to satisfy the binary relationship. Assuming that the conduction resistance of the switches is \( R_s \), the resistance value connected should be optimized to \( 2R - R_s \), ensuring that the circuit adheres to the binary relationship [21,22].

The resistance of the lowest position of the R-2R structure is \( 2R \), and according to Equation (3), the unit resistance \( r \) can be expressed as

\[ r = \frac{R}{2} \approx 9 \text{ K} \Omega \]
\[ \text{(17)} \]
This resistor value is less affected by the wires when designing the layout, making it easier to match.

![Structure of the proposed R-2R resistor network.](image)

**Figure 6.** Structure of the proposed R-2R resistor network.

2.3. Design of the Differential Operational Amplifier

In order to guarantee the DAC with sufficient driving capability, it is essential to add an operational amplifier at the voltage output of the weighted network, serving as the output stage for the DAC [23]. Typically, it is required that the error introduced by the DC gain should be less than the LSB of a 14-bit DAC. The gain error of the amplifier is approximately $1/A_V$, where $A_V$ represents the DC gain of the amplifier. Therefore, $\frac{1}{A_V} < \frac{1}{10^4}$, $A_V > 90$ dB, taking into account the design specifications, a significant margin should be left, and the DC gain should exceed 100 dB.

The settling time comprises two components: the large-signal settling time, which is contingent upon the slew rate; and the small-signal settling time, which is associated with the bandwidth of the amplifier [24]. The required settling time is 0.5 $\mu$s or less, particularly for large signals. Thus, a prescribed slew rate is necessitated for the amplifier as follows:

$$SR > \frac{1.8V}{0.5\mu s} = 3.6 V/\mu s$$

(19)

Considering the design criteria into account, it is advisable to maintain a certain margin, and the optimal design for the slew rate should exceed 5 $V/\mu s$.

The response time of an operational amplifier is within $7\tau$ constants. The time constant is related to the unity-gain bandwidth (GBW), as follows:

$$\tau = \frac{1}{GBW}$$

(20)

Hence, the requirement is $7\tau < 0.5 \mu s$.

Thus, $GBW > 14$ MHz.

Considering the design requirement, it is advisable to retain a certain margin, and the optimal choice for the unity-gain bandwidth design is above 15 MHz. The DAC is used to provide the reference voltage to the pixel front-end of the whole matrix. The digital signals inside the pixel are very close to the front-end, which will increase the noise of the front-end because of the crosstalk. An amplifier with a large driving capability can reduce the noise of the references; thus, the amplifier still needs to have a certain driving capability.

According to the above requirements, considering the need to bias multiple pixel units, the amplifier adopts the ACBC three-stage amplifier design, with the structure shown in Figure 7 [25–27]. The first stage adopts a folded cascode structure, where M16 constitutes a buffer stage to avoid the large input capacitance affecting the operating speed of the circuit in Miller’s equivalent, the output stage adopts a class AB output, and M18 and M19 are used to control the DC bias voltage of the output stage.
Figure 7. ACBC three-stage amplifier schematic.

The circuit is modeled as shown in Figure 8, simplifying the stages into transconductance as well as load, the circuit is compensated using both feed-forward compensation as well as two-stage Miller compensation to ensure the phase margin of the amplifier [28].

Figure 8. ACBC three-stage amplifier structure.

The gain of the amplifier can be expressed as

$$A_V = \frac{g_{m1}g_{m2}g_{m3}R_1R_2R_3}{1 + s \frac{g_{m1}g_{m2}}{g_{m1}g_{m2}g_{m3}R_1R_2R_3}}$$

(21)

The transfer function of the system can be expressed as

$$A_V(s) = \frac{A \left(1 + \frac{s}{\omega d} + \frac{s^2}{\omega_1 \omega_4} + \frac{s^3}{\omega_1 \omega_4 \omega_3}\right)}{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})(1 + \frac{s}{\omega_3})}$$

(22)

where each zero pole can be expressed as

$$\omega d = -\frac{1}{g_{m1}g_{m2}g_{m3}R_1R_2R_3}$$

$$\omega_1 = \frac{1}{g_{m2}^2/g_{ma}}$$

$$\omega_2 = (g_{m2} + g_{ma}) \frac{g_{m2}}{C_L}$$

$$\omega_3 = \frac{1}{g_{ma} C_2}$$

$$\omega_4 = -(g_{m2} + g_{ma}) \frac{g_{m2}}{C_m}$$

(23)
The circuit has four poles and three zeroes. The first non-primary pole $\omega_1$ is equal to the first zero, then the effects of the zero and pole on the phase cancel each other out. The second non-primary pole can affect the phase margin, whereas when the second non-primary pole is located at twice the GBW, the phase margin can achieve 60 degrees.

3. Simulation, Layout, and Testing

3.1. Simulation

The chip is developed using the GSMC 180 nm CMOS process with a power supply voltage of 3.3 V.

3.1.1. Simulation of Bandgap Reference Circuit

The bandgap reference operates at a voltage of 3.3 V with a target output voltage of 1.8 V. It can be observed that the temperature drift coefficient is approximately 26.77 ppm/°C when the temperature varies from $-40$ °C to $85$ °C. At room temperature, the output voltage is around 1.8003 V.

The simulated curves for the reference voltage under various process corners are depicted in Figure 9. Three distinct curves correspond to the TT, SS, and FF process corners, with respective temperature drift coefficients of 26.77 ppm/°C, 33.06 ppm/°C, and 27.7 ppm/°C. Table 1 presents the specific simulation results of the bandgap reference.

![Figure 9. Simulation results of reference voltage at TT, SS, and FF process corners.](image)

**Table 1.** Specific simulation results for bandgap reference at TT, SS, and FF process corners.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT</th>
<th>SS</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>VBG max (V)</td>
<td>1.8003</td>
<td>1.8052</td>
<td>1.7965</td>
</tr>
<tr>
<td>VBG min (V)</td>
<td>1.7944</td>
<td>1.7978</td>
<td>1.7903</td>
</tr>
<tr>
<td>TCBG (ppm/°C)</td>
<td>26.77</td>
<td>33.06</td>
<td>27.7</td>
</tr>
</tbody>
</table>

3.1.2. Simulation of the Differential Amplifier

Figure 10 illustrates the gain curves of the operational amplifier. It can be observed that the simulated gain of the operational amplifier is above 130 dB for the TT, FF, and SS process corners, meeting the 14-bit DAC requirements. Table 2 displays the corner simulation results for various amplifier specifications, whereby all of the specifications are acceptable.
Table 2. Specific simulation results for amplifier reference at TT, SS, and FF process corners.

<table>
<thead>
<tr>
<th>Corner</th>
<th>TT</th>
<th>SS</th>
<th>FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain (dB)</td>
<td>130.483</td>
<td>131.105</td>
<td>131.457</td>
</tr>
<tr>
<td>GBW (MHz)</td>
<td>20.43</td>
<td>18.4</td>
<td>26.35</td>
</tr>
<tr>
<td>Phase Margin (°)</td>
<td>76.96</td>
<td>85.57</td>
<td>61.86</td>
</tr>
</tbody>
</table>

3.2. Layout and Post-Simulation

During the layout design, to reduce the mismatch, dummy resistors are used in the R-2R resistor network array [29,30]. The placement of the R-2R resistor network should strive for symmetry, wherein a parallel-then-series arrangement of multiple identical resistors is used [31,32].

The post-simulation results for DNL and INL analyses are depicted in Figure 11a,b, indicating that DNL is less than ±0.63 LSB, and INL is less than ±0.904 LSB.

Figure 11. (a) DNL analysis results for post-simulation of DAC; (b) INL analysis results for post-simulation of DAC.
3.3. Test Results

The DAC designed in this paper is fabricated using the GSMC 0.18 µm process, and the micrograph of the chip obtained after wafer fabrication is shown in Figure 12a,b.

![Micrograph of the Topmetal-CEE chip](image)

**Figure 12.** (a) Die micrograph of the Topmetal_CEE; (b) die micrograph of the DAC; (c) layout of the DAC.

The DAC is integrated within the Topmetal-CEE chip. The test system setup comprises a PC, an FPGA board, the chip test board, and an oscilloscope. The PC conveys inputs to the Topmetal-CEE chip test board through the FPGA. A full binary code scan of the DAC output voltages is performed, recording the DAC output voltages. These results are then imported into MATLAB R2020b for DNL and INL analyses, as illustrated in Figure 13a,b. The test results indicate that the designed 14-bit DAC exhibits a DNL less than ±1.07 LSB and INL less than ±1.57 LSB. Additionally, the bandgap output is 1.799 V at room temperature with a temperature coefficient of 48.25 ppm/°C.

![DNL and INL analyses](image)

**Figure 13.** (a) DNL analysis of DAC test results; (b) INL analysis of DAC test results.

Table 3 shows the parameter comparison between the DAC in this design and the related references. The DAC in this paper is designed with higher accuracy and better synthesized parameters compared to the circuits in [31,32].
4. Conclusions

To meet the stringent precision requirements for a bias voltage in the Topmetal-CEE chip, a high-precision integrated DAC is realized. In the design, a low-voltage bandgap structure is designed to enhance the stability and a high-performance buffer is used to enhance its driving capability. An R-2R resistor network with switch resistance matching is used to improve the accuracy of the DAC. The test results reveal that the DAC chip, operating at a 3.3 V power supply voltage, can realize output voltages ranging from 0 to 1.8 V. The differential non-linearity error is less than 1.07 LSB, and the integral non-linearity is less than 1.57 LSB. The test results are as expected.

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