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Fully Tunable Analog Biquadratic Filter for Low-Power Auditory Signal Processing in CMOS Technologies

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Abstract: A novel Gm-C structure of a second-order continuous-time filter is proposed that allows for the independent control of the filter's natural frequency (ω_0) and quality factor (Q). The structure consists of two capacitors and four transconductors. Two transconductors together with the capacitors form a lossless second-order circuit with tunable ω_0 . The other two transconductors form a variable gain amplifier (VGA) which realizes an adjustable loss and thereby adjustable Q . The proposed solution can be used to implement low-voltage and low-power tunable front-end filter banks for fully integrated CMOS cochlear implants and edge intelligence accelerators. An example filter bank powered by 0.5 V and consuming 40 nW of power per single filter is designed and simulated using a 180 nm CMOS process. Circuitries for the adaptive control of transistor bias at a reduced supply voltage are proposed. The ω_0 and Q control circuitries are also proposed: a delay-locked loop (DLL)-based system for fine ω_0 tuning and a binary-weighted current mirror for Q adjustment. The proposed solution allows for the independent regulation of ω_0 and Q within the ranges of 0.25–8 kHz and 1–14, respectively, with a relative tolerance of up to 5% across a filter bank.

Keywords: CMOS analog circuits; low power; low voltage; auditory; audio filters; analog integrated filters; hearing devices; edge intelligence accelerators; energy-efficient filters



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1. Introduction

The natural auditory process takes place, in simple words, in three stages: the conversion of a mechanical sound wave to an electrical signal, the decomposition of the wide sound spectrum to narrower bands, and neural processing [1]. This natural scheme is energy- and computationally efficient and is exploited in bio-inspired electronic devices such as hearing aids, cochlear prosthesis implants [2–7], and edge AI accelerators [8–14]. In these devices, the sound wave is converted to a voltage signal by a MEMS transducer and then applied to a set of band-selective filters which divide the sound spectrum into a number of adjacent channels. The channel signals are then shaped and converted into pulses that stimulate the patient's auditory nerves or drive artificial neural networks in edge devices.

The filter set, referred to as a filter bank, typically contains up to sixteen filters with different frequency and selectivity [15,16]. The parameters are set individually to each filter in a bank depending on the content and dynamics of sound, patient characteristics, etc. Commercial solutions widely use digital filters because their characteristics are practically insensitive to process, voltage, and temperature (PVT) variations. However, research on analog filter banks is still being carried out worldwide [5–7,9–14,17–24], and in recent years, several solutions have been reported with very competitive performance in terms of power consumption, e.g., [9–14]. Thus, analog filters can be energy-efficient, but their limited tunability, relatively high sensitivity to technological imperfections, and limited dynamics at low supply voltage are still a challenge for designers. A supply voltage of, e.g., 0.5–0.6 V [7,10,11,19,22] means in practice that MOS transistors are biased slightly above

the triode region. As a consequence, the transistor output resistance is reduced, which limits a filter selectivity (a filter quality factor). Thus, at low supply voltages, additional control circuits are necessary to prevent the transistors from entering the triode region. The tunability problem is related to the fact that known topologies of continuous-time filters [23] feature a not fully independent (separated) control of the filter frequency and quality factor [24]. This fact complicates the tuning of a whole filter bank and makes it more difficult to control the filter characteristics under PVT variations.

The continuous-time filter presented in this paper addresses the requirements of full tunability and low-voltage operation. The solution exploits the new proposed G_m -C schematic of a biquadratic filter with the separate control of the natural frequency (ω_0) and quality (Q) factor. The following sections present the concept, theoretical analysis, transistor-level schematic, and simulation results of the filter designed in the X-Fab 180 nm CMOS process, together with a DLL-based frequency tuning system and circuits controlling the bias and threshold voltage of transistors. An example filter bank is also presented.

2. Filter

Figure 1a shows the G_m -C topology of the proposed filter. The transconductance amplifiers G_{m1} and G_{m2} together with the capacitors C_1 and C_2 are a second-order, lowpass, and lossless circuit with a natural (resonance) frequency ω_0 [24]. The loss is introduced to the circuit by a negative feedback loop established on the transconductors G_{m3} and G_{m4} .

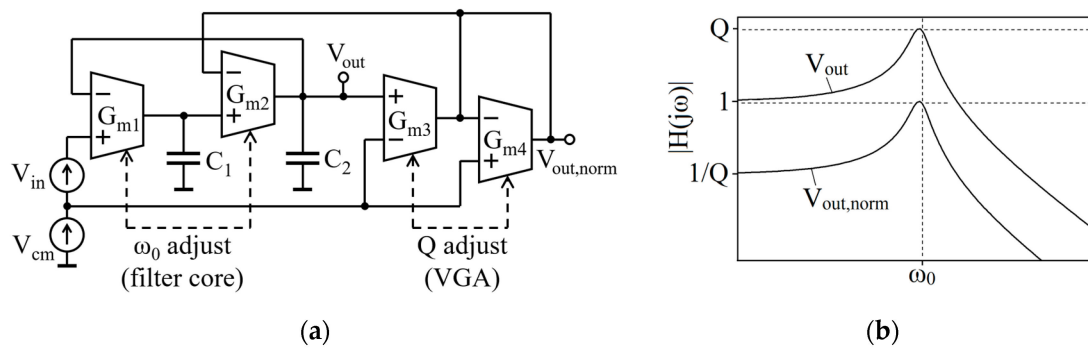


Figure 1. Proposed lowpass filter: (a) G_m -C topology; (b) typical amplitude characteristic (the vertical scale is logarithmic).

The input AC voltage V_{in} is applied to the filter with respect to a common (DC) potential V_{cm} . The filter's main output terminal is V_{out} . The filter's AC transmittance is

$$H(j\omega) = \frac{V_{out}(j\omega)}{V_{in}(j\omega)} = \frac{\omega_0^2}{-\omega^2 + j\omega\frac{\omega_0}{Q} + \omega_0^2} \quad (1)$$

where

$$\omega_0 = \sqrt{\frac{G_{m1}G_{m2}}{C_1C_2}}, \quad Q = \frac{G_{m4}}{G_{m3}} \cdot \sqrt{\frac{G_{m1}C_2}{G_{m2}C_1}} \quad (2)$$

To simplify the filter design, G_{m1} and G_{m2} as well as C_1 and C_2 can be assumed to be equal, i.e., $G_{m1} = G_{m2} = G_{m1,2}$, and $C_1 = C_2 = C_{1,2}$. With these assumptions, (2) simplifies to

$$\omega_0 = \frac{G_{m1,2}}{C_{1,2}}, \quad Q = \frac{G_{m4}}{G_{m3}} \quad (3)$$

The CMOS realization of the G_m -C structure is shown in Figure 2a. The transconductors have an identical topology composed of a differential pair (M_1 , M_2) loaded with a current mirror (M_3 , M_4). The consecutive differential pairs are biased with the currents I_{B1} to I_{B4} generated by the transistors M_{B1} to M_{B4} . The transistors M_5 , M_6 , and additional

capacitors of 20 pF over M_5 compose the DC voltage shifters to increase the drain-source voltage of the M_2 transistors [23].

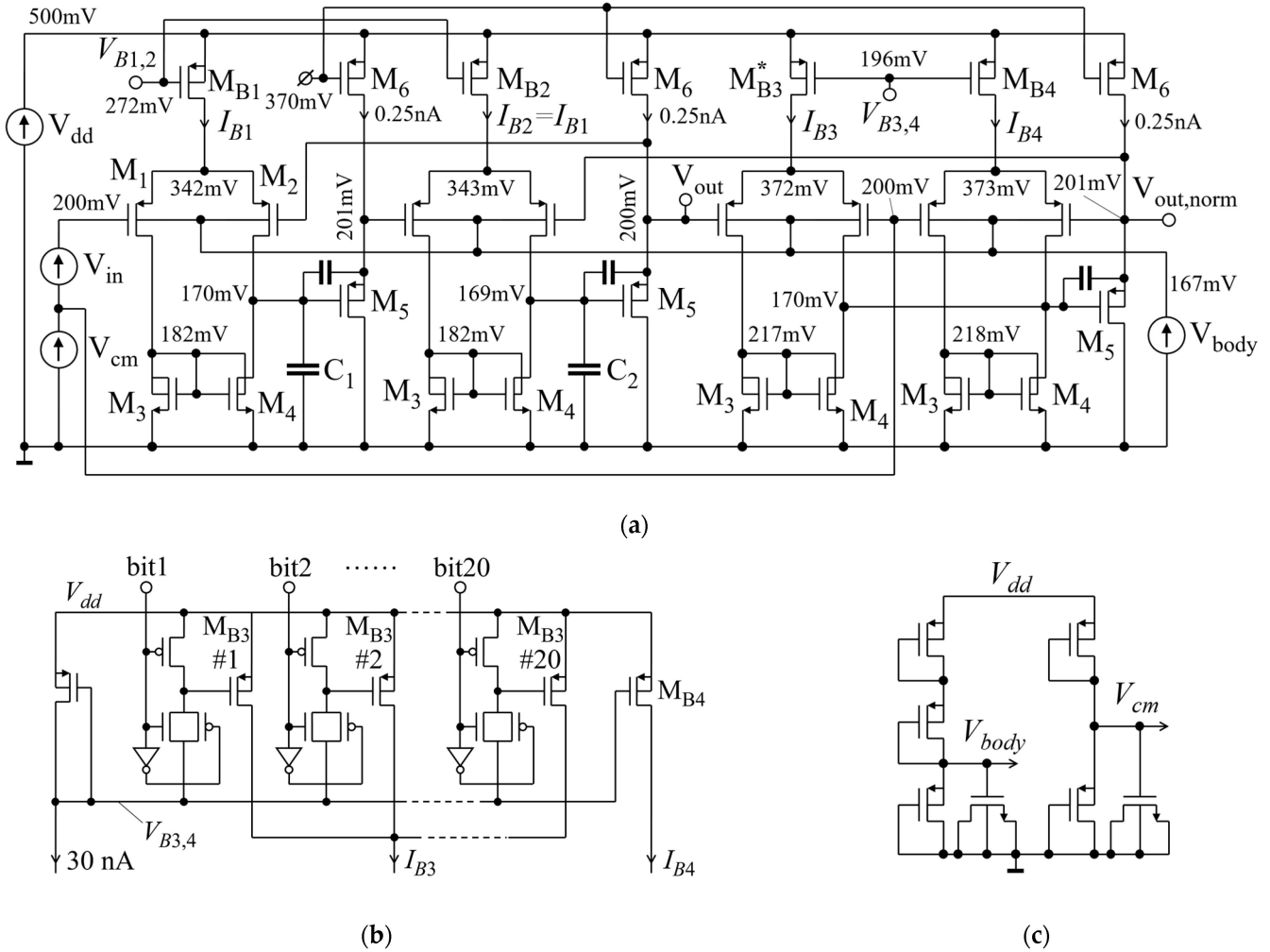


Figure 2. The CMOS realization of the filter: (a) electrical diagram; (b) programmable current mirror generating I_{B3} and I_{B4} ; and (c) the generator of V_{cm} and V_{body} . The node voltage values are with $I_{B1} = I_{B2} = 10 \text{ nA}$, $I_{B3} = I_{B4} = 30 \text{ nA}$, and temperature 27°C .

The transconductance of the i -th ($i = 1 \dots 4$) transconductor, G_{mi} , is equal to the transconductance of the transistors M_1 and M_2 ($g_{m1} = g_{m2} = g_{m1,2}$) in the respective differential pair, i.e., $G_{mi} = (g_{m1,2})_i$. M_1 and M_2 operate in saturation and weak inversion regions; thus,

$$G_{mi} = (g_{m1,2})_i \cong \frac{I_{Bi}}{2nV_t} \quad (4)$$

where $i = 1 \dots 4$, $V_t = kT/q$ is the thermal voltage, and n is a technology-dependent parameter [21,22].

The bias currents I_{B1} and I_{B2} are equal ($I_{B1} = I_{B2} = I_{B1,2}$), so the natural frequency and quality factor of the filter can be expressed as follows

$$\omega_0 = \frac{G_{m1,2}}{C_{1,2}} \cong \frac{I_{B1,2}}{2nV_t C_{1,2}}, \quad Q = \frac{G_{m4}}{G_{m3}} \cong \frac{I_{B4}}{I_{B3}} \quad (5)$$

As indicated by (5), Q is determined by the ratio of the bias currents I_{B4} and I_{B3} . Therefore, Q can be adjusted by means of a scalable (programmable) current mirror shown in Figure 2b where a current ratio, once programmed, does not change with PVT. However,

ω_0 depends on the absolute values of the parameters $I_{B1,2}$, n , and V_t , so it varies with process and temperature, and thus, a tuning system based on a PLL or DLL is necessary.

It is worth noting that the filter operates in a unity gain buffer configuration [25]. The filter is covered with a global negative feedback loop (established by connecting a V_{out} terminal to an inverting input of the amplifier G_{m1}), which forces V_{out} to follow V_{in} at low frequencies. As a result, the filter gain at low frequencies is 1 V/V regardless of mismatch and PVT variations. Note also that at the additional output, $V_{out,norm}$, the filter peak gain is unity, as the graph in Figure 1b shows.

The detailed data on the transistor sizes and bias conditions are given in Table 1.

Table 1. DC operating point simulated at the following: $V_{dd} = 0.5$ V, $V_{cm} = 0.4V_{dd}$, $V_{body} = V_{dd}/3$, $I_{B1} = I_{B2} = 10$ nA, $I_{B3} = I_{B4} = 30$ nA, and $T = 27$ °C. Nominal corner.

Transistor ¹	Size [$\mu\text{m}/\mu\text{m}$]	I_{DS} [nA]	g_m [nS]	$ V_{DS} $ [mV]	$ V_{DSsat} $ [mV]
M1	$2 \times 10/2$	5 (20 ²)	154 (425 ²)	160 (155 ²)	47 (47.5 ²)
M2	$2 \times 10/2$	5 (20 ²)	154 (425 ²)	172 (202 ²)	47 (47.5 ²)
M3	1/2	5 (20 ²)	129 (342 ²)	182 (217 ²)	35 (37 ²)
M4	1/2	5 (20 ²)	129 (342 ²)	170 (170 ²)	35 (37 ²)
M5	40/0.5	0.25	8.5	200	44
M6	10/6	0.25	8.2	200	48
MB1,2	$2 \times 10/4$	10	282	157	49
MB3*	$20 \times 1/4$	30	740	128	47.5
MB4	$20 \times 1/4$	30	740	127	47.5

¹ The nominal threshold voltages of the transistors are $V_{Th} = 0.34$ V and $V_{Tp} = -0.39$ V. ² In the transconductors G_{m3} and G_{m4} .

2.1. Effect of Reduced Resistance

With a V_{dd} of 0.5 V, the transistor drain-source voltages (V_{DS}) are significantly reduced, so they are only slightly above saturation voltages (V_{DSsat}). According to detailed data in Table 1, the saturation margin $|V_{DS}| - |V_{DSsat}|$ is 80–150 mV across all transistors. The low V_{DS} voltages result in the reduced output resistance (r_{ds}) of the transistors. E.g., the output resistance of M_2 is $r_{ds2} = 980$ M Ω at $V_{DS} = 170$ mV and would be 1.5 G Ω when assuming $V_{DS} = 270$ mV. The reduced transistor resistance causes the actual Q value to be smaller than its ideal value given by (3).

Including the output resistances, the actual ω_0 and Q are

$$\omega_0 = \frac{G_{m1,2}}{C_{1,2}} \sqrt{1 + \frac{k}{G_{m1,2}R_{o1,2}} + \left(\frac{1}{G_{m1,2}R_{o1,2}}\right)^2} \cong \frac{G_{m1,2}}{C_{1,2}} \quad (6)$$

$$Q = \frac{1}{\frac{2}{G_{m1,2}R_{o1,2}} + k} \sqrt{1 + \frac{k}{G_{m1,2}R_{o1,2}} + \left(\frac{1}{G_{m1,2}R_{o1,2}}\right)^2} \cong \frac{1}{\frac{2}{G_{m1,2}R_{o1,2}} + k} \quad (7)$$

where $R_{o1,2} = R_{o1} = R_{o2} = r_{ds2} \parallel r_{ds4}$ is the output resistance of the transconductors G_{m1} and G_{m2} , and k is the voltage gain of the VGA,

$$k = \frac{V_{out,norm}}{V_{out}} = \frac{G_{m3}}{G_{m4} + 1/R_{o3} + 1/R_{o4}} \quad (8)$$

Since the transconductor's gain ($G_{m1,2}R_{o1,2}$) remains approximately constant and equal to $G_{m1,2}R_{o1,2} \approx 100$ over a wide range of $I_{B1,2}$, the actual ω_0 is practically equal to its ideal value (3), as indicated by (6). On the other hand, the finite $G_{m1,2}R_{o1,2} \approx 100$ reduces Q by 10–30% with respect to its ideal value (3), i.e., $Q_{actual} = 0.7(G_{m4}/G_{m3})$ for high Q values, and $Q_{actual} = 0.9(G_{m4}/G_{m3})$ for low Q . Figure 3 presents the simulated filter characteristics where $I_{B1,2}$ is set to 5, 10, and 20 nA (the ω_0 adjustment), and I_{B4}/I_{B3} is programmed as 2, 4, 10, and 20 (the Q adjustment). The resulting Q values are reduced by 15–35% with respect

to the I_{B4}/I_{B3} ratios, which is caused by the reduced resistances, as mentioned, and in addition by the inequality $G_{m4}/G_{m3} \cong I_{B4}/I_{B3}$. However, the Q values are well repeatable at different ω_0 .

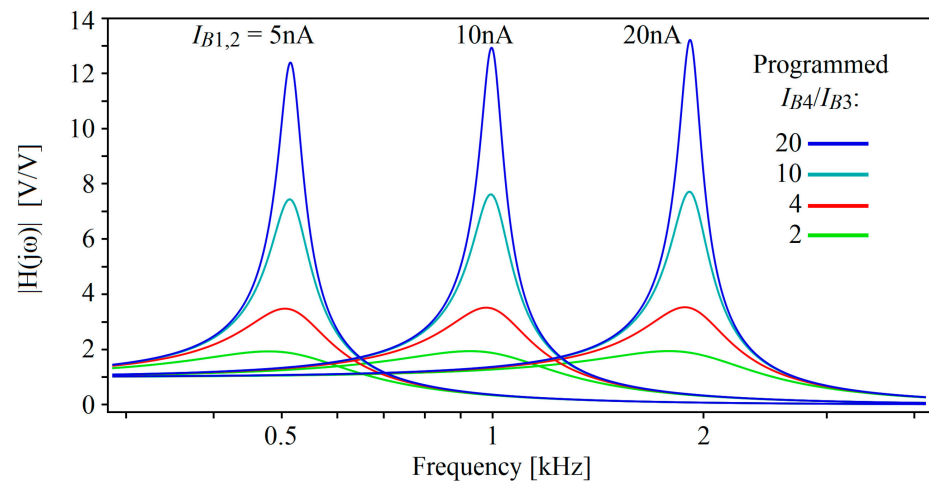


Figure 3. Simulation of ω_0 and Q adjustments. Nominal corner. $C_{1,2} = 24$ pF. $T = 27$ °C.

2.2. Bias and Threshold Voltage Control

Due to the low supply voltage, the threshold voltages of the selected transistors are reduced using the body effect. Thus, the bodies of the n-channel devices (M_3 , M_4) are connected to the higher potentials at their gates (n-channel transistors on insulated p-wells, available in the X-Fab process, are used). The bodies of the p-channel pairs (M_1 , M_2) are connected to the low reference potential V_{body} . The V_{body} is regulated depending on the supply voltages V_{dd} to prevent the forward biasing of the body-source (p-n) junctions in M_1 and M_2 . The common potential V_{cm} is also regulated so that the transistor drain-source voltages (V_{DS}) are maximized. The simple and effective control scheme with $V_{body} = V_{dd}/3$ and $V_{cm} = 0.4 \cdot V_{dd}$ is used in this design. The V_{cm} and V_{body} are generated by the active dividers, shown in Figure 2c, that have simple topology and are immune to PVT variations. With this adaptive bias, the transistors are kept in saturation for a wide range of V_{dd} , from 1.8 V down to 0.4 V. Unfortunately, the simple dividers in Figure 2c transmit AC noise from the V_{dd} line to the V_{body} and V_{cm} lines, which reduces the power supply rejection ratio (PSRR) of the entire filter. However, additional grounded capacitors connected to the V_{body} and V_{cm} lines effectively reduce the V_{dd} noise. Simulations show that the additional capacitors of about 25 pF result in a PSRR of 72 dB and 51 dB at 10 Hz and 1 kHz, respectively (the mismatch of the differential pairs and current mirrors was included in the PSRR simulations). The grounded capacitors can be made from n-channel transistors, as shown in Figure 2c.

3. Frequency Tuning System

Due to PVT variations, continuous-time filters require an automatic frequency tuning system. The most common way to tune Gm-C filters is through a master-slave structure [26–30]. This approach requires a good match between master and slave circuits. To achieve the best match, the proposed tuning system, shown in Figure 4, uses a copy of one of the filters from the filter bank as the master circuit.

The system in Figure 4 is a typical delay-locked loop which utilizes the fact that biquadratic lowpass filters have a phase shift of -90° ($-\pi/2$) at ω_0 . Thus, the reference sine signal (V_{gen}) with a frequency of ω_{gen} is transmitted along two paths: the reference and filter paths. If the signal after passing through the (master) filter is delayed exactly by 90° with respect to the reference path, this means that the natural frequency of the (master) filter is equal to the reference frequency, i.e., $\omega_0 = \omega_{gen}$. If the 90° shift remains constant, then the XOR gate generates a square wave with a constant duty cycle of exactly 50%. As a

result, the charge pump equally charges and discharges its capacitor, and consequently, a voltage on the tuning signal line remains constant.

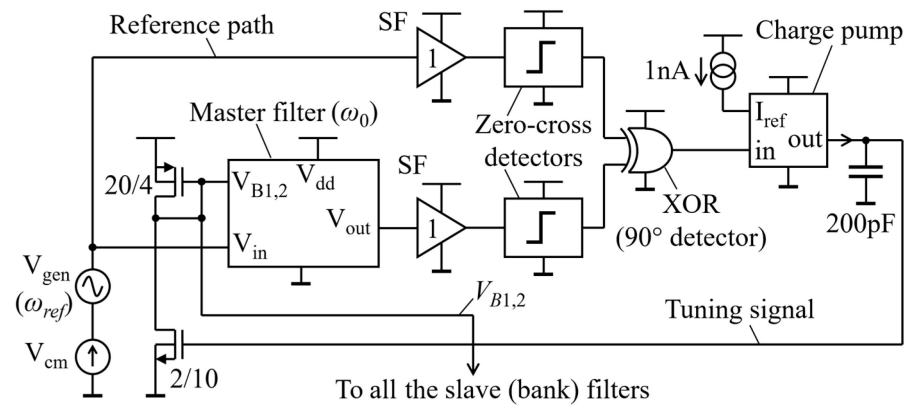


Figure 4. DLL-based tuning system.

The amplitude of the input reference sine is limited by the dynamics of the filter and is $V_{gen} = 20\text{--}50\text{ mV}_{pp}$ for the filter with $Q = 1$ and $V_{dd} = 0.5\text{ V}$. The phase detector, based on a simple digital XOR gate, requires high amplitude signals. Therefore, weak sine signals are amplified by the zero-cross detectors, which convert them to square waves with a rail-to-rail amplitude. The correct system operation requires the cross-detectors to be insensitive to the DC levels at their inputs. Thus, a solution with a decoupling capacitor is used [29], whose schematic is shown in Figure 5a. Other sub-blocks of the tuning system are depicted in Figure 5b–d.

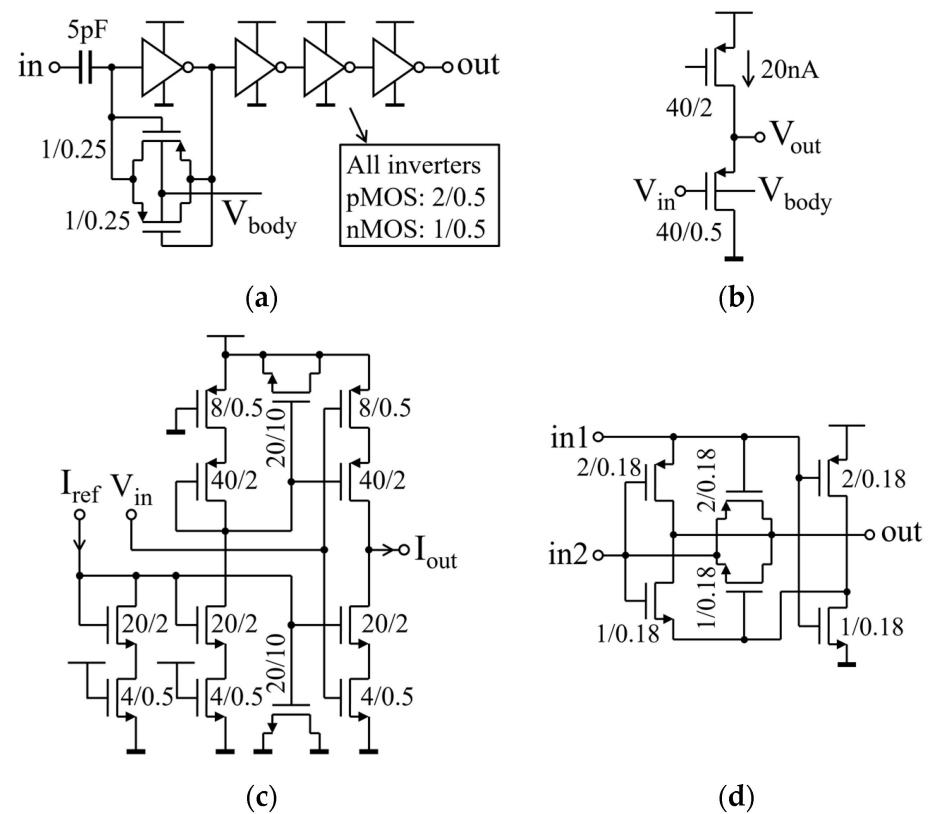


Figure 5. The sub-circuits of the tuning system: (a) zero-cross detector; (b) source follower (SF); (c) charge pump; and (d) XOR gate. The transistor body terminals not shown are connected to the V_{dd} (PMOS) and ground (NMOS) potentials, respectively.

The source followers (SFs) use p-channel transistors biased with 20 nA currents (Figure 5b). The SFs have their threshold voltages reduced by means of the body effect (V_{body}), resulting in a gain that is not unity. However, both SFs are identical, and therefore, their non-unity gain does not affect the phase shift detection process. The charge pump (Figure 5c) is a bidirectional current source (I_{out}) controlled by voltage (V_{in}). Thus, $I_{out} = I_{ref}$ at $V_{in} = L$ (low state), and $I_{out} = -I_{ref}$ at $V_{in} = H$ (high state). Additional capacitors, made of transistors 20 μm wide and 10 μm long (20/10), reduce glitches in the output current caused by commutation. The XOR gate (Figure 5d) is a traditional low-voltage solution with a transmission gate. The transistor body terminals not shown explicitly in the schematics in Figure 5a–d are connected to the V_{dd} and ground potentials for the p- and n-channel transistors, respectively.

All sub-blocks of the tuning system, including the master filter, operate with the same supply voltage, $V_{dd} = 0.5$ V. Assuming an external reference generator, the power consumption of the tuning system is 80 nW, and the occupied silicon area is smaller than two filters in a filter bank.

The master filter is the filter of Figure 2 with $C_{1,2} = 24$ pF and $Q = 1$. In the ideal case, i.e., no PVT variations, the natural frequency of the master filter is $\omega_0 = 1$ kHz at $I_{B1,2} = 10$ nA and $T = 27$ °C, as shown in Figure 3. Under PVT variations, the ω_0 changes substantially, from about 400 Hz to 1.2 kHz (changes in the filter quality factor are negligible), as shown in Figure 6a where the following variations are assumed: (P)rocess across five typical corners, supply (V)voltage from 450 to 550 mV, and (T)emperature from 0 to 50 °C. The tuning system with $\omega_{gen} = 1$ kHz effectively stabilizes the filter characteristics. The resulting ω_0 deviates by $\pm 2\%$ from 1 kHz, as visible in Figure 6b (note that the tuning system is also under PVT variations).

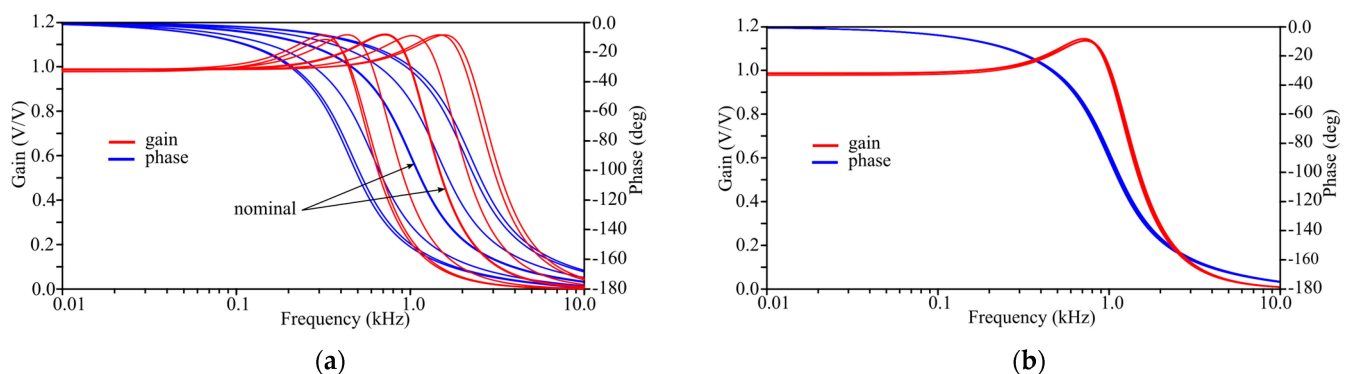


Figure 6. The master filter characteristics simulated under PVT variations: (a) without tuning and (b) with the tuning system. The process variation is simulated in 5 corners: tm, wp, ws, wo, and wz. (Supply) Voltage variation: $0.5 \text{ V} \pm 50 \text{ mV}$. Temperature variation: 0, 27, and 50 °C.

4. Filter Bank

Table 2 shows an example of 16 filters scaled from 250 Hz to 8 kHz.

Table 2. Filter bank example.

ω_0 (Hz)	254	320	403	508	640	806	1015	1280	1612	2031	2560	3225	4063	5120	6450	8127
$I_{B1,2}$	10 nA															
$C_{1,2}$ (pF)	94.19	74.56	59.17	46.97	37.28	29.58	23.48	18.64	14.79	11.74	9.32	7.39	5.87	4.66	3.69	2.93
Power	16.40 nW at $Q = 1$ ($I_{B3} = 30 \text{ nA}$, $I_{B4} = 30 \text{ nA}$) 16.27 nW at $Q = 10$ ($I_{B3} = 3 \text{ nA}$, $I_{B4} = 30 \text{ nA}$)															

The bias current $I_{B1,2}$ can be the same for all channels, which simplifies the biasing, scaling, and tuning of the entire bank. The frequencies of the individual channels are then obtained simply by scaling the capacitance $C_{1,2}$. Thanks to this, relations between the

channels' frequencies are relatively lowly sensitive to PVT variations. Mismatch, though, affects the bank characteristics, as shown in Figure 7 (for better visualization, six filters selected of the sixteen are plotted). The 1-sigma spreads in ω_0 and Q are 2.2% and 4.4%, respectively, across the entire bank.

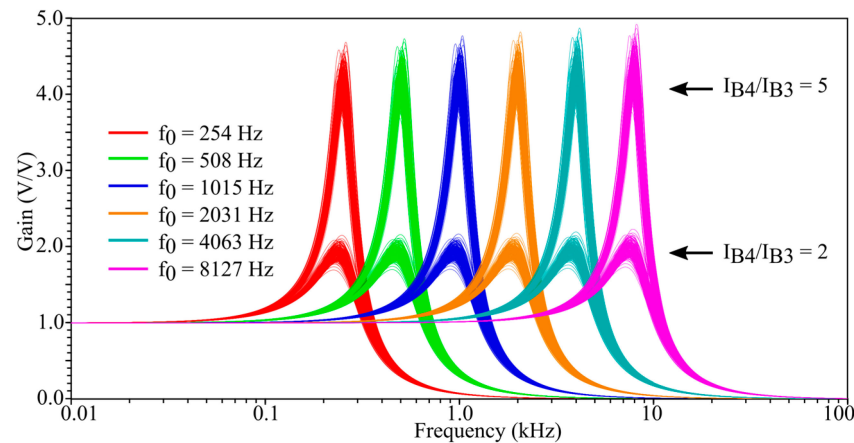


Figure 7. The filter bank simulated under mismatch (500 Monte Carlo runs).

The power consumption of the whole bank depends on the programmed value of Q . Assuming the same Q in all channels, the 16-filter bank consumes $16 \cdot 27 = 432$ nW at $Q = 10$ and $16 \cdot 40 = 640$ nW at $Q = 1$. The lower power consumption can be achieved by reducing the filter bias currents. Unfortunately, lower currents mean larger mismatches between transistor transconductances [31,32] and thus greater spreads in ω_0 and Q .

The typical noise of the individual filter is 18–33 μV_{RMS} , when referred to the filter input and integrated over the filter band. The total harmonic distortion (THD) parameter is 1% with the input sine excitation with an amplitude of 72 mV_{RMS} and a frequency of $\omega_0/5$. The 1 dB input-referred compression point is -13.82 dBm (45.5 mV_{RMS}) with the excitation at a frequency close to ω_0 . Thus, the filter dynamics are 66 dB and 62 dB regarding the 1% THD and 1 dB compression point, respectively.

The silicon area occupied by the filters is determined by the area of their capacitors [22,24,25]. E.g., the filter with $\omega_0 = 1.015$ kHz contains two capacitors of 23.48 pF and additionally, three capacitors at M_5 transistors of 20 pF, each. Assuming typical double MIM capacitors of $2.2 \text{ fF}/\mu\text{m}^2$, the filter area is $48,500 \mu\text{m}^2$ ($221 \mu\text{m} \times 221 \mu\text{m}$). However, using triple-high-capacitance MIMs of $7 \text{ fF}/\mu\text{m}^2$, also available in the X-Fab process, the filter area reduces threefold, to $15,300 \mu\text{m}^2$ ($124 \mu\text{m} \times 124 \mu\text{m}$).

5. Discussion

Table 3 presents a brief review of the continuous-time filters for auditory and edge devices, published across the last decade. Edge devices typically need filters with a constant Q parameter of low value, e.g., $Q = 1.3$ [19] or $Q = 2$ [10,11,20]. Filters with a fixed Q can have simplified, transistorized topology and therefore consume relatively low power, even several nanowatts per a whole filter bank [11]. On the other hand, cochlear implants require filters with precisely controlled frequency, bandwidth, and gain, due to individual patient characteristics [5,7,17,22]. Thus, cochlea-intended filters have more complicated topology and higher power consumption compared to edge filters.

Table 3. Continuous-time filter banks published in the last ten years.

Parameter	2014, [17]	2016, [19]	2016, [7]	2017, [20]	2019, [10]	2021, [11]	2021, [5]	2024, [22]	This Work (Simulated)
Application	cochlea	edge	cochlea	edge	edge	edge	cochlea	cochlea	cochlea
Process, nm	350	90	180	350	180	65	180	180	180
Supply, V	3.3	0.5	0.5	2.5	0.6	0.6	1.0	0.5	0.5
Filter type	LPF	BPF	BPF	BPF	BPF	BPF	BPF	LPF	LPF
Bank	OTA-C	OTA-C	SF-based	OTA-C	SSF-based	FVF-based	OTA-C	Buffer-based	OTA-C
Range, kHz	64	16	64	12	16	16	12 ¹	5 ²	16
Q	0.1–20	0.075–5	0.008–20	0.1–5	0.1–5	0.1–5	0.085–6.5	0.5–8	0.3–10
Bank power consumpt.	5-bit control	1.3	1.3–39	2	2	2	1–3.7	2–11	1–14
S/N, dB	mW-range	0.3 nW @75 Hz 20 nW @5 kHz	<55/2 μ W	150 μ W	61.3 nW	14 nW	13.2 nW @950 Hz	2.2–52 nW @1 kHz	640 nW @Q = 1 432 nW @Q = 10
	36–52	40–45	40–55	-	55	-	52	59	62

¹ The simulation results from [6]. ² Simulated.

The filter proposed in this work consumes less power than the other cochlea-dedicated filters [5,7,17,22] but still more compared to the simple filters in the edge accelerators [10,11,19,20]. Most of the filter power (75%) is dissipated in the VGA used to adjust Q . Assuming a fixed Q , e.g., 2, the VGA is not needed, and thus, the power of the filter bank can be reduced from 640 nW to 170 nW.

To reduce power consumption, supply voltages of filter banks are reduced when compared to the nominal voltages specified for the CMOS processes in which the filter banks were made. E.g., the filter bank of [20] was developed in a 3.3 V process and is supplied with a 2.5 V voltage. Similarly, the filters developed in 1.8 V processes operate at a supply voltage reduced to 1 V [5], 0.6 V [10], and 0.5 V [7,22], [this work]. Also, the works [19] and [11], made in 1 V processes, use 0.5 and 0.6 V supplies, respectively. In this regard, a typical practical limit of an analog filter supply voltage is about 0.5 V considering many CMOS processes. This practical limit applies to the analog continuous-time filters as well as discrete-time, switched-capacitor ones [12–14] (not included in Table 3). A further reduction in a supply voltage is, however, possible through a further reduction in transistor threshold voltages, to below 200 mV. Unfortunately, a significant increase in mismatch and noise is observed at such low threshold voltages, so more sophisticated bias control and tuning systems, based on digital circuits, are required.

6. Conclusions

The novel transconductance-C structure of a lowpass second-order filter with the separate control of the natural frequency and quality factor was proposed. The feasibility of implementing the proposed filter structure in 180 nm X-Fab CMOS technology at a significantly reduced supply voltage was investigated. The advantage of this technology, i.e., the ability to control the body potentials of both p-channel and n-channel transistors (and thus the ability to reduce and control the threshold voltages in both types of transistors), was exploited in order to achieve an optimal operating point at a 0.5 V supply. The impacts of the supply voltage noise, temperature changes, and technological imperfections on the filter's performance were carefully analyzed. A low-voltage tuning system with a phase detector to stabilize the filter natural frequency was also proposed.

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