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A Novel SiC Vertical Planar MOSFET Design and Optimization for Improved Switching Performance

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Abstract: A novel cell topology for a vertical 1200 V SiC planar double-implanted MOSFET (DMOSFET) is proposed in this work. Based on the conventional linear cell topology and the calibrated two-dimensional (2D) technology computer-aided design (TCAD) model parameters, a novel cell topology with the insertion of P+ body implanted regions over a fractional part of the channel and junction field effect transistor (JFET) regions was designed and optimized to achieve a low high-frequency figure of merit (HF-FOM, $R_{on} \times C_{gd}$). Utilizing three-dimensional (3D) TCAD simulations, the new proposed cell topology with optimized selected structure parameters exhibits an HF-FOM of 328.748 mΩ·pF, which is 10.02% lower than the conventional linear topology. It also shows an improvement in the switching performance, with an 11.73% reduction in switching loss. Moreover, the impact of source ohmic contact resistivity on the performance of the proposed cell topology was highlighted, indicating the dependency of the source ohmic contact resistivity on the switching performance. This research provides a new perspective for enhancing the switching performance of SiC MOSFETs in high-frequency applications, considering practical factors such as contact resistivity.

Keywords: SiC MOSFET; TCAD; HF-FOM; switching performance

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1. Introduction

Silicon carbide (SiC) is a type of wide-bandgap semiconductor that has a high breakdown electric field, high electron drift velocity, and high thermal conductivity [1–3]. Thus, it makes SiC a promising semiconductor material for use as a power device with great potential in high-power, high-temperature, and high-frequency applications [4,5]. The use of a SiC power device as a rectifier/switch in the power module of an EV charger has been widely accepted and realized for fast and super-fast DC/DC charging piles [6–8].

Currently, in terms of the SiC power switch MOSFET devices on the market, they take the form of vertical planar gate and trench gate MOSFETs with a voltage rating ranging from 30 V to 3300 V. Between the two forms of MOSFET structure, the vertical planar gate double-implanted MOSFET (DMOSFET) structure is the first commercialized one and still the dominant SiC MOSFET structure on the market. Figure 1 shows the principal structure of a conventional vertical planar double-implanted MOSFET (DMOSFET) structure. As can be seen in Figure 1, the presence of the junction field effect transistor (JFET) region and the planar gate poses the limitation of scaling down the device pitch of a planar gate MOSFET [9]. The device pitch directly affects the total width of the device given per area. Thus, it translates to current density and on-resistance (R_{on}) at a specific breakdown

voltage (BV) and in a specific active area. This is particularly relevant to the key requirements for high-power level AC/DC converter applications, especially for DC/DC EV fast charging stations, which demand high power density, efficiency, and reliability. This raises a technical challenge in developing a SiC MOSFET power switch that has low static and dynamic losses to meet the requirements of high-frequency switching operations, thereby achieving greater power and efficiency in smaller and more reliable solutions.

As a vertical structure in which the conducting electron current flows vertically from top to bottom, the width layout topology is another dimensional aspect in optimizing device performance parameters. The arrangement of the width layout in stripe, square, hexagonal, octagonal, and graphene configuration cells determines the R_{on} , BV, and reverse transfer capacitance/gate-drain capacitance (C_{rss}/C_{gd}) of a particular vertical device [10–12].

The two-dimensional (2D) technology computer-aided design (TCAD) simulation is widely used in device design prediction, process flow, optimization, and characterization [13,14]. For the width layout cell topology to have variation along the z-direction plane requires three-dimensional (3D) simulation in predicting the impact of geometry effects on the current flow [15].

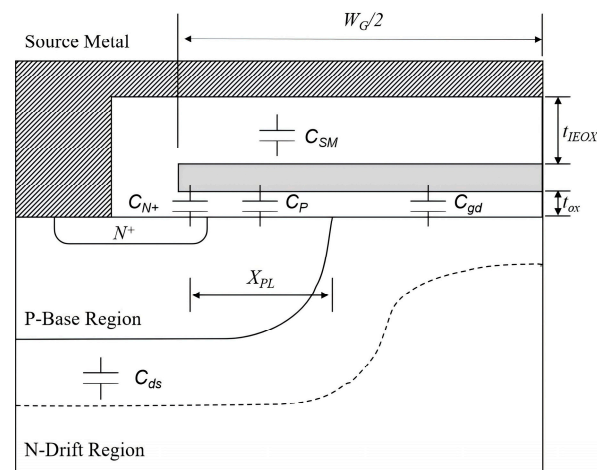


Figure 1. Schematic cross section of vertical planar DMOSFET structure.

Various cell topologies, including linear, square, hexagonal, and octagonal structures, have been evaluated and optimized for vertical planar MOSFETs in previous studies [10,11,16–18].

Hower et al. [16], through cell geometry analysis, compare the optimized source-gate geometry dimensions of hexagonal, rectangle, and triangle cells. They conclude that no particular MOSFET geometry has a major advantage with regards to minimizing R_{on} . Since the study is based on the optimization of source-gate geometries without considering applied design rules, it also concludes that other factors, such as source contact resistance, the reduction of parasitic bipolar effects, and the effects of 3D current flow, need to be considered, as they will influence the choice of cell geometry.

Zhu et al. [10], through analytical calculation, derive the breakdown resistance path of vertical planar MOSFET (epitaxial layer, JFET, accumulation layer, channel) with respect to cell geometry. They report a similar conclusion to [16], that essentially the same minimum R_{on} can be achieved using any of six different cellular cell geometries (square well in a square cell, circle in a square cell, hexagon in a square cell, square in a hexagonal cell, circle in a hexagonal cell, and hexagon in a hexagonal cell). In particular, the on-resistance of all cellular designs is identical if the P-well width and the ratio of well area to cell area are the same.

Liu et al. [17] compare the impact of various cell geometries (linear, orthogonal short, atomic lattice layout (ALL), and cylindrical circular) of 1200 V SiC power MOSFETs on

switching loss by numerical simulation. Using mixed device/circuit modeling, the various cell geometries are optimized for zero-energy turn-off and minimum on-state loss. They conclude that all studied cell designs are capable of near-zero-energy turn-off with appropriate gate drive circuitry. Zero turn-on loss, however, is not achievable. Turn-off losses are smaller over a larger range of gate drive resistances for designs optimized to minimize the $R_{on} \times Q_{gd}$ figure of merit rather than $R_{on,sp}$. For the $R_{on} \times Q_{gd}$ optimized case, the ALL and orthogonal short cells achieve the largest zero-energy turn-off window.

Agarwal et al. [11] compare the measured electrical characteristics of 600 V vertical planar inversion 4H-SiC MOSFETs fabricated with different cell topologies (linear, square, hexagonal, and octagonal). For this comparison study, all the cell topologies are fabricated with the same JFET width, channel length, and active size in the same process flow. Experimental electrical measurement indicates that the square and hexagonal cells have the lowest R_{on} due to the highest channel and JFET density but have a BV below the 600 V rating due to the presence of sharp corners. The octagonal cell has excellent BV with superior C_{rss} and Q_{gd} but higher R_{on} due to its smaller JFET density.

Han et al. [18] compare four fabricated cell topologies (linear, square, hexagonal, and octagonal) of 1200 V accumulation and the inversion channel 4H-SiC with the same design rules and process flow. It is observed that the square and hexagonal cell topologies with the same structural dimensions show similar electrical performance. It is also observed that the JFET spacing design impacts the breakdown of the square and hexagonal cells. For the same JFET spacing of 1.1 μm between the square and hexagonal cells, the square cell shows a drop of 2.5% compared to the hexagonal cell. And for the same JFET spacing of 0.7 μm between the linear and hexagonal cells, the hexagonal cell shows a drop of 1.8% compared to the linear cell. This is due to localized high electric field concentration at the corners of the square and hexagonal cells [19].

In view of all the past publications on the impacts of design and cell topology, whether through optimization, comparison of design rules, or fabrication flows, there is no significant absolute advantage of one topology over another in terms of R_{on} and C_{rss}/C_{gd} . Furthermore, there has been no true evaluation of optimization from a genuine 3D simulation perspective.

Based on the calibrated 2D TCAD model parameters on the fabricated 1200 V-80 m Ω planar DMOSFET with linear topology design, this work proposes a new cell topology of the planar gate DMOSFET. Using true 3D TCAD simulation, a new topology has been designed with additional P+ implanted regions over a fractional part of the channel and JFET regions. This design was optimized to achieve the lowest high-frequency figure of merit (HFOM, $R_{on} \times C_{gd}$) [20]. Consequently, the switching performance as compared to the conventional linear topology structure also showed a much reduced switching loss. The improved switching performance mostly benefits applications in which switching losses are dominant over conductance losses and in which switching and conductance losses are equally distributed. In addition, the impact of source ohmic contact resistivity dependency on the switching performance of the new proposed cell topology was also highlighted.

2. Scope of the Topology Design

There are three main parasitic capacitances between the three electrodes of SiC MOSFET, gate-source capacitance (C_{gs}), gate-drain capacitance (C_{gd}), and drain-source capacitance (C_{ds}). Referring to Figure 1, it can be seen that the parasitic capacitance C_{gs} is composed of C_{N+} , C_P , and C_{SM} connected in parallel [21]. C_{N+} is the capacitance where the gate electrode overlaps with the source region. C_P is the capacitance where the gate electrode overlaps with the P-base region. C_{SM} is the capacitance where the gate electrode overlaps with source metal. The calculation of specific gate capacitance for the power DMOSFET structure is as follows:

$$C_{gs,sp} = C_{N+} + C_P + C_{SM} = \frac{2X_{PL}}{W_{cell}} \left(\frac{\epsilon_{OX}}{t_{OX}} \right) + \frac{W_G}{W_{cell}} \left(\frac{\epsilon_{OX}}{t_{IEOX}} \right) \quad (1)$$

where ϵ_{OX} is the dielectric constant of the oxide layer, t_{OX} is the thickness of the gate oxide layer, t_{IEOX} is the thickness of the inter-electrode oxide layer, and X_{PL} is the width of the overlap between the gate and P-base region.

The gate-drain capacitance C_{gd} is determined by the series connection of the capacitance of the SiO₂ layer and the capacitance of the depletion layer below. The calculation of specific gate-drain capacitance for the power DMOSFET structure is as follows:

$$C_{gd,sp} = \frac{(W_G - 2X_{PL})}{W_{cell}} \left(\frac{C_{OX}C_{S,M}}{C_{OX} + C_{S,M}} \right) \quad (2)$$

where C_{OX} is the characteristic capacitance of the gate oxide layer (ϵ_{OX}/t_{OX}), and $C_{S,M}$ is the characteristic capacitance of the depletion layer, calculated as follows:

$$C_{S,M} = \frac{\epsilon_S}{W_{D,MOS}} \quad (3)$$

$$W_{D,MOS} = \frac{\epsilon_S}{C_{OX}} \left(\sqrt{1 + \frac{2V_{ds}C_{OX}^2}{q\epsilon_S N_D}} - 1 \right) \quad (4)$$

where $W_{D,MOS}$ is the width of the depletion layer under the gate oxide in the semiconductor, which is related to the drain-source voltage V_{ds} . From the above equations, it can also be seen that the larger the V_{ds} , the wider the $W_{D,MOS}$, and the smaller the C_{gd} . In this work, the V_{ds} for extracted C_{gd} and C_{gs} is 800 V.

The C_{ds} is the depletion layer capacitance formed by the P-base region and N-drift region under drain voltage bias. The calculation formula is as follows:

$$C_{S,J} = \frac{\epsilon_S}{W_{D,J}} \quad (5)$$

$$W_{D,J} = \sqrt{\frac{2\epsilon_S(V_D + V_{bi})}{qN_D}} \quad (6)$$

$$C_{ds,sp} = \left(\frac{W_{PW} + 2X_{PL}}{W_{cell}} \right) C_{S,J} \quad (7)$$

where $C_{S,J}$ is the specific junction capacitance, $W_{D,J}$ is the depletion layer thickness, N_D is the doping concentration of the donor in the N-region, V_{bi} is the built-in potential of the junction, and W_{PW} is the width of the polysilicon window.

The electrical characteristics of the device are typically characterized by the input capacitance (C_{iss}), the output capacitance (C_{oss}), and the reverse transfer capacitance (C_{rss}). The relationship between these three types of capacitance and the parasitic capacitance mentioned above can be expressed as

$$C_{iss} = C_{gs} + C_{gd} \quad (8)$$

$$C_{rss} = C_{gd} \quad (9)$$

$$C_{oss} = C_{gd} + C_{ds} \quad (10)$$

Among these three types of capacitance, the reverse transfer capacitance (C_{rss}) is the most closely related to the switching performance of the power MOSFET, so the focus of this work is on C_{rss} (i.e., C_{gd}). However, in reality, both C_{iss} and C_{rss} can have an impact on the switching performance of the power MOSFET. This work also considered the influence of C_{gs} on C_{iss} during the design process.

Figure 2a shows a schematic diagram of the planar SiC DMOSFET structure with dimensional design parameters. Figure 2b,c show the conventional linear/stripe topology and the improved shrunk cellular linear/stripe topology, respectively. In the conventional linear/stripe topology, the source contact is continuous, and longer grooves make it difficult to ensure uniformity over a long device width. This will affect the reliability of devices using conventional linear/stripe topology. Therefore, this work uses a cellular linear/stripe topology and improves it to achieve better switching characteristics.

Additional P+ body implanted regions were added to replace the channel and JFET at the original position. This method can convert the original C_{gd} at that position into C_{gs} , resulting in an increase in C_{iss} and a decrease in C_{rss} . In order to reduce the additional C_{iss} , the polysilicon gate at this position is shrunk to decrease C_{gs} . Due to the introduction of additional P+ body implanted regions, the current path in this region is blocked, and consequently, the R_{on} of the device increases. Therefore, as parameter A in Figure 2c increases, C_{gd} decreases while R_{on} increases. In order to achieve better device performance (lower HF-FOM), a compromise needs to be made between C_{gd} and R_{on} .

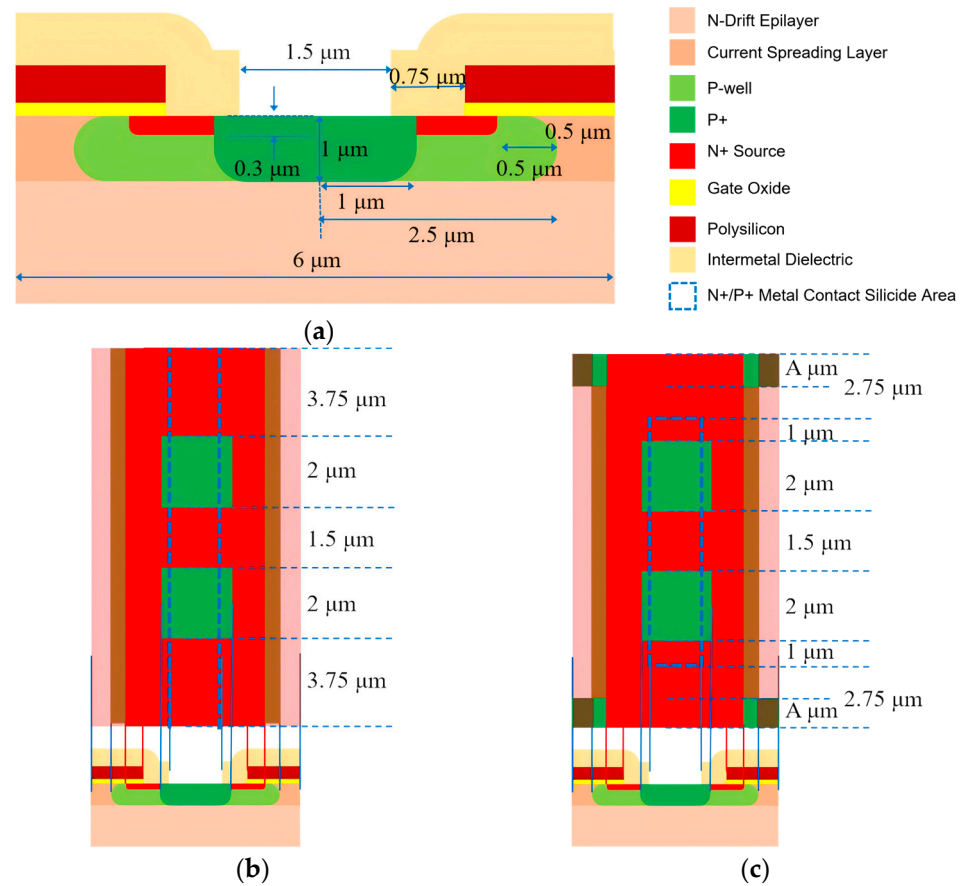


Figure 2. (a) Schematic diagram of planar SiC DMOSFET structure; (b) conventional linear/stripe topology; (c) improved shrunk cellular linear/stripe topology.

The implementation of the new methodology from the conventional linear topology is practical without requiring an additional process step. A total of 3 process mask layers out of a mask set of the DMOSFET process flow [22] need to be re-designed/retrofit, i.e., P+ body implant, polysilicon gate formation, and intermetal dielectric (IMD) mask layers, as shown in Figure 3.

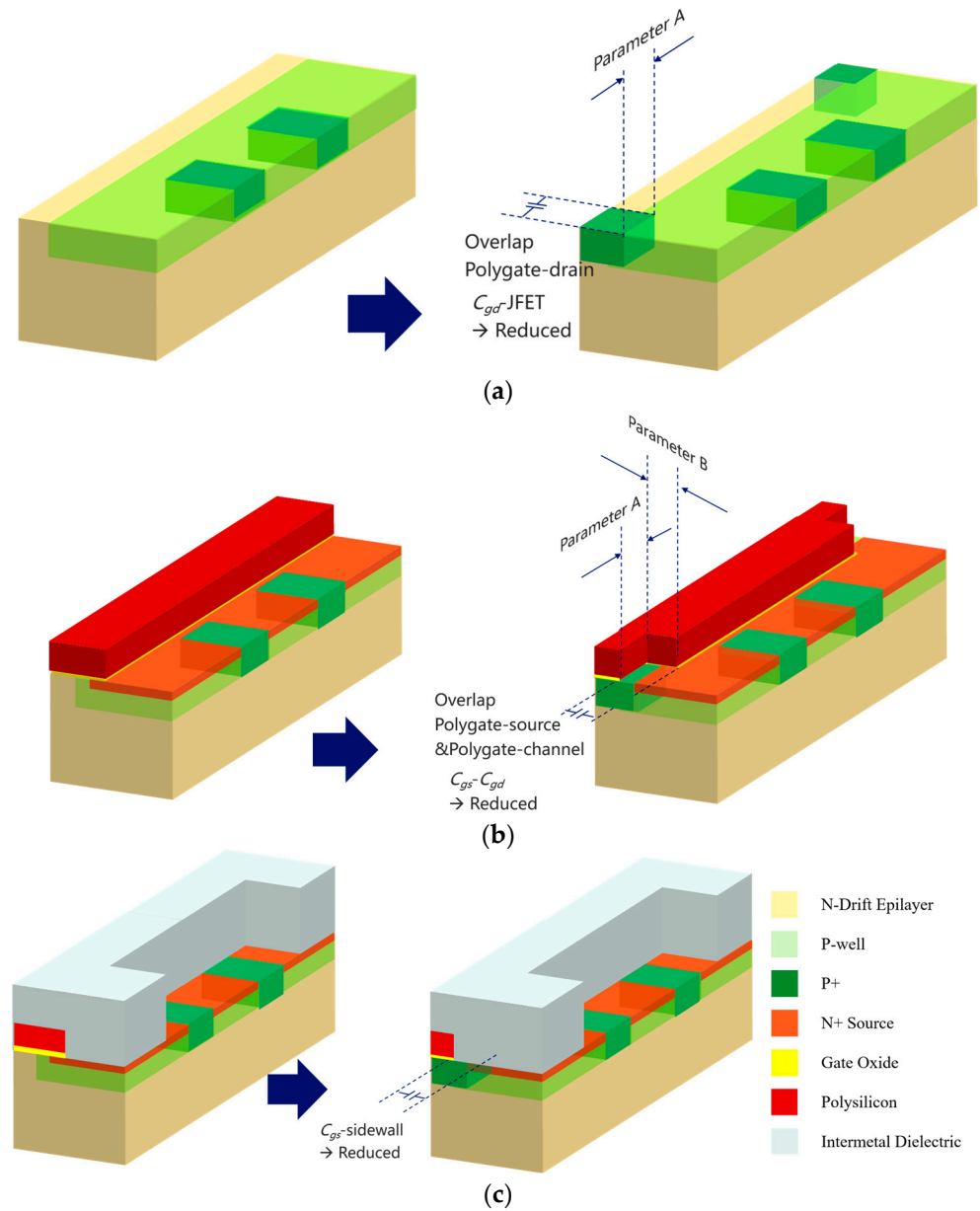


Figure 3. (a) Inserting of P+ into the JFET region; (b) shrink or notch polysilicon gate on the inserted P+ in the JFET region, (c) cellular opening of source contact windows on intermetal dielectric (IMD).

3. Preliminary Two-Dimensional Simulation-Based Work

A fabricated 80 mΩ-1200 V Planar MOSFET of the same design rule was measured and characterized. Electrical input, output, and reversed BV characteristics were matched with TCAD simulation, including the density/near-interface trap density. The representative of the 2D model was used in proposed 3D simulation works to give more realistic simulation results data.

Two-dimensional TCAD simulation was carried out by using the commercial simulator Sentaurus by Synopsys. The device used as a reference was set up in 2D TCAD following the measurement of the DUT (device under test). Material-specific models for the incomplete ionization and the channel mobility, accounting for the degradation of mobility caused by the interface electric field, phonon scattering, and surface roughness, were adopted with default parameters. The interface trap was extracted by calibrating the simulated characteristics to the measurements. Based on the measurement, acceptor-like traps and donor-like traps with exponential and uniform distribution were added at the

SiO₂/SiC interface as shown in Figure 4a. Furthermore, the concentration of the fixed charge was set as $1.4 \times 10^{12} \text{ cm}^{-2}$ at the interface. Trap density, especially traps near the conduction band of the device, determines a large part of the specific on-resistance [23]. The density of interface traps closer to the conduction energy level can be attributed to monitoring the subthreshold slope in the I_d - V_{gs} curve [24]. The model was calibrated based on transfer characteristic measurements with low (0.1 V) and high (10 V) V_{ds} , which further improved the accuracy of calibration. It is worth noting that such distribution was sufficient to reproduce the behavior of transfer characteristics (Figure 4b,c), output characteristics under different gate biases (Figure 4d), and the leakage current level of the break-down curve (Figure 4e).

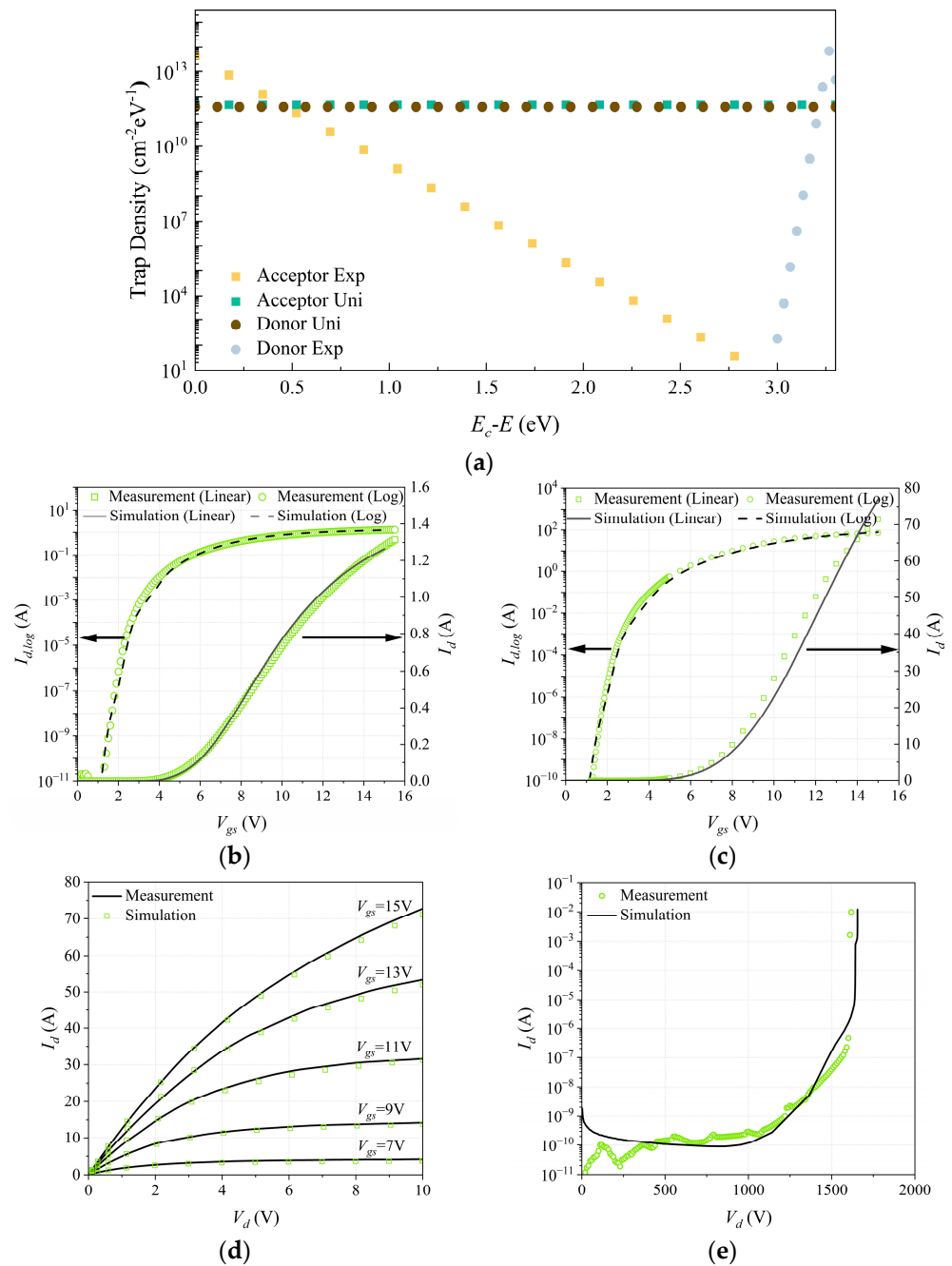


Figure 4. (a) Interface trap density as a function of energy from the top of the valence band to the bottom of the conduction band; calibration results: (b) transfer characteristics $V_{ds} = 0.1 \text{ V}$; (c) transfer characteristics $V_{ds} = 10 \text{ V}$; (d) output characteristics under various gate biases; and (e) reverse bias characteristic.

4. Results and Discussion

A 3D structural diagram was constructed based on the 2D structure, with adjustments made only to the topology structure. Figure 5a shows a schematic diagram of the 3D structure, and Figure 5b shows the topology of the structure.

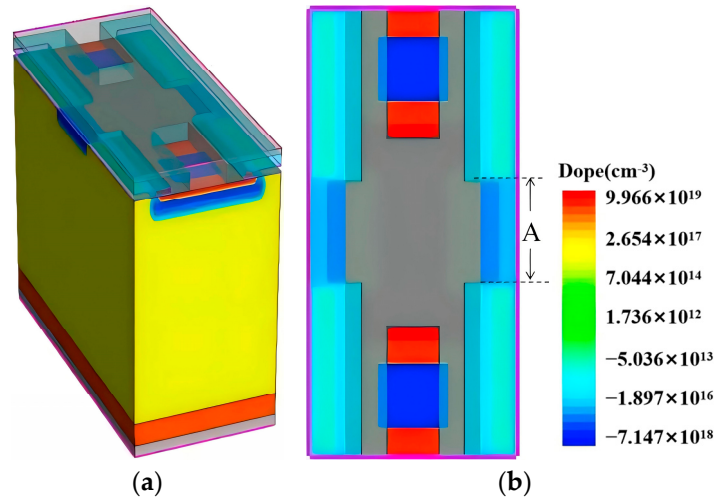


Figure 5. (a) Schematic diagram; and (b) topology of 3D structure.

Using a fixed source opening size, adjusting the value of parameter A, as shown in Figure 5b, reveals the impacts of changes in parameter A on device performance. With the increase in parameter A, the replaced JFET and channel regions become larger, and the C_{gd} decreases. The original existing current path is blocked, and the R_{on} increases. At the same time, the shrunk polysilicon gate is also wider; hence, the overlap area is smaller, and the C_{gs} decreases. The simulation results as parameter A changed from 0.5 μm to 2.5 μm are shown in Table 1, indicating that the changes in C_{gs} , C_{gd} , and R_{on} are in line with expectations.

Table 1. Simulation results of the proposed structure with different parameter A values.

	C_{gs} (pF)	C_{gd} (pF)	R_{on} (m Ω)	HF-FOM (m Ω ·pF)
A = 0.5 μm	1454.042	4.239	83.050	352.049
A = 1 μm	1414.433	3.862	88.214	340.681
A = 1.5 μm	1376.029	3.497	94.009	328.748
A = 2 μm	1337.308	3.138	101.547	318.654
A = 2.5 μm	1299.058	2.775	111.678	309.905
Conventional Structure	1443.362	4.889	74.728	365.344

From the perspective of switching performance, a lower HF-FOM is desired. On the other hand, considering static performance, the impact on R_{on} should not be too large. The optimal value of parameter A through a compromise between the R_{on} and HF-FOM is shown in Figure 6. As parameter A increases from 0.5 μm to 2.5 μm , R_{on} gradually increases while the HF-FOM gradually decreases, intersecting at A = 1.5 μm , indicating a balanced compromise in device performance. The structure with A = 1.5 μm is chosen for comparison with the conventional linear structure.

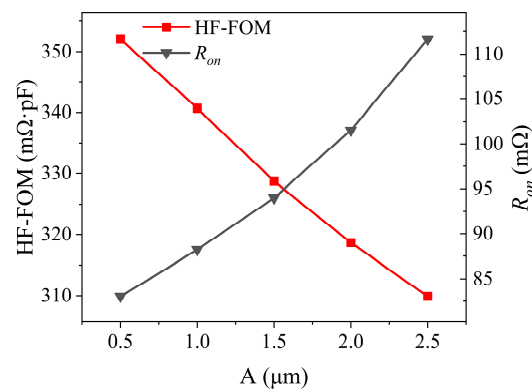


Figure 6. R_{on} and HF-FOM curves of the proposed structure as a function of parameter A.

The double pulse test (DPT) of the proposed structure and the conventional structure was run through mixed-mode TCAD simulations, and the results are shown in Figure 7. Figure 7 shows that the proposed structure has better switching characteristics. In order to better demonstrate the changes in switching characteristics, the rise time (t_r), fall time (t_f), turn-on delay time ($t_{d(on)}$), and turn-off delay time ($t_{d(off)}$) of the two structures were extracted, and the results are shown in Table 2.

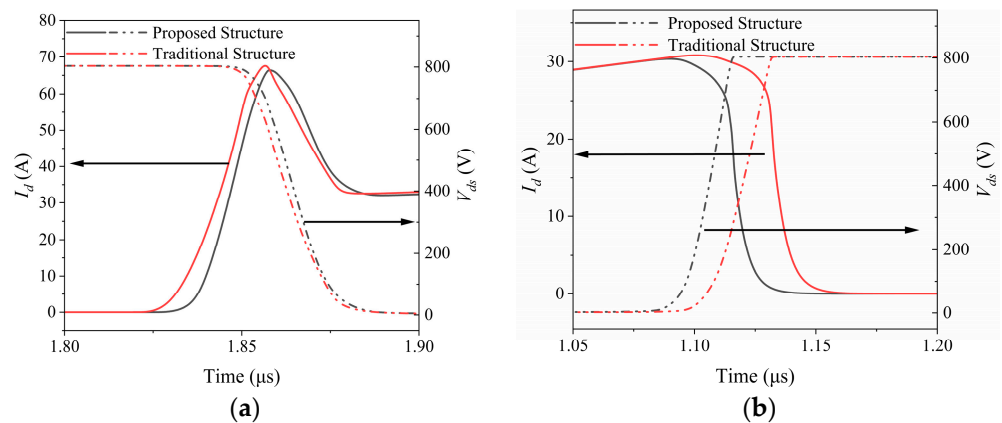


Figure 7. (a) Turn-on curve; and (b) turn-off curve extracted from DPT simulations.

Table 2. Switching performance parameters for proposed and conventional structures.

	t_r (ns)	t_f (ns)	$t_{d(on)}$ (ns)	$t_{d(off)}$ (ns)
Proposed Structure	18.82	17.39	29.96	29.91
Conventional Structure	21.03	21.89	29.09	40.73

It can be observed that the proposed structure has lower t_r and t_f . The reason is that the lower C_{gs} and C_{gd} provide a faster charging speed and shorter Miller platform. The trends of $t_{d(on)}$ and $t_{d(off)}$ are the opposite. This is mainly due to the rising platform voltage caused by changes in the channel and polysilicon gate. The proposed structure's reduced effective channel region as compared to the conventional structure results in a lower transconductance, leading to an increase in platform voltage. During the turn-on process, the power supply charges the gate, and as the gate voltage gradually increases, the drain voltage begins to decrease near the Miller platform voltage. Therefore, the increase in Miller platform voltage contributes to an increase in turn-on delay. The turn-off process is opposite to the turn-on process, and the increase in Miller platform voltage causes a decrease in turn-off delay. Figure 8a shows the gate voltage curves of the conventional structure and the proposed structure during the turn-on process. As shown in Figure 7a, the proposed structure's V_{gs} rises faster due to its smaller C_{gs} , while the Miller platform is shorter due to its smaller C_{gd} . Because of the rise in the Miller platform voltage, the time to reach

the Miller platform is longer. The decrease in capacitance will also accelerate the charging and discharging speed and reduce the delay time, but it does not have such a significant impact.

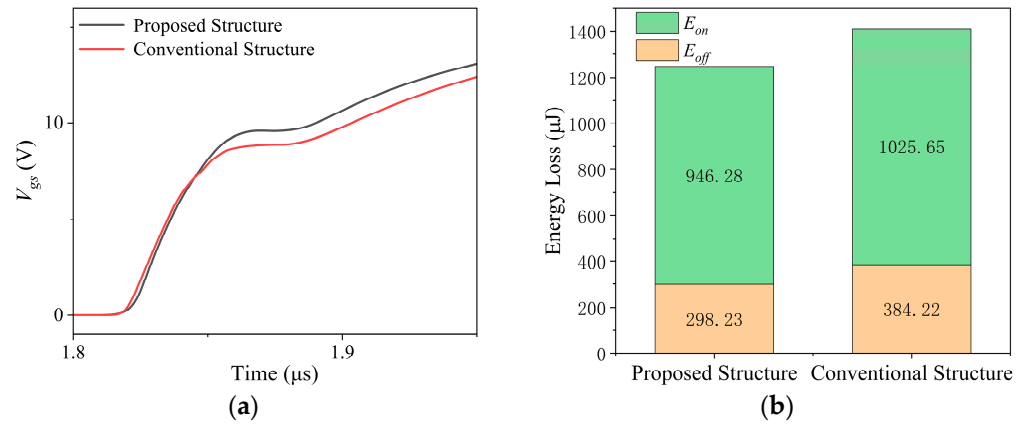


Figure 8. (a) Gate voltage curve during turn-on process; (b) comparison of energy loss between the proposed structure and the conventional structure.

Comparing the derived switching energy loss, the proposed structure has a lower energy loss, as shown in Figure 7b. The proposed structure has an E_{on} of 946.28 μJ and an E_{off} of 298.23 μJ . The conventional structure has an E_{on} of 1025.65 μJ and an E_{off} of 384.22 μJ . The proposed structure reduces E_{on} by 7.74%, E_{off} by 22.38%, and total reduction of switching energy loss by 11.73%.

The shrunk width of the polysilicon gate above the P+ region is another structure parameter that can be optimized. As shown in Figure 9a, as parameter B increases, C_{gd} remains almost unchanged while C_{gs} gradually increases. The results of C_{gd} and C_{gs} as parameter B changed from 0.25 μm to 1 μm are shown in Table 3.

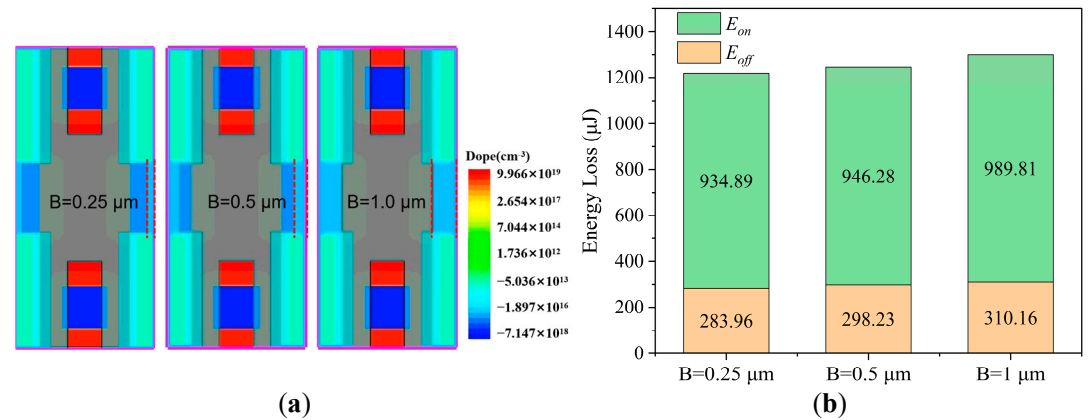


Figure 9. (a) Top schematic diagram of proposed structures for different parameter B values; (b) comparison of energy loss of proposed structures under different parameter B values.

Table 3. C_{gs} and C_{gd} results for different parameter B values.

	C_{gs} (pF)	C_{gd} (pF)	R_{on} (m Ω)	HF-FOM (m Ω ·pF)
B = 0.25 μm	1346.753	3.496	93.355	326.369
B = 0.5 μm	1376.029	3.497	94.009	328.748
B = 1 μm	1581.561	3.539	93.137	329.613

C_{gs} increases with the increase in parameter B values, which can have a negative impact on device switching. C_{gd} and R_{on} show slight changes, while the HF-FOM shows a slight increase, leading to a deterioration in device performance. From the perspective of

the HF-FOM, the larger the shrunk width (i.e., the smaller the value of parameter B), the better the device performance. Considering the variation in C_{gs} , the extracted switching parameters under different parameter B values are shown in Table 4. The results indicate that as C_{gs} increases, the switching performance gradually deteriorates. Figure 9b shows the energy loss with different parameter B values, and the simulation results show that the energy loss increases with the increase in parameter B. This is mainly due to the increase in C_{gs} , which slows down the charging speed of the device and increases the energy loss. The proposed structure has a longer turn-on delay and a higher turn-on loss due to the increase in Miller platform voltage. However, the decrease in capacitance will accelerate the switching process and reduce switching losses. The capacitance increases with the increase in parameter B, so the impact of the increased Miller platform voltage becomes more pronounced, and the turn-on loss will gradually increase. Therefore, the appropriate shrunk width should be selected based on the actual process level and capability.

Table 4. Switching parameters of proposed structures for different parameter B values.

	t_r (ns)	t_f (ns)	$t_{d(on)}$ (ns)	$t_{d(off)}$ (ns)
Proposed Structure	18.82	17.39	29.96	29.91
Conventional Structure	21.03	21.89	29.09	40.73

Another important aspect is the source ohmic contact resistivity of SiC MOSFET. The difference between the two compared structures of R_{on} mainly originates from the different source areas, so the magnitude of the source ohmic contact resistivity will affect the gap in R_{on} between the two structures. The value of resistivity has little effect on the value of capacitance, so lower resistivity will result in a lower HF-FOM. The HF-FOM of devices with different resistivities were simulated, and the results are shown in Figure 10. It can be observed that the higher the resistivity, the larger the HF-FOM, and the smaller the gap in HF-FOM between the proposed structure and the conventional structure. Therefore, for the proposed structure, the low ohmic contact resistivity is recommended to be lower than $6 \times 10^{-5} \Omega \cdot \text{cm}^2$. In previous simulations the source ohmic contact resistivity was set following the fabricated 80 m Ω -1200 V Planar MOSFET. From the test monitoring transmission line method (TLM) structure, the extracted source ohmic contact resistivity is $9.66 \times 10^{-6} \Omega \cdot \text{cm}^2$.

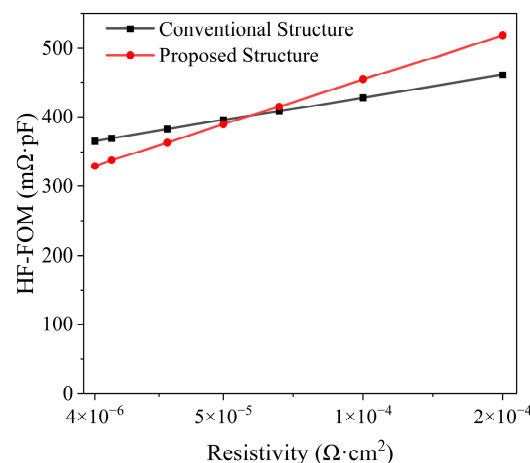


Figure 10. The influence of resistivity on the HF-FOM of the conventional structure and proposed structure.

5. Conclusions

This work proposes an improved shrunk cellular linear/strip topology structure of SiC MOSFET that improves switching performance and reduces energy loss, by introducing additional P+ body implant and shrunk polysilicon gate above the additional P+ body

implanted regions to reduce C_{gd} and C_{gs} , respectively. Based on the calibrated TCAD parameter models, the critical parameters that represent the additional P+ body implant width (A) and shrunk width of the polysilicon gate length (B) were optimized in 3D TCAD simulations. The lowest HFOM was achieved in a device with parameters A and B set to 1.5 μm and 0.5 μm , respectively. Compared with the conventional linear/stripe topology structures, the proposed structure reduces E_{on} by 7.74%, E_{off} by 22.38%, and total switching energy loss by 11.73%. In addition, the influence of the shrunk width and source ohmic contact resistivity was also analyzed and discussed. The gap in the HF-FOM between the conventional structure and the proposed structure increases with the decrease in resistivity. When the resistivity is lower than $6 \times 10^{-5} \Omega\cdot\text{cm}^2$, the proposed structure has a lower HF-FOM and better switching characteristics. The proposed structure reduces the total switching energy loss by 11.73% when $B = 0.5 \mu\text{m}$. Increasing the shrunk width (i.e., reducing the value of parameter B) can result in a lower energy loss. Therefore, it is necessary to pursue smaller resistivity and larger shrunk width to achieve lower energy loss. The improved switching performance most benefits applications in which switching losses are dominant over conductance losses and in which switching and conductance losses are equally distributed. Applications such as AC-DC and DC-DC converters that require higher switching frequency (higher than 30 kHz) benefit most in terms of efficiency and overall system cost. The device and application implementation and confirmation of these initial findings will be part of the direction of future works.

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