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A 6–18 GHz Low-Noise Amplifier with 19 dBm OP_{1dB} and 2.6 ± 0.3 dB NF in 0.15 µm GaAs Process

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Abstract: A three-stage low-noise amplifier (LNA) operating over the 6–18 GHz frequency range is designed and implemented, featuring a flat noise figure (NF) and enhanced output 1 dB compression point (OP_{1dB}). To improve linearity and minimize distortion, a power high-electron-mobility transistor (HEMT) is employed in the final stage. Additionally, resistive feedback and self-biasing techniques are integrated to extend the amplifier's bandwidth. The proposed LNA exhibits a high and flat power gain of 25 ± 1 dB, with an input return loss of more than 10 dB. The measured NF remains stable at 2.6 ± 0.3 dB over the 6–18 GHz range. Furthermore, the OP_{1dB} exceeds 19.5 dBm across the entire 3 dB gain bandwidth (BW). The circuit is fabricated using a 0.15 µm GaAs pHEMT process, occupying a compact chip area of 1.2 × 1.8 mm^2.

Keywords: ultra-wideband (UWB); low-noise amplifier (LNA); GaAs; noise figure (NF); output 1 dB compression points (OP_{1dB})

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1. Introduction

Ultra-wideband (UWB) communication systems operating within the 3.1–10.6 GHz spectrum demonstrate broad applicability in diverse fields, including high-resolution radar systems, precision instrumentation, short-range communication, and high-speed transceiver architectures [1,2]. As the first active module in a UWB receiver, the low-noise amplifier (LNA) is a key component whose noise figure, gain, linearity, and bandwidth considerably influence receiver sensitivity. Recent studies have indicated that GaAs technology is well suited for the design of LNAs. GaAs achieves a better balance of low noise figure, high linearity, and compact footprint at a relatively low cost [3]. This makes it an excellent choice for applications where both high performance and cost-effectiveness are crucial. In modern radar and communication systems, LNAs must simultaneously handle weak signals and strong interference, necessitating high OP_{1dB} to maintain linearity and prevent distortion under dynamic conditions. However, current LNAs do not have sufficiently high OP_{1dB}, which renders them unable to meet the various requirements of multiple frequency bands and higher standards. Consequently, it is crucial to design a broadband LNA with high OP_{1dB}, which is of great research significance.

In recent years, researchers have reported several approaches to extending the bandwidth of LNAs, including distributed topologies, inductive peaking, and resistive feedback techniques. Distributed topologies can achieve significant bandwidth extension [4,5]. However, their practical implementation faces constraints including excessive component

footprint, poor noise figure, and high power consumption. The inductive peaking technique [6], though effective for frequency response improvement, similarly requires a large chip area. In contrast, resistive feedback topologies have been extensively reported [7] as a space-efficient bandwidth expansion solution. Hybrid microwave integrated circuits (HMICs) offer a distinct alternative [8], achieving compact size, low noise figure, and optical sensing capability, but their bandwidth is limited by lumped-element matching and they are sensitive to environmental factors like light exposure. According to the above literature research, few LNAs have been reported to operate across the C- to Ku-bands with NF below 3 dB, power gain over 20 dB, and OP_{1dB} over 10 dBm.

In this paper, a broadband three-stage LNA with a flat NF and high OP_{1dB} is proposed, addressing the critical challenge of achieving high linearity, wide bandwidth, and low noise figure across the 6–18 GHz spectrum. By leveraging a power high-electron-mobility transistor (HEMT) in the final stage and optimizing the output matching network, the design achieves a record-high OP_{1dB} of 19.5 dBm across the entire operational bandwidth. Furthermore, to extend bandwidth while maintaining flat gain and noise performance, resistive feedback networks are employed in the latter two stages, expanding the 3 dB bandwidth (BW) to 12.9 GHz (5.7–18.6 GHz) and ensuring a flat NF of 2.6 ± 0.3 dB and gain of 25 ± 1 dB. Additionally, a self-biasing architecture reduces the chip area to 1.2×1.8 mm^2 and eliminates the need for dual power supplies, overcoming the multi-power supply complexity and large footprint issues. The LNA's high OP_{1dB} and wide bandwidth enable dual-use in both receive and transmit chains, thereby broadening the scope of potential applications and offering a compact, high-performance solution for applications including military radars, wireless communication systems, and broadband instrumentation (such as spectrum analyzers and vector network analyzers).

2. LNA Circuit Design

2.1. Topology of the LNA

The schematic of the proposed three-stage LNA is presented in Figure 1. Self-biasing technology is adopted in all stages, in which $R_{S1}/C_{S1}/L_3$ participate in M_1 biasing. The gate of M_1 is biased to the ground by inductor L_3, and the source terminal is biased by resistor R_{S1}. The principle behind this self-biasing technique is that the source resistor R_{S1} raises the source potential of the transistor M_1. With the gate grounded via the inductor L_3, a gate–source voltage V_{GS} of -0.6 V is generated without the need for a negative power supply. Based on the bias condition of M_1, analogous voltage distributions can be derived for the gate and drain bias of M_2/M_3. The parallel capacitor C_{S1} plays a crucial role in circuit performance. Due to the frequency response of the capacitors, C_{S1} can bypass low-frequency signals, reducing low-frequency resonance. By suppressing low-frequency resonance, C_{S1} helps to stabilize the gain across the frequency band, thereby improving the gain flatness. Moreover, it optimizes the impedance characteristics of the circuit, reducing oscillations and enhancing the overall stability of the circuit. For the three-stage amplifier design, the values of the source resistors R_S are determined by the bias currents I_{DD}. Given that the LNA is biased at $V_{GS} = -0.6$ V and the total bias current is 180 mA (I_1 = 20 mA, I_2 = 70 mA, I_3 = 90 mA), we can calculate that R_{S1} = 30 Ω, R_{S2} = 9 Ω, and R_{S3} = 7 Ω. Self-biasing technology effectively reduces the number of power supplies from two (1 gate, 1 drain) to a single supply, minimizes power pads, and decreases the chip footprint. In addition, the resistive feedback technique is utilized in the latter two stages. The resistive feedback network comprises a resistor R_f and a blocking capacitor C_f, forming a negative feedback path between the gate and the drain. The function of this particular negative feedback path is to suppress low-frequency gain, thereby achieving a flat broadband response and enhancing stability, which leads to an expansion of the bandwidth.

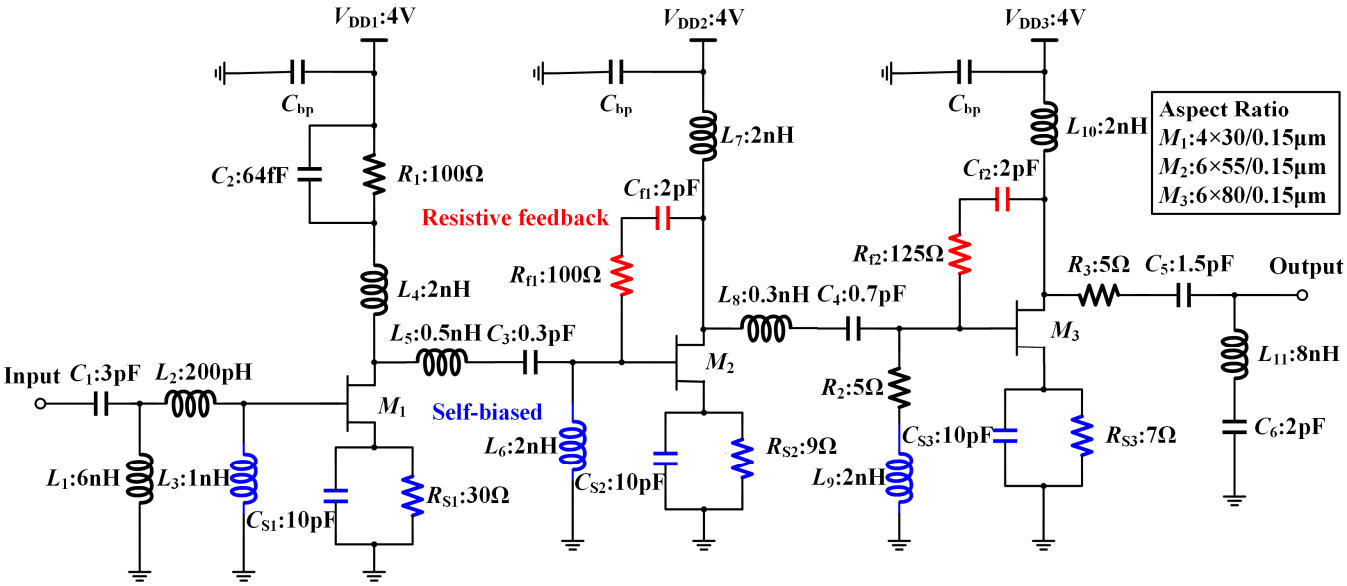

Figure 1. Schematic of the LNA.

A basic guideline is given regarding the circuit design: low NF is the key parameter for the first stage, while high linearity is the main index for the third stage. Inter-stage impedance matchings achieve an overall flat gain response. Hence, the first two stages of the circuit are designed with low-noise HEMTs, and the final stage uses a power HEMT with higher linearity, which significantly improves the OP_{1dB} of the LNA while maintaining high gain and low noise. What is more, the widths of transistors are selected as $W_{M1} = 4 \times 30$ μm, $W_{M2} = 6 \times 55$ μm, and $W_{M3} = 6 \times 80$ μm. The width of the transistor is gradually increased from the first to the third stage to improve OP_{1dB} while saving power consumption. Since the NF of the first stage dominates the LNA's overall NF, minimizing its noise contribution is critical. The bias voltage of the first-stage transistor is adjusted to 2 V through the insertion of a series resistance R_1 in its drain bias path, which suppresses short-channel effects and minimizes the NF_{min} of the first stage. In addition, inductor L_3 participates in forming a reactive impedance π-matching network with inductors L_1 and L_2, approximating the optimal noise impedance while balancing wideband input standing-wave ratio (VSWR) performance. At the same time, the linearity of the final stage contributes more to the overall linearity of the amplifier [9]. The output matching network is formed with capacitor C_6 and inductors L_{11} to achieve output impedance matching and a trade-off between OP_{1dB} and the standing wave. Resistor R_3 improves stability at the cost of consuming output power.

2.2. Resistive Feedback Technique

The resistive feedback technique is utilized in the last two stages, enhancing circuit stability while moderately reducing broadband gain. However, it is unsuitable for the LNA input stage. The feedback resistance R_f would significantly increase the noise figure because of its inherent thermal noise. Since the first stage plays a dominant role in the LNA's overall noise performance, excluding R_f here is essential to minimize the noise figure, ensuring the LNA meets the low-noise design requirement. Figure 1 illustrates the optimized feedback network (highlighted in red). The capacitor C_f, assigned a substantial capacitance value of 2 pF, effectively minimizes its influence on the system's frequency characteristics. This capacitor primarily serves as a DC blocking component to maintain proper bias isolation between the transistor's gate and drain terminals, ensuring stable operating conditions.

Figure 2 comparatively demonstrates three critical performance parameters, maximum gain, output 1 dB compression point (OP_{1dB}), and stability factor k, for both the standalone transistor and the third-stage feedback amplifier. Furthermore, we evaluate how variations in the feedback resistance R_f influence the frequency response of the circuit. It can be seen that as the resistor R_f increases, the maximum gain and OP_{1dB} increase and the stability factor k decreases. The feedback amplifier circuit improves the stability of the circuit and prevents the circuit from generating self-excitation. At the same time, although the feedback amplifier circuit reduces the maximum gain and OP_{1dB} by decreasing the amplitude of the input signal of the transistor, it suppresses the low-frequency gain and greatly improves the gain flatness. The circuit's unconditional stability condition ($k > 1$) requires $R_f \leq 125\ \Omega$. Through comprehensive trade-off analysis, the feedback resistance value was established at 125 Ω, achieving balanced performance characteristics. After completing the design of the input and output matching networks, the circuit's stability factor k will be further improved, ensuring the circuit achieves unconditionally stable operation.

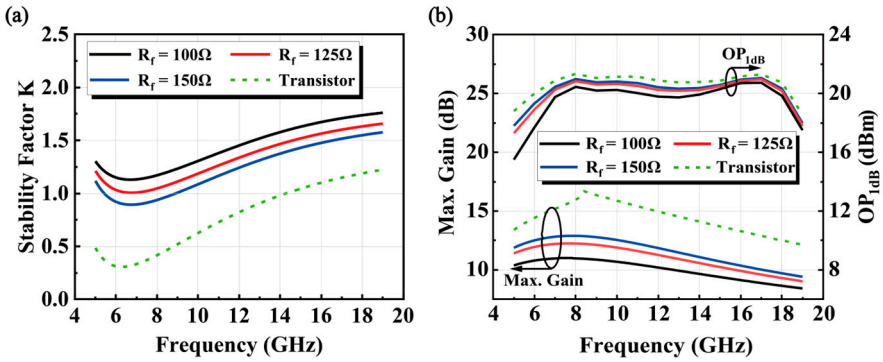

Figure 2. Simulated (**a**) stability factor k and (**b**) maximum gain and output 1 dB compression points for the transistor and the feedback amplifier.

3. Results and Discussion

The proposed LNA is fabricated using a 0.15 μm GaAs pHEMT process with a chip size of 1.8 × 1.2 mm^2. Figure 3 presents the annotated chip micrograph. The S-parameters, OP_{1dB}, and NF of this LNA are measured using Keysight PNA-X N5247B via on-wafer probing. As shown in Figure 4a, the measured stability factor k of the LNA exceeds 2 across the entire 5–20 GHz band, confirming absolute stability. Comparative results between simulated and measured S-parameters are illustrated in Figure 4b, where the LNA exhibits a maximum gain of 26.4 dB at 9 GHz and a 3 dB bandwidth (BW) spanning 5.7–18.6 GHz. Input/output matching performance demonstrates broadside optimization, with the measured S_{11} remaining below −9 dB across 6–19 GHz and S_{22} suppressed under −10 dB from 7.6 to 19 GHz. In addition, Figure 4c provides the measured and simulated NF and OP_{1dB}. It can be seen that the measured NF is below 2.9 dB over 5–19 GHz and OP_{1dB} exceeds 19.5 dBm within the 6–19 GHz operational bandwidth. Table 1 summarizes the key performance of LNAs for quantitative evaluation. To better evaluate the LNA's performance, a widely adopted figure of merit (FOM) is employed, incorporating critical parameters including power gain, noise figure, BW, DC power consumption, and linearity (P_{1dB}). The FOM is defined as follows [10]:

$$\mathrm{FOM} = \frac{\mathrm{Gain_{max}(dB)} \times \mathrm{BW(GHz)} \times \mathrm{P_{1dB}(mW)}}{(\mathrm{NF_{mean}} - 1) \times \mathrm{P_{DC}(mW)}} \quad (1)$$

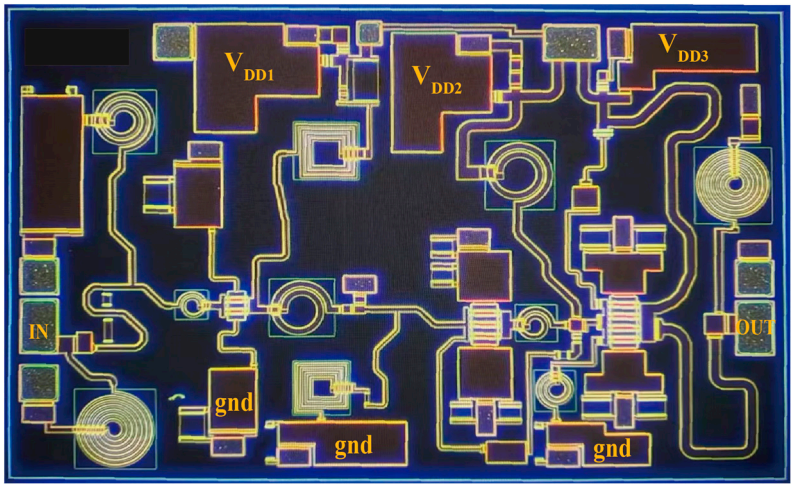

Figure 3. Chip micrograph of the LNA.

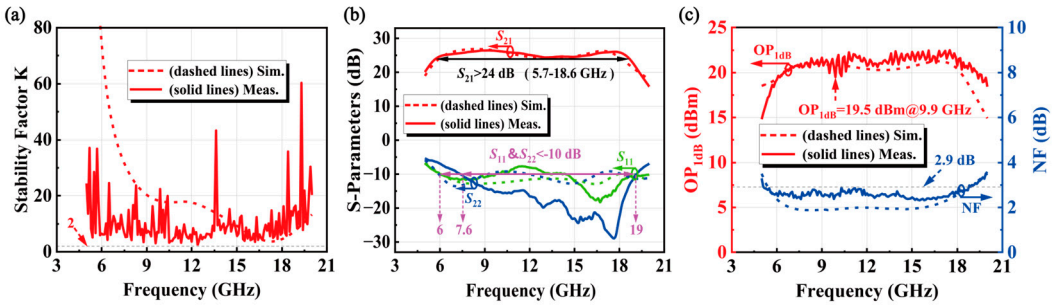

Figure 4. Simulated and measured (**a**) stability factor k, (**b**) S-parameters, and (**c**) NF and OP_{1dB}.

Table 1. Performance summary and comparison with other broadband LNAs.

Reference	Technique	Freq. (GHz)	Gain (dB)	NF (dB)	OP_{1dB} (dBm)	P_{DC} (mW)	Area (mm^2)	FOM
[5]	0.15-μm GaAs	2–42	14.1	3	10	129	1.53	21.86
[11]	0.15-μm GaAs	0.5–24	24.7	1.7-2.8	10	212	1.47	27.38
[12]	0.15-μm GaAs	17–28	17	2.2	6	30	1.5	20.66
[13]	0.15-μm GaAs	32–40	21.5	2.2	10	56	1.35	25.59
[14]	0.15-μm GaAs	22.5–34	22.5	3–4.5	−2.5	36	2.5	1.44
[15]	0.15-μm GaAs	0.01–22	23	NA	21	NA	3.75	NA
This Work	0.15-μm GaAs	6–18	25	2.3–2.9	21	720	2.16	35.52

In comparison with other work, the proposed LNA achieves a low and flat NF response (competitive with [5,11]), delivers a 25 dB gain surpassing those of [5,12], and reaches the highest OP_{1dB} of 21 dBm among these works for superior linearity. Despite the higher P_{DC}, the LNA achieves the highest FOM, effectively balancing gain, noise, bandwidth, linearity, and power consumption. Overall, the proposed low-noise amplifier demonstrates advantages in key parameters, achieving a low and flat NF, high power gain, the highest OP_{1dB}, and a competitive FOM.

4. Conclusions

In this paper, a broadband LNA with high OP_{1dB} is presented. The LNA is implemented in a 0.15 μm GaAs pHEMT process. It achieves 12–18 GHz bandwidth, 25 ± 1 dB gain, and 2.6 ± 0.3 dB NF. The OP_{1dB} is greater than 19.5 dBm over the entire 3 dB gain BW. This design's combination of high OP_{1dB}, low NF, and wide bandwidth makes it suitable for applications such as military radar jamming mitigation, multi-user communication, and broadband instrumentation, where robust signal handling and integration density are critical.

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