

Article

A 50 Gb/s 0.42 pJ/b Non-Return-to-Zero Transmitter for Extra-Short-Reach SerDes

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Abstract: An energy- and area-efficient non-return-to-zero (NRZ) transmitter with feed-forward equalization (FFE) is proposed for an extra-short-reach (XSR) data interface in chiplet-based system in packages (SiPs) and multi-chip modules (MCMs). At the system level, the final-stage 2:1 multiplexer (MUX) in the transmitter is combined with the driver to reduce the hardware and power consumption; at the circuit level, charge-steering-based moderate-swing signal processing further reduces the circuit power consumption and inter-symbol interference. Fabricated in a 28 nm CMOS process with a core area of 0.032 mm², the prototype NRZ transmitter demonstrates an energy efficiency of 0.42 pJ/b at a data rate of 50 Gb/s with an insertion loss of 10 dB, which makes it a promising candidate for XSR die-to-die (D2D) interfaces.

Keywords: wireline transmitter; non-return-to-zero (NRZ); extra short range (XSR); energy efficient; feedforward equalization (FFE); multiplexer (MUX); charge steering logic (CSL)



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1. Introduction

With the rapid advancement of artificial intelligence (AI), machine learning (ML), and hyperscale computing, the amount of data that need to be manipulated and transported increases exponentially [1–4]. While improving the yield of a single chip, allowing process optimization of each die, and reducing the cost of the whole system, the chiplet-based system in package (SiP) and multi-chip module (MCM) technology impose stringent requirements on the data communication between dies [5–7]. With a usual insertion loss of less than 10 dB, the extra-short-reach (XSR) die-to-die (D2D) interface requires data lanes with a large data rate, compact area, and small power consumption, where NRZ encoding is preferred for its relaxed SNR requirement, less circuit complexity, and lower power consumption [8]. Meanwhile, appropriate equalization such as feedforward equalization (FFE) has been proven to play an important role in the signal bandwidth extension in wireline communication, and its adjustable equalization weights are crucial for addressing different channels [9]. By leveraging system- and circuit-level innovations, a power- and area-efficient non-return-to-zero (NRZ) transmitter with FFE is proposed in this paper, which makes it a promising candidate for XSR D2D interfaces.

The most challenging and power-hungry part of the transmitter consists of the 4:1 MUX and channel driver because they operate at the highest frequency. In the traditional architecture, as shown in Figure 1a [10], the front end of the transmitter consists of a 4:1 data MUX followed by a retiming flip-flop driven by the full-rate clock to align and send the data to the driver. The data retiming using a full-rate clock requires large power consumption to meet the timing specification. Therefore, it is favored to eliminate the

full-rate flip-flops and align the data using multi-phase clocks at a half-rate or quarter-rate for an improved energy efficiency. As shown in Figure 1b, the main path and FFE path data are multiplexed by two sequential stages of 2:1 MUX before the driver. In this structure, the data retiming is achieved by a 50% duty cycle half-rate clock at the second-stage 2:1 MUX. Both the second-stage 2:1 MUX and the driver manipulate the data at their full rate; the current of the two parts will be very large and therefore dominate the power consumption of the whole system [11]. The combination of the 4:1 MUX and the driver is proposed in [12] to minimize the blocks that operate at high frequency. As shown in Figure 1c, to combine 4:1 multiplexing and FFE, eight differential pairs of transistors merge at the output node of the driver, resulting in excessive parasitic capacitance. Therefore, a more complicated bandwidth extension network is required at the driver output that involves multiple inductors with large inductance values, which significantly increases the chip area. Furthermore, a half-rate clock with a 25% duty cycle is required for the single-stage 4:1 multiplexing. The circuit of the 25% duty cycle generation consumes more power and deteriorates the data eye diagram due to the duty cycle mismatch.

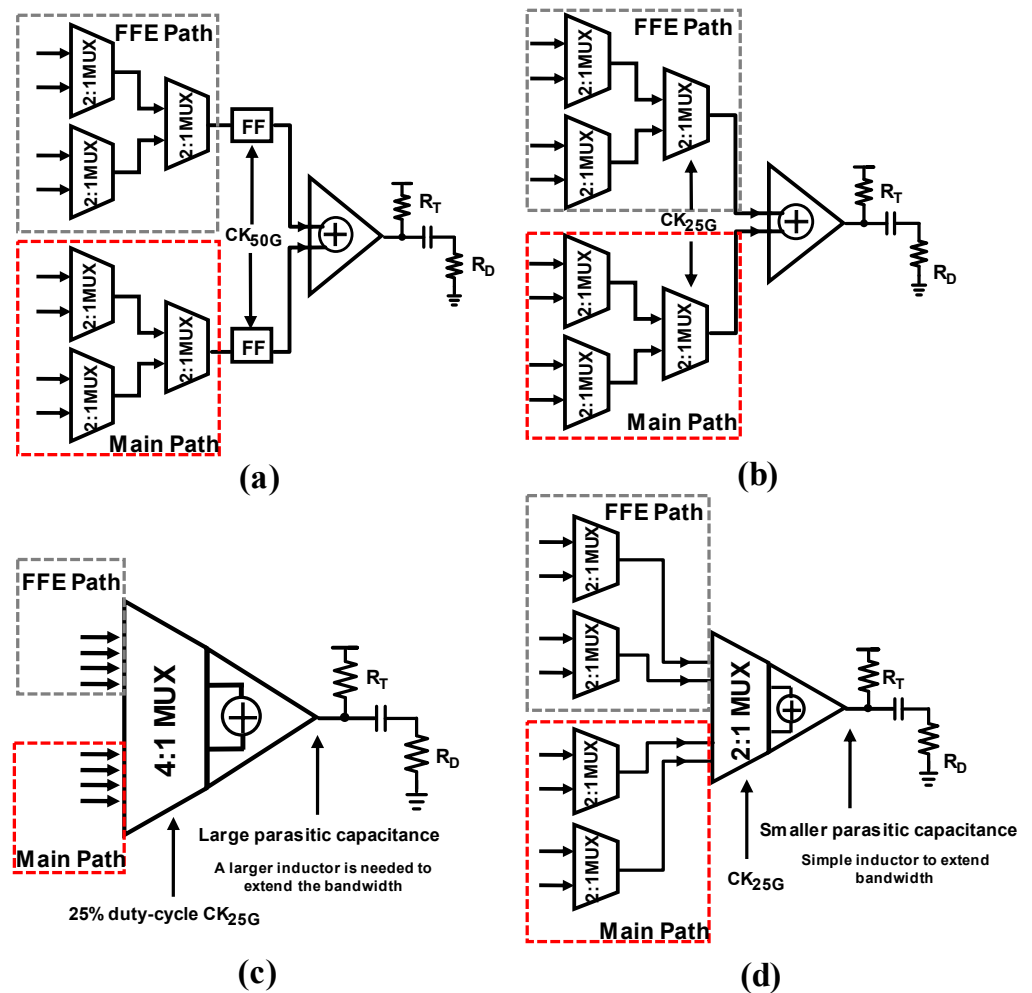


Figure 1. Transmitter with (a) full-rate clock-driven flip-flop. (b) Half-rate clock-driven 2:1 MUX. (c) A 4:1 MUX combined with driver driven by 25% duty cycle half-rate clock. (d) The proposed half-rate clock-driven 2:1 MUX combined with driver.

The proposed transmitter architecture is shown in Figure 1d: low power and a compact area are achieved by leveraging the following techniques at both the system and circuit levels. At the system level, the final-stage 2:1 MUX is incorporated into the current mode logic (CML) driver. To maintain the same CML output swing, the current consumed in this

combined 2:1 MUX and driver module is equal to the current of the output driver in Figure 1b. Therefore, the 2:1 MUX power consumption is saved in the proposed structure compared to that in Figure 1b. On the other hand, the combination of the 2:1 multiplexing and driver in the proposed structure introduces much less parasitic capacitance at the output node compared to the 4:1 MUX and driver architecture in Figure 1c; therefore, a simple series inductance peaking can be utilized to mitigate the bandwidth penalty, resulting in both low power consumption and a small area. At the circuit level, instead of maintaining the full-swing signals in the conventional CMOS transmitter architecture, a signal path with a moderate swing is adopted in this transmitter to save the power consumption. This is achieved by the charge-steering logic (CSL)-based 4:2 MUX followed by a CML driver combined with the 2:1 MUX. Because the CSL circuits operate with moderate data swings while drawing power for only a fraction of the clock cycle, they afford a design faster than rail-to-rail logic [13]. Please note that a CML driver instead of an inverter-based driver is chosen in this design for the following reasons. First, the NMOS input CML driver accommodates the common mode voltage of the preceding CSL MUX outputs, which is closer to VDD. Second, the CML driver can accept and amplify moderate-swing signals while the inverter-based driver usually needs power-hungry pre-drivers to achieve a near full-swing input signal [5]. Last but not least, more slices are needed to make FFE programmable in an inverter-based driver, which introduces more parasitic capacitance at the driver output nodes [14].

The main contents are organized as follows. Section 2 explains in detail the whole transmitter architecture. Section 3 explains the specific circuit designs. Section 4 describes the measurement setup and results, followed by the conclusion in Section 5.

2. Architecture of Transmitter

The overall architecture of the proposed transmitter is shown in Figure 2. In the signal path, an on-chip four-bit pseudo-random binary sequence (PRBS) generator is implemented to generate four parallel paths of the PRBS7 sequence. A latch array driven by four-phase quarter-rate clocks (C4) is designed to retime the data with a maximized timing margin for the subsequent 4:2 MUX. Meanwhile, since the rising edge of the previous phase and the next phase clock triggers the latch to generate the main path data and FFE path data, respectively, the FFE data path with one unit interval (UI) delay is also generated in the latch array with the same timing margin as the main data path. The following CSL-based 4:2 MUX serializes the data in both main and FFE paths, and the half-rate data are sent to the combined 2:1 MUX and driver, which is driven by C2 clocks to complete the final serialization. The FFE weighting is made four-bit-programmable to optimize the equalization for different channel loss. Furthermore, a series inductor is utilized to mitigate the bandwidth degradation due to the capacitive loading at the driver output nodes. In the clock path, the differential half-rate clocks C2 are generated through an external balun and the four-phase quarter-rate clocks C4 are generated through a CML divider-by-2. A variable delay chain is introduced in the clock path before the CML DIV2 to optimize the timing margin between the four-phase clocks (C4 CLK) and the data path. The clock chain is simulated with process, voltage, and temperature (PVT) variations to ensure the reliability of the design.

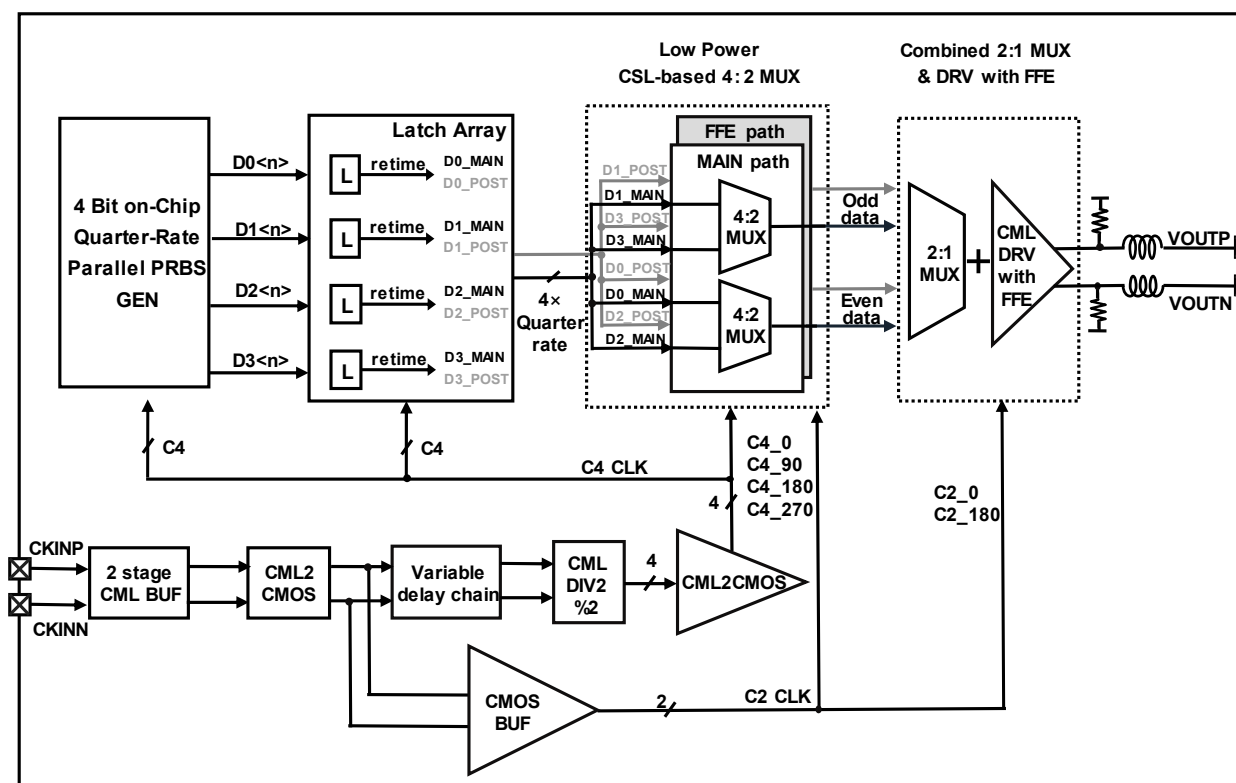


Figure 2. Overall architecture of the proposed transmitter.

3. Circuit Implementation

The system structure and timing diagram of the latch array is shown in Figure 3. It receives four parallel data paths ($D0<n>$, $D1<n>$, $D2<n>$, $D3<n>$) from the preceding PRBS generator and retimes the data for both main ($D0_MAIN$, $D1_MAIN$, $D2_MAIN$, $D3_MAIN$) and FFE ($D0_POST$, $D1_POST$, $D2_POST$, $D3_POST$) paths for the following 4:2 MUX. The circuit of the latch consists of a transmission gate followed by an inverter. As shown in Figure 3, with the input data aligned with $C4_270$, the first stage of latches clocked by $C4_0$ sample the input data at the middle of the data window, maximizing the timing margin and reducing the latch speed requirement. The sequential-phase clocks ($C4_90$, $C4_180$, and $C4_270$) sample the data generated by the preceding phases, rendering the same optimal timing margin for all the four-path output data. Please note that, with an extra latch clocked by a clock 90 degrees later, the FFE path data can be generated from the corresponding math path data with the same optimal timing margin.

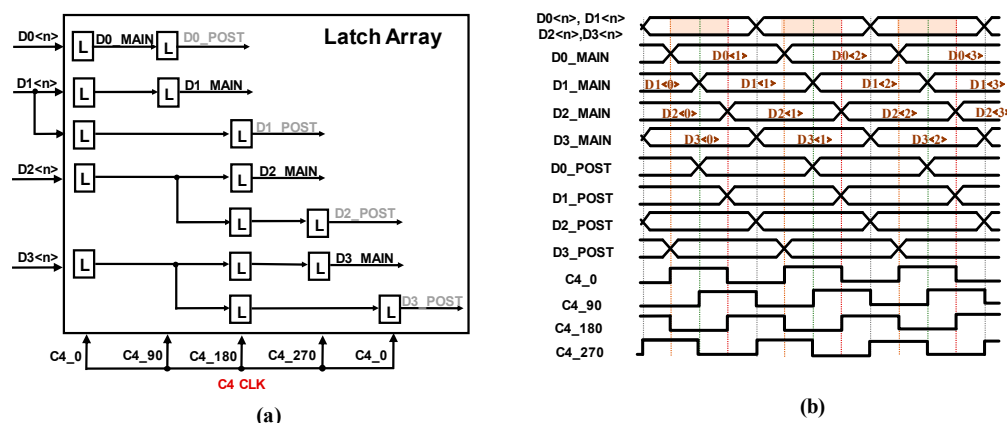


Figure 3. (a) The system structure and (b) timing diagram of the latch array.

Reducing the data swing helps to reduce the power consumption and inter-symbol interference (ISI) in the MUX design. In this work, a CSL-based MUX is designed for low-power 4:2 multiplexing. The CSL circuits maintain moderate signal swings and draw power for only a fraction of the clock cycle; therefore, they can achieve a faster speed than rail-to-rail circuits and draw less power than current mode logic circuits. The detailed circuit of the 4:2 MUX and its corresponding timing diagram is depicted in Figure 4. Taking the even main path as an example (as shown on the top of Figure 4), the MUX toggles between reset mode and amplification mode, which is controlled by C2_180 and C2_0. Meanwhile, the output data are chosen between D0_MAIN and D2_MAIN, dictated by C4_180 and C4_0. Therefore, the output of the even main stage is return-to-zero (RZ) half-rate even data. With appropriate clock assignment, the output of the odd main stage (as shown at the bottom of Figure 4) is RZ half-rate odd data with 1UI delay compared to the even main path. Therefore, the output data of the even and odd main stage can be multiplexed in the following stage to obtain the fully serialized data. It is worth noting that the gain and output swing of the CSL-based MUX are closely related to the ratio of C_T and C_D [13], where C_T is the tail capacitance and C_D is the capacitance of the output node. Meanwhile, the size of the C_T value is also closely related to the speed of the circuit. When one of the input transistors is turned on, the charge accumulated at the output node during the reset mode will be redistributed between the C_D and C_T . Therefore, the larger the C_T , the lower the voltage at the source of the input transistor, resulting in a larger V_{GS} and V_{DS} of the input MOS, thus making the CSL-based 4:2 MUX operate faster. In this design, the value of C_T and C_D are 56f and 13f, respectively, which is designed to consider the output swing and circuit speed.

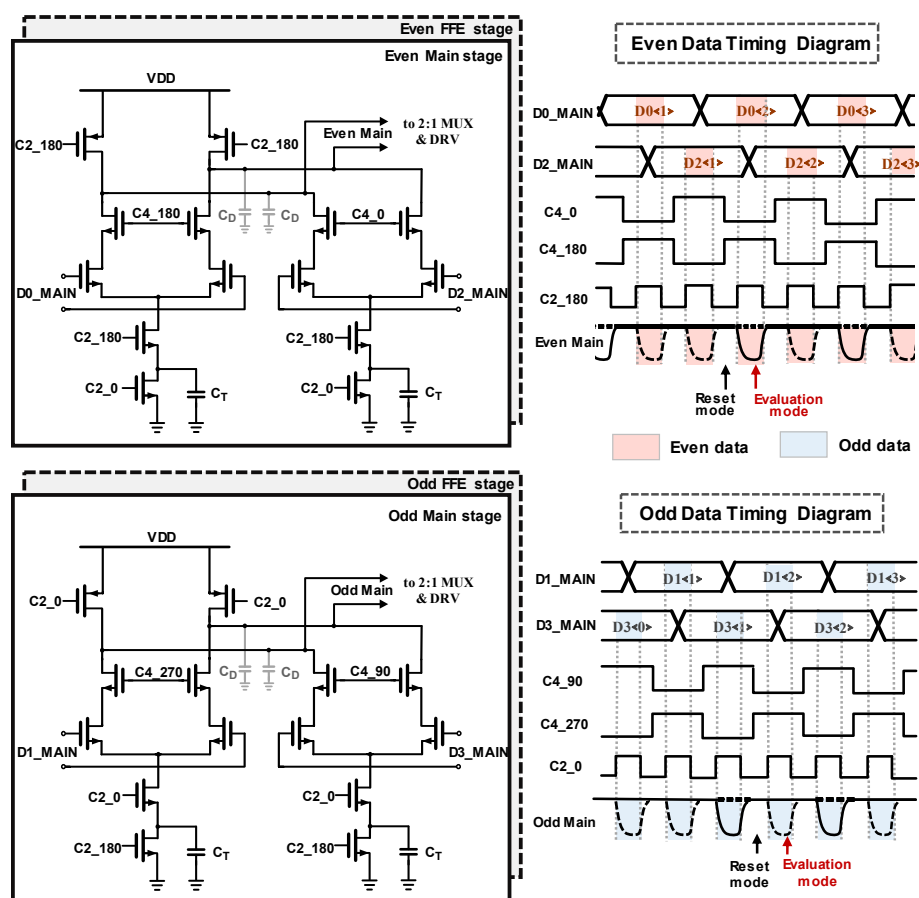


Figure 4. Circuit and timing diagram of the CSL-based 4:2 MUX.

In order to achieve efficient data processing and transmission, the circuit of the combined 2:1 MUX and driver with FFE is adopted and shown in Figure 5, where the last-stage 2:1 MUX is integrated with the output driver. Selected by C2_180 and C2_0, respectively, the even and odd paths of the data are serialized into the final full-rate data. As shown in the timing diagram of the main path in Figure 5, the driver samples the odd main data when C2_0 is high and samples the even main data when C2_180 is high. In this way, the even and odd paths of the data are multiplexed into the final full-rate data in the driver stage under the drive of the half-rate clock. Meanwhile, the tail currents of both the main and FFE path are controlled by four-bit digital signals to implement a programmable FFE weighting, which accommodate it for different channel responses. In this 2:1 MUX and driver combined circuit, the average current drawn from the power supply is the same as that of a conventional CML driver [15] for the same output signal swing, therefore saving the extra power consumption in the preceding 2:1 MUX shown in Figure 1b. It is worth noting that a current mode driver instead of an inverter-based voltage mode driver is chosen in this design because the output of the CSL-based MUX is a moderate-swing signal with a common-mode voltage closer to VDD. The output network consists of a 50-ohm loading resistor with a series peaking inductor, which extends the signal bandwidth with the presence of a parasitic capacitor at the driver output nodes. The series peaking technique has been proven to have a very good bandwidth extension ratio [16].

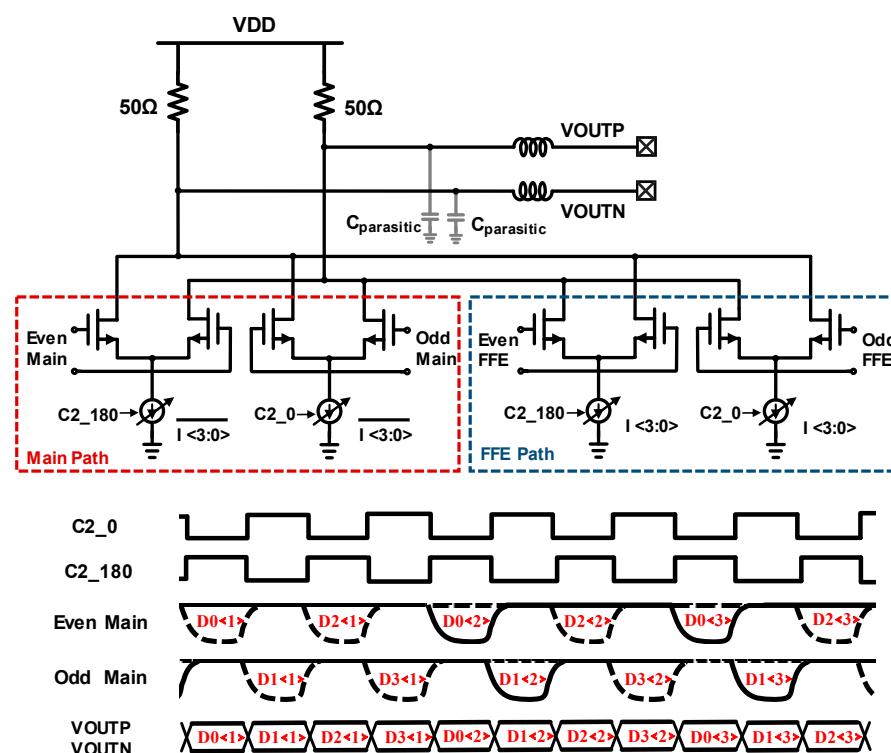


Figure 5. Circuit and timing diagram of the combined 2:1 MUX and driver with FFE.

4. Measurement Results and Discussion

The proposed NRZ transmitter is designed and fabricated with 28 nm CMOS technology. The chip micro-photograph is shown in Figure 6, with a core area of 0.032 mm², including all the blocks listed in the table on the right. For power integrity, decoupling caps are added on the chip between power supplies and the ground to mitigate the power supply ripples introduced by the bonding wire inductance.

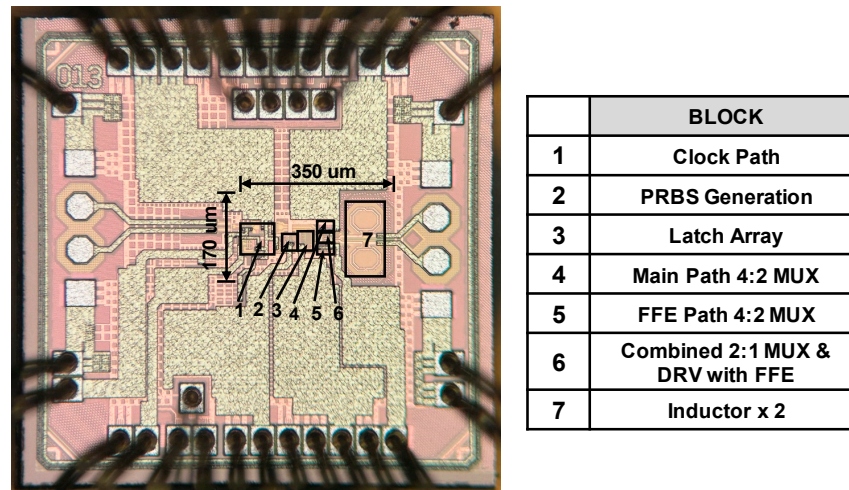


Figure 6. Chip micro-photograph.

The measurement setup is shown in Figure 7. The transmitter die is chip-on-board-packaged on a daughter board, which is mounted on an RF probe station for high-speed connection. The power supplies and control signals are generated on a motherboard and connected to the daughters through wires. The half-rate clock is generated by the Keysight E8257D, which is converted from single-ended to differential through a balun HL9405 with a bandwidth of up to 50 GHz. The clock signal is transmitted through connectors and cables, and is delivered to the RF probe (GGB Picoprobe 50A) with the same bandwidth of 50 GHz. The transmitter output data are measured through the 50A RF probe, 48-inch cables, DC blocks, and connectors of the real-time oscilloscope (Teledyne LeCroy 8590HD), which introduces 10 dB loss at 25 GHz.

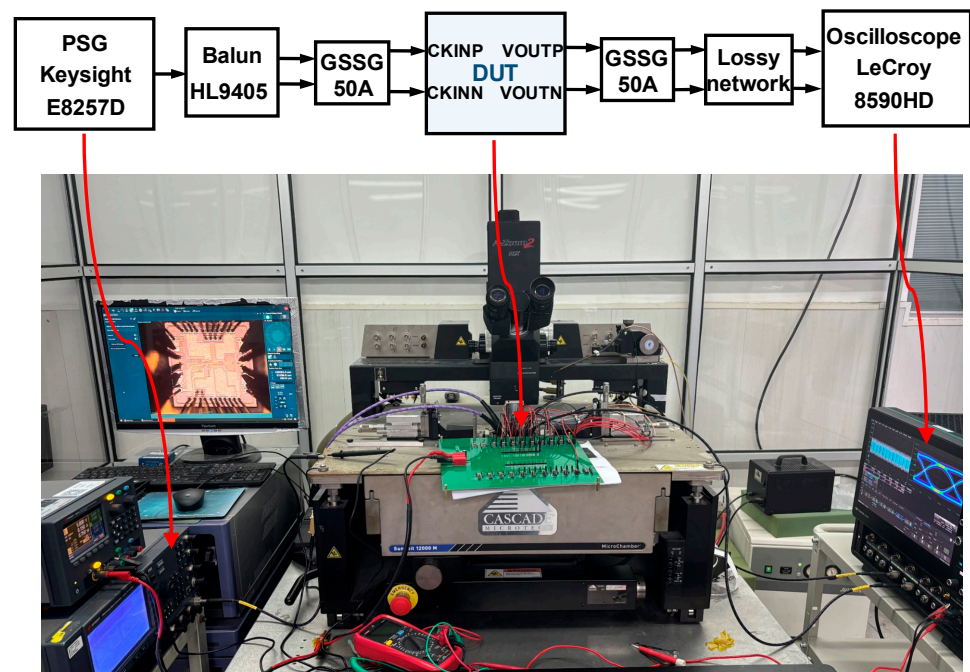


Figure 7. Measurement setup.

The measured eye diagrams of the proposed transmitter at a data rate of 30–50 Gb/s with and without FFE are shown in Figure 8. At the data rate of 30 Gb/s, the measured eye height increases from 150.2 mV to 231.5 mV and the measured eye width increases from 0.69 UI to 0.8 UI when FFE is turned on. At the data rate of 40 Gb/s, the measured

eye height increases from 77.7 mV to 168.7 mV and the measured eye width increases from 0.58 UI to 0.78 UI when FFE is turned on. When the data transmission rate is further increased to 50 Gb/s, the measured eye height increases from 22.9 mV to 111.2 mV and the measured eye width increases from 0.26 UI to 0.7 UI when FFE is turned on, as shown in Figure 8e,f. Meanwhile, the performances of the transmitter under various PVT corners were also verified in the post-simulation, which shows the reliability of this work.

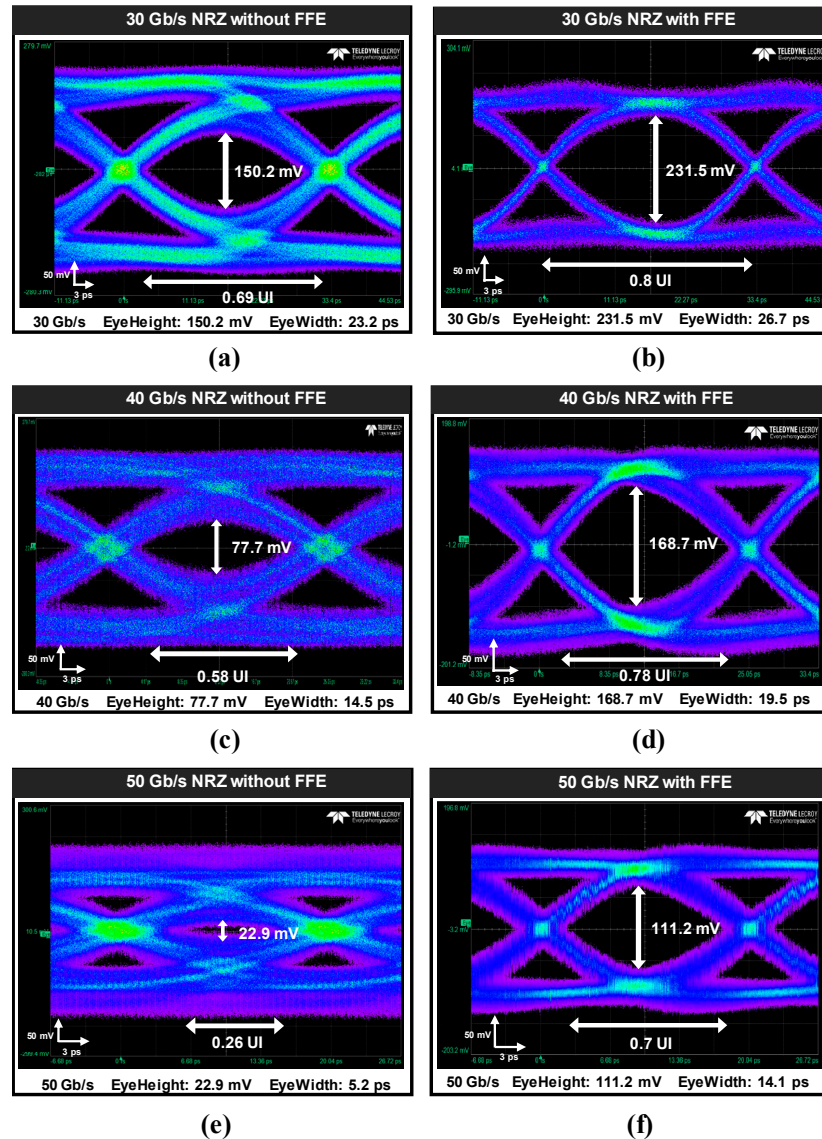


Figure 8. Measured transmitter output eye diagrams: (a) 30 Gb/s without FFE; (b) 30 Gb/s with FFE; (c) 40 Gb/s without FFE; (d) 40 Gb/s with FFE; (e) 50 Gb/s without FFE; (f) 50 Gb/s with FFE.

The frequency response of the transmitter output network in the measurement is shown in Figure 9a, showing a loss of 10 dB at the Nyquist frequency of 25 GHz. The power breakdown of the transmitter at 50 Gb/s is shown in Figure 9b. During the measure, by dividing the VDD of each module and testing the current flowing through each module, the corresponding power consumption can be calculated. Excluding the PRBS generator and clock path, the total power consumption in the data path is 21 mW, achieving an energy efficiency of 0.42 pJ/b.

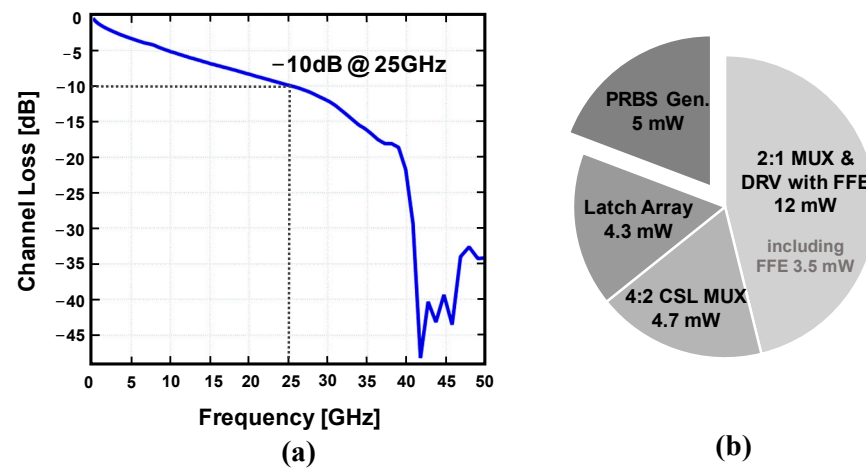


Figure 9. (a) Insertion loss of the transmitter output network. (b) Power breakdown in data path.

Table 1 summarizes and compares the measured performance of the designed transmitter with some state-of-the-art transmitters. The smallest core area combined with the lowest data path energy efficiency makes it a promising candidate for future die-to-die applications.

Table 1. Performance comparison of advanced transmitters.

	[11]	[12]	[14]	[17]	[18]	[19]	This Work
Process [nm]	65	28	28	14	28	28	28
Data rate [Gb/s]	40	128	35	64	32	32 64	50
Supply [V]	1.2	N/A	1.25	0.95	1	N/A	0.9
Signaling	NRZ	PAM4	PAM4	NRZ	PAM4	NRZ PAM4	NRZ
Driver Type	CML	CML	SST	CML	SST	SST	CML
Equalization	4-tap FFE	4-tap FFE	2-tap FFE	3-tap FFE	4-tap FFE	3-tap FFE	2-tap FFE
IL@Nyquist Frequency	6 dB	4 dB	5.2 dB	6 dB	N/A	11 dB	10 dB
Test PRBS length	7	N/A	7	31	N/A	N/A	7
Eye Height [mV]	180	44	101	N/A	38	180 36	111.2
Eye Width [UI]	0.68	0.2	0.68	N/A	0.16	0.6 0.36	0.7
Power * [mW]	74	115	166.85	139	37.7	56	21
Energy Efficiency * [pJ/bit]	1.85	0.9	4.76	2.1	1.178	0.875	0.42
Area [mm ²]	0.6	0.137	0.18	0.048	0.08	0.085	0.032

* The data path excluding clock path and PRBS generator. N/A means not reported.

5. Conclusions

This paper proposes a power- and area-efficient NRZ transmitter for XSR SerDes. At the system level, the final 2:1 MUX is combined with the driver to save the hardware and power consumption compared to traditional designs, and a simple single-inductance series peaking network effectively extends the signal bandwidth in the presence of the parasitic capacitance at the driver output nodes. At the circuit level, CSL-based moderate-swing signal processing further reduces the power consumption and inter-symbol interference. The prototype transmitter demonstrates a data path energy efficiency of 0.42 pJ/b with a core area of 0.032 mm² at a data rate of 50 Gb/s, which makes it a promising candidate for low-power and small-area XSR wireline communication applications such as chip-to-chip and die-to-die data interfaces.

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