

Article

Development of a New Solid State Fault Current Limiter for Effective Fault Current Limitation in Wind-Integrated Grids

Mohamed S. A. Zayed ^{1,*}, Hossam E. M. Attia ¹, Manal M. Emara ² , Diao-Eldin A. Mansour ^{3,4,*}  and Hany Abdelfattah ¹

¹ Electrical Department, Faculty of Technology and Education, Suez University, Suez P.O. Box 43221, Egypt; hossam.attia@ind.suezuni.edu.eg (H.E.M.A.); hany.abdelfattah@ind.suezuni.edu.eg (H.A.)

² Department of Electrical Engineering, College of Engineering, King Khalid University, Abha 61421, Saudi Arabia; memara@kku.edu.sa

³ Electrical Power and Machines Engineering Department, Faculty of Engineering, Tanta University, Tanta 31511, Egypt

⁴ Electrical Power Engineering Department, Faculty of Engineering, Egypt-Japan University of Science and Technology (E-JUST), New Borg El Arab City, Alexandria 21934, Egypt

* Correspondence: mohamed.arafat@ind.suezuni.edu.eg (M.S.A.Z.); mansour@f-eng.tanta.edu.eg (D.-E.A.M.)

Abstract

The increasing penetration of wind energy into modern power grids introduces new challenges, particularly regarding fault current levels and voltage stability during disturbances. This study proposes and evaluates a new Solid State Fault Current Limiter (SSFCL) topology for mitigating the adverse effects of faults in wind-integrated power systems. The proposed SSFCL consists of a bridge section and a shunt branch, designed to limit fault current while maintaining power quality. Unlike conventional SSFCLs, the proposed topology incorporates both DC and AC reactors with an Integrated Gate-Commutated Thyristor (IGCT) switch, to provide current limiting and voltage stabilization, effectively mitigating the negative impacts of faults. A comprehensive MATLAB/Simulink-based simulation is conducted on a realistic grid model. First, appropriate AC and DC reactor impedances are selected to balance fault current suppression, cost, and dynamic response. Then, three fault scenarios, transmission line, distribution grid, and domestic network, are analyzed to assess the fault current limiting performance and voltage sag mitigation of the SSFCL. In the simulation analysis, the DC reactor current and the voltage across the SSFCL device are continuously monitored to evaluate its dynamic response and effectiveness during fault and normal operating conditions. In addition, the fault current contribution from the wind farm is assessed with and without the integration of the SSFCL, along with the voltage profile at the Point of Common Coupling (PCC), to determine the limiter's impact on system stability and power quality. Finally, the performance of the proposed SSFCL is compared to that of the resistive-type superconducting fault current limiter (R-SFCL) under identical fault scenarios to assess the technical and economic standpoints of the proposed SSFCL. Simulation results show that the SSFCL reduces the peak fault current by up to 29% and improves the voltage profile at the PCC by up to 42%, providing comparable performance to the R-SFCL while avoiding the need for cryogenic systems.

Keywords: solid state fault current limiter; wind power integration; superconducting fault current limiter; power quality; voltage sag mitigation



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1. Introduction

The global transition toward sustainable energy systems has significantly increased the penetration of renewable energy sources (RESs), such as wind and solar, into modern electrical power grids. This shift not only enhances energy diversity by reducing reliance on fossil fuels but also contributes to climate change mitigation by lowering greenhouse gas emissions and promoting cleaner production cycles [1]. Moreover, integrating renewables improves energy security by diversifying the energy mix and reducing the vulnerability of national grids to uncontrolled prices and possible supply disruptions of conventional fuels. In parallel with centralized deployment, RESs are increasingly being integrated into decentralized systems such as microgrids [2,3]. Among the various RESs, wind energy has emerged as one of the most extensively deployed technologies worldwide due to its scalability, technological maturity, and declining cost of generation.

1.1. Challenges to Wind Energy Integration

Large-scale wind farms are now a common feature in both developed and developing countries, contributing significantly to national energy mixes. Its ability to be installed at utility scale, coupled with supportive policies and advancements in turbine efficiency, has made wind energy a basis of the global clean energy transition.

However, the intermittent and stochastic nature of wind energy introduces significant operational challenges to power system stability and reliability. One major challenge is the occurrence of voltage and frequency deviations [4,5], which result from the mismatch between fluctuating wind energy generation and real-time load demand, particularly in weak or poorly interconnected grids. In addition, wind energy systems that employ power electronic converters contribute minimal inertial response, thereby making frequency regulation more difficult during disturbances [6]. A second critical challenge is the potential increase in fault current levels [7]. These elevated fault currents can exceed the design limits of conventional protection devices and complicate coordination among protection schemes. Another challenge is harmonic distortion, which is commonly introduced by the switching operations of converter-based wind energy [8]. These harmonics degrade power quality, damage sensitive equipment, and increase system losses in distribution networks [9].

Among the various operational challenges associated with wind energy integration, the increase in fault current levels is widely regarded as one of the most critical. Unlike voltage or harmonic issues, which degrade power quality over time, excessive fault currents can cause immediate and catastrophic equipment damage. This is because fault currents directly impact the safety, reliability, and protection coordination of power systems. In conventional grids, protection devices such as circuit breakers and relays are designed based on anticipated fault levels derived from synchronous generators. However, with the integration of wind energy, the aggregate fault current contribution can exceed the interrupting capacity of existing protection equipment, risking equipment failure, potential outages, or even cascading faults. Therefore, limiting fault currents becomes essential for protecting infrastructure, ensuring safety, and enabling the secure operation of wind energy-integrated grids [10].

1.2. Superconducting Fault Current Limiters' Progress

Superconducting Fault Current Limiters (SFCLs) have been widely used to manage fault currents in wind-integrated power systems. SFCLs utilize the unique properties of high-temperature superconductors, which exhibit near-zero resistance under normal operating conditions but transition to a resistive state when exposed to excessive current. In [11], an SFCL was implemented in an offshore wind farm connected to two feeders to enhance Low Voltage Ride-Through (LVRT) capability. Without the SFCL, the point of

common coupling (PCC) voltage dropped to approximately 0.7 pu during the fault, leading to the disconnection of the offshore wind farm from the grid at 2.37 s. When the SFCL was applied, the PCC voltage sag was reduced to 0.86 pu, which extended the wind farm's grid connection to 3 s. To further ensure continuous operation, the overcurrent relay at the feeder head was adaptively reset to account for the limited fault current, successfully isolating the faulted feeder at 2.8 s. This sequence allowed the offshore wind farm to remain connected, fully complying with grid code requirements.

In [12], the study utilized the IEEE 4-machine 2-area benchmark system to assess a grid-connected wind power generation system using power system stabilizer (PSS), R-SFCL, and Static Synchronous Compensator (STATCOM). An index called Sum of Maximum Deviations (SMD) was used for evaluation, which is based on the sum of mean deviations for all machines with reference to the slack bus. Without R-SFCL, the SMD was 1280.3, whereas PSS could decrease it to 1270.5. Adding a 20 Ω R-SFCL could decrease SMD to 973.6 when placed at Bus L9, which is the best location. A further reduction in SMD was observed when the R-SFCL and PSS were combined with a STATCOM.

In [13], a superconducting saturated core fault current limiter was proposed to enhance the Fault Ride-Through (FRT) capability of Doubly Fed Induction Generator (DFIG)-based wind energy systems. Without the limiter, the PCC voltage dropped to zero and remained at that level for 150 ms, resulting in severe consequences such as a rotor current rise to 4.91 pu, far exceeding the safety limit of 2.0 pu. During the fault condition, the limiter introduced additional inductive reactance, effectively limiting the rotor current to 1.693 pu, thereby keeping it within safe operating limits and ensuring continuous system operation.

In [14], a R-SFCL was evaluated in a DC microgrid incorporating a Permanent Magnet Synchronous Generator (PMSG) to assess its effectiveness during solidly grounded DC-bus faults. Without the SFCL, the DC output current of the PMSG converter increased from approximately 115 A to 215 A, and the DC voltage collapsed to zero, remaining at zero for nearly 0.4 s after fault clearance. When a 3 Ω R-SFCL was introduced, the fault current was constrained to 159 A, and the voltage drop was limited to 20% of the nominal, thereby maintaining nearly 80% of the rated DC voltage. This allowed for uninterrupted power injection and ensured compliance with grid-code FRT requirements. Additionally, the peak three-phase fault current reached 282 A (220% of nominal) without the SFCL, but was significantly mitigated with the R-SFCL, indicating effective current limiting without compromising the generator's operational stability. In [15], a coordinated control scheme was proposed combining R-SFCL with adaptive control for a PMSG-based wind turbine. Simulation results under severe fault conditions (90% voltage sag) showed that the uncontrolled system experienced a 5.45 pu DC-link overvoltage, whereas the SFCL-only and coordinated approaches limited the overvoltage to 1.10 pu and 1.17 pu, respectively. For milder faults (30% voltage sag), the coordinated strategy stabilized the DC-link voltage within 1.05 pu and prevented converter tripping. Furthermore, whereas SFCL-only caused the grid side converter to inject 2.5 MW, the coordinated technique moderated output to 1.24 MW with reactive support and reduced superconducting tape length from 8825.5 m to 5042 m, demonstrating enhanced stability, FRT compliance, and cost-effectiveness.

In [16], a resistive-type SFCL was used in a DC microgrid incorporating a wind farm, a Photovoltaic (PV) system, and battery storage. Without SFCL, a DC fault increased the current to 6.16 kA and reduced the bus voltage to 30 V, preventing FRT. With an SFCL of 5 Ω , the fault current was reduced to 2.26 kA (63.3% decrease), while the bus voltage recovered to 251 V (about 62.7% of nominal), allowing renewable sources to comply with FRT standards. Furthermore, the microgrid maintained 40 kW of power transmission throughout the fault, proving the SFCL's dual role in fault current suppression and voltage sag compensation. To improve transient stability in standalone hybrid wind/PV microgrids,

Ref. [17] proposed a novel SFCL insertion topology that is only connected in series with the faulty phase. Compared to the old technique, the suggested scheme decreased wind generator speed oscillations from $\pm 6\%$ to less than $\pm 1\%$ and limited active power variations during the fault from $+80/-40$ kW to $+27/+12$ kW. Reactive power fluctuations were reduced from a $-5/-45$ kVAR range to a $-7/-17$ kVAR range. Bus voltages across the microgrid recovered quickly in 0.01 s compared to nearly 1 s without using SFCL. The results show that the suggested topology delivers higher stability, quicker voltage recovery, and improved overall microgrid power quality with no additional hardware costs.

In [18], the authors addressed FRT enhancement in a meshed microgrid integrating Virtual Synchronous Generator (VSG)-controlled wind and PV units. By optimally placing both an SFCL and a Superconducting Magnetic Energy Storage (SMES) unit using a particle swarm optimization algorithm, the proposed strategy reduced voltage drops by 88.7%, power fluctuations by 56.94%, and peak fault current to 9.68 pu. These outcomes highlight the benefit of coordinated usage of SFCL and SMES for improving dynamic stability and fault tolerance across varying fault locations.

Despite their technical effectiveness, SFCLs involve high capital and operational costs due to the use of superconducting materials and the requirement for continuous cryogenic cooling [19]. To address these cost challenges, researchers have focused on developing multifunctional superconducting devices that combine fault current limiting with other functions. In [20], a Superconducting Fault Current Limiting Transformer (SFCLT) was proposed and proposed to simultaneously perform voltage transformation and fault current limiting in a 50 MW wind farm, thereby reducing system costs. For a single line-to-ground fault, the SFCLT limited the first peak of the primary side fault current to 12.7 kA from a prospective 15.1 kA (an 15.9% reduction) and further suppressed the current to 54% of the steady-state fault current during the fault period, while the secondary side current was reduced from 2 kA to 1 kA. In a large-scale 29 GW power system model, the SFCLT improved stability by reducing frequency excursions during faults from 380 mHz (without SFCLT) to 110 mHz (with SFCLT).

Another multifunctional Superconducting Magnetic Energy Storage-Fault Current Limiter (SMES-FCL) was introduced in [21], combining energy storage and fault current limiting capabilities for wind farm applications. In a 50 kW wind generator system, the SMES-FCL smoothed output power fluctuations while limiting the first peak of fault current from 6 kA (without SMES-FCL) to 0.5 kA and reducing the sustained fault current to 0.23 kA. Additionally, it prevented voltage collapse during faults, maintaining generator terminal voltage near zero sag, thus improving the system's fault ride-through capability and compliance with grid codes. However, despite these multifunctional superconducting solutions, the cost and operational complexity of cryogenic systems remain a barrier, prompting researchers to explore alternative technologies such as Solid State Fault Current Limiters (SSFCLs) for wind energy applications.

1.3. Solid State Fault Current Limiters' Progress

Several studies have investigated the integration of SSFCLs in wind energy-based power systems to enhance fault ride-through capability and system resilience. In [22], a comparative analysis was conducted between the Series Dynamic Braking Resistor (SDBR) and a Resistive-type Solid State Fault Current Limiter (R-SSFCL), both using an Insulated-Gate Bipolar Transistor (IGBT) switch, to enhance the (LVRT) capability of DFIG-based wind farms. Simulation results demonstrated that the R-SSFCL maintained the PCC voltage at around 0.91 pu during a three-phase fault while greatly minimizing fault current surges up to three times normal. Furthermore, it efficiently regulated the DC-link voltage, keeping it from rising above 2190 V compared to the nominal 1200 V, and maintained a stable

machine speed with fewer oscillations. Unlike the SDBR or the case without FCL, the R-SSFCL maintained the generated active power near its nominal value rather than falling to zero, demonstrating greater transient stability performance.

In [23], two SSFCLs are analyzed and evaluated in a MATLAB/SimPower-modeled radial distribution network. The first topology, a Current-Controlled Fault Current Limiter (CCFCL), utilizes a thyristor-controlled inductive branch in combination with an IGBT switch. The second, referred to as the Fault Current Limiting and Interrupting Device (SSFCLID), incorporates IGBT switches, a Metal Oxide Varistor (MOV), and snubber circuits. Both devices were tested under a severe 7 kA short-circuit condition. Although each successfully limited the fault current to 600 A within 0.08 s, the SSFCLID demonstrated superior performance. Specifically, it achieved a lower voltage sag at the PCC, reducing it to just 1.3% compared to 4.6% in the CCFCL case. Moreover, it significantly decreased harmonic distortion (57% THD vs. 94.6%) and conduction energy losses (44 J vs. 76 J).

In [24], an SSFCL topology was presented, as depicted in Figure 1a, featuring a full-bridge diode configuration in series with a self-turn-off IGCT (Integrated Gate-Commutated Thyristor) and a shunt path comprising an inductor and variable resistor. Under normal conditions, the IGCT remains closed, and the current flows through alternating diodes depending on the voltage half-cycle. Upon fault detection, the IGCT is turned off, diverting the fault current through the inductive shunt, thereby limiting the fault magnitude. This configuration was implemented in a wind-turbine-connected distribution network using MATLAB/Simulink, demonstrating its effectiveness in reducing voltage sag during faults from nearly zero to 0.7 pu and limiting peak fault current from 6.74 pu to near nominal levels. This study was later expanded in [25], where the SSFCL was integrated into a more complex distribution system consisting of multiple wind turbine generators, where a detailed investigation was carried out on the transient behavior of the SSFCL under different fault conditions and was further validated through a small-scale experimental prototype. A similar SSFCL topology was used in [26], as shown in Figure 1b, to improve the transient stability of a DFIG-based wind farm under various fault conditions. However, this approach introduces abrupt current transitions when the switch opens, resulting in high di/dt , potential current overshoots, and elevated stress on the IGBT and diodes, especially under millisecond-level switching, potentially leading to thermal degradation or device failure under repetitive faults.

An alternative SSFCL configuration using a bridge with a DC reactor and internal resistor was proposed in [27], as illustrated in Figure 1c. During steady-state, the inductor is charged to the peak line current, and thus the current is bypassed via diodes. During fault conditions, the increase in the current magnitude redirects the current to the DC reactor branch, thereby limiting the fault current. Nonetheless, the reactor gradually saturates over multiple cycles, reducing its current-limiting efficacy in sustained faults. Additionally, post-fault recovery may cause overvoltages due to inductor discharge, and sudden current diversion can induce voltage spikes. To address these drawbacks, the study in [28] modified the design by placing a diode parallel with the DC reactor—resistor and a high-speed IGBT switch in series with the DC reactor—resistor, as shown in Figure 1d. During normal operation, the IGBT is closed to prevent the shunt impedance path, and the bridge part of the fault current limiter ideally provides zero impedance for the line current, while during a fault, it opens to insert the inductive—resistive path, enhancing current limiting. Despite improvements, this design still suffers from abrupt current shifts, high di/dt , and thermal stresses on IGBT and operating diodes until transition. Additionally, prior studies didn't evaluate the performance of SSFCLs in realistic, renewable-integrated distribution feeders, such as those incorporating wind energy systems.

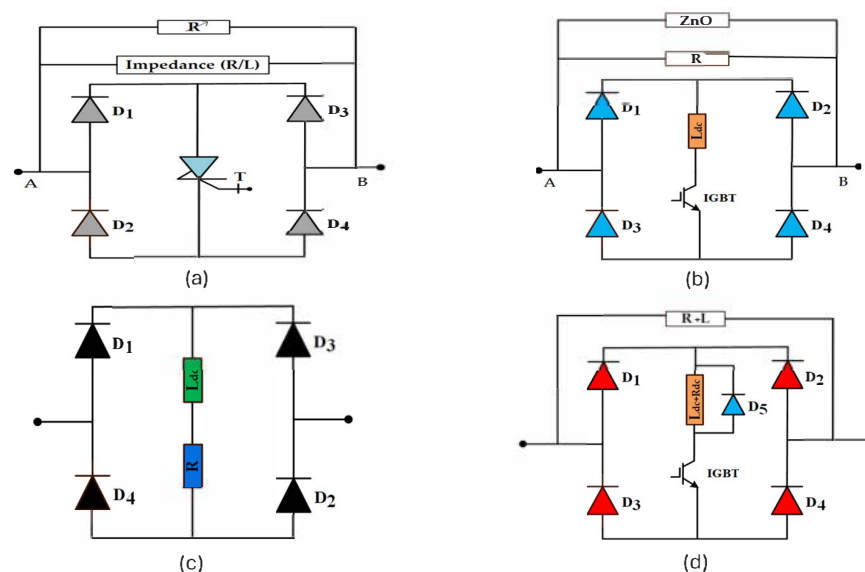


Figure 1. Schematic diagram of various SSFCL topologies from previous research: (a) SSFCL topology in [24,25], (b) SSFCL topology in [26], (c) SSFCL topology in [27], (d) SSFCL topology in [28].

1.4. Research Gap and Contribution

This paper presents a new SSFCL (SSFCL) topology designed to overcome the limitations of conventional SSFCL topologies in wind energy-integrated power systems. The topology incorporates both DC and AC reactors, together with an IGCT switch, to provide dual-stage current limiting and voltage stabilization, effectively mitigating the negative impacts of faults. Furthermore, the design includes a coordinated control strategy to optimize the operation of the IGCT switch, ensuring smooth current transition and minimizing device stress. To validate its effectiveness, the proposed SSFCL is benchmarked against the conventional R-SFCL, highlighting its advantages in suppressing fault currents, reducing voltage sags, and facilitating system recovery. The results demonstrate the suitability of the proposed SSFCL as a high-performance and scalable solution for enhancing the fault resilience of renewable-rich smart grids. The benefits of the proposed SSFCL can be further enhanced by the latest generations of components, notably Silicon Carbide (SiC) switching devices, that offers superior switching speed, thermal stability, and reduced conduction losses compared to silicon-based counterparts.

The main contribution of the current research can be summarized as follows:

- Proposing a Solid State Fault Current Limiter (SSFCL) optimized for wind energy-integrated power systems, incorporating a dual-reactor configuration (AC and DC reactors) to achieve both fault current limitation and voltage sag mitigation, improving system stability during symmetrical faults.
- Validating the effectiveness of the proposed SSFCL through detailed MATLAB/Simulink simulations under different fault locations, including transmission-level faults, distribution network faults, and domestic load faults.
- Conducting a comparative performance analysis between the proposed SSFCL and a conventional R-SFCL, evaluating fault current suppression, voltage recovery, and dynamic system response.

This paper is organized as follows: Section 2 presents the power system model incorporating wind energy as a distributed generation source, illustrated through a single-line diagram. Section 3 describes the circuit structure and operating principles of the proposed SSFCL and explains its operational behavior. Section 4 provides a detailed demonstration and analysis of the simulation results, highlighting the effectiveness of FCL installation

under various scenarios. Section 5 presents a comparative study between the R-SFCL and the proposed SSFCL, evaluating their performance for the identified fault scenarios. Finally, Section 6 summarizes the conclusions of the study.

2. Power System Modeling and Wind Farm Integration

The modeled power system, illustrated in Figure 2, was extracted from [29] to facilitate a performance comparison with the R-SFCL. It represents a typical electric transmission and distribution network and was developed using MATLAB/Simulink R2024a software. The system includes a three-phase synchronous generator representing a 120 MVA conventional power plant operating at a rated line-to-line RMS voltage of 20 kV. This conventional power station supplies a 100 MW local load. Power from the generator is transmitted through 200 km of 154 kV three-phase π -section transmission lines, connected via the primary transformer TR1.

To maintain voltage stability under normal operating conditions, a static var compensator is installed near substation TR2, which steps the voltage down from 154 kV to 22.9 kV. This voltage regulation is essential to counteract the voltage drop caused by the long-distance transmission lines and reactive power demands. From TR2, the system branches into two independent distribution networks. The first branch supplies a high-power industrial load rated at 6 MW and 2 MVAR, while the second branch feeds three domestic low-power loads, each rated at 1 MW active power and 0.3 MVAR reactive power. The wind farm is connected directly to the second branch through transformer TR3, providing additional power to both the industrial and residential loads.

The wind farm has a total capacity of 9 MVA, consisting of six fixed-speed induction-type wind turbines, each rated at 1.5 MVA. The detailed configuration and parameters of the system components are summarized in Table 1.

When the wind farm is connected to the grid, the fault current levels increase, leading to a more pronounced voltage sag during fault events. This additional current contribution from the wind farm can reduce overall system reliability by stressing protection devices and negatively affecting voltage stability issues [30,31]. Therefore, the use of Fault Current Limiters (FCLs) has become crucial for mitigating these adverse effects. The role and operation of FCLs in this system are further detailed in Section 3. The considered fault scenarios include a transmission line fault on the 200 km high-voltage line, a distribution grid fault near Domestic Load 3, and a domestic load fault at Domestic Load 1. These cases represent typical disturbances at different voltage levels and locations to assess the system's response and the effectiveness of FCL deployment. The proposed SSFCL is placed at the PCC, which has been identified as the most effective location for fault current mitigation across the three fault scenarios when using R-SFCL [29]. This strategic placement ensures that the fault current contribution from the wind farm is effectively suppressed at the network interface, thereby minimizing voltage sags and limiting the stress on downstream protection devices. By reducing the peak fault current and stabilizing voltage profiles, the SSFCL installation at the PCC significantly enhances the system's fault ride-through capability, improves power quality, and ensures better overall grid reliability and operational stability under fault conditions. Figure 3 illustrates the effect of a three-phase fault at the distribution grid on the network with and without wind farm integration. The fault is initiated at 0.2 s and sustained for 0.1 s. The fault current waveforms, measured downstream to the domestic loads at the limiter location, reveal that incorporating the wind farm leads to a noticeable increase in the fault current peak, from approximately 2.8 kA without the wind farm to 3.23 kA with it.

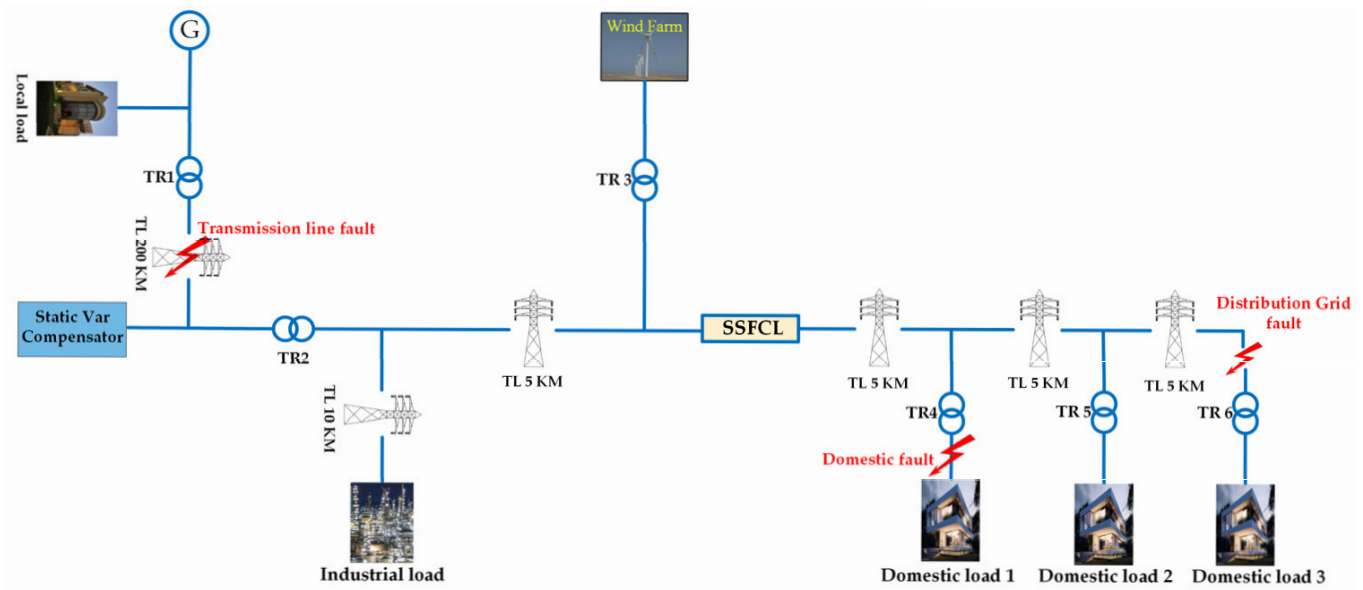
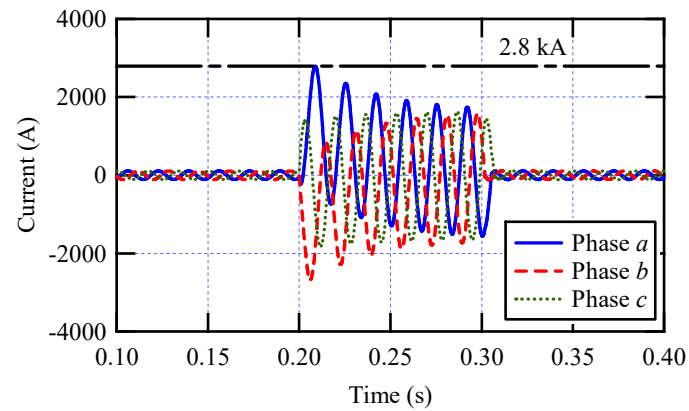
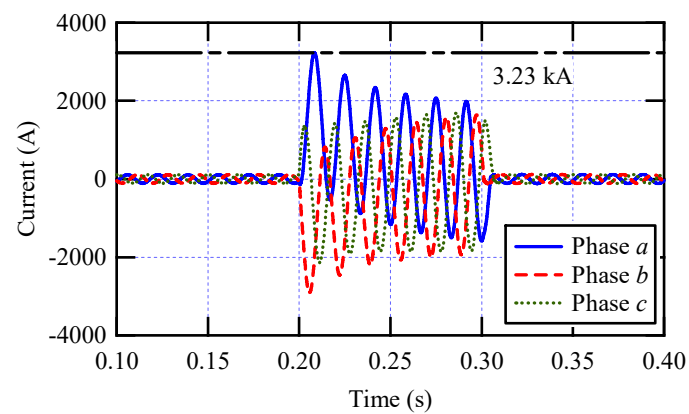


Figure 2. Single-line diagram of the modeled transmission and distribution system used for evaluating the proposed SSFCL performance.



(a)



(b)

Figure 3. The effect of the distribution grid fault on the network (a) without wind farm integration, (b) with wind farm integration.

Table 1. Simulation parameters for the Power System Model under testing.

Parameter	Value	Unit
Generation Sources		
Synchronous generator		
Nominal power	120	MVA
Line-to-line voltage (RMS)	20	kV
Frequency	60	Hz
Wind farm		
Nominal power	1.5×6	MVA
Line-to-line voltage (RMS)	575	V
Frequency	60	Hz
Transformers		
Step-up transformer (TR1)	20/154	kV
Step-down transformers (TR2)	154/22.9	kV
Step-up transformer (TR3)	575/22.9	V/kV
Step-down transformer (TR4, TR5, TR6)	22.9/6	kV
Load demand		
Local load	100	MW
Power factor	Unity	-
Industrial demand	6/2	MW/MVAR
Power factor	0.95	-
Domestic loads (1, 2, 3)	1/0.3	MW/MVAR
Power factor	0.96	-
line impedance	$0.01273 + j0.35197$	Ω/kM

3. Circuit Structure and Operational Behavior of the Proposed SSFCL

Figure 4 illustrates the single-phase equivalent circuit of the proposed SSFCL. The topology is composed of two primary functional parts:

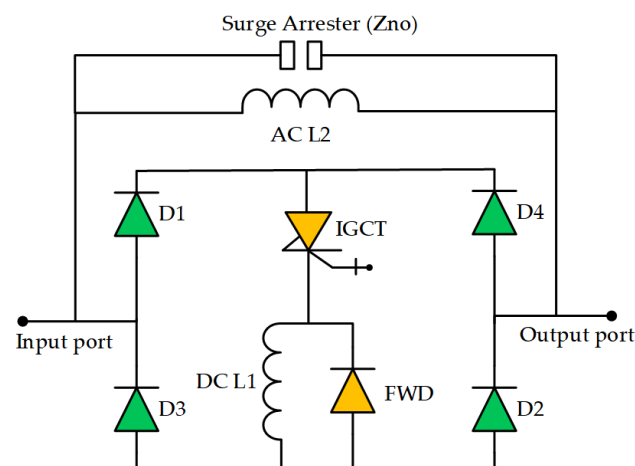


Figure 4. Schematic diagram for the proposed SSFCL topology, featuring an AC reactor for fault current limitation and a parallel ZnO arrester for overvoltage suppression during fault recovery.

- **Bridge part**

The bridge section comprises a non-superconducting DC reactor (L_1), a Freewheeling Diode (FWD), a high-power IGBT serving as a controllable switch, and a semiconductor rectifier bridge consisting of diodes D1 to D4. Under normal conditions, the IGBT is fully

turned on, allowing the line current to flow through the bridge rectifier and the DC reactor without interruption. In the positive half-cycle, the current path is through D1, D2, and L1, while in the negative half-cycle, it flows through D3, D4, and L1. The IGCT symbol in the circuit diagram generically represents a high-power, gate-controlled switch. While IGCTs were historically associated with silicon technology, recent advancements have enabled the development of IGCTs using SiC as discussed in prior studies [32].

Since the DC reactor carries the current in the same direction during both half-cycles, it functions as a current smoothing element, minimizing ripple [33]. Figure 5 shows the Total Harmonic Distortion (THD) of the voltage at the PCC, demonstrating that the proposed SSFCL does not introduce significant harmonic distortion under steady-state conditions. The resulting THD remains within the IEEE 519-2022 standard limits [34], confirming that the proposed SSFCL topology meets the power quality requirements. Additionally, under normal load conditions, the DC reactor L1 behaves as a near-short circuit due to the nearly constant di/dt , resulting in minimal voltage drop, except for the small conduction losses across the semiconductor devices. For proper arrangement of the semiconductor devices to handle the expected voltage and current stresses, the IGCT used in the DC bridge is selected based on its high current-carrying capacity, typically in the range of several kiloamperes. As the main controllable switching element, it is rated to withstand the peak fault current anticipated in the system. To protect the IGCT during turn-off events, a snubber circuit is implemented across its terminals to suppress voltage transients and reduce switching losses. The rectifier bridge diodes (D1–D4) can be based on SiC technology due to their superior reverse blocking voltage capability and high thermal conductivity. To achieve the required voltage withstand level, multiple diodes are connected in series per leg.

During fault conditions, the IGCT operates as a high-speed, solid state switch, quickly turning off upon receipt of a fault signal. This action redirects the fault current away from the bridge and forces it into the shunt path, thereby relieving stress on the semiconductor devices. Although the DC reactor is placed in series with the switch, its inductance is deliberately selected to be small, ensuring it does not significantly delay the switch opening time. The bridge-type configuration enhances the current interruption capability and improves system reliability while minimizing main circuit costs, as it utilizes only one controllable switch on the DC side.

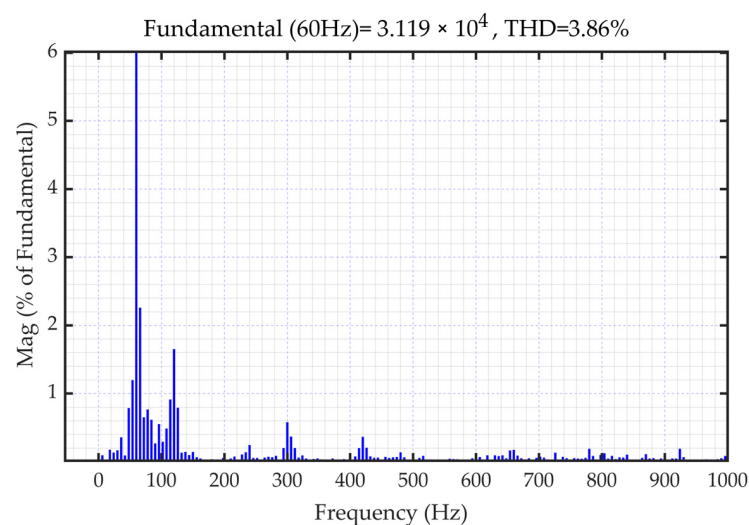


Figure 5. The (THD) of the voltage profile at the PCC, using MATLAB Simulink.

The proposed SSFCL could further benefit from the use of SiC switches, which offer significant advantages in switching speed, blocking voltage capacity, and current density, thereby enabling more compact designs with lower thermal management requirements.

These collective advantages make SiC-based switches highly suitable for fault current limiting applications, improving their reliability in electrical networks [35–38].

- The shunt branch part

The shunt branch consists of a bypass reactor (L2) and a Zinc Oxide (ZnO) surge arrester connected in parallel. When a fault occurs, the current is diverted from the main bridge into L2, which provides a high-impedance path to suppress the magnitude of the fault current. The ZnO arrester serves as an overvoltage protection device during fault current interruption. When the circuit attempts to stop a large current abruptly, voltage transients can occur, potentially damaging sensitive components. The ZnO arrester remains in a high-impedance (OFF) state during normal operation but transitions to a low-impedance (ON) state when the voltage exceeds its conduction threshold, thereby clamping the overvoltage and protecting the commutation circuit.

Additionally, a FWD is connected in parallel with the DC reactor (L1). This diode provides a safe path for the stored energy in L1 to dissipate gradually, allowing the reactor current to decay smoothly to zero over approximately one cycle, avoiding sudden interruptions that could cause voltage spikes.

4. Simulation Results and Discussion

The simulation model of the proposed SSFCL incorporates key component parameters that must be carefully selected to ensure reliable operation and seamless integration with the overall power system. These parameters include the AC and the DC reactor impedances. The AC reactor impedance was selected to maximize fault current suppression while avoiding excessive increases in cost, physical size, and reactive power losses. As illustrated in Figure 6, increasing the AC reactor impedance leads to a marked and nearly linear improvement in fault current limitation up to a certain threshold. However, beyond an impedance value of approximately 20 Ω , the curve begins to flatten, indicating a region of performance saturation. In this range, additional increases in impedance result in only marginal gains in current limiting effectiveness. Consequently, an AC reactor impedance of 20 Ω was selected for the proposed SSFCL design. In parallel, the DC reactor was configured with an impedance of 0.11 Ω , which effectively smooths current ripples and supports a rapid transient response, enabling the SSFCL to recover swiftly following fault clearance.

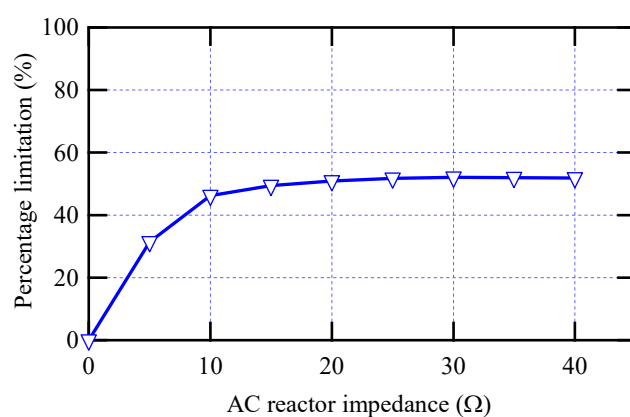


Figure 6. Effect of AC reactor impedance on fault current limitation percentage in the proposed SSFCL design.

To assess the fault current limiting capability of the proposed SSFCL, a three-phase symmetrical fault, the most severe type of electrical fault, was applied at the considered locations in the network. This fault scenario serves as a benchmark for evaluating the limiter's ability to reduce excessive fault currents and mitigate associated voltage sags. By

focusing on this worst-case fault, the effectiveness and robustness of the SSFCL design can be validated.

4.1. Case Study 1: Transmission Line Fault

Transmission lines are typically well-engineered and elevated to minimize their exposure to external disturbances, making them less susceptible to faults compared to other parts of the power network. Nevertheless, when a fault does occur, such as a three-phase symmetrical short circuit, it results in a substantial surge in fault current. This is particularly critical in hybrid generation systems, where both the wind power plant and the conventional synchronous generator contribute significant fault current magnitudes.

In this scenario, the fault current is simultaneously injected from both generation sources: the wind farm, through the substation and into the transmission line, and the conventional plant, directly toward the fault location. The convergence of these two sources amplifies the stress on the transmission system and its protection devices. Under steady-state (normal) conditions, the DC reactor current exhibits a relatively constant value over time, as depicted in Figure 7. However, the occurrence of a transmission line short circuit causes a sudden collapse in this value toward zero.

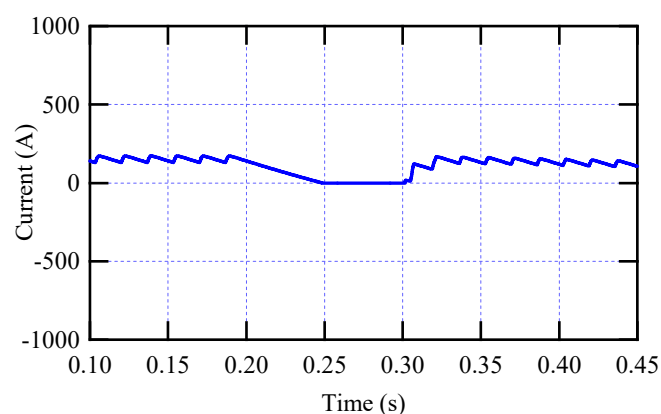


Figure 7. DC reactor current in case of transmission line fault.

The voltage drop across the SSFCL under normal and fault conditions is depicted in Figure 8. During normal operation, the SSFCL introduces a slight voltage drop of approximately 542 V, equivalent to 0.024 pu. This minimal drop is primarily due to the conduction losses across the power electronic components, particularly the IGCT and associated diodes, within the device's bridge circuit. Despite being measurable, this drop is considered negligible in terms of its impact on overall power quality and remains well within acceptable limits.

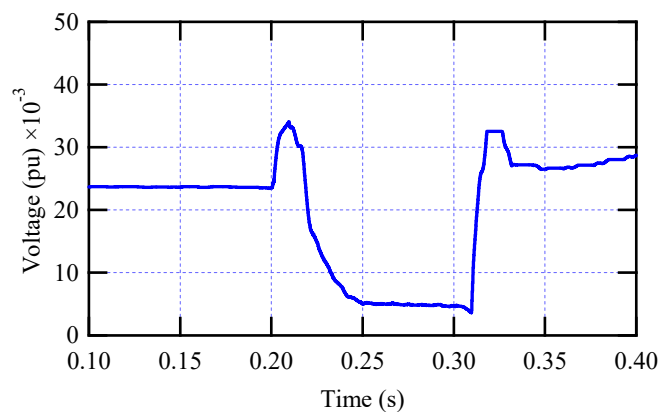


Figure 8. The voltage drop across the proposed SSFCL in case of transmission line fault.

Following the onset of the fault at 0.2 s, a noticeable voltage sag occurs across the system. Although the SSFCL is located outside the primary path of the fault current, it still experiences a slight voltage drop during the fault period. This behavior is due to the distribution of current paths governed by the impedance of each branch. Because the impedance toward the fault is significantly lower than that toward the load, the majority of the current flows toward the faulted section, while a small portion continues to flow toward the loads, causing a minor voltage drop across the SSFCL.

The fault current contribution from the wind farm reveals approximately no difference with and without the SSFCL device, as shown in Figure 9. This is because the SSFCL is not positioned within the primary fault current path for this specific fault scenario. Consequently, the SSFCL does not actively engage in current suppression. Similarly, as depicted in Figure 10, no improvement in the voltage profile at PCC is observed under this fault condition.

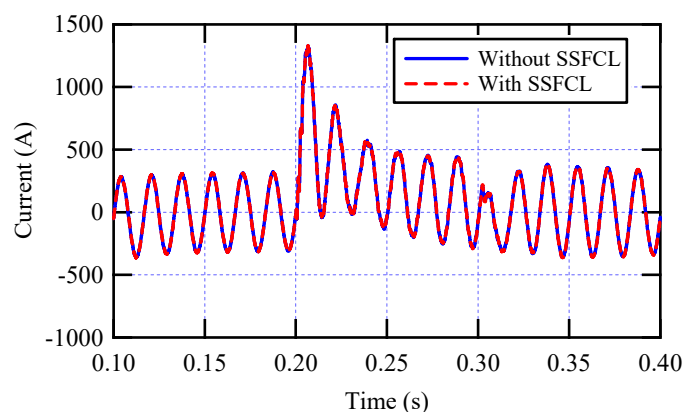


Figure 9. The fault current contribution from the wind farm with and without the proposed SSFCL in case of transmission line fault.

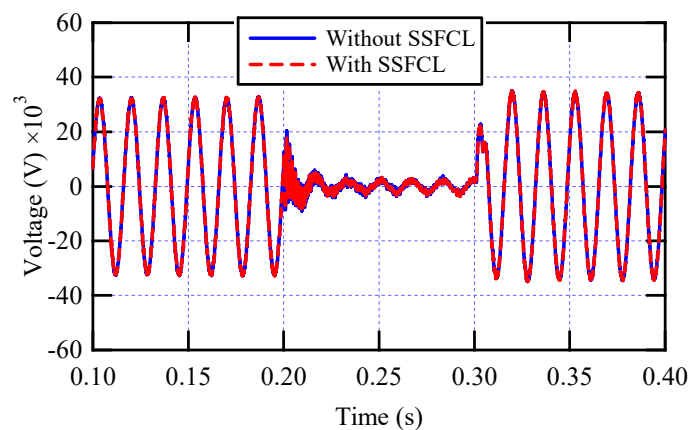


Figure 10. The voltage profile at PCC with and without the proposed SSFCL in case of transmission line fault.

4.2. Case Study 2: Distribution Grid Fault

In contrast to transmission lines, which are usually found in open and remote locations, distribution networks are more vulnerable to fault events. This susceptibility arises from the proximity of distribution feeder lines to densely populated urban areas and other environmental elements that increase the likelihood of short circuits, insulation failures, and mechanical damage.

The simulation results reveal consistent behavior of the proposed SSFCL under normal operating conditions, similar to the observations in the first case study. However, a notable

difference is observed during fault conditions, as illustrated in Figure 11, particularly at the moment of fault clearance at 0.3 s. At this instant, the system experiences a sharp current overshoot due to the abrupt transition from faulted to post-fault operation. This sudden increase in current is due to the abrupt reconnection of the DC reactor as the system's need to re-establish continuity of current. Following this peak, the current gradually decreases until it settles back into steady-state conditions.

This fault scenario results in a significant voltage drop across the SSFCL between 0.2 and 0.3 s, as illustrated in Figure 12, indicating a severe condition for the limiter. To safeguard the limiter's internal components during the sharp voltage drop, a ZnO surge arrester is employed in parallel with the bypass reactor to clamp the overvoltage and dissipate the excess energy when the voltage exceeds its threshold.

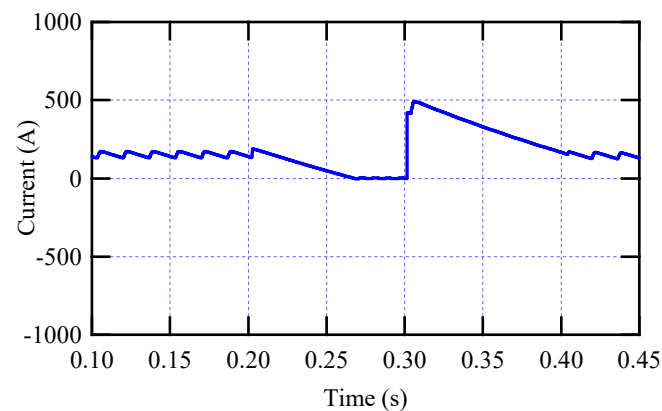


Figure 11. DC reactor current in case of distribution grid fault.

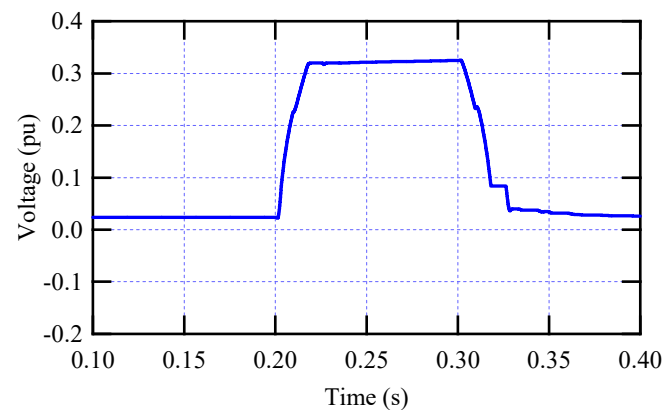


Figure 12. The voltage drop across the proposed SSFCL in case of distribution grid fault.

As depicted in Figure 13, the proposed SSFCL demonstrates a notable ability to reduce the current fault contribution from both the conventional power plant and the wind farm by approximately 29% during a distribution grid fault scenario. This significant reduction is achieved due to the direct positioning of the SSFCL in the fault current path. Correspondingly, Figure 14 illustrates that the SSFCL substantially improves the voltage profile at the PCC by reducing the severity of the voltage sag during the fault period. The voltage dip, which would otherwise reach critical undervoltage levels, is curtailed by about 42% due to the device's action. This mitigation is particularly beneficial for maintaining the voltage above the undervoltage protection threshold, thereby improving fault ride-through capability. The response time of the proposed SSFCL is less than 1 ms, measured from fault detection to the initiation of current limitation. This rapid response is primarily due to the fast switching capability of semiconductor devices and the instantaneous current redirection mechanism of the topology.

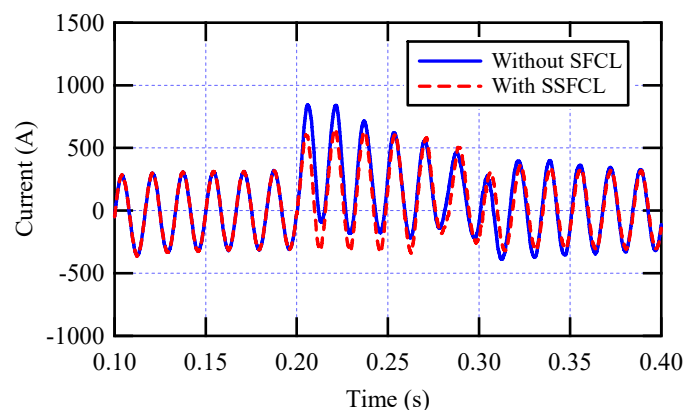


Figure 13. The fault current contribution from the wind farm with and without the proposed SSFCL in case of distribution grid fault.

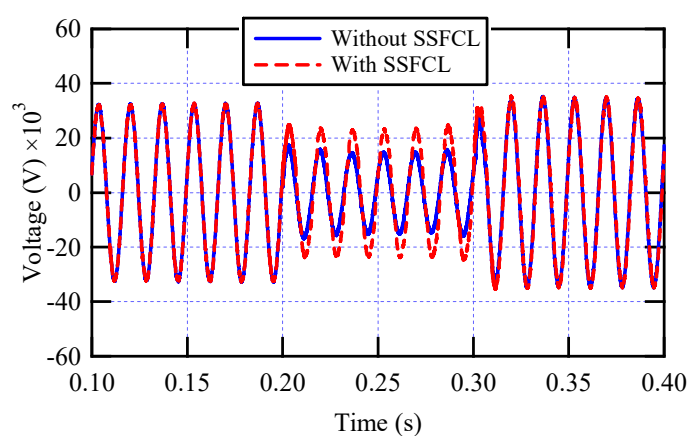


Figure 14. The voltage profile at PCC with and without the proposed SSFCL in case of distribution grid fault.

4.3. Case Study 3: Domestic Fault

In this scenario, a fault is introduced within the domestic load network, which is electrically downstream of the distribution transformer. Due to the presence of the transformer, which adds impedance between the fault location and the upstream supply, the resulting fault current is attenuated compared to faults occurring in the transmission or distribution grid.

The DC reactor current profile depicted in Figure 15 closely resembles the behavior observed during the distribution grid fault scenario, with some notable distinctions. Since the SSFCL is positioned directly along the fault current path, it actively responds during the fault event. However, due to the increased impedance introduced by the transformer and the lower voltage level of the domestic network, the magnitude of the fault current is considerably smaller compared to higher voltage faults. This results in a lower current overshoot following fault clearance and a rapid back to steady-state condition.

Additionally, it is noted that the voltage drop across the proposed SSFCL during the domestic fault scenario is notably lower compared to the case of a distribution grid fault, as illustrated in Figure 16. This reduction in voltage drop is primarily attributed to the smaller fault current magnitude associated with faults occurring on the customer side of the system.

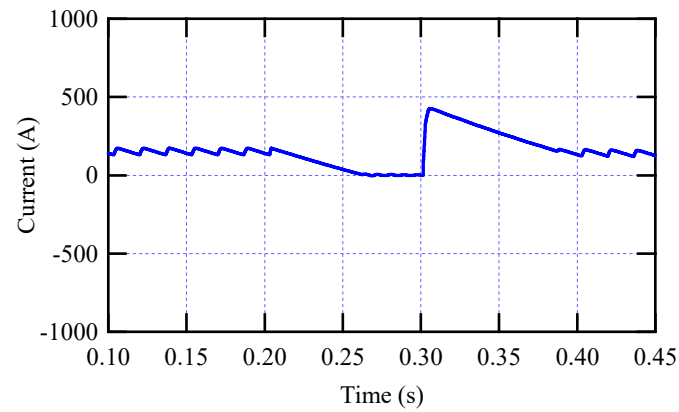


Figure 15. DC reactor current in case of domestic fault.

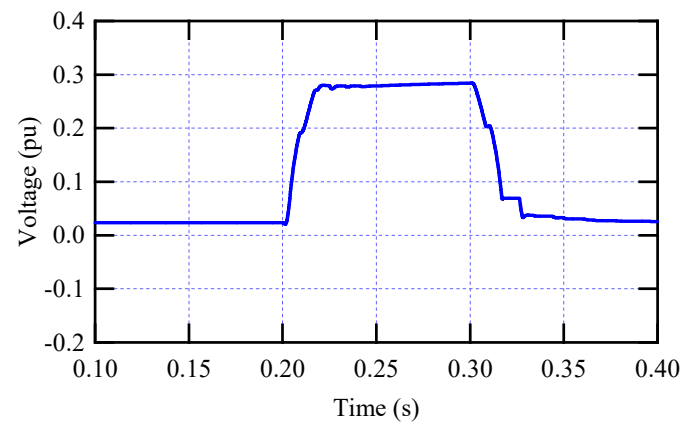


Figure 16. The voltage drop across the proposed SSFCL in case of domestic fault.

The proposed SSFCL continues to demonstrate effective fault current limitation under the domestic fault scenario, as shown in Figure 17. Specifically, the device reduces the peak fault current magnitude by approximately 14% compared to the system operating without the limiter. Correspondingly, Figure 18 reveals that the proposed SSFCL also plays a substantial role in alleviating voltage sag during the fault event. The voltage at the wind farm terminal shows an improvement of nearly 14%. Collectively, these improvements validate the proposed SSFCL's contribution to enhancing overall system resilience and maintaining power quality across a range of fault conditions.

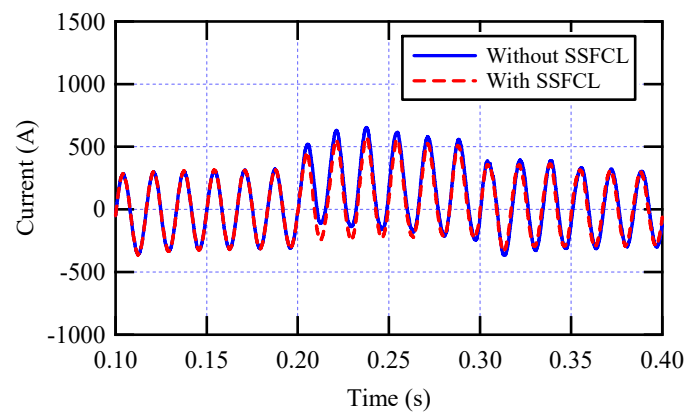


Figure 17. The fault current contribution from the wind farm with and without the proposed SSFCL in case of domestic fault.

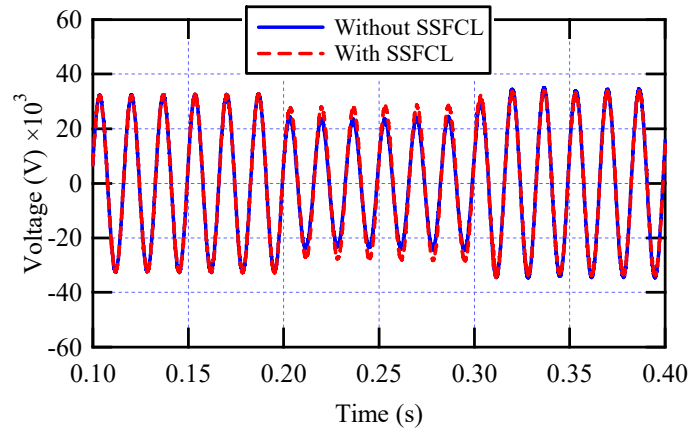


Figure 18. The voltage profile at PCC with and without the proposed SSFCL in case of domestic fault.

5. Comparative Study Between the R-SFCL and the Proposed SSFCL

There exist several variants of SFCLs, including inductive, resistive, hybrid, and flux-lock types. This work focuses specifically on the conventional R-SFCL, which operates based on quenching behavior. Specifically, the limiter incorporates a superconducting element that transitions to a high-resistance state upon detecting a fault, thus limiting the fault current. This quenching phenomenon is intrinsic to the superconducting material used and does not rely on external switching mechanisms.

The dynamic behavior of the R-SFCL, including its quenching and recovery characteristics, is modeled mathematically by Equation (1):

$$R_{SFCL}(t) = \begin{cases} 0, & (t_0 > t) \\ R_m \left[1 - \exp\left(-\frac{t-t_0}{\tau_{sc}}\right) \right]^{\frac{1}{2}}, & (t_0 \leq t < t_1) \\ a_1(t-t_1) + b_1, & (t_1 \leq t < t_2) \\ a_2(t-t_2) + b_2, & (t_2 \leq t) \end{cases} \quad (1)$$

where R_m represents the maximum resistance of the R-SFCL in its quenched state in Ω , and τ_{sc} is the time constant associated with the transition from the superconducting state to the resistive state. The time t_0 denotes the onset of the quenching process, while t_1 and t_2 represent the beginning of the first and second recovery phases, respectively. The coefficients a_1 , a_2 , b_1 , and b_2 are empirical parameters that characterize the slope and offset during the respective recovery intervals [39,40]. In this work, this behavior was implemented using a lookup table to ensure accurate modeling of the nonlinear resistance evolution during fault and recovery. The electrical topology of the R-SFCL used in this study follows the classical resistive configuration, comprising a superconducting element connected in parallel with a fixed shunt impedance, as shown in Figure 19. Under normal operating conditions, the current flows predominantly through the superconducting path, which exhibits negligible resistance. However, once a fault occurs and the superconducting element quenches, its resistance rises sharply to a very high value, effectively diverting the current to the parallel shunt branch. So, the shunt impedance governs the overall resistance of the limiter, which is referred to as the quench impedance.

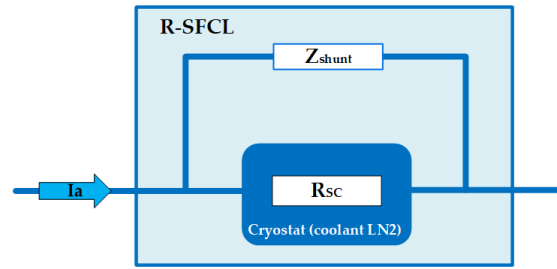


Figure 19. Electric scheme for a resistive-type SFCL with Z_{shunt} .

Figure 20 illustrates the comparative performance of the R-SFCL and the proposed SSFCL under a distribution grid fault scenario, specifically analyzing the percentage of fault current limitation as a function of the limiting impedance. The current measured corresponds to the fault current flowing toward the domestic loads. The percentage limitation is defined as follows:

$$\text{Current limitation\%} = \frac{I_{\text{without FCL}} - I_{\text{with FCL}}}{I_{\text{without FCL}}} \quad (2)$$

where these currents denote maximum instantaneous line currents. As the impedance increases up to 40Ω , both devices exhibit improved fault current suppression. Notably, the proposed SSFCL consistently achieves a lower fault current limitation compared to the R-SFCL across the entire impedance range. However, the SSFCL offers advantages in terms of cost and thermal management, unlike the R-SFCL, which requires costly superconducting materials and cryogenic systems and relies on resistive elements that generate significant heat during quenching.

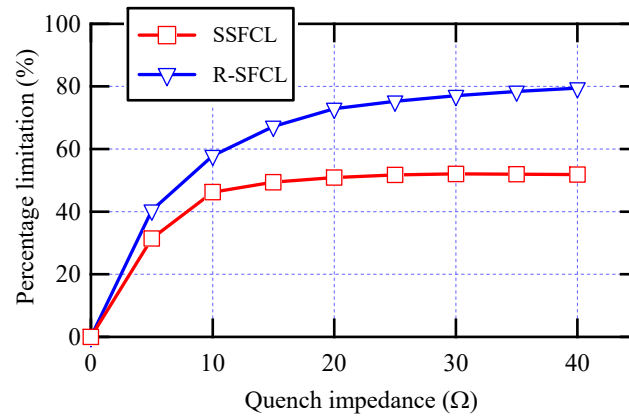


Figure 20. Comparison of fault current limitation (%) versus limiting impedance for the proposed SSFCL and R-SFCL under a distribution grid fault, highlighting performance boundaries of both topologies.

The performance of the R-SFCL and proposed SSFCL device will be compared in this section using the same fault current limiting impedance value of 20Ω . The location of both was kept the same in order to ensure accuracy and objectivity in the evaluation. A detailed comparison is conducted under a distribution grid fault scenario of symmetrical type, with analyzing the fault current contribution from the wind farm and the voltage profile at PCC.

5.1. Comparison with Distribution Grid Fault

The effectiveness of both the R-SFCL and the proposed SSFCL devices in mitigating fault conditions is validated under the distribution grid fault scenario, as shown in Figure 21. During the first half-cycle of the symmetrical fault, the R-SFCL achieved only 6% greater fault current reduction compared to the SSFCL. In terms of voltage sag mitigation, Figure 22 illustrates that the R-SFCL significantly improves voltage profile at the PCC by up to 77%

compared to the case without any fault current limiter, while the improvement reached around 42% with the proposed SSFCL.

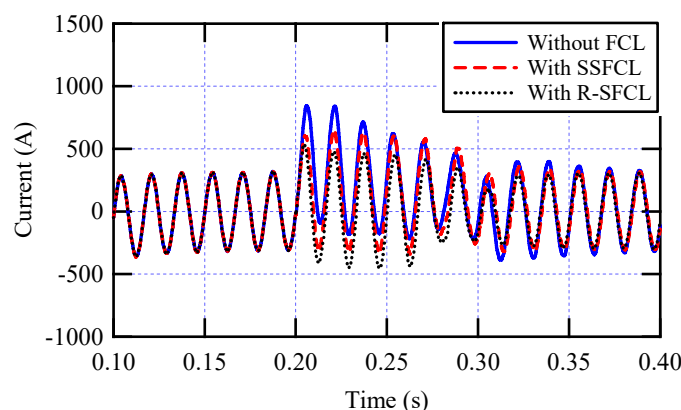


Figure 21. Comparison of fault current waveforms at the wind farm output during a distribution grid fault without FCL, with SSFCL, and with R-SFCL.

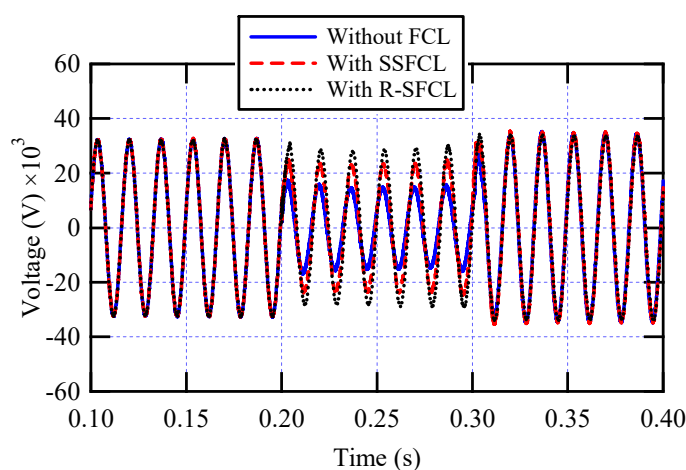


Figure 22. Voltage profile at the wind farm output under a distribution grid fault using R-SFCL and SSFCL compared to without FCL.

The two fault current limiter types, R-SFCL and SSFCL, are compared in Table 2 based on their performance under the three distinct fault scenarios: transmission line fault, domestic fault, and distribution grid fault. The results indicate that both FCL technologies have minimal impact on fault current mitigation and voltage sag reduction in the case of transmission line faults due to the device's location relative to the fault path. However, in scenarios involving distribution grid and domestic faults, both devices demonstrate effective current limiting performance. With regard to voltage sag mitigation, neither device contributes significantly during transmission line faults. However, both effectively alleviate voltage dips during distribution grid and domestic faults. Based on the comparative analysis across the three fault scenarios, the proposed SSFCL demonstrated effective fault current limitation comparable to R-SFCL, while providing a more practical and cost-effective solution than R-SFCL.

Table 2. Comparative performance summary of R-SFCL and SiC-SSFCL under transmission line, distribution grid, and domestic fault scenarios.

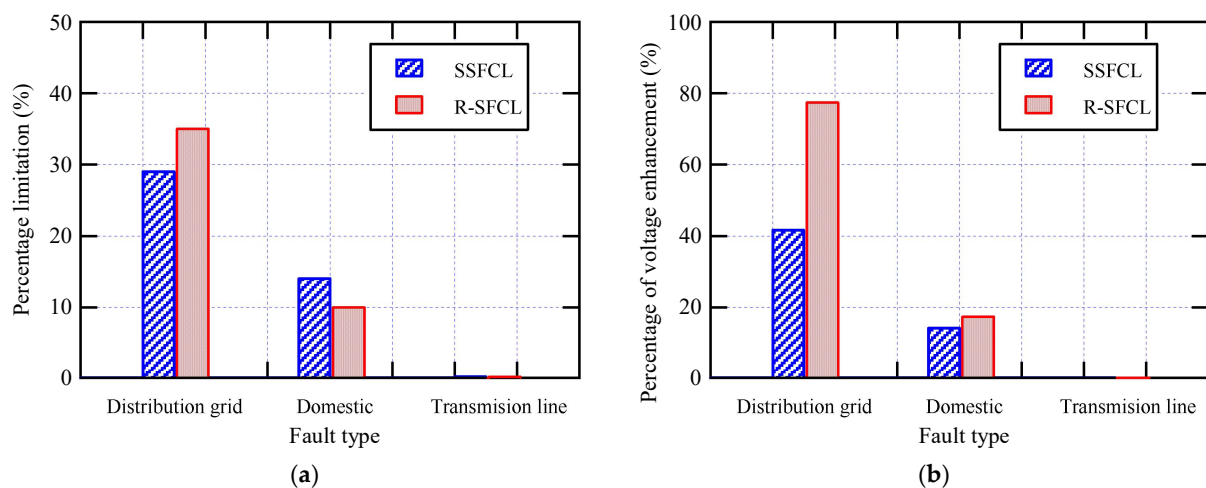
FCL Device	Parameters	Transmission Line Fault		Domestic Fault		Distribution Grid Fault		Equipment Volume	Maintenance Frequency
		% Effect	Influence	% Effect	Influence	% Effect	Influence		
R-SFCL	Current	0.14%	Decreased	10%	Decreased	35%	Decreased	Large	High
	Voltage	0.0%	-	17%	Increased	77%	Increased		
Proposed SSFCL	Current	0.11%	Decreased	14%	Decreased	29%	Decreased	Small	Low
	Voltage	0.0%	-	14%	Increased	42%	Increased		

Values in bold indicate better performance.

5.2. Graphical Analysis of the Results

A comparative study was conducted to determine how well the R-SFCL and proposed SSFCL limit fault current and improve voltage during fault occurrence. The following are the main results, as shown in Figure 23:

1. In case of a fault with the transmission line, as previously mentioned, neither device could limit the fault current. and mitigation of voltage sag.
2. In case of a fault with the distribution grid, in comparison to the SSFCL, the R-SFCL exhibited more efficiency in limiting the fault current with a difference of 6%. Additionally, it performed better than the SSFCL in terms of improving the voltage during the fault, with an improvement rate of almost 77% as opposed to 42% for the SSFCL.
3. In the case of a fault in the Domestic Fault, in the first half-cycle at the beginning of the fault, the SSFCL performed better than the R-SFCL in limiting the fault current with a difference of 4% almost.

**Figure 23.** Overall comparison of R-SFCL and proposed SSFCL performance under different fault scenarios: (a) Percentage limitation of fault current and (b) Percentage improved voltage.

In conclusion, from both technical and economic standpoints, the proposed SSFCL emerges as the more favorable solution for enhancing fault ride-through performance in modern power systems. Although the R-SFCL demonstrates slightly superior effectiveness in fault current limitation and voltage sag mitigation, the margin of improvement is relatively modest when compared to the proposed SSFCL. However, the R-SFCL's reliance on superconducting materials necessitates continuous cryogenic cooling using liquid hydrogen, which introduces high operational complexity, maintenance demands, and significant cost. In contrast, the proposed SSFCL eliminates the need for cryogenic systems, offering a more compact, thermally robust, and maintenance-friendly design. Its ability to operate at

high temperatures, withstand harsh electrical stress, and reliably suppress fault currents makes it a technically sound and cost-efficient choice for grid integration, particularly in wind energy applications. However, the proposed SSFCL introduces its own design considerations, particularly the need for advanced semiconductor switches, which must be included in any comprehensive economic assessment.

6. Conclusions

This paper proposed a new Solid State Fault Current Limiter (SSFCL) topology, incorporating both DC and AC reactors with an Integrated Gate-Commutated Thyristor (IGCT) switch, and investigated its performance for fault current limitation and voltage sag mitigation in a wind-integrated power grid. The proposed topology combines a bridge section with the IGCT switch and the DC reactor, and a shunt branch comprising the AC reactor with a ZnO arrester to ensure reliable fault current limitation. Under normal conditions, the IGCT remains fully conducting, allowing the current to flow smoothly through the rectifier bridge and DC reactor with minimal voltage drop and without introducing significant harmonic distortion. During fault conditions, the IGCT is triggered to turn off rapidly, diverting the fault current into the shunt path where the AC reactor suppresses the current magnitude and the ZnO arrester clamps overvoltages, thereby protecting sensitive components. Simulation results demonstrated that a 20 Ω AC reactor offers near-optimal current limiting performance before saturation, while a 0.11 Ω DC reactor effectively mitigates current ripples and ensures fast recovery post-fault. Through detailed simulation of three fault scenarios, transmission line, distribution grid, and domestic faults, the proposed SSFCL demonstrated effective current-limiting capabilities and improved voltage profiles. For transmission line fault, the fault current contribution from the wind farm revealed approximately no difference with and without the proposed SSFCL device, as the SSFCL was not positioned within the primary fault current path. On the other hand, the proposed SSFCL demonstrated a notable capability in reducing the fault current contribution from the wind farm by approximately 29% and 14% during the distribution grid fault and domestic fault, respectively. Regarding the voltage profile at the Point of Common Coupling (PCC), the proposed SSFCL mitigated voltage sag at the PCC by approximately 42% during a distribution grid fault scenario and by about 14% in the case of a domestic fault, thereby supporting system stability. Finally, the performance of the proposed SSFCL was compared with that of R-SFCL. The comparison indicated that the SSFCL demonstrated effective fault current limitation comparable to R-SFCL, while providing a more practical and cost-effective solution than R-SFCL. Future work will extend the study to asymmetric and unbalanced fault conditions to better reflect real grid scenarios. In addition, experimental validation through a hardware prototype will be pursued to verify the practical performance of the proposed SSFCL.

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Abbreviations

The following abbreviations are used in this manuscript:

SSFCL	Solid State Fault Current Limiter
R-SFCL	Resistive-Superconducting Fault Current Limiter
RESs	Renewable Energy Sources
SFCLs	Superconducting Fault Current Limiters
LVRT	Low Voltage Ride-Through
PSS	Power System Stabilizer
STATCOM	Static Synchronous Compensator
SMD	Sum of Maximum Deviations
FRT	Fault Ride-Through
PCC	Point of Common Coupling
DFIG	Doubly Fed Induction Generator
PMSG	Permanent Magnet Synchronous Generator
PV	Photovoltaic
VSG	Virtual Synchronous Generator
SMES	Superconducting Magnetic Energy Storage
SFCLT	Superconducting Fault Current Limiting Transformer
SMES-FCL	Multifunctional Superconducting Magnetic Energy Storage-Fault Current Limiter
SDBR	Series Dynamic Braking Resistor
CCFCL	Current Controlled Fault Current Limiter
SSFCLID	Fault Current Limiting and Interrupting Device
IGBT	Insulated-Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor
DC	Direct current
AC	Alternating Current
TR	Transformer
FCLs	Fault Current Limiters
RMS	Root Mean Square
FWD	Freewheeling Diode
THD	Total Harmonic Distortion
IEEE	Institute of Electrical and Electronics Engineers
ZnO	Zinc Oxide
SiC	Silicon Carbide

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