

Article

A Large-Scale Neuromodulation System-on-Chip Integrating 128-Channel Neural Recording and 32-Channel Programmable Stimulation for Neuroscientific Applications

Gunwook Park, Joongyu Kim , Minjae Kim, Minsung Kim, Byeongwoo Yoo, Jeongho Choi, Daehong Kim and Sung-Yun Park * 

Department of Electronic Engineering, Pusan National University, Busan 46241, Republic of Korea; rjsdnr9702@pusan.ac.kr (G.P.); hwasinme@pusan.ac.kr (J.K.); minje906@pusan.ac.kr (M.K.); tiger451912@gmail.com (M.K.); 100au@pusan.ac.kr (B.Y.); hoyadul02@pusan.ac.kr (J.C.); kdh2387@pusan.ac.kr (D.K.)

* Correspondence: sungyun@pusan.ac.kr; Tel.: +82-51-510-2416

Abstract

We present a large-scale neuromodulation system-on-chip (SoC) that integrates a 128-channel neural recording and 32-channel stimulation ASIC designed for a wide range of neuroscientific applications. Each recording channel achieves low-noise performance ($\sim 4 \mu\text{V}_{\text{rms}}$) with a configurable bandwidth of 0.05 Hz–7.5 kHz and supports 16-bit digitization with scalable sampling rates up to 30 kS/s. To enhance signal quality, the ASIC includes an adjustable digital high-pass filter and a fast-settling function for rapid recovery from stimulation artifacts. SoC also incorporates on-chip electrode-impedance measurements as a built-in safety feature by reusing the recording channels. The stimulation subsystem generates current-controlled monopolar biphasic pulses with a high compliance voltage of $\pm 6 \text{ V}$ using standard low-voltage (1.8 V/3.3 V) CMOS devices. Each of the 32 stimulation channels provides arbitrary 9-bit programmable waveforms and dual current modes ($4 \mu\text{A}/\text{bit}$ and $8 \mu\text{A}/\text{bit}$), supporting both fine-resolution microstimulation and high-current applications such as spinal-cord and deep-brain stimulation. On-chip charge-balancing switches in each channel further ensure safe and reliable stimulation delivery. The SoC supports digital communication via a standard SPI with both 3.3 V CMOS and low-voltage differential signaling options and integrates all required analog references and low-dropout regulators. The prototype was fabricated in a standard 180 nm CMOS process, occupying 31.92 mm^2 (equivalently, 0.2 mm^2 per recording-and-stimulation channel), and was fully validated through benchtop measurements and in vitro experiments.

Keywords: neural recording; neural stimulation; brain–computer interface (BCI); biphasic current stimulation; electrode impedance measurement; low-noise analog front-end



Academic Editor: Nicola Lusardi

Received: 14 September 2025

Revised: 12 October 2025

Accepted: 13 October 2025

Published: 15 October 2025

Citation: Park, G.; Kim, J.; Kim, M.; Kim, M.; Yoo, B.; Choi, J.; Kim, D.; Park, S.-Y. A Large-Scale Neuromodulation System-on-Chip Integrating 128-Channel Neural Recording and 32-Channel Programmable Stimulation for Neuroscientific Applications. *Electronics* **2025**, *14*, 4057. <https://doi.org/10.3390/electronics14204057>

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1. Introduction

Understanding and modulating neural activity with high spatial and temporal resolution is a cornerstone of modern neuroscience and neuro-engineering. Advances in multichannel neural recording and stimulation technologies have enabled unprecedented insights into brain function, neural circuit dynamics, and the mechanisms underlying neurological disorders [1–6]. These technologies also underpin emerging therapeutic approaches, including deep brain stimulation (DBS), spinal cord stimulation (SCS), and brain–computer interfaces (BCI), which require precise, reliable, and scalable neural interfaces. However, as

experimental and clinical demands grow, existing neural interface systems face several significant challenges. These include achieving simultaneous large-scale neural recording with low noise and high fidelity, providing programmable and temporally precise multichannel stimulations with safe charge balancing (CB), and integrating all functionalities into a compact, low-power, and scalable platform suitable for chronic implantation or portable use. Furthermore, the real-time monitoring of electrode–tissue interface conditions is essential to ensure long-term safety and stability yet is often overlooked or implemented externally. Recently, several neuromodulation system-on-chip (SoC) solutions have been introduced that integrate neural recording, stimulation, on-chip power management, safety mechanisms, and flexible communication protocols [1–4]. For example, a 64-channel neural recording and 2-channel time-multiplexed stimulation SoC with an integrated DC–DC converter and digital compression was presented in [1]. A 32-channel neuromodulation SoC capable of covering a wideband neural signal and delivering arbitrary high-voltage stimulation was demonstrated using commercial PtIr electrodes [2]. Furthermore, a BCI chipset supporting a 32-channel electrocorticogram (ECoG) recording and 4-channel stimulation was reported with a custom ECoG electrode in vitro [3]. A 128/8-channel, wireless neural interface based on custom neuromodulation SoCs and commercial off-the-shelf field-programmable gate array (FPGA) and radio modules was also demonstrated in combination with a commercial microelectrode array [4]. However, none of the previous works have achieved large-scale neural recording and concurrent multi-channel stimulation within a single monolithic chip. In [1], only two stimulation channels were implemented, limiting its applicability to experiments requiring parallel, multi-site stimulation. In [2], although a single-chip solution was demonstrated, the high-voltage stimulator circuits occupied a substantial portion of the $\sim 25 \text{ mm}^2$ die area, representing a fundamental bottleneck to scaling the channel count on a single die. Furthermore, other systems [3,4] adopted a two-chip architecture—a common practice in which low-noise recording front ends and high-voltage stimulation circuits are fabricated in separate, process-optimized dies. This multi-chip strategy, however, fundamentally constrains system miniaturization and increases packaging complexity. These issues are directly addressed in our single-chip integration using a standard CMOS process, which also provides a high compliance voltage. Among these prior works, only [2] incorporated an on-chip impedance-measurement feature to enhance safety. A detailed quantitative comparison of these systems is provided in the final section of this paper.

To address these challenges, we developed a neuromodulation SoC that integrates a 128-channel neural recording front-end and a 32-channel stimulation circuit within a single application-specific integrated circuit (ASIC). The recording channels are designed to capture the widest range of neural signals, from slow LFPs to high-frequency action potential (AP, or spike) activity with a reconfigurable bandwidth spanning 0.05 Hz to 10 kHz and providing a 16-bit digitization at scalable sampling rates up to 30 kS/s. The inclusion of an on-chip digital high-pass filter (HPF) and a fast-settling function allows for efficient artifact suppression and rapid signal recovery with $<1 \text{ ms}$, which are critical for accurate neural data acquisition, especially during simultaneous stimulation. In addition, the SoC features integrated electrode impedance measurement (ZCHK) capabilities, spanning from 50 k Ω to 10 M Ω , allowing for the continuous monitoring of the electrode–tissue interface (ETI) to detect changes that may indicate degradation or failure, thereby enhancing device safety and reliability. The stimulation subsystem delivers current-controlled biphasic pulses with a high compliance voltage of $\pm 6 \text{ V}$ and output currents up to 2.048 mA. Each stimulation channel incorporates an independent 8-bit digital-to-analog converter (DAC) operating at up to 1 MS/s, enabling fully programmable waveforms with a minimum temporal resolution of 32 μs . Dual current modes—fine-resolution (4 $\mu\text{A/bit}$) and high-current (8 $\mu\text{A/bit}$)—support a broad spectrum of stimulation paradigms, from low-amplitude

micro-stimulation to high-intensity therapies such as DBS and spinal cord stimulation. On-chip CB switches further ensure safe and effective stimulation delivery.

The SoC's digital interface employs a standard serial peripheral interface (SPI) protocol with support for both 3.3 V CMOS input and output (I/O) and low-voltage differential signaling (LVDS), facilitating flexible integration with external control units. Additionally, the chip integrates all necessary analog reference generators and low-dropout regulators (LDOs), minimizing the need for external components and simplifying system design. Fabricated using a standard 180 nm CMOS process, the prototype SoC has undergone extensive characterization in benchtop setups as well as in vitro experiments, demonstrating robust performance and versatility across a wide variety of neuroscientific and neuromodulation applications. By integrating high-density, low-noise recording with flexible, high-compliance stimulation and built-in safety monitoring in a compact and power-efficient SoC, this work represents a significant step toward next-generation closed-loop neural interfaces and advanced bioelectronic therapies.

2. System Overview

This section describes the overall architecture of the proposed neuromodulation SoC. To accommodate the high channel count within a limited silicon area, a modular design and floorplan have been used.

2.1. Floor-Planning and Layout Overview

Figure 1a illustrates the physical layout and block allocation of the SoC. To support diverse applications, the SoC should offer flexible interfacing with neural probes through 128 recording and 32 stimulation pads, and the accommodation of >160 pads within the moderate size of the chip is challenging. For the interconnection, various bonding techniques, such as flip-chip, ball-bumping [5], and anisotropic conductive film (ACF) bonding [7,8], can be considered. If advanced flip-chip or anisotropic conductive film (ACF) bonding were employed, the footprint required for interconnection could be significantly reduced thanks to area-reuse bonding and the fine pitch ($\sim 20\ \mu\text{m}$ for ACF, depending on the bump size) [7,8]. However, these methods require special post-processing and incur additional fabrication costs. Moreover, the ball-bumping process requires a dedicated pad area, which introduces similar geometric constraints to wire bonding when conventional bonding equipment is used, and it is effective only for very large chip sizes [4]. Therefore, in this work, standard wire bonding was selected for its compatibility and simplicity. Given the pad pitch limitations ($\sim 100\text{--}150\ \mu\text{m}$), a staggered pad arrangement with $90\ \mu\text{m}$ pitch was adopted for recording inputs, enabling 128 input and 4 reference pads to be placed along the bottom edge of the chip. Accordingly, each recording channel (R_{PX}) was assigned a width of $45\ \mu\text{m}$, resulting in a total die width of $5670\ \mu\text{m}$ ($128 \times 45\ \mu\text{m}$). To manage layout complexity and provide local biasing, 32-channel recording modules were grouped, each sharing a reference circuit occupying the same width of $45\ \mu\text{m}$. Stimulation pixels (S_{PXs}) are located at the top, spaced at $180\ \mu\text{m}$ pitch, reflecting the 4:1 ratio of recording to stimulation channel numbers. Between the recording and stimulation blocks lies a digital interface comprising digital high-pass filters (D-HPF), SPI controllers, and register files, which control both subsystems and relay data externally. The power management unit (PMU), which supplies all required on-chip voltages, is centrally located. LVDS and 3.3 V CMOS I/Os are placed near the stimulation circuits to minimize interference with sensitive analog blocks. All critical blocks—including analog circuits and reference generators—are isolated using deep N-wells (DNWs) to suppress substrate noise and support the negative supply voltages ($-6\ \text{V}$) required by the stimulators. The final chip size is

5940 $\mu\text{m} \times 3895 \mu\text{m}$, comprising (i) a recording pixel: $\sim 1050 \mu\text{m}$ height, (ii) an ADC and A-MUX: $\sim 400 \mu\text{m}$, (iii) a digital interface: $\sim 750 \mu\text{m}$, and (iv) a stimulation pixel: $\sim 850 \mu\text{m}$.

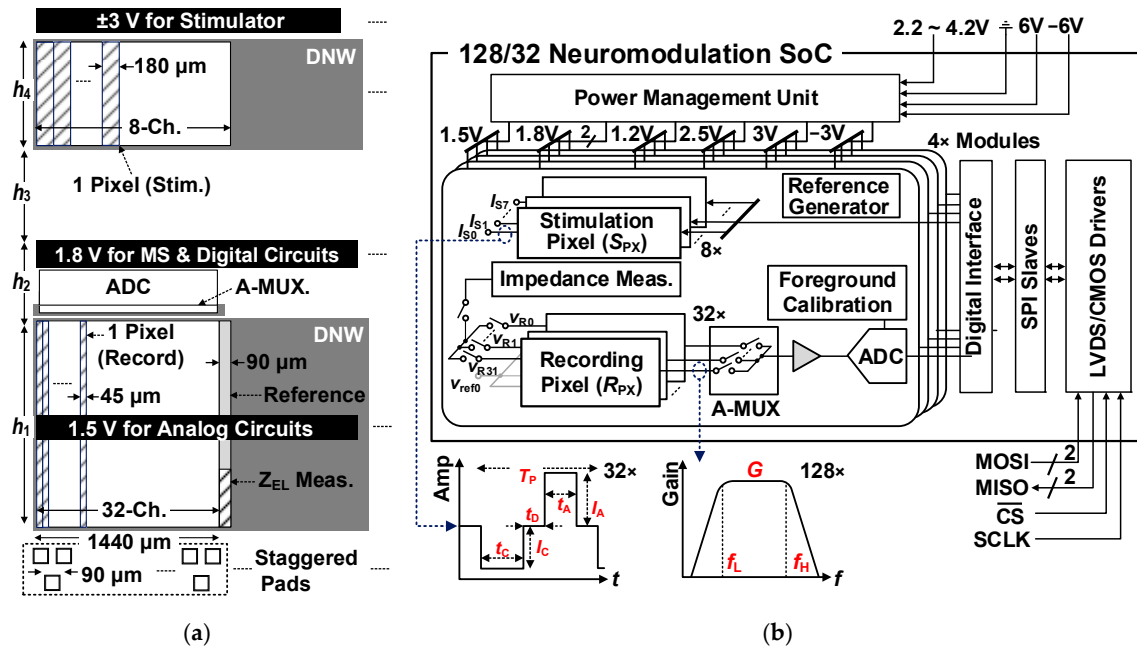


Figure 1. Proposed 128/32-channel neuromodulation SoC: (a) block allocation and layout overview, and (b) block-level circuit architecture.

2.2. Overall Circuit Architecture

Figure 1b shows the block-level architecture of the SoC. Each R_{PX} provides a bandpass filter (BPF)-shaped frequency response with a programmable mid-band gain (G), low- and high-pass cutoff frequencies (f_L and f_H); G is selectable among a fixed set of 200 and 400 V/V, and f_H can also be chosen from 0.5, 0.85, 2, and 7.5 kHz, each coincides to the bands of LFP, Electrocorticogram (ECoG_{0,1}, respectively), and LFP + AP, respectively. Unlike it, f_L is fixed as <0.5 Hz and is allowed to be tuned only if the fabricated chip results in a too-high or too-low f_L . A 16-bit ADC is shared by each 32-channel module and digitizes signals using time-division multiplexing (TDM) via an analog multiplexer (A-MUX). The sampling rate is 30 kS/s per channel, sufficient for spike recording. The digitized data are filtered by a digital HPF, routed through an SPI, and transmitted via LVDS or CMOS drivers depending on user preference. Each S_{PX} supports monopolar biphasic stimulation with independent control over anodic and cathodic amplitudes (I_A and I_C), pulse widths (t_A , t_C), and inter-phase delay (t_D). The control timing resolution is defined by the SPI clock (25 MHz nominal), requiring 32 μs to update all 32 channels using 10-bit registers per stimulator. The stimulation current is programmable from 4 μA to 2.048 mA using on-chip 8-bit DACs. All parameters are configured via the SPI and shared digital interface. An integrated PMU includes seven LDOs and a low-voltage bandgap reference (BGR, 0.9 V), supporting internal voltages of 1.5 V, 1.8 V, 2.5 V, and ± 3 V. The chip operates from a single 3.3 V supply (2.2–4.2 V range), with additional ± 6 V supply for high-voltage stimulator operation.

3. Implementation

The detailed circuit implementation is described in this section, with conventional blocks omitted for clarity and brevity.

3.1. Recording Pixel (R_{PX})

Figure 2 shows a circuit block diagram of a single channel R_{PX} . It consists of a low noise amplifier (LNA), a programmable gain amplifier (PGA), and switches for TDM. Since the R_{PX} is sensitive to interference, the entire signal processing circuits are physically isolated in a DNW from the TDM switches that generate switching noise. The TDM switches are also on a separate DNW. The LNA adopts a capacitively coupled architecture for high gain uniformity across channels and to avoid saturation due to electrode dc-offset drift [9]. C_{in} and C_f in the LNA are designed as 10 and 0.1 pF, respectively, to implement a nominal 40 dB of the mid-band gain. The f_L and f_H are primarily determined by the LNA. The f_L , set by R_f and C_f , should be low enough (~ 0.1 Hz) to embrace slow-varying neural signals, such as LFP and ECoG, while rejecting the electrode dc-offset. Thus, R_f is implemented using four series-connected pseudo-resistors (PRs), as shown in Figure 2 [10], each comprises back-to-back, diode-connected high voltage (HV) PMOS transistors (M_{P1} and M_{P2}), i.e., 3.3 V I/O transistors with a tunability using digital codes. In this work, 2-bit has been assigned with a nominal current of 10 nA, so that f_L can be tuned from 0.01 to 1.5 Hz in simulation.

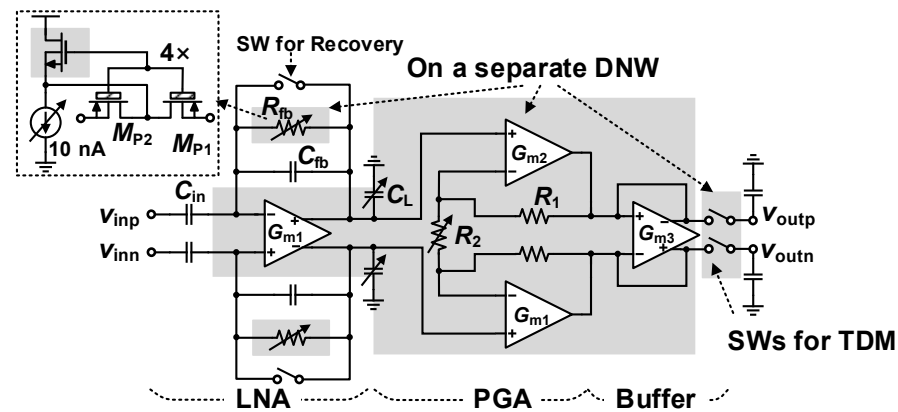


Figure 2. Circuit block diagram of a single-channel R_{PX} .

In addition, the AFE in neural recording interfaces is often designed to acquire band-limited neural signals such as LFP (~ 1 Hz–250 Hz), ECoG (~ 1 Hz–1–2 kHz), APs (300 Hz–7.5 kHz), etc. [9], thus it is necessary to control the f_H of the LNA. In this work, the f_H can be controlled using selectable output capacitance (C_L) and varying transconductance of the LNA (G_{m1}) with 4 b code. The f_H can be tuned from 0.5, 0.85, 2, and 7.5 kHz; thus, the LNA acts as an anti-aliasing filter to maintain the integrity of the neural signal and consumes only necessary power in accordance with the signal bands of interest. Additionally, to aid in rapid recovery from stimulation artifacts, a recovery switch is incorporated within the LNA. In the current implementation, this recovery switch is controlled manually via an SPI command. The 2nd-stage PGA has a standard instrumentation amplifier (IA) topology with resistive feedback, setting its gain to $1 + 2R_2/R_1$. The unity-gain frequencies (ω_T) of the operational amplifiers in this stage are also controlled by adjusting its bias currents, so the bandwidth can be programmed. The R_1 and R_2 in the PGA are set as 240 and 480 k Ω , respectively, at their nominal values to achieve a 6 dB gain; R_2 can be programmable as 160 k Ω to increase overall gain G (200 $\rightarrow$ 400 V/V) using a switch [11]. The PGA is followed by a buffer to drive the switches used for the TDM. The maximum TDM rate is 1.024 MHz considering 32 $\times$ multiplexing and 31.25 kS/s for each R_{PX} . The switches are implemented using a separate triple well NMOS transistor to suppress artifacts from fast switching actions from degrading performance of the R_{PX} . The entire circuit in a single R_{PX} is laid out within 40 μ m pitch and 5 μ m (2.5 μ m for the left and right) is used for physical separation

between the channels to minimize crosstalk [12]. The R_{PX} operates with a 1.5 V power supply and consumes $\sim 36 \mu\text{A}$ of current.

3.1.1. Low-Noise Amplifier Design

Figure 3a depicts transistor-level circuit diagram of the G_{m1} for the LNA. G_{m1} has been implemented using a two-stage operational transconductance amplifier (OTA) with local positive feedback (M_5 and M_6), and design principles of it for the LNA have been adopted from our previous implementation [13]. The spectral density of an input-referred noise (IRN) of the OTA, including thermal and flicker noises, is given by the following:

$$\bar{v}_{n,in}^2 \approx \frac{8kT\gamma(1-\alpha)^2}{g_{m1}} + \frac{2K_p}{WLC_{ox}f} \quad (1)$$

where g_{m1} is the transconductance of $M_{1,2}$, γ is a constant for the transistor channel noise, k is Boltzmann constant, T is the absolute temperature, K_p is a process-dependent flicker noise coefficient, WL is the area of $M_{1,2}$, and C_{ox} is the gate oxide capacitance of $M_{1,2}$. In addition, the value of G_{m1} and ω_T of the OTA are given by the following:

$$G_{m1} = g_{m1} \cdot \frac{B}{1-\alpha} \quad (2)$$

$$\omega_T = \frac{G_{m1}}{C_L} = g_{m1} \cdot \frac{B}{(1-\alpha)C_L} \quad (3)$$

where g_{m1} is the transconductance of the input transistor, α and B are the ratios of $(W/L)_{5,6}/(W/L)_{4,3}$ and $(W/L)_{10,9}/(W/L)_{4,3}$, respectively, and C_L is the load capacitance of the LNA. As shown, the advantage of the OTA is that the additional two design variables: α and B , separate the linear dependency of IRN and ω_T (one is proportional, and the other is inversely proportional to G_m) on G_m in conventional OTAs. Thus, increasing $g_{m1,2}$ and decreasing α ($\alpha < 1$) can contribute to low noise performance, while the noise bandwidth (NBW) can be adjusted using B , instead of C_L , which otherwise occupies large area. The overall noise of the LNA is determined by the product of a multiplication ratio (m , in Figure 3b) and IRN of the OTA, resulting in $\sim 3 \mu\text{V}_{\text{rms}}$ from 0.5 Hz to 50 kHz in simulations. As mentioned in the previous section, the f_H of the LNA, which is given as $(\omega_T/2\pi) \cdot (C_{fb}/C_{in})$, is programmable using a 2 b digital code and adjustable bias current via V_{B1} . The designed f_H and IRN of the LNA for the 2 b code are as follows: (00): 9 kHz/2.64 μV_{rms} , (01): 2.5 kHz/2.88 μV_{rms} , (10): 1 kHz/3.00 μV_{rms} , and (11): 0.5 kHz/3.07 μV_{rms} , which can fully cover the AP, ECoG, and LFP bands. The LNA operates in fully differential manner. The LNA consumes 25 μA of bias current (including a bias network and the CMFB circuit) from a 1.5 V power supply.

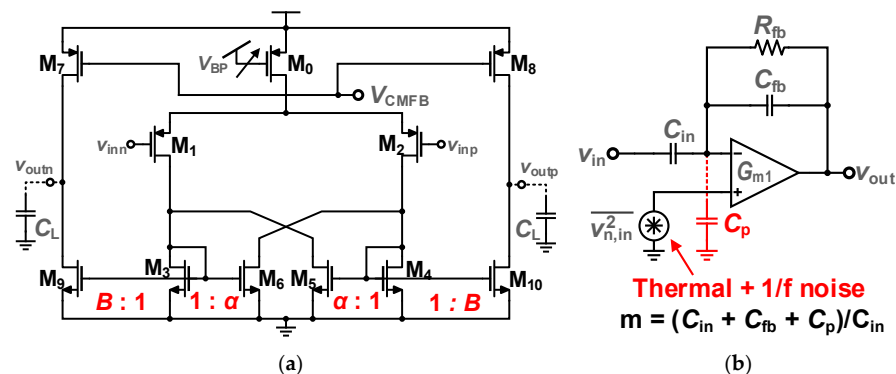


Figure 3. Transistor-level implementation of the OTA used for the LNA (a), and IRN equivalent circuit (b).

3.1.2. Programmable Gain Amplifier and TDM Buffer Design

Figure 4 shows the block and transistor-level implementation of the PGA. It is implemented as an IA with DC-coupled resistive feedback to minimize gain variation by mismatch and achieve a high common-mode rejection ratio (CMRR). The PGA is controlled by a 1 b digital code, as shown in Figure 4a, so it can generate 6 or 12 dB gains. To ensure that the bandwidth of the R_{PX} is unaffected by the different gains, the high frequency corner is designed to have >25 kHz at gain conditions of 12 dB. The OTA that configures the IA (G_{m2}) must satisfy the near output rail-to-rail condition and drive a resistive load (R), so a rail-to-rail input and output folded cascode (FC-OTA) with a class AB output topology has been adopted, and cascode Miller compensation (C_C) was used to frequency-compensate G_{m2} [14]. The bias of G_{m2} can be adjusted by V_{BP} and V_{BN} , and the bias for the floating current sources for the class AB operation can also be adjusted by V_{CPF} and V_{CNF} .

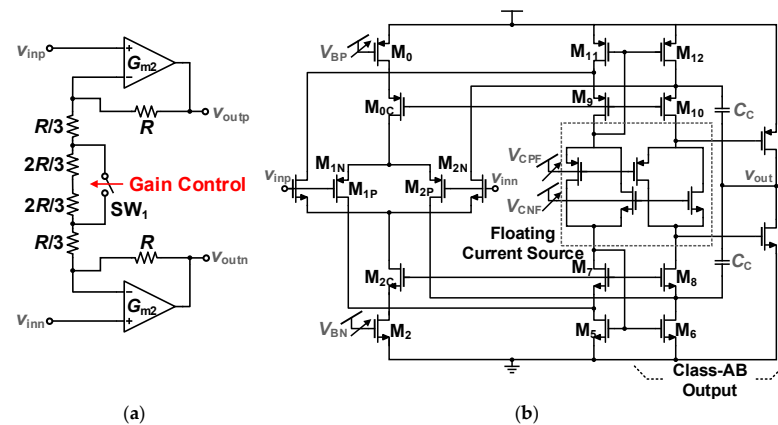


Figure 4. PGA implementation: (a) circuit block diagram, (b) transistor-level implementation of G_{m2} used for the PGA.

A TDM buffer is needed to prevent linearity degradation of the previous block, such as the LNA and PGA, due to switching artifacts and settling time in TDM approaches. The TDM buffer is designed to maintain the linearity of the LNA and PGA, showing low distorting and meeting the near rail-to-rail input/output. Thus, a class AB unity gain buffer has been adopted [15]. The unity gain buffer is designed with a cutoff frequency of 20 MHz to ensure a stable settling time within 500 ns. The schematic of G_{m3} is the same as G_{m2} with the different aspect ratios for the constituent transistors.

3.2. Analog-to-Digital Converter

3.2.1. 16 b SAR ADC with Synchronous MSB and Asynchronous LSB Conversion

A 16-bit successive approximation register (SAR) analog-to-digital converter (ADC) is implemented for each 32-channel recording pixel (R_{PX}) module. Figure 5 shows the capacitive digital-to-analog converter (CDAC) employed in the ADC, comprising three segmented capacitor arrays based on an 84 fF unit capacitor (C_U). To enhance energy efficiency and maintain top-plate common-mode stability, a split-capacitor switching scheme is adopted. This approach eliminates the need for an additional bottom-plate reference voltage (V_{CM}) for the ADC, as noted in [16]. The red-dotted box in the figure highlights the implementation of the C_U based on this switching technique, with the switch positions configured for sampling at V_{CM} . Since no dedicated bottom-plate V_{CM} is used, a precise buffer is unnecessary. Instead, simple diode-connected transistors generate the top-plate V_{CM} during sampling. The sampling capacitance is composed solely of the MSB segment of the CDAC (b_{14} to b_9), with a total value of approximately 6 pF, which satisfies the required kT/C noise constraint ($\sim 26.27 \mu V_{rms}$). To accommodate incomplete charge settling during

SAR conversion, three redundant bits (b_{11r} , b_{7r} , and b_{3r}) are included. These redundant bits also serve as foreground calibration, as will be detailed later. Although the ADC is nominally designed to operate within 16 SPI clock (SCLK) cycles, 20 clocks are needed to account for the redundant bits. To support this, a hybrid control scheme is adopted: the first seven conversion steps—up to the bridge capacitor—are handled by synchronous logic to ensure adequate settling, while the remaining bits are processed asynchronously to improve speed and power efficiency [17].

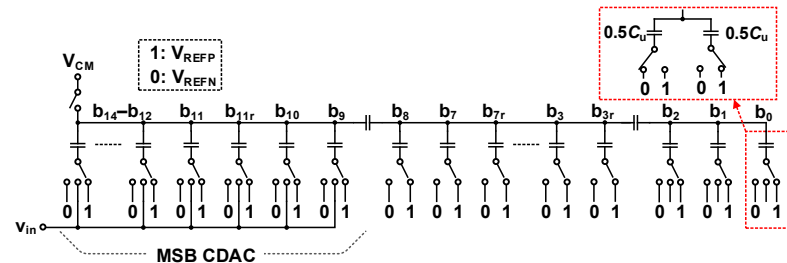


Figure 5. Capacitive DAC used for the 16 b SAR ADC.

The comparator plays a critical role in determining ADC performance, particularly in balancing power consumption, noise sensitivity, operational speed, and architectural scalability. Figure 6 presents the transistor-level implementation of the comparator used in this work, which comprises a preamplifier stage followed by a dynamic latched comparator [18]. To suppress memory effects across successive conversions, the preamplifier is reset at the beginning of each comparison cycle via a Φ_{RST} signal. The preamplifier operates as a differential integrator, and its load incorporates cross-coupled positive feedback to enhance DC gain and eliminate the need for a common-mode feedback (CMFB) circuit. The second stage consists of a single-phase dynamic latched comparator. Auto-zeroing (AZ) is also implemented at the preamplifier output; the AZ phase is aligned with the ADC sampling phase. During this phase, the inputs of the preamplifier are shorted and its offset is sampled onto the auto-zero capacitor (C_{AZ}), effectively reducing systematic offset and $1/f$ noise. The overall comparator exhibits an estimated input-referred noise of approximately $140 \mu V_{rms}$, meeting the precision requirements of the 16-bit SAR ADC architecture. A single ADC consumes $740 \mu W$ where the buffer, preamplifier, comparators, logics, and DAC consume 470, 124, 38, 64, and $43 \mu W$, respectively, and occupy $1.08 \times 0.35 \text{ mm}^2$.

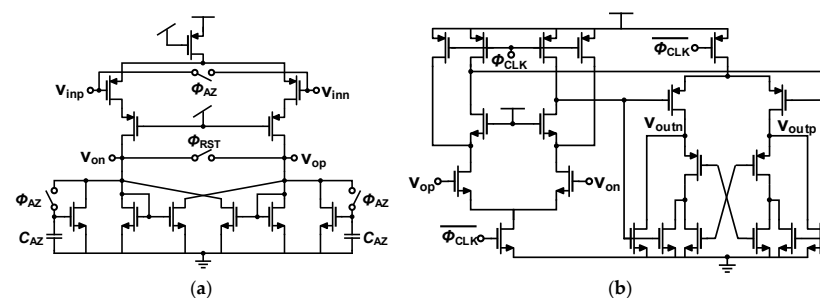


Figure 6. Comparator used for the ADC: (a) preamplifier, (b) two-stage latched-comparator.

3.2.2. Foreground Calibration

To correct bit weight errors caused by capacitor mismatch and parasitic, a foreground calibration is performed to improve linearity. Various SAR ADC calibration techniques have been proposed in the literature [19–23]. In this work, an on-chip foreground calibration method [21] with the split CDAC is proposed and implemented. The introduced split-CDAC not only eliminates the need for a dedicated reference generator (as discussed in

the previous section) but also improves common-mode stability. In a typical CDAC, the lower-weight capacitors are less sensitive to mismatch due to their smaller bit weights [19]. Hence, as shown in Figure 7a (top), the capacitors corresponding to b_0 – b_{3r} are assumed to be linear and are used to calibrate the higher-weighted capacitors (b_3 in this case). During calibration, the target bit is toggled, and its weight is estimated by remaining bits into the digital domain using a partial SAR operation. The calibration is performed by toggling the bit under test between V_{REFP} (=1) and V_{REFN} (=0), while all higher bits are fixed at V_{CM} . The lower bits are resolved by the SAR logic to estimate the digital output corresponding to the weight of the bit being calibrated. To eliminate the effect of offset during calibration, two weights: $w_{i,force0}$ and $w_{i,force1}$ are obtained by setting the target digital bit to 1, and 0, respectively, then, taking their difference yielding the calibrated bit weight is given by the following [21]:

$$w_i = \frac{1}{2} (w_{i,force0} - w_{i,force1}) \quad (4)$$

$$w_{i,force0} = \sum_{j=0}^{i-1} d_{j,force0} w_j + v_{off}, \quad w_{i,force1} = \sum_{j=0}^{i-1} d_{j,force1} w_j + v_{off} \quad (5)$$

where $d_{j,force0}$ and $d_{j,force1}$ are digital bits 0 and 1, respectively, and v_{off} is the offset during the calibration. As a result, the extracted weight reflects only the true capacitor mismatch and is not affected by offset. This procedure is repeated sequentially for each bit up to the MSB, using the newly calibrated weights for the already corrected bits in the rest of Figure 7. Although the subtraction in (4) removes the offset ideally, this does not hold when the offset exceeds redundancy margin, resulting in saturation. To address this, during the sampling phase, the bottom plate of the capacitor under calibration is initially driven to 1 or 0 instead of V_{CM} , and is subsequently returned to V_{CM} , as shown in Figure 7b. This introduces a known offset proportional to the bit weight, which effectively shifts the calibration range and prevents output saturation. Since the same offset is introduced in both the “force 0” and “force 1” phases, it is canceled in the subtraction step in (4) and does not affect the linearity. Note that it is not necessary to apply a dither exactly equal to the circuit offset. Instead, a sufficiently large dither can be used to bring the signal within the valid calibration range, as illustrated in Figure 7b. This approach ensures robust calibration even in the presence of large offset.

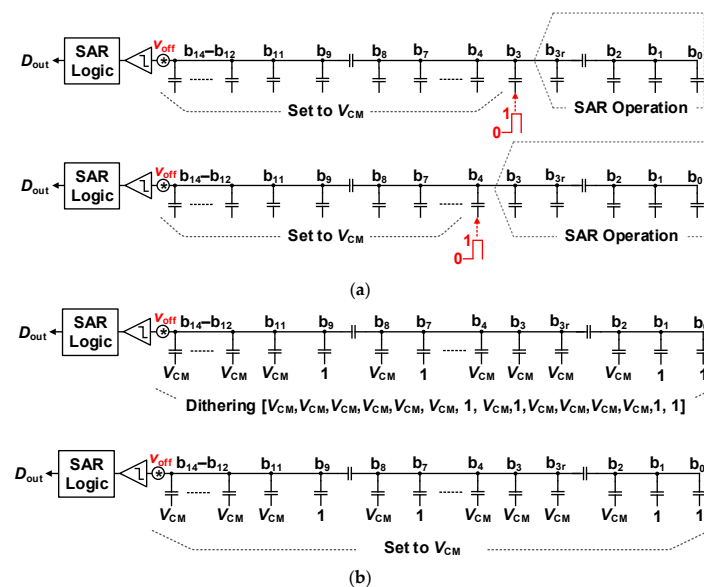


Figure 7. Self-calibration with LSB capacitors as the backend DAC when: (a) (top) calibrating the first capacitor, (bottom) calibrating the higher capacitor, (b) calibrating the MSB capacitor.

3.3. Stimulation Pixel (S_{PX})

Neural stimulation typically uses a current-mode technique to inject a controlled charge into excitable tissue via electrodes [24]. Stimulation is delivered as biphasic current pulses (I_A and I_C), with adjustable phases (t_A , t_C , t_D , and T_C in Figure 1) for each current to ensure net-zero charge after stimulations. Stimulation currents typically range from tens of μA to a few mA, requiring voltage compliance from a few volts up to over 10 V due to varying ETI impedances. In this work, a high-compliance, fully on-chip neural monopolar stimulator is designed in a standard 1.8 V/3.3 V 0.18 μm CMOS process—avoiding HV CMOS. Custom circuit techniques ensure all devices' voltage drops remain within their breakdown limits, enabling integration with other SoC components on a single chip.

Figure 8a shows a single channel block diagram of S_{PX} . Current mode stimulation is realized by a current driver (I-Driver) where balanced current sink and source are placed to provide I_A and I_C from 4 μA to 2.048 mA range with 9-bit resolution (8 b from DAC and 1 b for I_A or I_C selection). Covering the versatile applications of this neuromodulation SoC, in other words, the different ETI impedance ranges, for example: Cochlear [$R_S \approx 4 k\Omega$, $C_{DL} \approx 50$ nF, 0.1–1.2 mA] [25], DBS [$R_S \approx 1 k\Omega$, $C_{DL} \approx 500$ nF, 0.2–3.6 mA] [26], and muscle [$R_S \approx 3 k\Omega$, $C_{DL} \approx 20$ nF, 0.2 mA] [27], the I-Driver has a compliance of ± 6 V in consideration of its maximum current. The bias currents for the I-Driver are generated by a current amp (I-Amp) that scales 5–10 $\times$ up of the current from 8 b DAC, which has the least significant bit (LSB) of 200 nA. As shown in the gray boxes in Figure 8a, The S_{PX} requires both low voltages of 1.8 and 2.5 V, and high voltages ± 6 and ± 3 V, hence dedicated level shifters relay across those voltages. The level shifter not only delivers the timing information for I_A and I_C , but also does so for the compliance monitoring signals. Each S_{PX} also has some combinational logic and flip-flops that decode the command from the SPI and deliver the violence of the compliance of the stimulator. The static current consumption of the S_{PX} is $\sim 167 \mu A$.

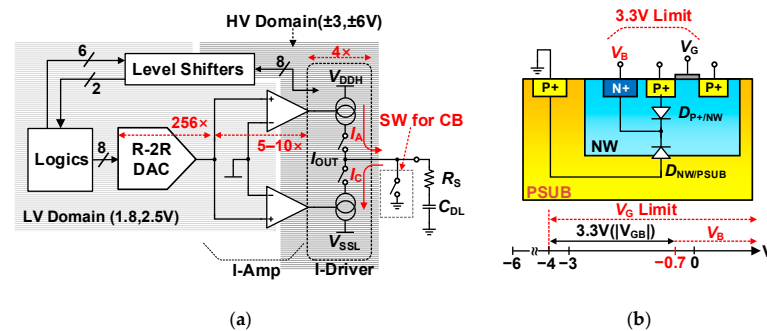


Figure 8. (a) Block diagram for a stimulation pixel (S_{PX}), (b) conceptual cross-sectional view of the PMOS transistor.

3.3.1. Current Driver for Stimulation

This monopolar biphasic stimulation requires both positive and negative voltages. Thus, circuits operating with negative voltage must carefully handle parasitic p - n junctions, as the p -substrate (PSUB) in SoC integration must remain at 0 V to ensure compatibility across all blocks. Since the selected 180 nm CMOS process has DNW, all NMOS within the DNW can be placed regardless of polarity of the voltage rails if the junction voltages are within their breakdown voltages (BVs). However, a PMOS has difficulty being used between -6 and -3 V rail because a bias (V_B) applied to the n -well (NW) of the PMOS must not be less than -0.7 V, otherwise a p - n junction diode between the PSUB and NW ($D_{NW/PSUB}$) will be turned on, resulting in a significant leakage current or a gate oxide breakdown, as shown in Figure 8b.

According to the datasheet of the selected technology, the BVs of p - n junction diodes, $D_{NW/PSUB}$ and $D_{P+/NW}$ (P^+ -to- NW diode), are 14.8 and 10.3 V in their I/O transistors (3.3 V), respectively, and it means that a 3.3 V I/O PMOS and NMOS can sustain 14.8 V and -10.3 V, respectively, if the proper DNW bias for the NMOS is applied. However, we limited the supply rails within ± 6 V in the current design to avoid too many transistor stackings and to ease design complexity, strictly imposed by the gate oxide BV limitation of 3.3 V.

Figure 9 illustrates a transistor-level schematic of a low side (LS) in the I-Driver to generate IC. The high-side (HS) of the I-Driver has the same configuration with different polarity of transistors. To sustain 6 V using 3.3 V I/O transistors (HVMOS: high-voltage MOS), multiple transistors are stacked, as shown in the configurations of M_{6L-8L} and diode-connected transistors. The DNW for all diode-connected transistors are shared with the bias of the highest potential of 0 V in the LS circuit to minimize the area consumption. The I-Driver is basically a current mirror, copying a current from the I-AMP (M_{1L}) and amplifying $4\times$ (M_{1L}) into the output of the driver (I_{OUT}), turning on and off are governed by S_{0-2} .

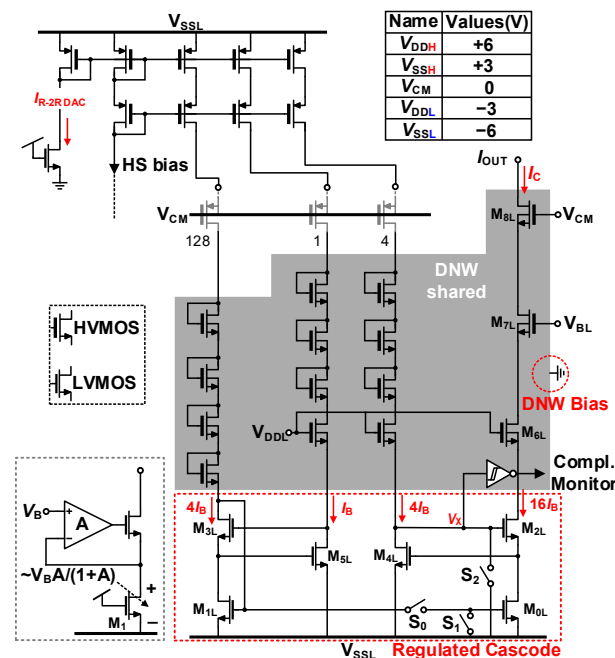


Figure 9. Transistor-level implementation of the LS circuit in the I-Driver.

Note that the current mirror (M_{0L} - M_{5L}) is implemented using low-voltage transistors (LVMOS) for better matching, and it also uses a regulated cascode technique to control drain potentials (V_{DS}) of M_{0L} and M_{1L} both to increase output resistance of the mirror and to improve matching (the red dotted box in Figure 9). The regulated cascode using amplifiers can suppress the voltage headroom of a current mirror [28], while improving matching of the current mirror by pinning V_{DS} of the mirror transistors (M_1) to $V_B \cdot A / (1 + A)$ with the aid of an amplifier (its gain is A), as shown in the gray dotted box in Figure 9; however, in this specific stimulator, PMOS transistors for the implementation of the amplifiers are unavailable in the V_{SSL} to V_{DDL} rails and implementing amplifiers are too much resource-consuming. Therefore, we implemented the regulated cascode using only two NMOS transistors (M_{4L} and M_{5L}) and bias currents. By applying proper bias currents, those are proportional to the output (or input) current, the V_{DS} for M_{0L} and M_{1L} can be well matched because V_{GS} in a transistor is proportional to a ratio of the drain current (I_D) and aspect ratio (W/L) of the transistor ($V_{GS} \propto \sqrt{I_D / (W/L)}$), assuming the all NMOS are deviated

in the same direction under process, voltage, and temperature variations. The stimulator retains $\sim 64\%$ ($16I_B/25I_B$) of its current efficiency regardless of the magnitudes of I_A and I_C . The I-Driver also has a compliance monitoring function using a node information (V_X), which can detect the triode region operation of M_{2L} when the I_{OUT} reaches ~ -6 V. The voltage rise at V_X is snatched by an inverter with hysteresis.

3.3.2. 8 b R-2R Digital-to-Analog Converter

To enable independent current control in each S_{PX} , it must have a dedicated DAC. However, implementing a dedicated DAC per channel significantly increases chip area, posing a considerable integration challenge. Specifically, a conventional current-steering DAC structure, although its straightforward in operation, results in exponential transistor multiplication, consuming excessive chip area. Thus, an R-2R DAC architecture has been implemented to exploit its compact size compared to current-steering DACs. The resistance required for the R-2R DAC has been realized PMOS transistors ($2.5\ \mu\text{m}/2.2\ \mu\text{m}$) operating in their triode region [29]. The transistor's on-resistance ($R_{on} \sim 1.1\ \text{M}\Omega$) is leveraged as the resistive element, significantly shrinking the DAC's physical footprint. The R-2R DAC can be laid out within $65.6 \times 25.6\ \mu\text{m}^2$. The implemented DAC has an LSB (least significant bit) of 200 nA, and it can generate currents up to a maximum of 51.2 μA (I_{bias}), offering the required precision and dynamic range.

3.3.3. Current Amplifier (I-Amp) and Level Shifters

The I-Amp is a set of current mirrors that copy the current from the R-2R DAC and deliver to the HS and LS of the I-Driver. The maximum gain of the I-Amp is $10\times$ that is too large to copy in a single current mirror with a decent precision, thus it is segmented as $2.5\times$ and $2\times$ or $4\times$ paths. For better matching between the HS and LS drivers, the regulated cascode used for the I-Driver has also been adopted in the I-Amp.

Since the S_{PX} requires a different set of voltage rails, specific level shifters must be implemented. Figure 10a–c representatively shows some of the implemented level shifters from 1.8 V to $V_{DDH}-V_{SSH}$, 1.8 V to $V_{DDL}-V_{SSL}$, and $V_{DDL}-V_{SSL}$ to 1.8 V, respectively. Figure 10a,b can also be used for the shifting from 1.8 V to $V_{SSH}-V_{CM}$ and 1.8 to $V_{CM}-V_{DDL}$, respectively, and a complimentary version of Figure 10c can also be used to realize a $V_{DDH}-V_{SSH}$ to 1.8 V conversion. Figure 10a is basically a level shifter with a cross-coupled pair, but with a modification of $M_{1,2}$ to boost regeneration and also to provide voltage clamping of the node V_X by the diodes ($D_{1,2}$). Figure 10b is from [30] and the separation between the 1.8 V rail and negative rails are made from $5\times$ series connected diodes that are realized by PMOS 3.3 V I/O transistors.

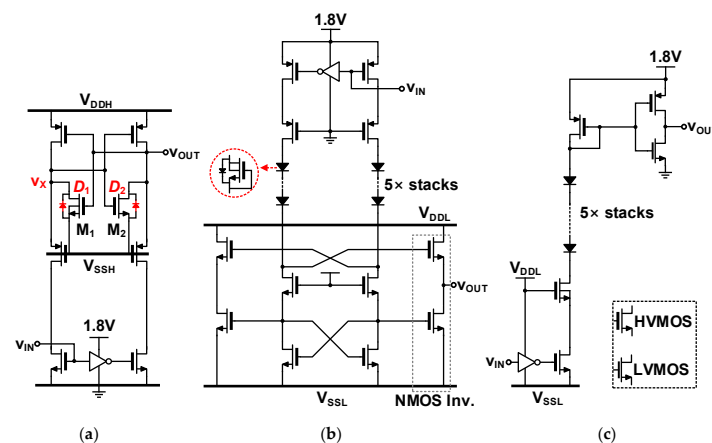


Figure 10. Level shifters: (a) 1.8 V to $V_{DDH}-V_{SSH}$, (b) 1.8 V to $V_{DDL}-V_{SSL}$, and (c) $V_{DDL}-V_{SSL}$ to 1.8 V.

3.4. Digital Interface

The digital interface consists of SPIs to communicate with the external world and first order digital high-pass filters (HPFs) for each channel to remove offsets induced by the mismatch of the analog frontend and to provide an additional adjustment of f_L according to users' demands. The SPI inputs and outputs are transmitted to the CMOS or low-voltage differential signaling (LVDS) drivers.

3.4.1. SPI and LVDS

The implemented SoC integrates three dedicated SPI slaves—two for 128-channel neural recording and one for 32-channel stimulation. The control lines of the SPI (SCLK and CSB) are shared among three SPIs and two outputs: master-input-slave output (MISO) lines are for 128 channel recordings (each supports 64 channels at most) and one MISO is for 32 channel stimulations. The inputs: master-output-slave-input (MOSI) lines are also separately assigned for the recording ($2\times$) and stimulation ($1\times$). Each SPI period spans 950 ns, comprising 16 SCLK pulses with each of ~ 40 ns period and one CSB. A complete SPI cycle consists of 32 standard SPI periods and 3 auxiliary periods (35×950 ns), which roughly supports ~ 30 kS/s for each channel. For the case where this neuromodulation SoC has to drive a long-line (a few meters) in a headstage [5], it integrates LVDS transmitters (TXs) and receivers (RXs) on the chip. The specifications of the LVDS RX and TX follow the industrial standard for compatibility with any commercial SPI masters. Since the standard LVDS waveforms have a specified amplitude (~ 350 mV) with a designated end-line resistance of $100\ \Omega$, the LVDS TX consumes ~ 4 mA current that is not appropriate for some biomedical applications. Therefore, the RX and TX are turned-on/off according to the users' settings and the communication can be replaced by standard 3.3 V I/O.

3.4.2. Digital High-Pass Filter

The block diagram of $32\times$ infinite impulse response (IIR) D-HPFs is shown in Figure 11a. A total of $4\times$ of them have been implemented. The HPF synchronously operates with the rising and falling edge of $\overline{CS}$ signal and channel information (Ch [4:0]). The z-domain which transfers function of the D-HPF is as follows:

$$H(z) = \frac{1 - z^{-1}}{1 - \alpha z^{-1}} \quad (6)$$

where α is a real pole and $0 < \alpha < 1$. The filter uses a first-order noise shaper (truncator) to reduce the truncation error due to the fixed-point error of the leaky integrator by the term, α [31]. Instead of the conventional cascade structure of a differentiator and a leaky integrator, this D-HPF realizes a single loop with a digital integrator in loop feedback. Due to single loop feedback without differentiator, no additional bit-extension for subtraction is required for 16 b data processing, resulting in area-efficient data processing with a 16 b bit-length. Also, to efficiently reduce this area, the 16 b multiplication logic is removed, and the D-HPF is configured to arithmetic shift logic for multiplication by two. This results in a dramatic $\sim 70\%$ reduction in the D-HPF to $\sim 10,000\ \mu\text{m}^2/\text{Ch}$. ($\sim 24,000\ \mu\text{m}^2$ for a 16 b multiplication logic). As a result, the area consumption of the D-HPF per channel is $\sim 32,000\ \mu\text{m}^2$ which contributes to the huge area of the on-chip DSP. Figure 11b shows the variable cutoff frequency ($f_{C,HPF}$) of the D-HPF vs. α . For $f_S = 20$ kS/s and 31.25 kS/s, $f_{C,HPF} = 0.04992$ and 0.078 Hz can be realized with the minimum α , which acts as a nearly perfect DC-blocker, while $f_{C,HPF} = 2.048$ and 3.2 kHz with the maximum α , respectively. The α is tunable with a 4-bit code.

topology has been adopted for the second-order LPF, thus it requires a single OTA for the implementation. The I/V converter consists of an array of capacitors and switches since it should drive a capacitive load (C_{in}) in the LNA. The Z_E measurement is performed only when there is a request, and then automatically shut down, thus the power consumption of the ZCHK in the normal operation is zero.

3.6. Power Management Unit and β -Multiplier

The PMU circuit consists of seven low dropout regulators (LDOs) for 1.2, 1.5, and 1.8 V used in the R_{PX} and Z_E measurements, and for 1.8, 2.5, ± 3 V used in the S_{PX} and a low voltage BGR. All supplies except for ± 3 V are provided by an external 3.3 V and ± 3 V supplies are generated by external ± 6 V. The low voltage BGR produces 0.9 V, which becomes the reference voltage for the LDOs except for the ± 3 V supplies. The BGR also generates all reference currents for the R_{PX} and S_{PX} . The design of the LDOs and BGR are adopted from our previous work [7]. The schematic of the β -multiplier is also adopted from [28] and modified.

4. Measurement

The proposed neuromodulation SoC has been fabricated using a 180 nm 1P6M CMOS process. A microphotograph of the fabricated chip is shown in Figure 13a, where the key circuit blocks are highlighted for visualization. The total active area occupied by the ASIC is $5940 \times 3895 \mu\text{m}^2$, excluding pads. The area must accommodate a large number of inputs, specifically 128 separate inputs and 4 reference inputs, all of which are directed toward the bottom side of the chip with staggered pads. Figure 13b depicts the power consumption breakdown. Total power consumption is 40.18 mW except for the LVDS drivers, which are used only when driving a meter-long cable. The LVDS drivers consume ~ 28 mW.

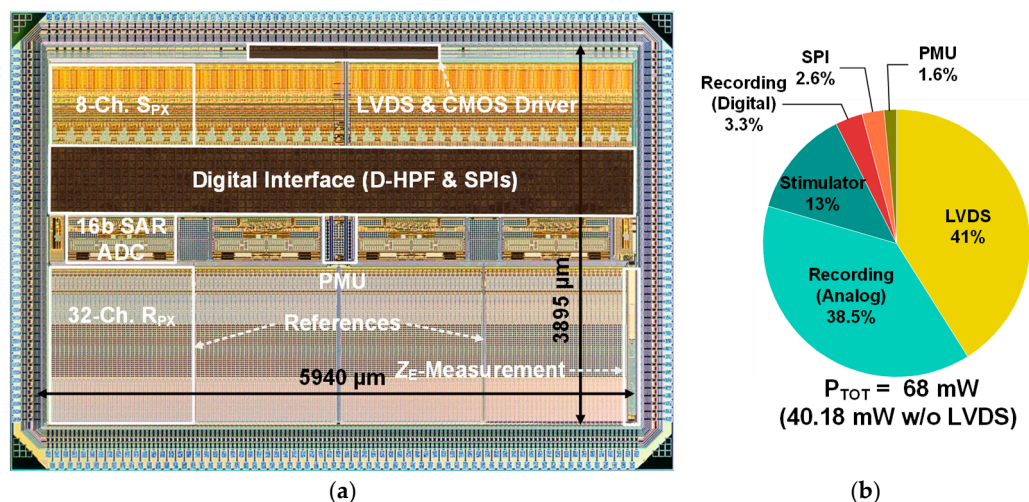


Figure 13. (a) Microphotograph of the fabricated neuromodulation SoC; (b) Power consumption breakdown.

4.1. Recording Pixel (R_{PX}) and ADC Measurement

Figure 14a shows the frequency response of a representative single channel R_{PX} measured with a dynamic signal analyzer (35670A, Agilent, Washington, USA). It exhibits a mid-band gain (G) of approximately 45.5 dB (~ 190 V/V) and >60 dB common mode rejection ratio (CMRR) with a bandwidth spanning from sub-Hz to 8 kHz—sufficient to simultaneously capture both LFPs and APs. The f_L is digitally programmable from $<<15$ mHz to 54 mHz. The f_H is also reconfigurable, enabling selectable high-frequency limits of 0.5, 0.85, 1, or 7.5 kHz. Figure 14b shows the IRN spectra of the R_{PX} measured

from 0.4 Hz to 50 kHz frequencies. The estimated $1/f$ -noise corner frequency (f_c) is ~ 300 Hz, and the thermal noise floor reaches approximately $30 \text{ nV}/\sqrt{\text{Hz}}$. The LFP (0.1 Hz–0.5 kHz), AP (300 Hz–7.5 kHz), and full band (0.1 Hz–7.5 kHz) noises are ~ 4.6 , ~ 1.8 , and $\sim 4 \mu\text{V}_{\text{rms}}$, respectively. All numbers indicate that the noise is low enough to measure neural signals in bands.

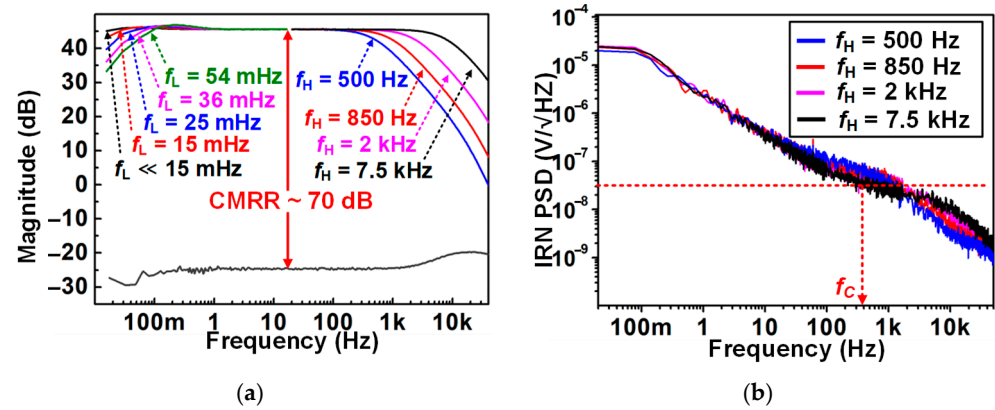


Figure 14. Spectral characteristics of the R_{PX} : (a) frequency response with different f_L and f_H sets, (b) input-referred noise spectra with different f_H sets.

Figure 15 shows the gain distributions of the entire 128 channels according to different gain and f_H sets. Inside each figure, the mean (μ) and standard deviation (σ) are also denoted. The gain spread is very narrow (e.g., $\sim 0.898\%$ in the worst case: LFP with $2\times$ gain set), showing decent channel uniformity. Figure 16 shows the noise distribution of the entire channels with different PGA gains and f_H . Due to the current scaling according to different f_H , the IRN variation is minimal from $f_H = 0.5$ to 7.5 kHz. The larger gain set in the PGA ($4\times$) reduces the noise contribution to the following blocks, such as the buffer and ADC, thus the IRN in this case showed a bit improvement, though it is minor.

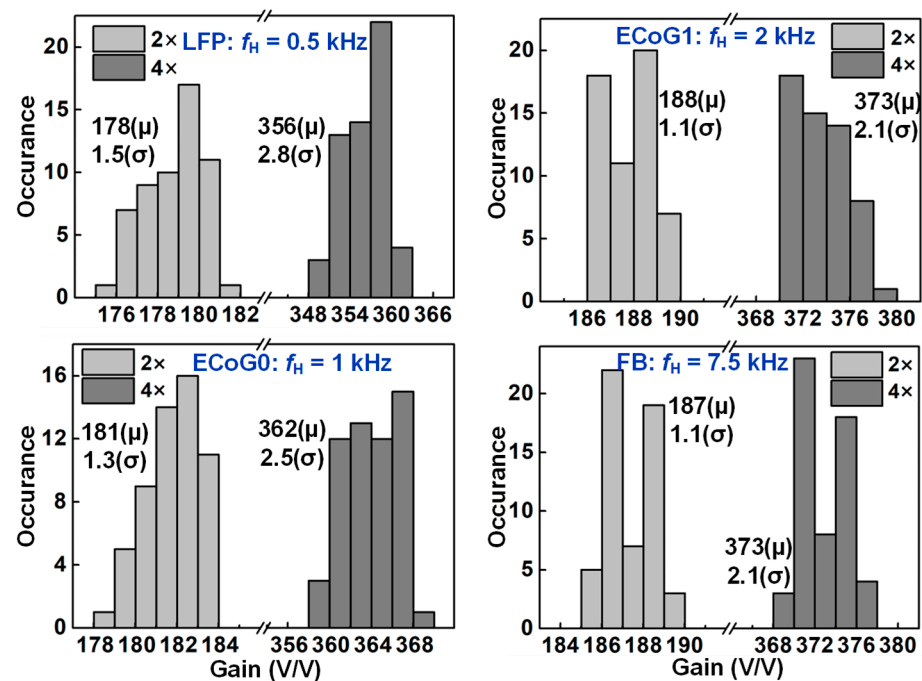


Figure 15. Gain distribution across the entire 128 channels with two gains of the PGA and different sets of f_H .

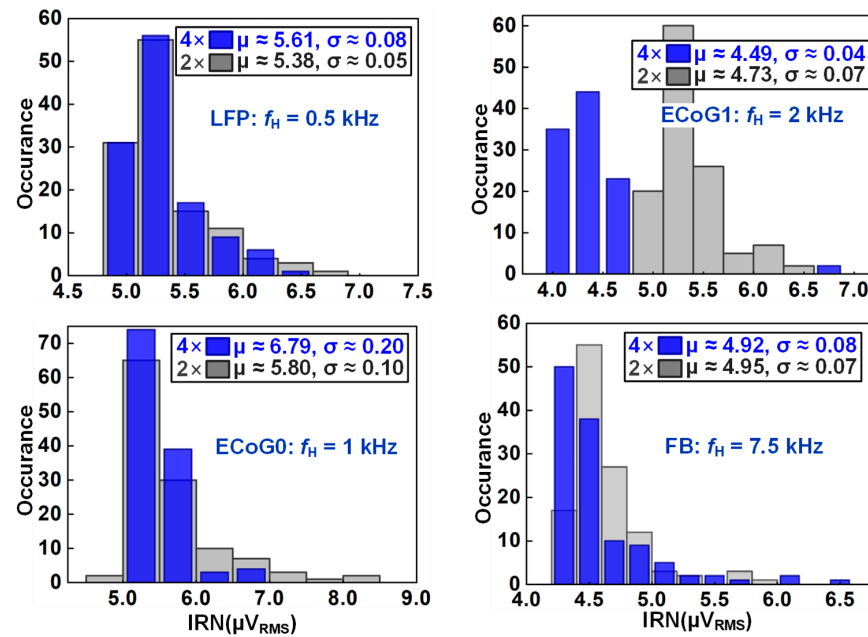


Figure 16. Noise distribution across the entire 128 channels with two gains of the PGA and different sets of f_H .

Figure 17a depicts the measured ADC spectra with (black) and without (dark gray) calibration with a -1.94 dBFS, 10 Hz sinusoidal input. Without calibration, the signal-to-noise and -distortion ratio (SNDR), spurious-free dynamic range (SFDR), and total harmonics distortion (THD) was measured as 53.49, 69.38, and -60.42 dB, respectively; those were recovered as 67.72, 82.49, and -76.78 dB with the calibration, indicating the effectiveness of the implemented foreground calibration. The measured SNDR was limited to ~ 70 dB, which is lower than the theoretical expectation. This discrepancy is attributed to the true single-phase clock (TSPC) dynamic logic used in the SAR controller for area efficiency. We identified that charge leakage in the TSPC gates caused transient glitches, elevating the noise floor. Since the implemented foreground calibration only corrects for static nonlinearities, these dynamic effects were not compensated. Future implementations should consider using static logic to mitigate this issue. Figure 17b shows the SNDR and SFDR versus frequencies from 5 Hz to 600 kHz. Note that the f_S of the ADC is 1 MS/s. This ADC shows a stable SNR of ~ 70 dB up to 10 kHz and exhibits a slight deviation near the $f_S/4$ (~ 66.62 dB). The effective number of bits (ENOBs) is 11.39 bits at 1 kHz.

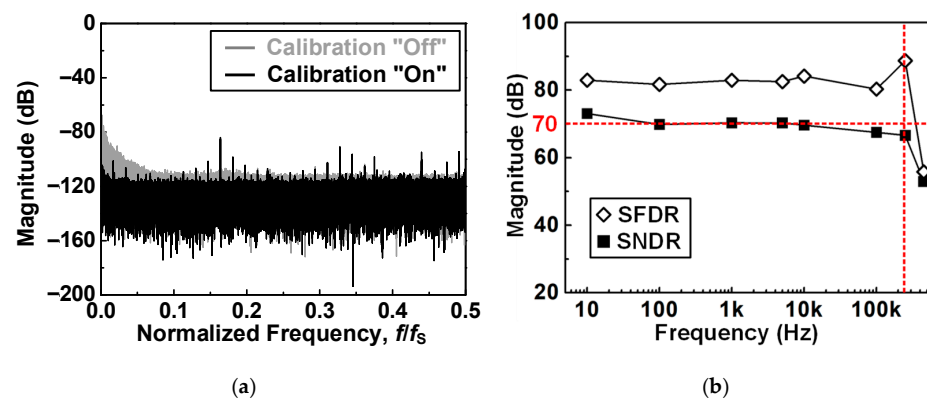


Figure 17. (a) Measured spectra of the ADC with and without calibration, (b) SNDR/SFDR performance vs. input frequency.

Figure 18 shows the measured results of the ZCHK circuit in comparison with a commercial product (RHD 2164, Intan Technologies, Los Angeles, CA, USA) that has a similar function [32]. For this measurement, a reference module where 32 combinations of different resistors and capacitors for a calibration of another commercial electrode impedance measurement instrument (NanoZTM, Plexon, Dallas, TX, USA) have been employed [33], as shown in Figure 18a. Overall, the two circuits work well for low impedance; however, the implemented circuit exhibits better accuracy regardless of the magnitude of the impedance, while the commercial product showed some deviations when the electrode impedance was high ($\sim 10\text{ M}\Omega$).

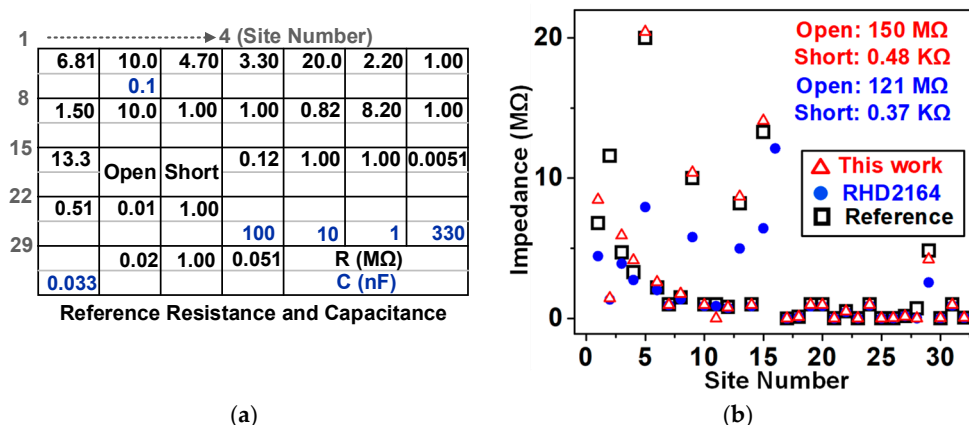


Figure 18. ZCHK circuit measurement: (a) reference values of the resistors and capacitors for the measurement, (b) measured results in comparison with a commercial product.

4.2. Stimulation Pixel (S_{PX}) Measurement

Figure 19a shows the I_A control using the different codes in the DAC ($10\times$ gain in the I-Amp). As shown, 0.1024 to 2.048 mA has been successfully delivered into a 2 k Ω resistive load. Figure 19b depicts a programmable pulse train of I_A and I_C (10 pulses). Each stimulation cycle consists of a 500 μ s cathodic phase (t_C), a 500 μ s inter-phase delay (t_D), and a 500 μ s anodic phase (t_A), with a stimulation amplitude of 2 mA. The inset shows the enlarged pulse trains.

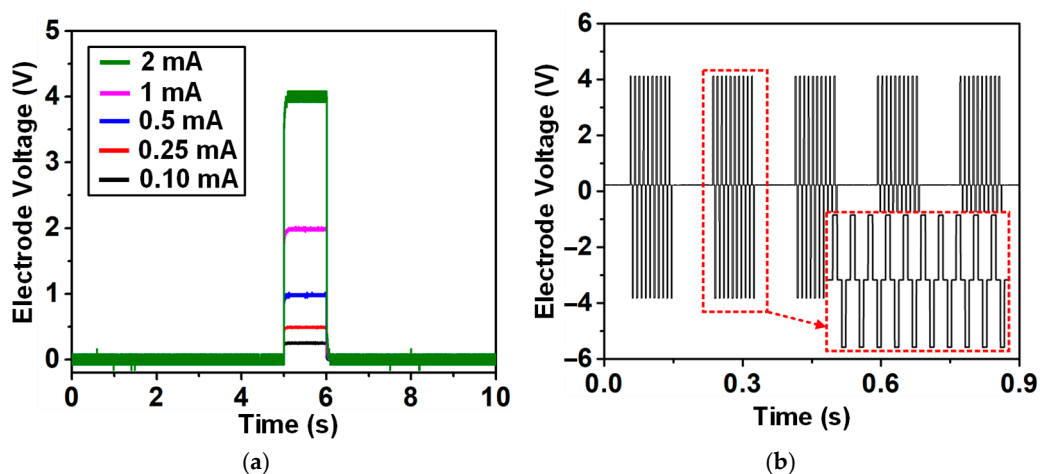


Figure 19. (a) I_A current control from 0.1024 to 2.048 mA, (b) I_A and I_C current pulse train.

Figure 20 illustrates mismatches of I_A and I_C from the entire 32-channel S_{PX} when each channel is programmed to generate 1 mA output current. Overall, the mismatches lie within $\pm 10\%$; however, some channels generating I_C show $>10\%$. This mismatch would not

affect the safety of the electrode thanks to the charge balancing switch that can eliminate the leftover charge.

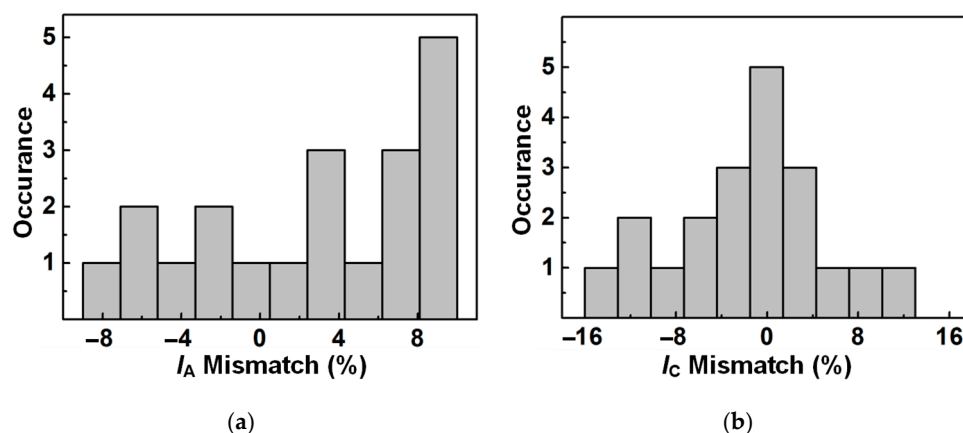


Figure 20. Distribution of the mismatch between I_A and I_C : (a) Mismatch of I_A , (b) Mismatch of I_C .

4.3. In Vitro Measurement and Summary

The signal acquisition performance of the fabricated ASIC has also been evaluated in an in vitro environment. A custom-designed silicon neural probe [34], interfaced with the ASIC, was immersed in a phosphate-buffered saline (PBS) solution along with reference and ground electrodes. To emulate biological neural activity, a set of previously recorded neural signals—acquired from the motor cortex of a rat—were replayed through the PBS medium. The overall configuration of the in vitro testing setup and an array of the microelectrode used for the in vitro experiments are shown in Figures 21a and 21b, respectively. For these tests, the ASIC was configured to operate at its maximum bandwidth setting to enable simultaneous recording of both LFPs and APs. The acquired data were transmitted to a host computer via a custom USB-based interface board for subsequent analysis.

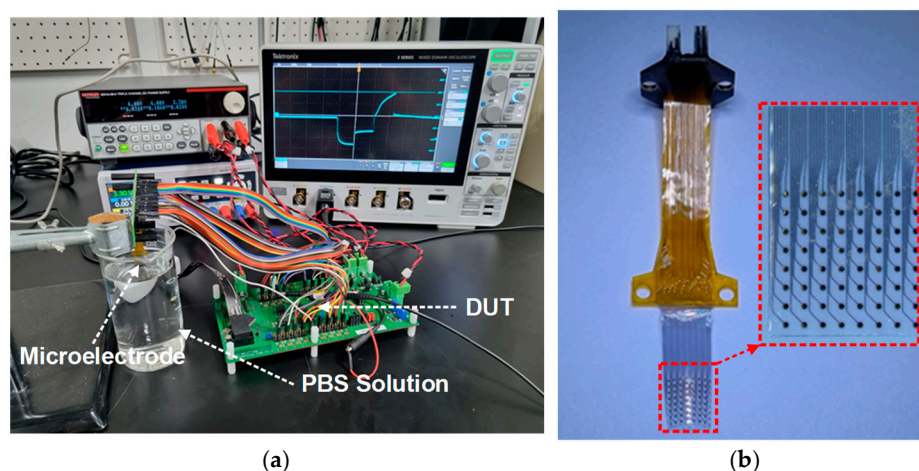


Figure 21. In vitro test setup (a), and microelectrode used for the in vitro test (b).

The unprocessed signals are presented in the upper panel of Figure 22a. To enhance signal clarity, the neural recordings were processed using a third-order Butterworth bandpass filter (passband: 0.8–7 kHz; stopband: <0.6 kHz and >8 kHz) implemented in MATLAB (R2025a, MathWorks, Natick, MA, USA). The filtered output, emphasizing AP activity, is shown in the lower panel of Figure 22b where a magnified view of approximately 80 μ s of concurrent LFP and AP signals is also provided. Figure 22b depicts the two different APs detected, extracted, and aligned in MATLAB. The clear distinction between the two

different APs is attributed to low noise and distortion performance of the R_{PX} . Figure 23a shows the in vitro recording with (red) and without (blue) fast-reset switching operations. After turning off the reset switch, there is no settling delay.

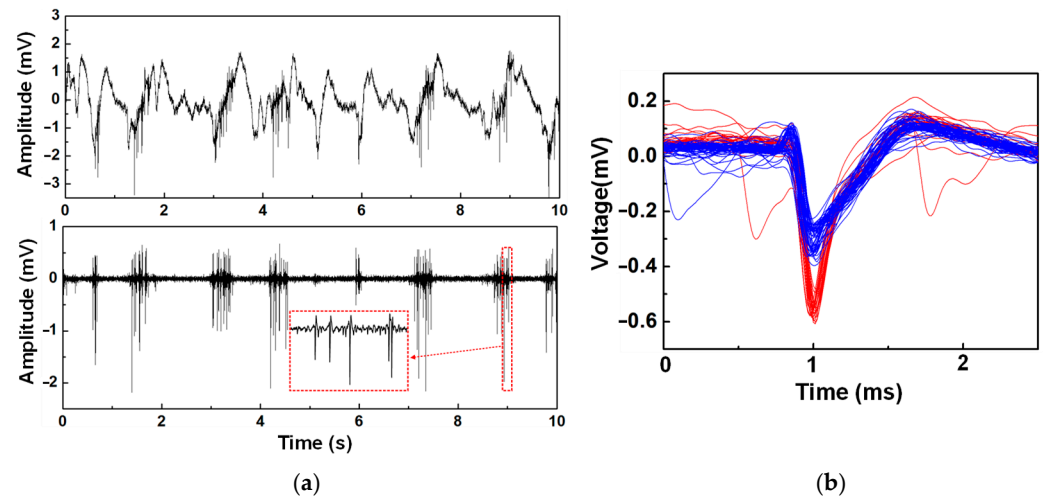


Figure 22. (a) Broadband (LFP + AP) neural signal recorded in vitro (upper), and the extracted AP (lower), (b) detected, extracted, and aligned AP signals.

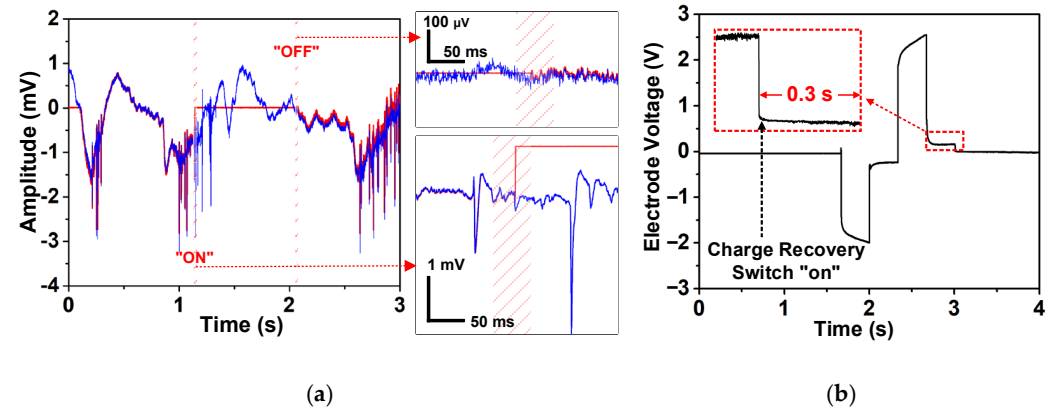


Figure 23. (a) Fast-recovery operation, (b) charge recovery switch operation.

The charge recovery switch for the CB was also verified in vitro. Figure 23b shows the measurement results under a condition where a 20% current mismatch was intentionally introduced. For this experiment, the electrode–tissue interface is modeled using a load comprising a 2 μ F double-layer capacitance (C_{DL}) and a 1 k Ω series resistance (R_S). When the charge recovery switch is enabled, the electrode potential quickly returns from approximately 160 mV back to 0 V, confirming the effectiveness of the implemented CB mechanism. The estimated on-resistance of the CB switch is ~ 1 k Ω .

Table 1 summarizes the measurement results and compares them with other state-of-the-art neuromodulation SoCs and a commercial product [35]. In terms of the number of recording and stimulation channels, this work shows the highest number ever reported with reasonable power and area consumption, and the highest density except for [1] and [4]. Furthermore, on a block-level, the recording ASIC achieves a competitive Noise Efficiency Factor (NEF) of 8.9, and the ADC demonstrates a Walden FoM of 100.4 fJ/c-s and a Schreier FoM of 160.4 dB, confirming that high integration was achieved without sacrificing performance efficiency. However, the presented work shows the highest level of integration by including all required circuit blocks on chip and has the largest number of parallel recording and stimulation in a single die. In addition, the proposed SoC is able

to operate with a single external supply of 3.3 V and equips important functionalities for neuromodulation, such as ZCHK, fast-reset, LVDS, and CB.

Table 1. Comparison table of neuromodulation SoCs.

	[1]	[2]	[3]	[4]	[35]	This Work
Neuromodulation SoC						
^(a) # of Channel (R./S.)	^(b) 64/2	32/32	32/4	128/8	16/16	128/32
^(c) System Integration	N	Y	Y	N	Y	Y
Z _E Measurement	N	Y	N	N	Y	Y
Chip area (mm ²)	4.78	24.91	30.25(R) + 36(S) (Two chips)	11.52 × 2 (Two chips)	23.42	31.96
Area/Ch (mm ²)	0.118	0.389	0.945/6	0.169	0.732	0.2
System Power (mW)	—	^(d) 6.2	—	^(h) 172	34.5	40.18
Power/Ch (mW)	—	^(d) 0.194	—	^(h) 1.265	1.078	0.251
Technology	65 nm CMOS	180 nm BCD	180 nm BCD	180 nm BCD	—	180 nm CMOS
Recording ASIC						
IRN (μV _{rms})	7.5	3.8/3.3 (LFP/AP)	1.03	^(e) 1.02	2.4	⁽ⁱ⁾ 4
BW (Hz)	10–8 k	0.2–7.5 k	2–200	^(e) 1–200	0.1–20 k	0.1–7.5 k
NEF	3.6	3.1/4.5 (LFP/AP)	2.37	15	—	8.9
f _S /Ch. (kS/s)	—	20	^(e) 0.4	1	40	30
ADC Resolution (bit)	10	16	12	15	16	16
ADC ENOB	8.2	12.1	10.47	10.2	—	11.39
FoM _S (dB)	167.1	153.2	—	—	—	160.4
FoM _W (fJ/c–s)	4.25	1170	—	—	—	100.4
Supply Voltage (V)	1.0	1.8	1.0	1.0	3.3	3.3
Fast Recovery	Y (switch)	N (—)	Y ^(f) SSCS	Y (Lin. Interp.)	Y (switch)	Y (switch)
Stimulation ASIC						
Mono (M)-/Bipolar (B)	B	M	M	M	M	M
Resolution (bits)	6	6	8	8	8	9
Min. Current (μA)	7	32	—	—	0.01	4
Max. current (mA)	0.9	10.2	12.75	5	2.55	2
Voltage compliance (V)	8	±9	40	12	±9 (–12/6)	±6
Multipolar stim.	N	Y	Y	Y	Y	Y
Charge Balancing	N	Y (switch)	Y ^(g) TBCB	Y (switch)	Y (switch)	Y (switch)

^(a) R: recording, S: stimulation, ^(b) up to eight channels covered by multiplexing, ^(c) system integration indicates that the implementation does not require any external supports except for a single power supply, ^(d) power consumption in the recording circuit only, ^(e) estimated based on the given information, ^(f) SSCS: stimulation-side contour shaping, ^(g) TBCB: time-based charge balancing, ^(h) radio power included, ⁽ⁱ⁾ full-bandwidth (0.1 Hz–50 kHz) considered.

5. Conclusions

This paper presents a fully integrated neuromodulation ASIC that combines a 128-channel neural recording system with a 32-channel current-mode stimulator on a single chip, fabricated using a standard 180 nm CMOS process. The proposed system supports bi-directional neural interfacing, enabling simultaneous high-fidelity neural signal acquisition and precise electrical stimulation, making it suitable for a wide range of neuroscience and clinical applications. The analog front-end (AFE) employs a capacitive-coupled LNA

architecture with a digitally programmable bandwidth via a 2-bit current DAC, achieving an input-referred noise of $3.8 \mu\text{V}_{\text{rms}}$ while consuming only $682 \mu\text{W}$ per channel. The PGA provides two gain settings, and a 16-bit SAR ADC with foreground calibration enables high-resolution digitization at sampling rates up to 30 kS/s . An area- and power-efficient digital high-pass filter (D-HPF) and SPI-based digital controller further contribute to compact system integration. On the stimulation side, the 32-channel current-mode stimulator supports a wide current range ($4 \mu\text{A}$ to 2 mA) using a 9-bit R-2R DAC, current amplifier, and high-voltage current driver with $\pm 6 \text{ V}$ compliance. A passive discharge switch is included in each pixel to ensure charge balancing and stimulation safety. Measurement results confirm accurate current delivery, programmable waveform generation, and robust passive charge balancing even under deliberate mismatch conditions. In vitro testing further verifies the recording functionality under biological-like conditions. Compared with existing state-of-the-art solutions, the proposed ASIC offers a high degree of integration and configurability while maintaining low power consumption and high signal quality. This work demonstrates a promising platform for future bi-directional closed-loop neural interface systems aimed at both research and clinical neuromodulation therapies.

Author Contributions: Conceptualization, G.P. and S.-Y.P.; methodology, G.P. and J.K.; software, J.C.; validation, G.P., J.K., J.C., and D.K.; formal analysis, G.P. and J.C.; investigation, G.P., J.C.; data curation, J.C. and B.Y.; writing—original draft preparation, G.P.; writing—review and editing, G.P., J.K., M.K. (Minjae Kim), M.K. (Minsung Kim), B.Y., J.C., D.K., and S.-Y.P.; visualization, J.C. and G.P.; supervision, S.-Y.P.; project administration, S.-Y.P.; funding acquisition, S.-Y.P. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the Challengeable Future Defense Technology Research and Development Program through the Agency For Defense Development (ADD) funded by the Defense Acquisition Program Administration (DAPA) in 2022(No. 915069201), the Seoul R&BD Program (BT240032) and also by BK21PLUS, Creative Human Resource Education and Research Programs for ICT Convergence in the 4th Industrial Revolution.

Data Availability Statement: Data are contained within this article. The raw data supporting the conclusions of this article will be made available by the author on request.

Acknowledgments: The EDA Tools was supported by IC Design Education Center (IDEC).

Conflicts of Interest: The authors declare no conflicts of interest.

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