

Article

Design Phase-Locked Loop Using a Continuous-Time Bandpass Delta-Sigma Time-to-Digital Converter

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Abstract

This paper presents an all-digital fractional-N phase-locked loop (ADPLL) operating in the 2.86–3.2 GHz range, optimized for IoT and high-frequency RF transceiver applications demanding stringent phase noise performance, fast settling time, and high integration capability. The key innovation lies in the introduction of a bandpass delta-sigma time-to-digital converter (BPDSTDC) that achieves high-resolution phase detection, an extended detection range of $\pm 2\pi$, and superior noise-shaping characteristics, completely eliminating the complex calibration procedures typically required in conventional TDC designs. The proposed architecture synergistically combines the BPDSTDC with digital down-conversion blocks to extract phase error at baseband, a divider chain integrated with phase interpolators achieving 1/4 fractional resolution to suppress in-band quantization noise, and a wide-bandwidth digital loop filter (>1 MHz) ensuring fast dynamic response and robust stability. The bandpass delta-sigma modulator is implemented with compact resonator structures and a flash quantizer, achieving an optimal balance among resolution, power consumption, and silicon area. The incorporation of highly linear phase interpolators extends fractional frequency synthesis capability without requiring complex digital-to-time converters (DTCs), significantly reducing design complexity and calibration overhead. Fabricated in a 180-nm CMOS technology, the proposed chip demonstrates robust measured performance. The band-pass delta-sigma TDC achieves a low integrated rms timing noise of 183 fs within a 1-MHz bandwidth. Leveraging this low TDC noise, the complete ADPLL exhibits a measured in-band phase noise of -120 dBc/Hz at a 1-MHz offset for a 3.2-GHz output frequency while operating with a loop bandwidth exceeding 1 MHz. This corresponds to a normalized phase noise of -216 dBc/Hz. The system operates from a 1.8-V supply and consumes 10 mW, achieving competitive performance compared with prior noise-shaping TDC-based all-digital PLLs.



Academic Editors: Nikolay Hinov,
Jožef Ritonja and Gergana Vacheva

Received: 15 January 2026

Revised: 1 February 2026

Accepted: 2 February 2026

Published: 4 February 2026

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Keywords: all-digital fractional-N phase-locked loop (ADPLL); time-to-digital converter; bandpass delta-sigma time-to-digital converter; phase interpolators quantization noise; phase noise

1. Introduction

Phase-locked loops (PLLs) operating in the multi-gigahertz frequency range with low reference frequencies are essential building blocks in modern Internet-of-Things (IoT) and highly integrated RF transceiver systems [1,2]. Contemporary IoT wireless standards, including IEEE 802.15.4 (ZigBee) [2], Thread, and proprietary sub-GHz protocols, increasingly

employ frequency bands around 2.4–3.2 GHz for unlicensed operation, while emerging ultra-wideband (UWB) ranging and radar applications target the 3.1–10.6 GHz range. These applications require frequency synthesizers capable of generating stable carriers in the 2.86–3.2 GHz range to support frequency translation, local oscillator generation, and direct digital modulation. Such applications impose increasingly stringent requirements on phase noise, settling time, power consumption, and scalability under advanced CMOS processes. In particular, the combination of low reference frequencies and wide output tuning ranges results in large division ratios, which significantly magnify the impact of phase detector and quantization noise on in-band phase noise performance. Therefore, the design of the phase detector block plays a crucial role in ensuring low phase jitter for the frequency synthesizer, especially when adhering to strict power and area constraints [3].

All-digital phase-locked loops (ADPLLs) have emerged as attractive alternatives to conventional analog PLLs due to their superior portability, programmability, and compatibility with digital CMOS scaling [4,5]. In ADPLLs, time-to-digital converters (TDCs) replace conventional phase-frequency detectors and charge pumps, enabling fully digital loop implementation. However, the finite resolution and limited detection range of conventional TDC architectures introduce substantial quantization noise and nonlinearity within the PLL loop bandwidth.

Several TDC architectures have been proposed to address the quantization noise challenge in ADPLLs. Delay-line-based TDCs [6,7] achieve fine resolution (10–20 ps) but suffer from limited detection range (± 1 unit interval), require extensive PVT calibration, and introduce significant DNL/INL that degrade phase noise when loop bandwidth exceeds 500 kHz. Vernier TDCs [8] provide sub-gate-delay resolution but face metastability issues at high reference frequencies and consume substantial power (>15 mW for multi-GHz operation). Gated-ring-oscillator (GRO) TDCs [9,10] achieve first order noise shaping with wide detection range but exhibit limited effective resolution due to coarse quantization levels. When integrated into PLLs with loop bandwidth approaching 1 MHz, the residual quantization noise floor remains high ($>300 f_{s_{rms}}$), limiting achievable phase noise performance. Low-pass delta-sigma TDCs [11,12] push quantization noise toward higher frequencies, which is highly effective when $f_{REF} \gg f_{BW}$. However, when reference frequency is constrained to tens of MHz while wide loop bandwidth (>1 MHz) is required for fast settling as typical in IoT transceivers, the available out-of-band spectral region becomes insufficient. This limitation leads to noise folding, elevated in-band quantization noise, and increased fractional spurious tones [13,14].

To overcome these limitations, bandpass noise-shaping techniques offer a fundamentally different approach by placing the zeros of the quantization noise transfer function around the PLL loop bandwidth rather than at DC [15,16]. By actively suppressing quantization noise within the frequency region where the PLL is most sensitive, bandpass delta-sigma architectures provide an opportunity to simultaneously support wide loop bandwidths and low in-band phase noise without resorting to excessively fine TDC resolution or aggressive calibration [17,18]. Nevertheless, the integration of bandpass delta-sigma TDCs into high-performance ADPLLs presents several challenges, including loop stability under nested feedback, quantization-induced spurious tones, and practical implementation trade-offs among resolution, power, and silicon area [19,20].

This paper presents an all-digital fractional-N PLL architecture incorporating a bandpass delta-sigma time-to-digital converter (BPDSTDC) to address these challenges in low-reference, multi-gigahertz frequency synthesis. The proposed BPDSTDC achieves high-resolution phase detection over an extended $\pm 2\pi$ detection range while eliminating the need for complex calibration procedures commonly required in conventional TDC designs. By combining bandpass delta-sigma noise shaping with digital down-conversion, the phase

error is extracted at baseband, enabling effective suppression of in-band quantization noise even with a wide loop bandwidth exceeding 1 MHz.

The proposed ADPLL further integrates a fractional divider chain with phase interpolators providing $1/4$ fractional resolution, significantly reducing in-band quantization noise without relying on digital-to-time converters or calibration-intensive linearization techniques [21,22]. The bandpass delta-sigma modulator is implemented using compact resonator structures and a flash quantizer, achieving a balanced trade-off among resolution, power consumption, and area. Through co-design of the phase detection, fractional synthesis, and digital loop filter, the proposed architecture achieves fast dynamic response, robust loop stability, and low phase noise [23,24].

Compared with earlier noise-shaping or bandpass-TDC PLLs, the key novelty of this work lies in the system-level integration and circuit realization of the bandpass delta-sigma phase detector under low- f_{REF} and wide-bandwidth constraints. This paper implements a continuous-time BPDSTDC that directly processes the reference–feedback phase error while providing $\pm 2\pi$ detection range, and explicitly co-designs the active bandpass loop filter, TIA isolation, and multi-bit quantizer to maintain loop stability and reduce quantization-induced spurious tones. In addition, the proposed architecture combines bandpass noise shaping with digital down-conversion to extract the phase error at baseband, targeting the frequency region where the PLL is most sensitive when the loop bandwidth exceeds 1 MHz. Finally, the fractional synthesis path employs phase interpolation in the feedback divider chain to reduce the effective phase step presented to the TDC, alleviating in-band quantization requirements without resorting to a DTC or calibration-intensive linearization. These features jointly enable low in-band phase noise and low timing jitter at multi-gigahertz output frequencies with a low reference frequency and modest power/area overhead.

Fabricated in a 180-nm CMOS technology, the chip demonstrates robust measured performance. The proposed band-pass delta-sigma TDC achieves an integrated rms timing jitter of $183 f_{s_{\text{rms}}}$ within a 1-MHz bandwidth. Leveraging this low TDC noise, the complete ADPLL exhibits a measured in-band phase noise of -120 dBc/Hz at a 1-MHz offset for a 3.2-GHz output frequency, while operating with a loop bandwidth exceeding 1 MHz. This corresponds to a normalized phase noise of -216 dBc/Hz. The entire system operates from a 1.8-V supply and consumes 10 mW, achieving competitive performance compared to prior noise-shaping TDC-based all-digital PLL implementations.

2. System Architecture

Figure 1 illustrates the overall architecture of the proposed all-digital fractional-N phase-locked loop (ADPLL). The system is designed to operate with a low reference frequency while achieving a multi-gigahertz output frequency range, wide loop bandwidth, and low in-band phase noise, making it suitable for highly integrated RF transceivers and frequency-modulated applications.

The phase detection path of the ADPLL employs a band-pass delta-sigma time-to-digital converter (BPDSTDC), which measures the time difference between the reference clock edge and the feedback signal, while shaping the quantization noise away from low frequencies through a band-pass noise transfer function. Since the output of the BPDSTDC is not located at baseband, a digital down-conversion (DDC) block is inserted immediately after the TDC to translate the band-pass-shaped signal to baseband and to suppress out-of-band components through digital low-pass filtering. As a result, the useful phase error component is accurately recovered before being processed by the loop filter.

The baseband phase error is processed by a type-II digital loop filter, which enables a loop bandwidth exceeding 1 MHz to achieve fast dynamic response and reduced settling time. The output of the loop filter is then applied to a delta-sigma modulator used for

fractional control, which shapes the quantization noise associated with the fractional control word before it affects the phase feedback path. This delta-sigma modulator is functionally distinct from the BPDSTDC and is dedicated to reducing in-band quantization noise and fractional spurs during frequency synthesis.

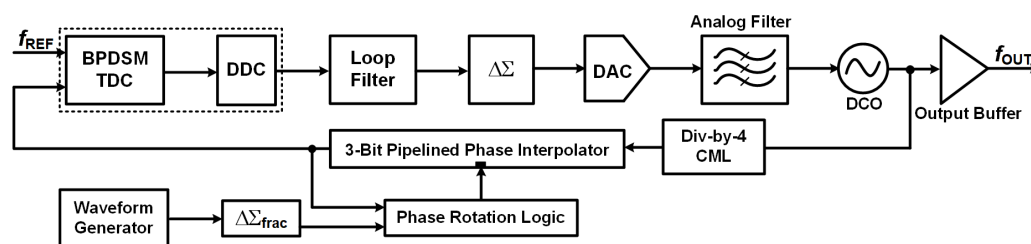


Figure 1. The proposed ADPLL architecture with BPDSTDC.

In the feedback path, a CML divide-by-4 divider generates four evenly spaced clock phases at 0° , 90° , 180° , and 270° . These phases are fed into a multi-stage pipelined phase interpolator with 3-bit resolution. The phase interpolator generates intermediate phase steps with fine resolution, enabling fractional-N frequency synthesis without the use of a digital-to-time converter (DTC). By reducing the effective phase step size during fractional operation, the phase interpolator significantly suppresses in-band quantization noise and fractional spurious tones.

A waveform generator, together with a dedicated delta-sigma modulator, provides control codes for the phase interpolator, enabling accurate frequency modulation and chirp generation. This modulation path operates in parallel with the main PLL loop and does not compromise loop stability.

The final frequency control signal drives a digitally controlled ring oscillator (DCO), in which the digital control word directly adjusts the delay elements or current control within the oscillator. This approach enables a fully digital PLL implementation with high integration density while avoiding the complex calibration procedures commonly required in analog-intensive architectures. The oscillator output is buffered and delivered as the output signal, and it is simultaneously fed back to the divider to close the PLL loop.

3. System Modeling and Analysis

3.1. Discrete-Time Phase Domain Modeling and Analysis

Figure 2 presents the discrete-time phase-domain model of the proposed ADPLL incorporating a BPDSTDC, DDC, a digital loop filter, and a phase-interpolator-based fractional feedback path. All signals are analyzed in the phase domain and sampled at the reference clock period T_{REF} , which is consistent with the fully digital nature of the proposed architecture.

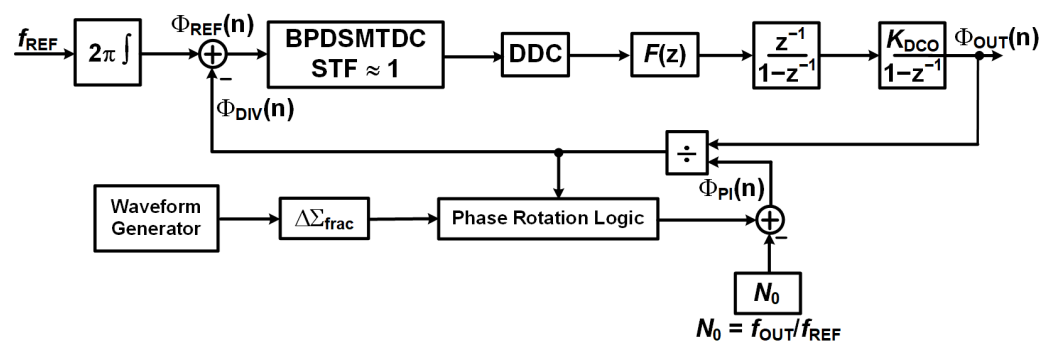


Figure 2. The discrete-time phase-domain model of the proposed.

The reference phase is given by $\Phi_{\text{REF}}(n)$, and the phase error is formed as $\Phi_e(n) = \Phi_{\text{REF}}(n) - \Phi_{\text{DIV}}(n)$. The BPDSTDC digitizes the phase error with a signal transfer function approximately equal to unity while shaping the quantization noise by a band-pass noise transfer function $NTF_{\text{BP}}(z)$. Since the TDC output is band-pass in nature, a DDC block translates the signal to baseband prior to loop filtering.

The baseband phase error is processed by a digital loop filter $F(z)$ and accumulated by a discrete-time integrator. The DCO is modeled as a phase integrator (in Equation (1)) with gain K_{DCO} , and $U(n)$ denotes the digital control word applied to the DCO.

$$\Phi_{\text{OUT}}(n) = \frac{K_{\text{DCO}}}{1 - z^{-1}} \cdot U(n) \quad (1)$$

In the feedback path, the output phase is divided by the integer division ratio as shown in Equation (2).

$$N_0 = \frac{f_{\text{OUT}}}{f_{\text{REF}}} \quad (2)$$

Fractional-N operation is realized through phase interpolation rather than divider modulation or digital-to-time conversion. Specifically, a fractional phase term $\Phi_{\text{PI}}(n)$ is injected into the feedback phase that using in Equation (3).

$$\Phi_{\text{DIV}}(n) = \frac{\Phi_{\text{OUT}}(n)}{N_0} + \Phi_{\text{PI}}(n) \quad (3)$$

The fractional phase $\Phi_{\text{PI}}(n)$ is generated by phase-rotation logic driven by a dedicated fractional delta-sigma modulator $\Delta\Sigma_{\text{frac}}$ and a waveform generator. This fractional path operates in parallel with the main PLL loop and provides fine phase resolution by selecting or interpolating among multiple evenly spaced clock phases. The associated quantization noise is spectrally shaped by $\Delta\Sigma_{\text{frac}}$, thereby significantly reducing in-band fractional spurs.

Combining the above relations, the closed-loop phase transfer function from the reference phase to the output phase can be expressed as Equation (4).

$$\frac{\Phi_{\text{OUT}}(z)}{\Phi_{\text{REF}}(z)} = \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{(1 - z^{-1}) \cdot \left[1 + \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{N_0 \cdot (1 - z^{-1})} \right]} \quad (4)$$

3.2. Phase Noise and Quantization Noise Analysis

Based on the discrete-time phase-domain model in Figure 2, the output phase noise of the proposed ADPLL can be expressed as the superposition of several independent noise sources, including the reference phase noise, BPDSTDC quantization noise, fractional phase interpolation noise, and DCO noise.

3.2.1. Reference Phase Noise

The reference phase noise $\Phi_{\text{REF}}(z)$ is transferred to the output through the closed-loop phase transfer function in Equation (5).

$$H_{\text{REF}}(z) = \frac{\Phi_{\text{OUT}}(z)}{\Phi_{\text{REF}}(z)} = \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{(1 - z^{-1}) \cdot \left[1 + \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{N_0 \cdot (1 - z^{-1})} \right]} \quad (5)$$

Within the loop bandwidth, the reference phase noise is multiplied by approximately N_0^2 , as expected in integer- or fractional-N PLLs. Outside the loop bandwidth, the reference contribution is strongly attenuated by the loop dynamics.

3.2.2. BPDSTDC Quantization Noise

The BPDSTDC quantization noise $Q_{\text{TDC}}(z)$ is shaped by a band-pass noise transfer function $NTF_{\text{BP}}(z)$, resulting in Equation (6).

$$\Phi_{\text{TDC}}(z) = NTF_{\text{BP}}(z) \cdot Q_{\text{TDC}}(z) \quad (6)$$

Unlike conventional TDCs that shape noise toward high frequencies or DC, the band-pass characteristic pushes most of the quantization noise away from baseband. After digital down-conversion, only the residual noise within the loop bandwidth contributes to the output phase noise. The corresponding transfer function to the output is Equation (7).

$$H_{\text{TDC}}(z) = \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{(1 - z^{-1}) \cdot \left[1 + \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{N_0 \cdot (1 - z^{-1})}\right]} \quad (7)$$

3.2.3. Fractional Phase Interpolation Noise

Fractional-N operation is realized through phase interpolation rather than divider modulation. The fractional phase $\Phi_{\text{PI}}(n)$ is generated by a phase rotation logic controlled by a delta-sigma modulator $\Delta\Sigma_{\text{frac}}$. According to Equation (8), the quantization noise of $\Delta\Sigma_{\text{frac}}$, denoted as $Q_{\text{frac}}(z)$, is spectrally shaped toward high frequencies.

$$\Phi_{\text{PI}}(z) = NTF_{\text{frac}}(z) \cdot Q_{\text{frac}}(z) \quad (8)$$

This fractional phase is injected additively into the feedback path and therefore experiences the same closed-loop attenuation as other feedback-related disturbances. Due to the noise shaping of $\Delta\Sigma_{\text{frac}}$ and the fine phase resolution of the pipelined phase interpolator, fractional spurs and in-band noise are effectively suppressed that is shown in Equation (9).

$$\Phi_{\text{DIV}}(z) = \frac{\Phi_{\text{OUT}}(z)}{N_0} + \Phi_{\text{PI}}(z) \quad (9)$$

3.2.4. DCO Noise

The intrinsic phase noise of the digitally controlled oscillator, denoted as $\Phi_{\text{DCO}}(z)$, is injected directly at the output and shaped by the complementary sensitivity function that is shown in Equation (10).

$$H_{\text{DCO}}(z) = \frac{1}{1 + \frac{K_{\text{DCO}} \cdot F(z) \cdot z^{-1}}{N_0 \cdot (1 - z^{-1})}} \quad (10)$$

Consequently, DCO noise dominates outside the loop bandwidth while being suppressed inside the loop. The wide loop bandwidth enabled by the digital implementation (>1 MHz) allows effective suppression of close-in DCO phase noise.

4. Circuit Implementation

Section 4 presents the circuit level implementation of the key building blocks in this proposed ADPLL, including the BPDSM modulator used in the TDC, DDC, the DCO, the high-speed frequency divider and the pipelined phase interpolator. The design choices are focused on achieving low in-band phase noise, wide loop bandwidth and robust operation under practical implementation constraints.

4.1. Bandpass Delta-Sigma Modulator TDC

The proposed band-pass delta-sigma time-to-digital converter is designed to directly process the time/phase error between the reference clock and the feedback signal while shaping the quantization noise away from low frequencies. As illustrated in the Figure 3,

the TDC consists of an active band-pass loop filter, a trans-impedance amplifier (TIA), and a multi-bit flash quantizer, which together form a continuous-time band-pass delta-sigma modulator operating in the time domain.

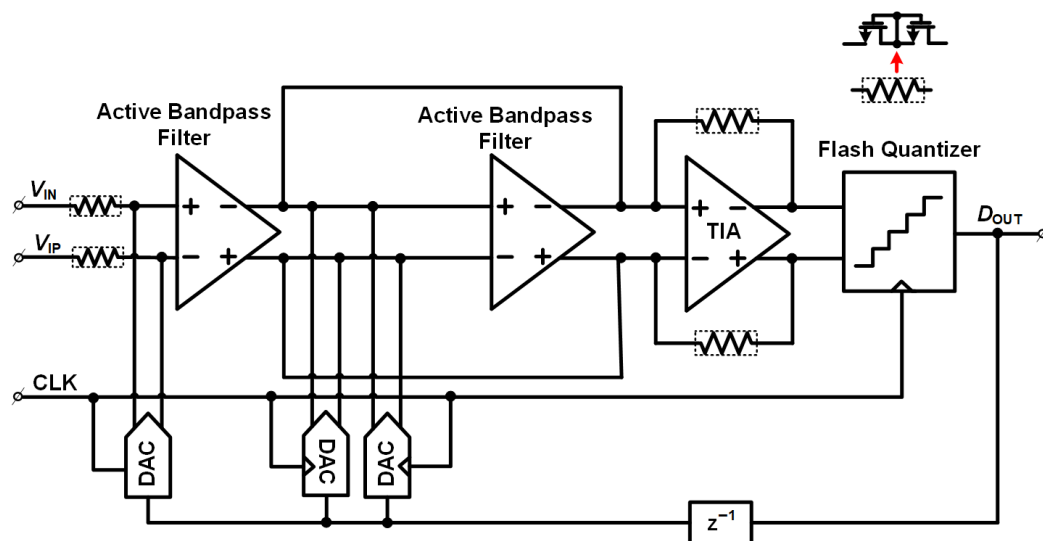


Figure 3. Block-level circuit implementation of the proposed band-pass delta-sigma TDC.

The differential input signals V_{IN} and V_{IP} represent the instantaneous phase or time difference between the reference edge and the feedback edge, encoded as a differential voltage through the preceding time-to-voltage conversion mechanism as shown in Figure 4a. These signals are first applied to the active band-pass filter implemented using the operational amplifier (OA1) and its surrounding RC network. The band-pass filter is realized by appropriately combining resistive and capacitive feedback paths, as indicated by the components R_{11} and C_{11} , such that a pair of complex conjugate poles is introduced at the desired center frequency. This center frequency is chosen to coincide with the offset frequency at which the phase error information is expected to reside, thereby suppressing low-frequency components while amplifying the desired band-pass signal.

At the transistor level, OA1 is implemented as a fully differential amplifier with cross-coupled loads and carefully biased current sources, as shown in the detailed schematic. The bias voltages V_{B11} , V_{B12} , V_{B13} and V_{B14} define the operating point of the amplifier, while the common-mode control nodes V_{CM1} and V_{CM2} stabilize the output common-mode levels at V_{ON1} and V_{OP1} . This fully differential implementation improves linearity, enhances common-mode noise rejection, and ensures robust operation under supply and substrate noise, which is critical for time-domain signal processing in a PLL environment.

The band-pass filtered differential signal is then fed into a TIA in Figure 4b, which converts the filter output current into a voltage signal with sufficient gain to drive the subsequent quantizer. The TIA also provides additional isolation between the loop filter and the quantizer, reducing the direct loading effect of the quantizer input and improving overall loop stability. The feedback resistors around the TIA, as indicated in the figure, define the effective transimpedance gain and contribute to the overall noise transfer function of the delta-sigma loop.

Following the TIA, the signal is digitized by a 5-bit flash quantizer as shown in Figure 4c. The quantizer consists of a resistive ladder generating evenly spaced reference voltages between V_{DD} and V_{SS} , and a bank of comparators whose outputs B_1 – B_5 are encoded into a thermometer code and subsequently converted to a binary output word D_{OUT} . The use of a multi-bit quantizer reduces the quantization step size and lowers the in-band quantization noise, which is particularly beneficial for suppressing fractional spurs and improving the effective resolution of the phase detection.

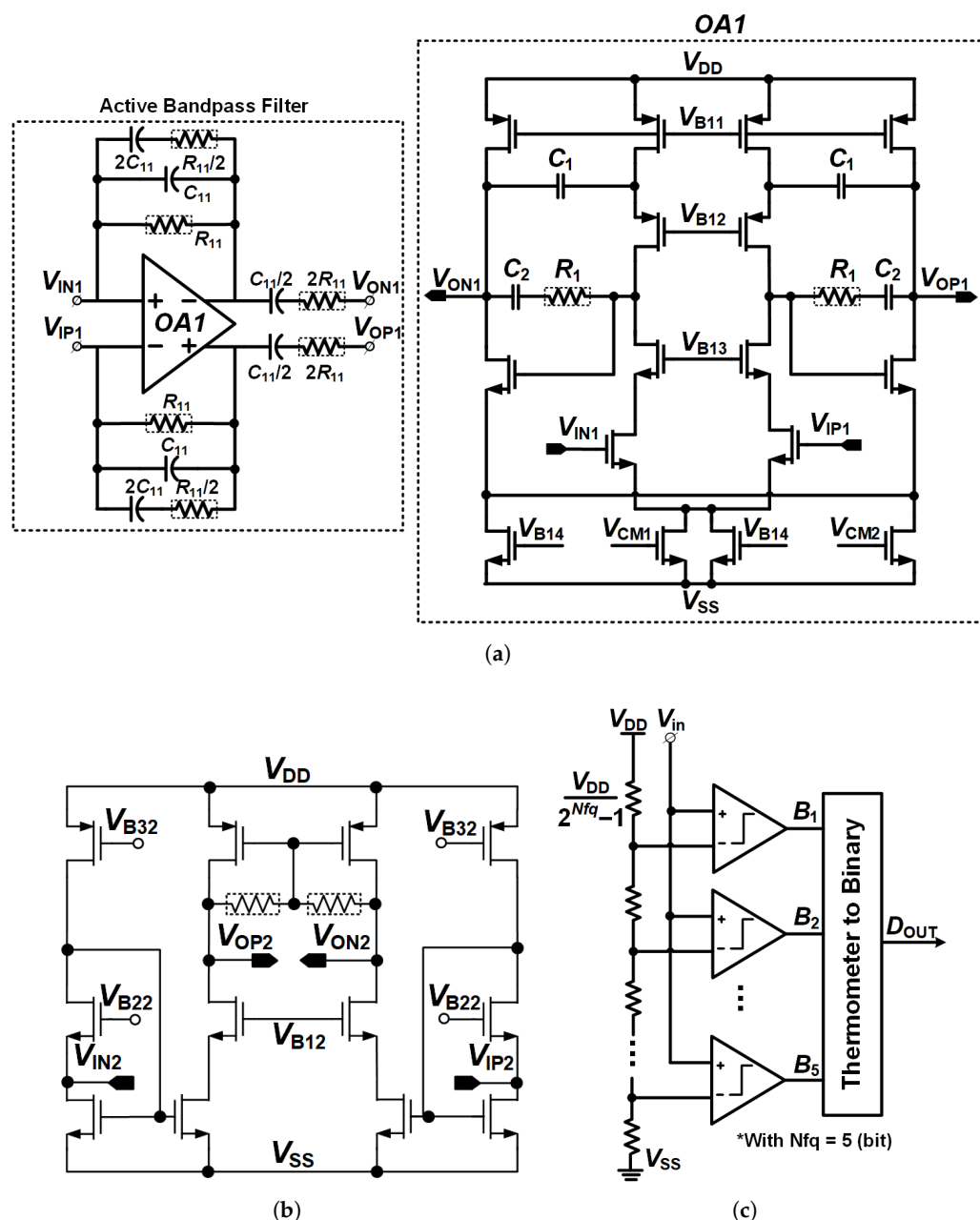


Figure 4. Circuit schematic of the active band-pass filter (a), transistor-level implementation of the transimpedance amplifier (TIA) (b), multi-bit flash quantizer with thermometer-to-binary encoding with $N_{fb} = 5$ -bit (c).

The digital output D_{OUT} is fed back through a unit-delay element z^{-1} and a set of DACs that reconstruct an analog feedback signal applied to the active band-pass filter input. This feedback path closes the delta-sigma loop and shapes the quantization noise according to a band-pass noise transfer function, pushing most of the quantization noise away from the low-frequency region of interest. As a result, the BPDSTDC achieves high time-resolution phase detection over a wide dynamic range without requiring fine delay elements or calibration-intensive delay lines.

Table 1 compares the proposed ADPLL with representative state-of-the-art TDC-based PLLs under similar technical schemes. Despite being implemented in a 180-nm CMOS process, the proposed design achieves superior in-band phase noise at a 1-MHz offset, highlighting the effectiveness of the band-pass $\Delta\Sigma$ TDC architecture under wide loop bandwidth operation.

Table 1. Performance comparison with representative TDC-based and all-digital PLL implementations.

Ref.	[25]	[26]	[27]	This Work
Tech. (nm)	65	40	65	180
Architecture	ADPLL	ADPLL	Frac-N PLL	ADPLL
Supply voltage (V)	1.2	1.1	1.2	1.8
Freq. Out (GHz)	2.4	5.2	33.5	3.2
Ref. frequency (MHz)	26	100	250	50
Bandwidth (MHz)	400 KHz	1.25	1	1
TDC Type	GRO	Flash $\Delta\Sigma$	PFD/CP + CT $\Delta\Sigma$	BPDSTDC
In-band PN (dBc/Hz)	−112 @ 1 MHz	−115 @ 1 MHz	−110 @ 1 MHz	−216 @ 1 MHz

4.2. DDC

To exploit the band-pass noise-shaping property of the proposed BPDSTDC in the PLL loop, the quantizer output is further processed in the digital domain to extract the phase-error information at baseband. Let D_{OUT} denote the discrete-time output word of the 5-bit quantizer at the BPDSTDC update rate f_s , where n is the sample index. Because the band-pass $\Delta\Sigma$ loop places the signal component around the modulator's center frequency rather than at DC, $D_{OUT}[n]$ is digitally down-converted prior to the digital loop filter. In this work, the down-conversion is implemented using a multiplier-free f_s mixing sequence $c[n] = \{+1, 0, -1, 0\}$, yielding the mixed sequence $x[n] = D_{OUT} \cdot c[n]$. This operation translates the band-pass component to baseband while avoiding the complexity and power overhead of a full-precision digital multiplier. The mixed sequence $x[n]$ is then passed through a low-pass filter $H_{LP}(z)$ of 2-order to suppress the image component and to prevent residual out-of-band quantization content from coupling into the control path. The filter cutoff is selected to comfortably pass the targeted PLL loop bandwidth (>1 MHz) while providing sufficient attenuation at the mixing-image frequency. Importantly, the DDC processing latency is explicitly included in the linearized loop-gain model as an additional factor z^{-D} (or equivalently a group delay τ_g), and the loop-filter coefficients are designed with this added delay taken into account to preserve adequate phase margin at the targeted bandwidth.

4.3. Voltage-Controlled Oscillator

The proposed oscillator that is shown in Figure 5 is implemented as a fully differential ring-based digitally controlled oscillator (DCO), in which an odd number of identical delay cells are connected in a closed-loop configuration to sustain oscillation. Oscillation occurs when the total phase shift around the loop equals 2π at the oscillation frequency and the loop gain is sufficient to compensate for losses. In this architecture, the oscillation frequency is directly determined by the total propagation delay of the delay cells; therefore, adjusting the delay characteristics of each cell provides effective frequency control.

As shown in the Figure 5, each delay cell adopts a differential topology with cross-coupled loads to provide regenerative gain and ensure reliable oscillation startup. The differential output nodes V_{OP} and V_{ON} generate balanced clock waveforms with improved duty-cycle symmetry and reduced sensitivity to supply and substrate noise. These differential outputs are directly connected to the subsequent CML divider stages in the feedback path, allowing low-jitter signal transfer at multi-gigahertz frequencies.

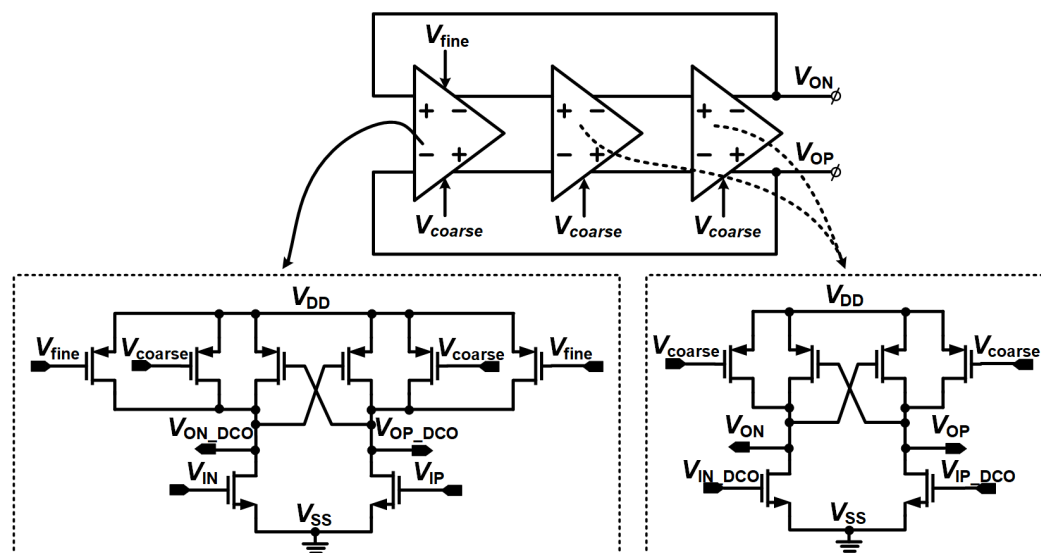


Figure 5. The proposed oscillator.

Frequency tuning is realized through two separate control paths, labeled V_{coarse} and V_{fine} in the figure. The coarse control voltage V_{coarse} adjusts the biasing condition or effective load strength of the delay cells, thereby shifting the overall operating point of the oscillator. This path provides a wide tuning range and is mainly used to compensate for process, voltage, and temperature variations and to place the free-running frequency within the desired operating range of the PLL. Due to its coarse resolution, V_{coarse} is primarily employed for frequency centering rather than dynamic loop correction.

The fine control voltage V_{fine} introduces small variations in the effective delay of the delay cells by modulating the corresponding current or control nodes, as indicated in the figure. This path enables high-resolution frequency adjustment and is driven by the noise-shaped digital control word generated by the loop filter and the delta-sigma modulator. As a result, fine frequency tuning can be achieved with reduced in-band quantization noise. The clear separation between coarse tuning through V_{coarse} and fine tuning through V_{fine} allows the oscillator to achieve both a wide tuning range and fine frequency resolution without requiring a high-resolution digital-to-analog interface.

Although ring-based oscillators inherently exhibit higher phase noise than LC-based oscillators due to their lower effective quality factor, this limitation is mitigated in the proposed architecture by employing a wide PLL loop bandwidth. The large loop bandwidth effectively suppresses the in-band phase noise contribution of the oscillator, while the ring-based topology offers fast frequency tuning, short settling time, and high integration capability. These characteristics make the proposed DCO well suited for all-digital fractional-N PLLs targeting wideband frequency synthesis and frequency-modulated applications.

Figure 6 summarizes the oscillator tuning behavior and its PVT sensitivity. As shown in Figure 6a, the DCO exhibits a continuous, monotonic tuning characteristic that covers the targeted near-3-GHz band (2.86–3.2 GHz), providing sufficient margin for frequency centering and closed-loop operation. Figure 6b further plots the free-running DCO frequency across temperature for major process corners, indicating the expected frequency spread under PVT variations; this spread motivates the use of coarse frequency centering and loop tracking to guarantee robust lock across corners.

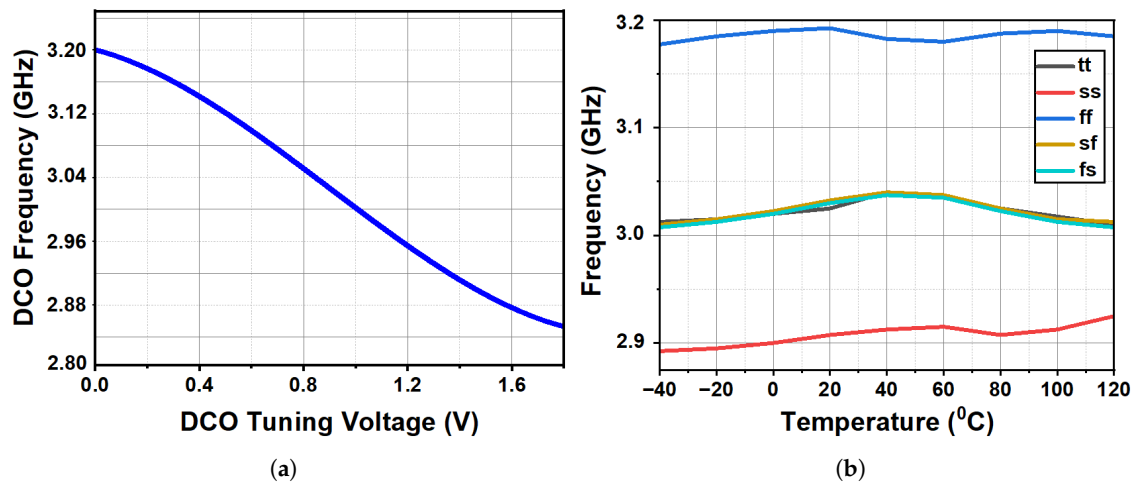


Figure 6. DCO frequency versus tuning voltage, showing a monotonic tuning range of approximately 2.86–3.2 GHz over a 0–1.8 V control swing (a). Simulated DCO free-running frequency versus temperature across process corners (tt/ss/ff/sf/fs), illustrating the PVT-induced frequency spread and its temperature dependence (b).

4.4. High-Speed Frequency Divider

The high-speed frequency divider employed in the proposed ADPLL (in Figure 7) is implemented using a current-mode logic (CML) architecture to ensure robust operation at multi-gigahertz frequencies with low timing uncertainty. The divider is constructed by cascading two identical CML divide-by-2 stages, resulting in an overall divide-by-4 operation. Each divide-by-2 stage is realized using a master–slave latch configuration, where two differential latches driven by complementary clock phases are connected in a regenerative feedback loop. This topology enables reliable toggling behavior at very high input frequencies, while maintaining precise phase relationships among the output signals.

At the transistor level, each CML divide-by-2 stage consists of a differential input pair driven by the input signals (IN and IP), a clock-controlled sampling network governed by the complementary clock signals CLK_N and CLK_P , and a cross-coupled load structure that provides positive feedback for bistable latch operation. The constant bias current characteristic of the CML topology minimizes voltage swing and supply current variations during switching, thereby reducing sensitivity to supply noise and lowering output jitter. The differential output nodes, labeled OP and ON, generate complementary clock signals that inherently preserve duty-cycle symmetry and enable accurate phase generation.

By cascading two such CML divide-by-2 stages, the divider produces four evenly spaced clock phases at the output, namely, 0° , 90° , 180° , and 270° , at one-quarter of the input frequency. The careful selection and routing of intermediate phase signals between the two stages, as indicated in the figure, ensures that the quadrature phase relationship is preserved across the full operating frequency range. This quadrature output is essential for the subsequent phase rotation logic and the multi-stage pipelined phase interpolator, which rely on well-defined phase spacing to achieve fine phase resolution and accurate fractional-N operation.

From a system perspective, the use of a CML-based divider is critical in the proposed architecture, as the divider directly interfaces with the output of the ring-based DCO operating in the 2–3 GHz range. Compared to conventional CMOS dividers, the CML implementation offers superior high-frequency capability, reduced duty-cycle distortion, and lower additive jitter, all of which are crucial for maintaining low in-band phase noise in the PLL feedback path. Moreover, by generating quadrature phases directly at the

divided frequency, the proposed divider eliminates the need for additional phase generation circuitry, thereby reducing complexity and avoiding extra noise sources.

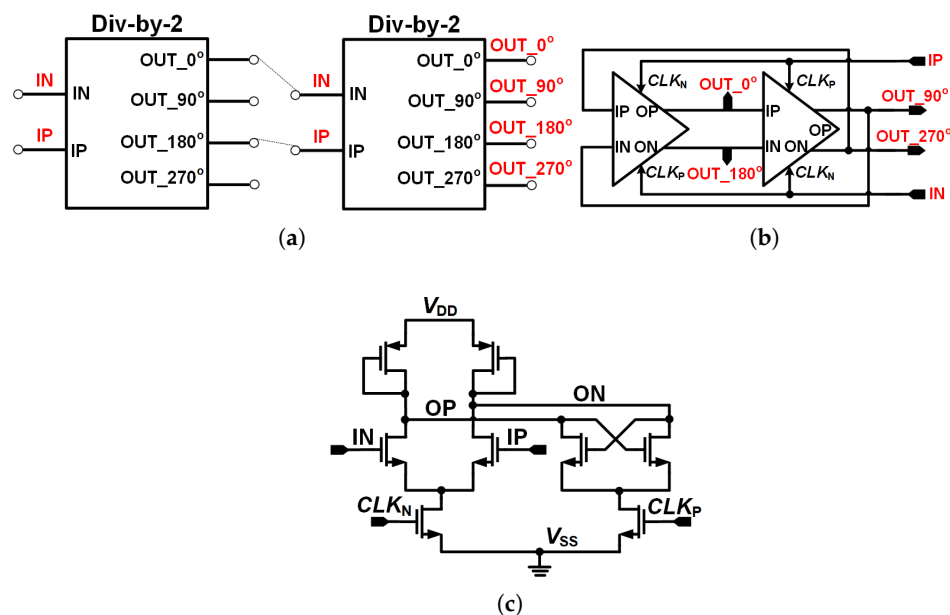


Figure 7. CML divider (a). Schematic of div-by-2 (b). CML latch (c).

4.5. Pipelined-Phase Interpolator

The 3-bit pipelined phase interpolator shown in Figure 8 is placed in the feedback path after the CML divide-by-4 block to generate finely resolved feedback phases for fractional-N synthesis. The CML divide-by-4 generates four evenly spaced reference phases, denoted as OUT_{270° , at a frequency of $f_{\text{DCO}}/4$. These phases are first applied to the Phase Rotation Logic, which selects the appropriate pair of adjacent phases according to the active quadrant and ensures phase continuity when the fractional control code changes. The selected phase pair, labeled Φ_{i1} and Φ_{i2} as shown in the figure, is then applied to the first interpolation stage (Stage 1). Within Stage 1, the interpolation cells PI1–PI3 generate three candidate output phases, denoted as Φ_{O1} , Φ_{O2} and Φ_{O3} . One of these phases is selected, based on the control code, and forwarded to Stage 2 as a new input phase pair Φ_{i1} and Φ_{i2} . The same operation is repeated in Stage 2 and Stage 3, where each stage performs partial interpolation and passes a selected intermediate phase to the next stage. Through this pipelined operation, the desired overall phase shift is accumulated progressively rather than being generated in a single interpolation step.

At the circuit level, each PI is implemented using a differential interpolation structure in which the two input phases Φ_1 and Φ_2 , as labeled in the transistor-level schematic, control weighted current or load paths to generate the interpolated output phase Φ_{OUT} . The interpolation weights are driven by digital control codes originating from the Waveform Generator and the associated $\Delta\Sigma_{\text{frac}}$ modulator, which provide the fractional control inputs to the Phase Rotation Logic and the selection logic within each stage. The three-stage pipelined architecture (Stage 1–Stage 3) reduces the interpolation range handled by each individual stage, thereby lowering sensitivity to device mismatch and weight nonlinearity in each PI1–PI3, and limiting jitter accumulation compared to a single-stage high-resolution phase interpolator. More importantly, by generating fine phase steps directly in the feedback path, the pipelined phase interpolator effectively reduces the phase step size observed at the input of the BPDSM-TDC, leading to reduced in-band quantization noise and fractional spurs without the need for a digital-to-time converter.

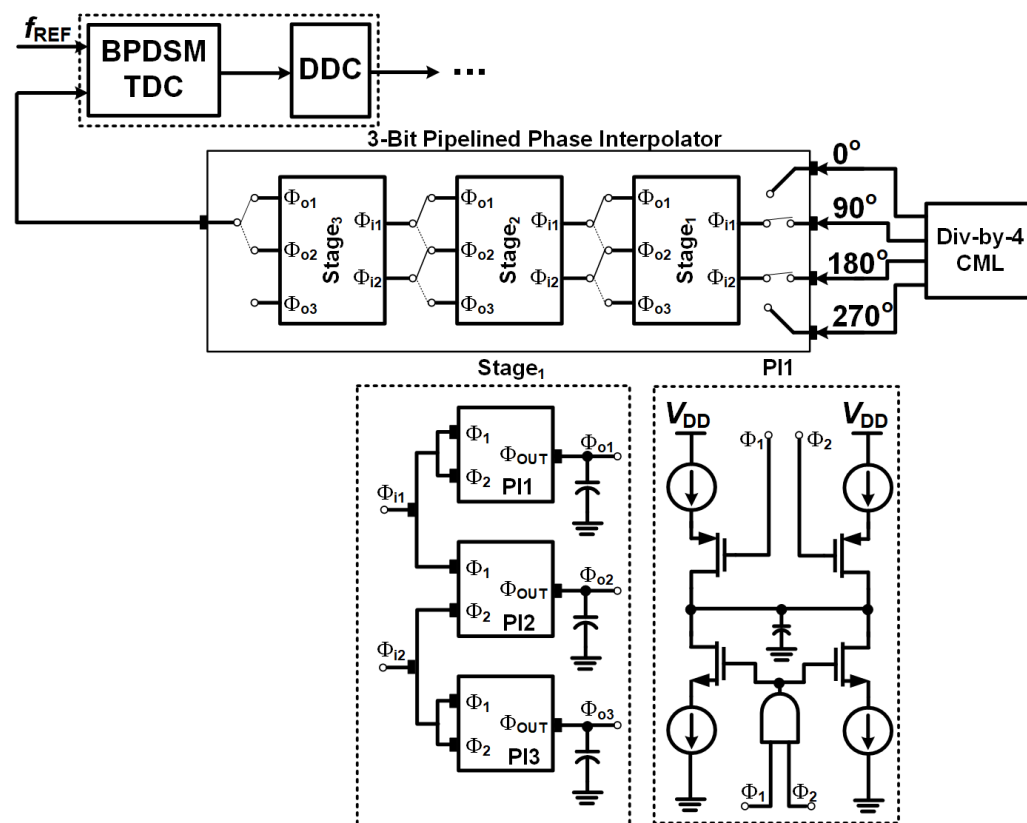


Figure 8. Pipelined phase interpolator.

5. Experimental Results

The prototype IC was fabricated in a 180-nm CMOS process, as shown in Figure 9. The proposed BPDSTDC occupies an active area of 0.05 mm^2 and consumes 10 mW from a 1.8-V supply. Stand-alone measurements of the BPDSTDC were performed using a 100-MHz input signal and an external 400-MHz clock. This Figure 10 shows the output power spectral density (PSD) after noise shaping, confirming the expected $\Delta\Sigma$ spectral slope. In the frequency range of approximately 10^6 to 10^7 Hz, the PSD rises with a slope of about 40 dB/dec, which is characteristic of second-order noise shaping. This indicates that the quantization noise is pushed away from low frequencies where the PLL is most sensitive and is redistributed toward higher offsets, thereby reducing its contribution to in-band phase noise and improving the integrated jitter within the band of interest. The measured SNDR reaches 63 dB over a 5-MHz bandwidth, corresponding to an ENOB of 10.03 bits, as illustrated in Figure 11.

The proposed BPDSTDC achieves a low measured integrated rms timing noise of $183 f_{s_{\text{rms}}}$ within a 1-MHz signal bandwidth, placing it among the lowest-noise noise-shaping TDCs reported to date and spur is shown as summarized in Figure 12. Benefiting from this low TDC noise, the complete PLL exhibits a measured in-band phase noise of -120 dBc/Hz at a 1-MHz offset for a 3.2-GHz output frequency while operating with a loop bandwidth exceeding 1 MHz (Figure 13). This performance corresponds to a normalized phase noise of -216 dBc/Hz .

A moderate phase-noise peaking observed around a 1-MHz offset originates from the loop transfer-function peaking, as the loop dynamics are intentionally designed to favor fast settling and wide bandwidth at the expense of reduced phase margin. A comparison with prior art is provided in Table 2. After normalization to a 28-nm CMOS process following the methodology in [28] the proposed PLL ranks among the best reported mm-wave all-digital PLLs. This normalization has inherent limitations, since ideal technology scaling does not

capture leakage trends, supply constraints, and the use of different device options (e.g., thick-oxide/I/O devices) that are often adopted in advanced nodes for mixed-signal/RF blocks. More importantly, even without normalization, the prototype in 180-nm CMOS achieves an integrated TDC timing jitter of 183 fs, which is lower than the values reported by the works listed in Table 2, including those fabricated in more advanced nodes.

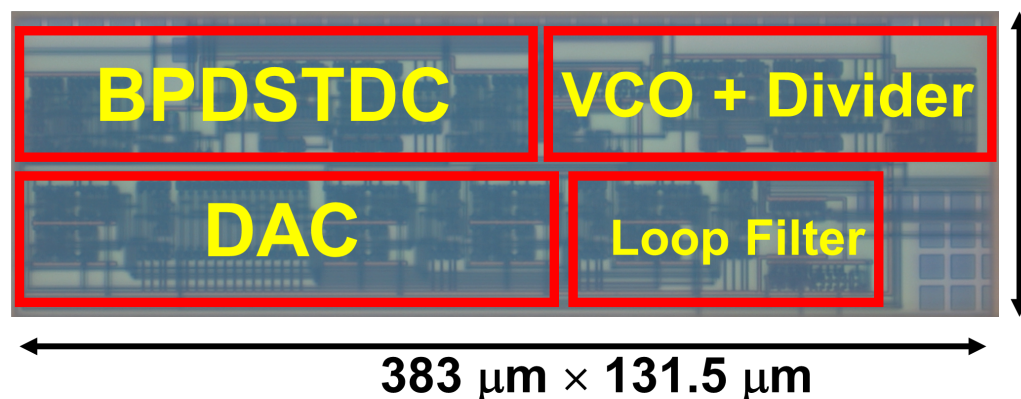


Figure 9. Die micrograph.

The measured 183-fs timing jitter and $-120\ \text{dBc}/\text{Hz}$ phase noise indicate a highly stable clock source, which is practically important for IoT and high-frequency transceivers. Low jitter reduces sampling/edge timing uncertainty in mixed-signal and digital interfaces, improving timing margin and lowering the probability of bit/packet errors, thereby enhancing system reliability under PVT variations. Meanwhile, low phase noise especially at MHz offset, reduces phase-noise induced interference folding (reciprocal mixing) from nearby strong signals, which improves coexistence and robustness against adjacent-channel interference in high-frequency operation. Therefore, the reported results translate directly into higher accuracy and improved interference tolerance in practical wireless systems.

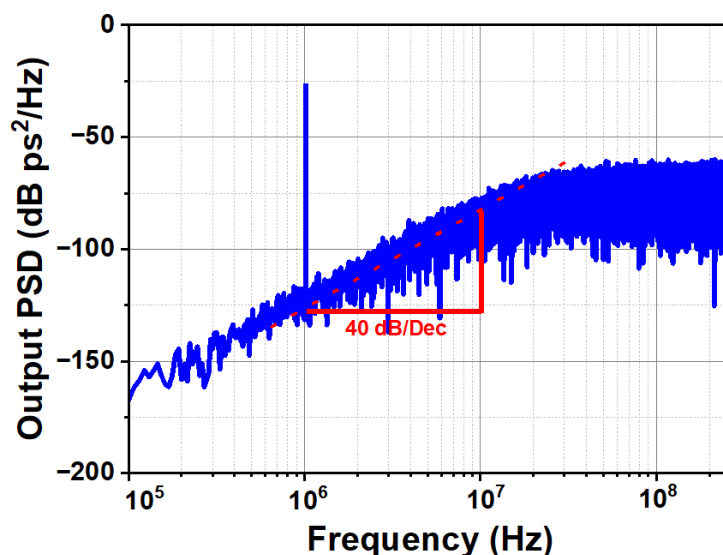


Figure 10. Measured output spectra of the BPDSTDC for 1 MHz PM.

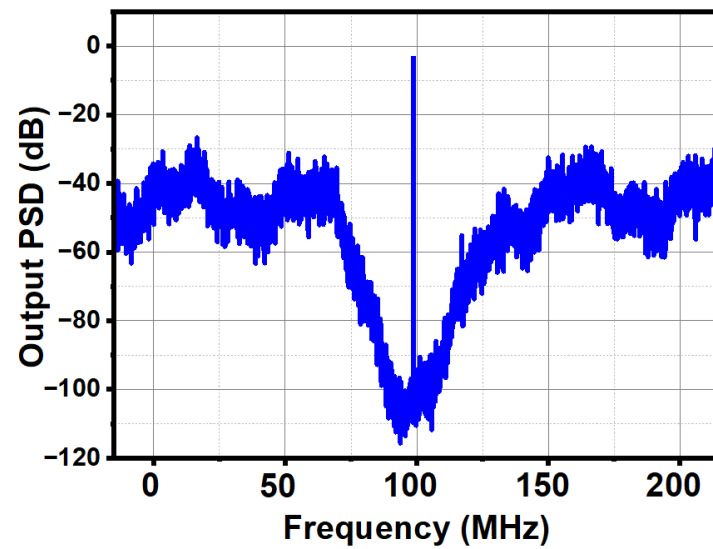


Figure 11. BPDSM output spectrum at $f_{IN} = 100$ MHz.

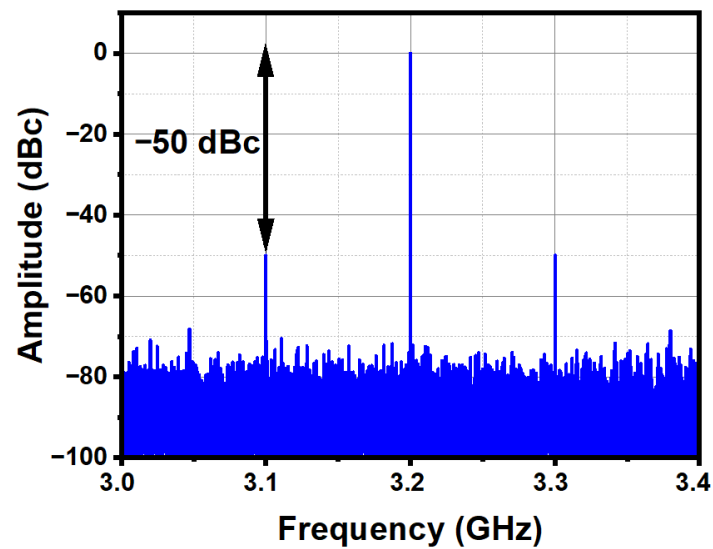


Figure 12. Output spectrum at 3.2 GHz.

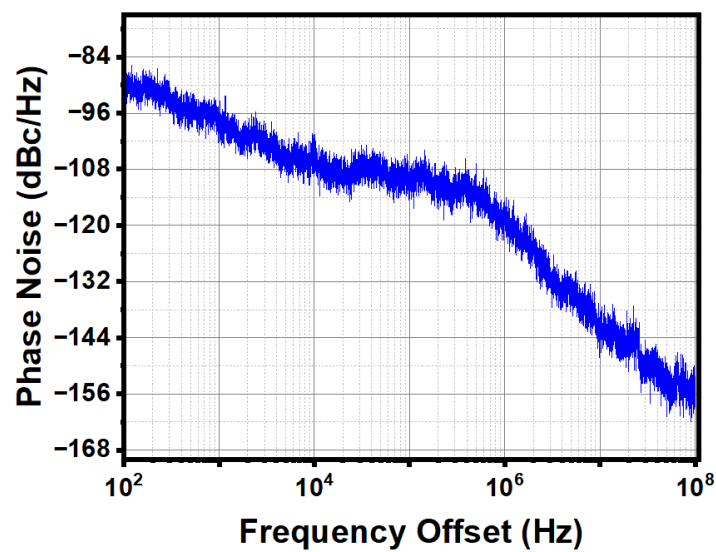


Figure 13. PLL output spectrum with measured phase noise.

Table 2. Comparison table.

Ref.	[29]	[30]	[31]	This Work
Tech. (nm)	65	28	40	180
Architecture	ADPLL	BBPLL	ADPLL	ADPLL
Ref. Freq (MHz)	26×2	250	40	50
Out. Freq (GHz)	2–2.6	8.5–10	2.56–4.1	18.4–20.6
FOM* (dB)	−246	−250.3	−249.4	−240
Ref. Spur (dBc)	−72	−70.2	0.043	−56
Phase Noise (dBc/Hz)	−112.2	−120.2	−119.76	−136
Power (mW)	0.98	20	3.48	3.1
Area (mm ²)	0.23	0.23	0.31	0.0012

$$FOM^* = 10 \log_{10} \left[\left(\frac{Jitter}{1 \text{ s}} \right)^2 \times \left(\frac{Power}{1 \text{ mW}} \right) \right] \text{ Scaled to 28 nm process following [28].}$$

6. Conclusions

This paper presented an all-digital fractional-N phase-locked loop operating from 2.86 to 3.2 GHz, targeting low integrated jitter, low in-band phase noise, and fast settling for highly integrated RF transceivers. A band-pass delta-sigma time-to-digital converter combined with digital down-conversion was introduced to enable high-resolution phase detection over an extended $\pm 2\pi$ range while shaping quantization noise away from low frequencies without delay-line-based calibration. The recovered baseband phase error allows the use of a wideband type-II digital loop filter, enabling a loop bandwidth exceeding 1 MHz and effective suppression of oscillator phase noise.

Fractional-N synthesis is realized using a CML-based divide-by-4 quadrature divider followed by a 3-bit pipelined phase interpolator in the feedback path. This phase-domain fractional approach significantly reduces the effective phase step size observed by the TDC, suppressing in-band quantization noise and fractional spurs without requiring a digital-to-time converter. A ring-based digitally controlled oscillator with separate coarse and fine tuning paths provides wide tuning range and supports fast frequency modulation.

Fabricated in a 180-nm CMOS technology, the proposed ADPLL achieves an integrated rms timing jitter of 183 fs within a 1-MHz bandwidth. The measured in-band phase noise reaches −120 dBc/Hz at a 1-MHz offset for a 3.2-GHz output frequency while operating with a loop bandwidth exceeding 1 MHz. This performance corresponds to a normalized phase noise of −216 dBc/Hz. The entire system operates from a 1.8-V supply and consumes 10 mW. These results validate the effectiveness of the proposed band-pass delta-sigma phase detection combined with phase-interpolator-based fractional synthesis for low-noise, wideband all-digital PLL implementations.

Regarding future work, the design can be implemented in more advanced process nodes to reduce power consumption and improve noise performance. In addition, incorporating adaptive control and calibration mechanisms to automatically optimize loop parameters under PVT variations is also a feasible direction to further enhance PLL performance.

Author Contributions: Writing—original draft, T.V.H.N.; writing—review and editing, T.V.H.N. and C.-K.P. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by JST NEXUS, Japan, Grant Number JPMJNX25D4.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Acknowledgments: The VLSI chip in this study has been fabricated through the activities of VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with Synopsys, Inc., Cadence Design Systems Inc., Mentor Inc., Rohm Semiconductor (ROHM), and Nippon Systemware Co., Ltd.

Conflicts of Interest: The authors declare no conflicts of interest.

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