

Article

A Low-Noise Equalizing Transimpedance Amplifier for LED-Limited Visible Light Communication

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Abstract

Solid-state lighting, especially light-emitting diodes (LEDs), is revolutionizing indoor lighting due to its energy efficiency, long lifespan, low heat output, and enhanced color rendering. LEDs can quickly adjust light intensity, enabling the development of visible light communication (VLC) technology. However, the modulation bandwidth of phosphor-converted white LEDs commonly used for illumination is limited, potentially affecting the speed of the VLC links. This paper presents a receiver-side equalization technique to overcome bandwidth limitations in VLC links due to LEDs. The proposed approach utilizes a novel transimpedance amplifier with an embedded T-network shunt-feedback equalizer (TIA-TE) to introduce adjustable high-frequency peaking in the TIA's frequency response. By incorporating this peaking, the system's bandwidth is extended without sacrificing important performance parameters like gain, noise, or power dissipation. The TIA-TE is followed by a main amplifier and a standalone continuous-time linear equalizer (CTLE) for further signal conditioning, while a 50 Ω buffer interfaces the receiver with measurement equipment. Post-layout simulations in a 0.35 μm CMOS process validate the approach. Using a 4 pF photodiode, the system bandwidth was initially limited by the LED's 3 MHz modulation bandwidth. The proposed TIA-TE extends the bandwidth to 8.4 GHz without sacrificing the gain or power dissipation. The subsequent CTLE further extends the bandwidth to 14 MHz. The receiver front end achieves a mid-band transimpedance of 110 dB Ω and an input-referred noise current of 7.2 nA_{rms}, while dissipating 2.48 mW (excluding the 50 Ω buffer). Simulated 28 Mb/s NRZ eye diagrams demonstrate the feasibility of the proposed TIA-TE architecture for LED-limited VLC links.

Keywords: continuous-time linear equalizer (CTLE); post-equalization; transimpedance amplifier (TIA); visible light communication (VLC); light-emitting diodes (LEDs)



Academic Editor: Hector E. Nistazakis

Received: 21 January 2026

Revised: 23 February 2026

Accepted: 27 February 2026

Published: 1 March 2026

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1. Introduction

Visible light communication (VLC) offers several advantages, such as high data rates, energy efficiency, enhanced security, immunity to RF interference, and access to a wide, license-free spectrum. Furthermore, VLC links leverage existing lighting infrastructure to transmit data in the 380–750 nm band. However, phosphor-converted white light-emitting diodes (LEDs) commonly used for illumination exhibit limited modulation bandwidth, typically from a few megahertz to tens of megahertz, due to carrier dynamics and phosphor relaxation [1,2]. To mitigate the LED bandwidth bottleneck, VLC links employ techniques such as blue filtering [3–5], transmitter-side pre-equalization [5], and receiver-side

post-equalization [3,5,6]. The blue filter suppresses the slow phosphor (yellow) spectral component [3]. In [3], data rates of 32 Mbps and 50 Mbps at a bit-error rate (BER) of 10^{-2} were obtained at a distance of 2 m without and with a blue filter, respectively, utilizing an LED with a modulation bandwidth of only 1.6 MHz. While effective at extending bandwidth, blue filtering reduces received optical power. Pre-equalization at the transmitter often requires the handling of high currents and voltages in the LED driver, which can lead to increased complexity and efficiency penalties. Consequently, receiver-side post-equalization remains attractive for low-complexity, energy-efficient VLC links. While some studies have focused on implementing transceiver circuits using off-the-shelf components [4,5,7,8], a limited number have explored fully integrated CMOS transceivers [3,6,9]. For example, in [6], an integrated receiver for VLC is implemented in the $0.18\ \mu\text{m}$ CMOS technology. The receiver consists of a current-reuse TIA, an ambient light rejection circuit, and a two-stage CTLE. The post equalization is performed for a light source that consists of a 4×5 phosphor-converted white LED array having a bandwidth of only 2.2 MHz. A bit-error rate (BER) of 10^{-2} at a data rate of 30 Mbit/s is achieved at a distance of 2.7 m. In [6], the equalizer is tuned by changing the transistor's capacitance, which is not linear over an applied control voltage. To overcome this limitation, the equalizer in [3] is tuned through a digitally controlled capacitor bank. The receiver in [3] is implemented in the $0.13\ \mu\text{m}$ CMOS technology and is successfully employed to equalize various off-the-shelf phosphorescent white LEDs. For each LED, around a $20\times$ improvement in data rate is achieved compared to the LED bandwidth. As an example, using an LED with a bandwidth of only 1.6 MHz, a BER of 10^{-2} at a data rate of 32 Mbit/s is achieved at a distance of 2 m. Furthermore, using a blue filter further increases the data rate to 50 Mbit/s. In [9], the employed equalizer compensates for the bandwidth limitation of an integrated large area photodiode. The CTLE uses a negative-capacitance technique to compensate for high-frequency loss. Using a blue laser diode with a bandwidth of 1 GHz as a source of light, the VLC link in [9] successfully achieved a data rate of 980 Mbit/s at a BER of 3.8×10^{-3} .

Based on the prior research discussed above, it is evident that in LED-limited VLC links, the dominant constraint originates from the intrinsic electro-optical pole of phosphor-converted white LEDs, which precedes the receiver and fundamentally dictates the overall link transfer characteristic [1,2]. Because this pole attenuates high-frequency components before photodetection, the received photocurrent is already spectrally distorted at the TIA input. Consequently, merely designing a broadband TIA does not alleviate the bandwidth bottleneck; the LED-induced roll-off continues to determine the effective $-3\ \text{dB}$ bandwidth of the link while unnecessarily increasing the receiver's noise bandwidth. Conventional receiver architectures compensate for this limitation by cascading a standalone CTLE after the TIA [6]. However, cascade equalization inherently amplifies both signal and pre-existing high-frequency noise, adds further colored noise components associated with the equalizer's transconductance stage, increases static power dissipation, and often requires supplementary gain to offset equalizer attenuation. Furthermore, this approach leaves the TIA loop characteristics unchanged, treating LED compensation as a post-processing function rather than integrating it into the transimpedance mechanism itself.

We introduce here a more efficient strategy to embed the equalization function directly within the TIA's shunt-feedback network, thereby reshaping the loop gain and introducing controlled high-frequency peaking in the feedback path. By relocating the compensating zero into the feedback network, the LED-induced pole can be effectively counteracted within the closed-loop response, allowing bandwidth extension without increasing core transconductance, input-referred device noise, or bias current. This feedback-embedded approach redistributes loop gain rather than boosting output amplitude, eliminates the

need for additional noisy equalizer stages, avoids amplification of high-order colored noise, and reduces cascade complexity. As a result, the classical noise–bandwidth–power trade-off of VLC receivers is fundamentally altered, enabling more power-efficient, noise-optimized operation in systems constrained by severely bandwidth-limited white LEDs.

Figure 1 illustrates the proposed VLC link. The transmitter driver biases and modulates the LED; the limited LED bandwidth introduces inter-symbol interference (ISI) at the receiver. A photodiode (PD) converts incident light into a small photocurrent that is amplified by a transimpedance amplifier (TIA). To enhance post-equalization performance, the TIA employs a T-network shunt-feedback topology that introduces tunable high-frequency peaking. A two-stage main amplifier (MA) provides additional gain and single-ended-to-differential (S2D) conversion. When further bandwidth extension is required, the CTLE is cascaded after the MA. A $50\ \Omega$ output buffer interfaces the receiver with measurement equipment.

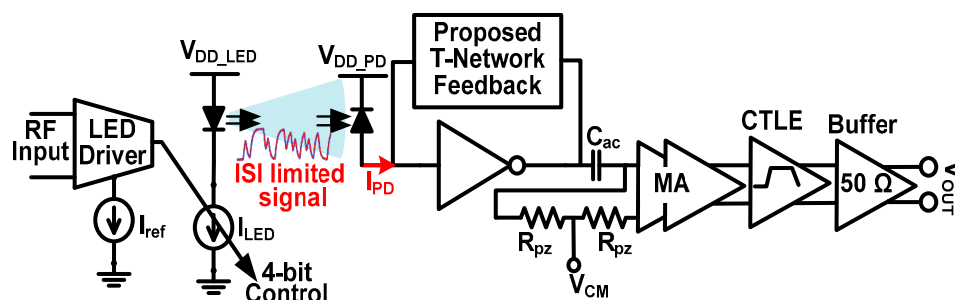


Figure 1. Block diagram of a proposed VLC link.

This paper investigates embedding the post-equalization function inside the TIA feedback path and quantifies the resulting noise–bandwidth–power trade-offs relative to conventional resistive-feedback TIAs and standalone equalizers, targeting LED-limited VLC links. The remainder of this paper is organized as follows. Section 2 details the proposed T-network shunt-feedback TIA and describes the main amplifier, single-ended-to-differential conversion, and CTLE considerations. Section 3 presents link-level evaluation and benchmarks the design against recent VLC front ends. Section 4 concludes the work.

2. Optical Transceiver Realization

2.1. System Architecture and Theoretical Analysis

Figure 2a shows the block diagram of the proposed equalizing TIA with T-network shunt-feedback (TIA-TE). The light signal is modeled by a random signal source (V_{Sig}). The LED is modeled by a low-pass filter (LPF) that consists of R_{LED} and C_{LED} to account for its limited modulation bandwidth $f_{LED} = 1/(2\pi R_{LED}C_{LED})$.

The low-pass-filtered voltage V_{LED} is converted to a current by an ideal voltage-controlled current source (VCCS) having a transconductance of $g_{m,VCCS}$. The current produced by the VCCS (I_{PD}) in parallel with capacitance C_{PD} model the PD. The TIA's core amplifier is modeled by a transconductance g_m and an output resistance r_o . A T-network that consists of R_{F1} , R_{F2} , R_T , and C_T shunts the core amplifier to provide feedback. The loading capacitance from the subsequent stage is modeled by C_L . The overall transfer function (V_{OUT}/V_{Sig}) can be approximated to $H(s)$ as shown in Equation (1)

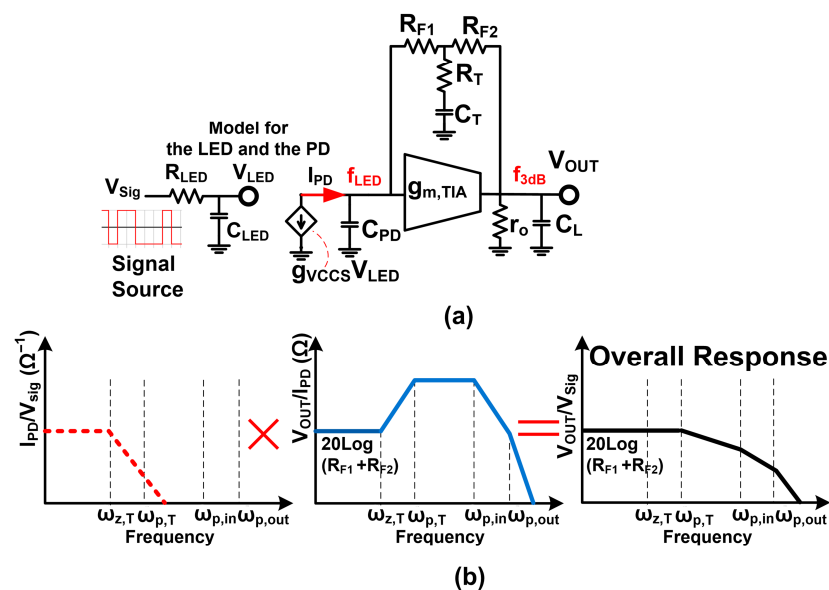


Figure 2. (a) Block diagram of the proposed equalizing TIA with T-network shunt-feedback and (b) illustration of the frequency response.

$$H(s) = \frac{V_{OUT}}{V_{sig}} = \frac{I_{PD}}{V_{sig}} \times \frac{V_{OUT}}{I_{PD}} = \frac{g_{m,VCCS}}{\left(1 + \frac{s}{\omega_{p,LED}}\right)} \times \frac{-Z_{mid} \left(1 + \frac{s}{\omega_{z,T}}\right)}{\left(1 + \frac{s}{\omega_{p,T}}\right) \left(1 + \frac{s}{\omega_{p,in}}\right) \left(1 + \frac{s}{\omega_{p,out}}\right)} \quad (1)$$

where Z_{mid} is the mid-band gain of the TIA and the negative sign reflects its inverting nature, $\omega_{p,LED}$ is the LED bandwidth-limiting pole, $\omega_{z,T}$ and $\omega_{p,T}$ are the zero and the pole introduced by the T-network feedback, respectively, and $\omega_{p,in}$ and $\omega_{p,out}$ are the poles associated with the TIA's input and output nodes, respectively. Z_{mid} , $\omega_{p,LED}$, $\omega_{z,T}$, $\omega_{p,T}$, and $\omega_{p,in}$ and $\omega_{p,out}$ are all defined in Equations (2)–(6)

$$Z_{mid} = R_{F1} + R_{F2} \quad (2)$$

$$\omega_{z,T} = \frac{1}{(R_T + (R_{F1} || R_{F2}))C_T} \quad (3)$$

$$\omega_{p,T} = \frac{(r_o + R_{F2} + R_{F1})}{[(r_o + R_{F2} + R_{F1})R_T + (R_{F1} + R_{F2})R_{F1}]C_T} \quad (4)$$

$$\omega_{p,in} = \frac{(g_{m,TIA} R_T + 1)r_o + R_T + R_{F2}}{[(R_T + R_{F1})r_o + (R_{F2} + R_{F1})R_T + R_{F1}R_{F2}]C_{PD}} \quad (5)$$

$$\omega_{p,out} = \frac{(r_o + R_{F2} + R_{F1})R_T + R_{F1}r_o + R_{F1}R_{F2}}{[(R_{F2} + R_{F1})R_T + R_{F1}R_{F2}]r_o C_L} \quad (6)$$

In the proposed design $R_{F1} = R_{F2}$, $C_T = C_{PD}$, $C_L \ll C_{PD}$, and r_o is significantly large (i.e., $r_o \rightarrow \infty$) due to the cascode implementation of the core amplifier. Therefore, the above analysis can be simplified to the Equations from (7) to (10).

$$\omega_{z,T} = \frac{1}{(R_T + R_{F1}/2)C_T} \quad (7)$$

$$\omega_{p,T} \cong \frac{1}{R_T C_T} \quad (8)$$

$$\omega_{p,in} \cong \frac{g_{m,TIA} R_T + 1}{(R_T + R_{F1})C_{PD}} \quad (9)$$

$$\omega_{p,out} \cong \frac{1}{[(R_T || R_{F1}) + R_{F1}]C_L} \quad (10)$$

The simplified analysis indicates that $\omega_{p,out} \gg \omega_{p,in} \gg \omega_{p,T} \gg \omega_{z,T}$. The proposed TIA-TE achieves a mid-band gain of approximately $R_{F1} + R_{F2}$. Therefore, the proposed TIA-TE achieves the same gain as the conventional shunt-feedback TIA while introducing a controllable amplitude peaking between the zero and the pole introduced by the T-network feedback as illustrated in Figure 2b. The peaking frequency and peaking amplitude can be tuned by varying C_T and R_T as indicated by Equation (8). The zero introduced by the proposed TIA-TE can be adjusted to cancel the LED's bandwidth-limiting pole at $2\pi f_{LED}$. This extends the bandwidth to be determined by the pole introduced by T-network feedback $\omega_{p,T}$ instead of being determined by the LED's modulation bandwidth, as shown in Figure 2b.

Embedding the equalizer within the AC response of the TIA eliminates the need for a standalone equalizer which reduces noise sources and saves power dissipation. To further elaborate on this point, the proposed TIA-TE is compared with a conventional receiver that employs a broadband TIA and a standalone CTLE as shown in Figure 3. In the conventional receiver, the TIA is designed with a wide bandwidth (f_{TIA}) which is typically much greater than the LED's bandwidth f_{LED} . However, the bandwidth at the output of the TIA is still limited by the f_{LED} which necessitates the use of a follow-on equalizer to restore the targeted 3 dB bandwidth (f_{3dB}). The input-referred noise power spectral density (PSD) of the conventional receiver in Figure 3 can be obtained after modifying the analysis in [10] as in Equation (11)

$$\overline{I_{n,con}^2}(s) = \frac{4kT}{R_F} + \frac{4kT\gamma}{g_{m,TIA}R_F^2} + \frac{4kT\gamma}{g_{m,TIA}}(2\pi C_{PD})^2 f^2 + \frac{4kT\gamma}{g_{m,ctle}R_F^2} + \frac{4kT\gamma}{g_{m,ctle}R_F^2} \left(\frac{f}{\sqrt{f_{p,in}f_{p,out}}} \right)^4 \quad (11)$$

where $g_{m,TIA}$ and $g_{m,ctle}$ are the transconductances of the input devices for TIA's core amplifier and CTLE, γ is the channel-noise factor, $f_{p,in} = \omega_{p,in}/2\pi$, and $f_{p,out} = \omega_{p,out}/2\pi$ with $\omega_{p,in}$ and $\omega_{p,out}$ defined in Equation (5) and (6). The analysis reveals that the equalizer contributes to the input-referred noise PSD through a white noise term and a more significant colored noise term increases with f^4 .

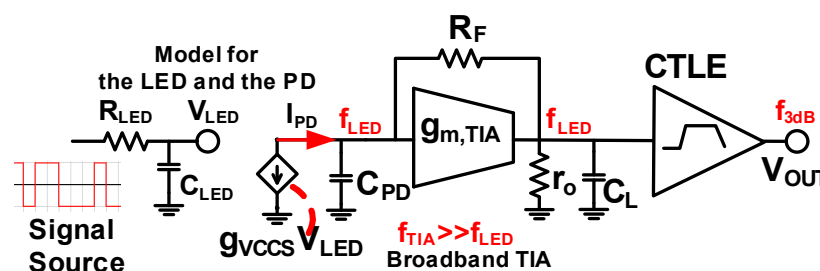


Figure 3. Conventional receiver with a broadband TIA and a standalone CTLE.

The input-referred noise PSD of the proposed TIA-TE is derived as

$$\overline{I_{n,TE}^2}(s) = \frac{4kT}{R_{F1}} \frac{|a_1 + b_1s + c_1s^2|^2}{|d_1 + d_2s|^2} + \frac{4kT}{R_{F2}} \frac{|a_2 + b_2s + c_2s^2|^2}{|d_1 + d_2s|^2} + \frac{4kT}{R_T} \frac{|a_3 + b_3s + c_3s^2|^2}{|d_1 + d_2s|^2} + \frac{4kT\gamma}{g_{m,TIA}(R_{F1} + R_{F2})^2} \frac{|a_4 + b_4s + c_4s^2|^2}{|d_1 + d_2s|^2} \quad (12)$$

where a_x , b_x , c_x , and d_x are coefficients that depend on the circuit parameters and are given in Appendix A. Two observations follow from Equations (11) and (12). First, embedding equalization in the T-network feedback removes the CTLE f^4 noise terms that appear in Equation (11), yielding a net improvement in input-referred noise. Second, the T-network

reshapes the individual contributions: the thermal noises of R_{F1} and R_{F2} become colored (rising with frequency through the numerators) rather than white, as in the CTLE case of Equation (11), and the core amplifier noise is filtered by the same rational factor and scales with $1/(R_{F1} + R_{F2})^2$.

2.2. Transistor-Level Realization

This section shows the transistor-level realization of the transceiver in Figure 1. Figure 4a shows the circuitry of the proposed TIA-TE. The core amplifier of the TIA is realized by a CMOS inverter M_{n1} and M_{p1} . Cascode transistors M_{n2} and M_{p2} boost the output impedance. Therefore, the transconductance $g_{m,TIA}$ and the output resistance r_o in the model shown in Figure 2a are calculated in terms of the circuit's parameters as

$$g_{m,TIA} = g_{m,n1} + g_{m,p1} \quad (13)$$

$$r_o = (g_{m,n2}r_{ds,n2}r_{ds,n1}) || (g_{m,p2}r_{ds,p2}r_{ds,p1}) \quad (14)$$

where $g_{m,x}$ and $r_{ds,x}$ are the transconductance and the drain-to-source resistance of the transistor M_x , respectively. Figure 4b shows the detailed realization of the T-network feedback circuit. A triode transistor M_{p3} with gate-control voltage V_{C1} shunts R_T , while capacitor-connected transistors M_{n3} and M_{n4} with gate-control voltage V_{C2} shunts C_T . Controlling R_T and C_T allows the circuit to provide tunable peaking amplitude and peaking frequency. The control voltages V_{C1} and V_{C2} are externally provided.

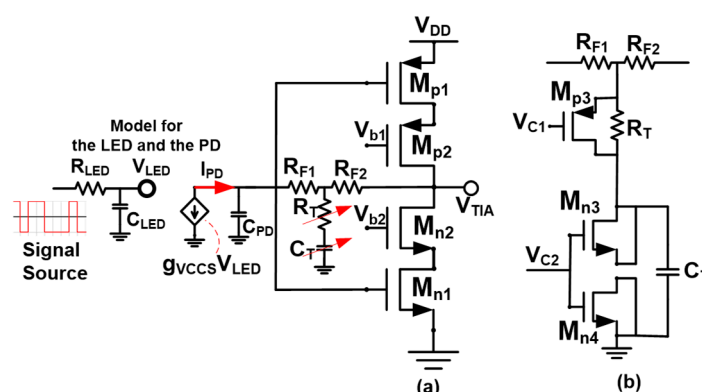


Figure 4. (a) Circuit-level realization of the proposed TIA-TE and (b) detailed realization of the T-network.

The TIA-TE is followed by a two-stage main amplifier (MA) as shown in Figure 5. In addition to signal amplification, the MA also performs single-ended-to-differential (SE2D) conversion. A conventional source-degenerated CTLE is used, as shown in Figure 6, to further extend the systems' bandwidth. Figure 6 also shows the final-stage $50\ \Omega$ buffer that interfaces the receiver with the measurement equipment. Cascaded stages are AC-coupled to isolate distinct DC levels and facilitate biasing. Common-mode (V_{CM1} – V_{CM4}) and bias (V_{b1} – V_{b6}) voltages are externally provided.

An LED driver with dimming control is realized as shown in Figure 7. A current source M_1 – M_4 and R_1 generates a reference current. $I_{ref1} = V_{GS1}/R_1$, where V_{GS1} is the gate-to-source voltage of M_1 . The generated I_{ref1} is amplified with a current mirror M_5 – M_6 with a mirroring ratio $N_1 = 10$ to generate I_{ref2} . The current I_{ref2} is mirrored with a digitally controlled, weighted ratio via M_{9a-e} to control the LED driving current. The mirroring ratio is controlled by D_{m1} – D_{m4} . The LED current is modulated by applying the RF input to the gates of $M_{in,a-d}$. The circuit of the LED driver is a modified version of our previously published work in [11].

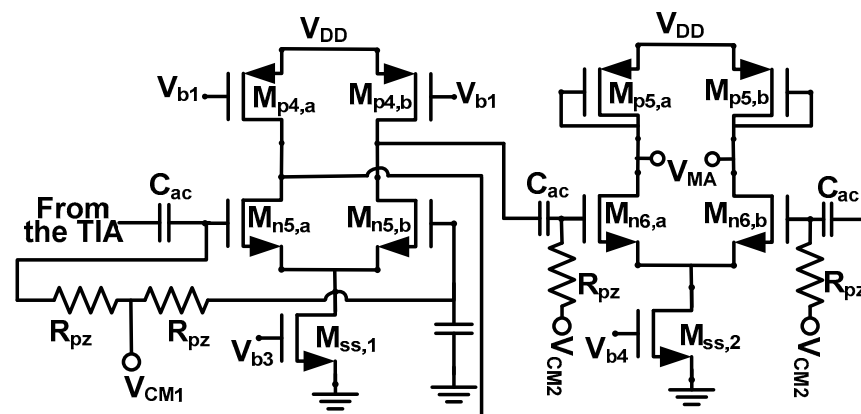


Figure 5. Transistor-level realization of the two-stage main amplifier.

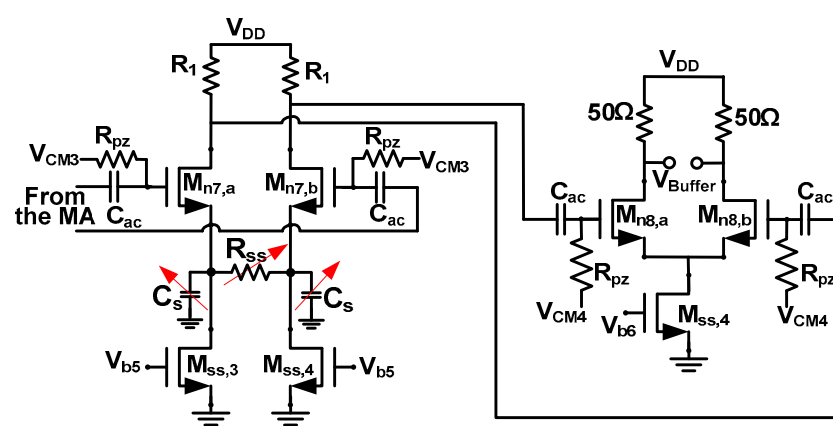


Figure 6. Circuitry of the standalone CTLE and the 50 Ω output buffer.

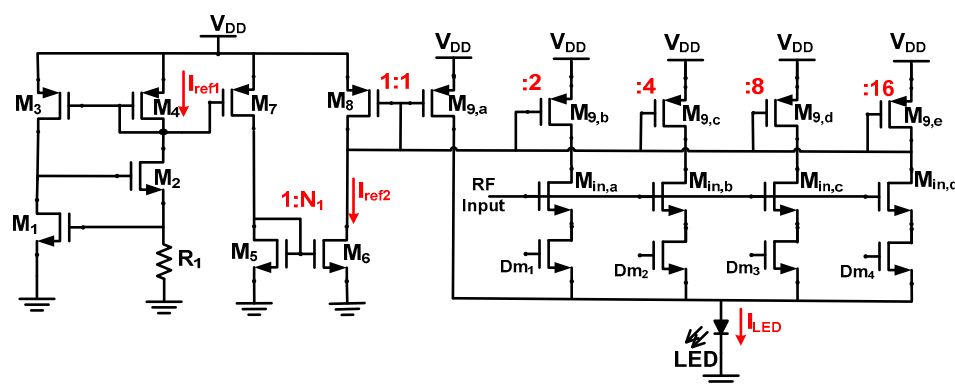


Figure 7. Transistor-level realization of the LED driver.

3. Post-Layout Simulation Results and Discussion

3.1. Comparison with the Conventional Design

To assess the improvement of the proposed TIA-TE in Figure 2 versus the conventional approach in Figure 3, the two receivers are compared through simulations. The circuitry of the proposed TIA-TE is shown in Figure 4 while the circuitry of the standalone CTLE required for the conventional design is shown in Figure 6. The comparison focuses solely on these two configurations, excluding downstream circuits, to maintain a direct assessment of their performance. In this simulation, both receivers are optimized to achieve a total bandwidth of 10 MHz. For a fair comparison, the power dissipation and the low-frequency gain of the TIA are fixed in the two receivers (i.e., referring to Figures 2 and 3,

$R_F = R_{F1} + R_{F2}$ and $g_{m,TIA}$ is unchanged). The modulation bandwidth of the LED is fixed at 3 MHz. In the conventional receiver, the CTLE dissipates a DC power of 427.9 μ W, contributes 44.5% of the total integrated input noise power, and attenuates the signal by 6.4 dB. Therefore, eliminating the standalone CTLE in the proposed receiver improves the input-referred noise PSD, overall gain, and power dissipation by $2.5\times$ and 6.4 dB, and 42.75%, respectively. Simulation results are depicted in Figure 8.

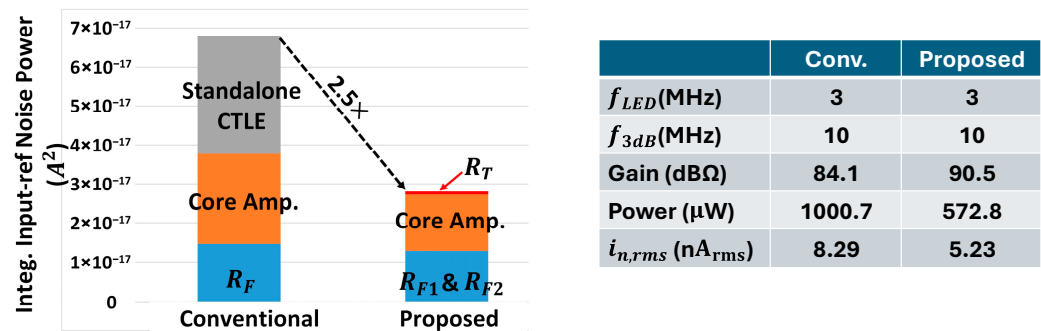


Figure 8. The proposed TIA-TE is evaluated against a conventional system comprising a full-bandwidth TIA followed by a standalone CTLE. The comparison focuses solely on these two configurations, excluding downstream circuits, to maintain a direct assessment of their performance.

3.2. Validation of the Proposed VLC Transceiver

This section extends the simulations to validate the entire VLC link. Figure 9a shows the layout of the proposed VLC transceiver in AMS 0.35 μ m CMOS technology. The chip occupies an area of 3.7 mm²; the total area is pad-limited, while the active area is only 0.81 mm $\times$ 0.75 mm. The chip dissipates a total DC power of 2.48 mW, excluding the 50 Ω output buffer. Figure 9b shows the power breakdown. In simulations that follow, C_{PD} and the LED's bandwidth are fixed at 4 pF and 3 MHz, respectively. The frequency response of the proposed TIA-TE is simulated in Figure 10, indicating that tunable peaking amplitude (up to 6 dB) and peaking frequency can be obtained by varying R_T and C_T , respectively. The performance of the TIA-TE is tuned by varying the control voltage V_{c1} and V_{c2} shown in Figure 4b.

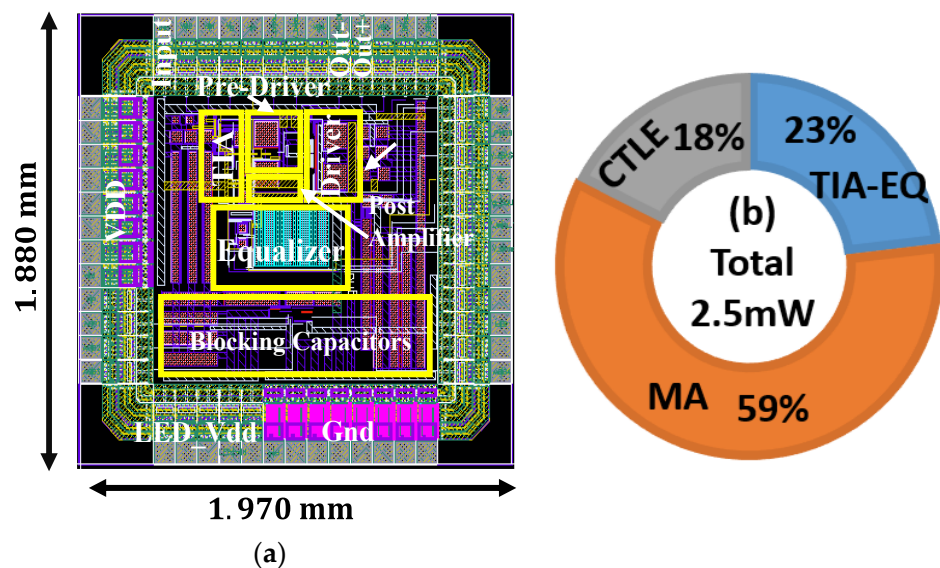


Figure 9. (a) Layout of the proposed VLC transceiver and (b) power breakdown.

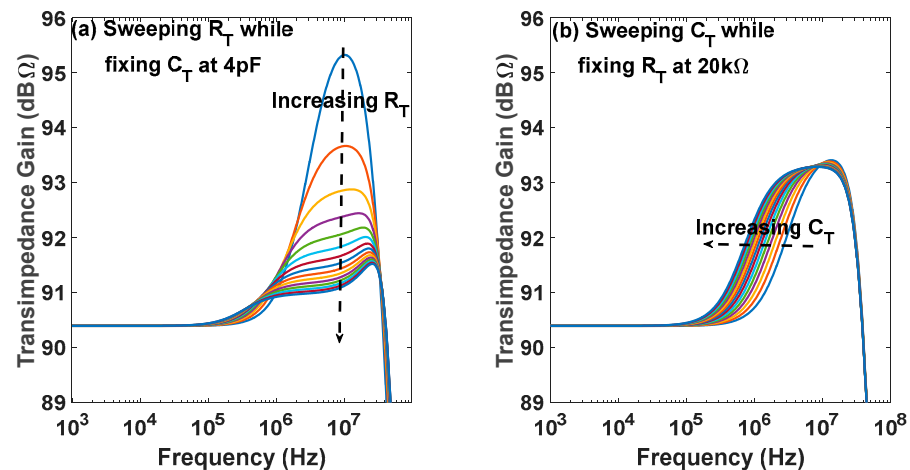


Figure 10. Simulated frequency response of the proposed TIA-TE (a) tunable peaking amplitude with fixed peaking frequency and (b) tunable peaking frequency with fixed peaking amplitude.

The progressive improvement in the bandwidth is indicated by the simulated frequency responses in Figure 11. Without equalization, the bandwidth at the output of the TIA is only 3.2 MHz, limited by the LED's bandwidth. Incorporating the T-network feedback extends the bandwidth at the output of the TIA by approximately $2.6\times$ to 8.3 MHz without compromising the low-frequency gain or DC power dissipation. The frequency response at the final output shows an amplitude peaking at less than 0.8 dB. The MA and the standalone CTLE together add 19.5 dB of gain, while the CTLE extends the bandwidth by 1.75 times to 14.1 MHz.

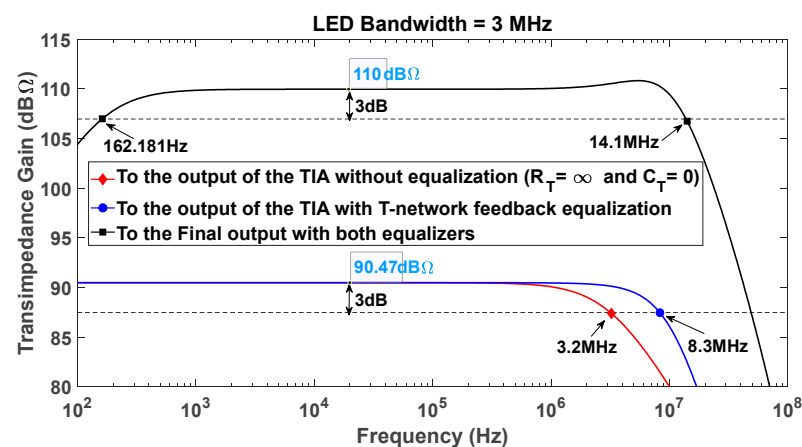


Figure 11. Simulated frequency responses indicate progressive improvements in the bandwidth.

The total integrated output-referred noise power is $5.184 \times 10^{-6} \text{ V}^2$. Taking the square root and referring the result to the input using the mid-band gain results in RMS input-referred noise current ($i_{n,rms}$) of 7.2 nA_{rms}. Figure 12 shows the simulated 28 Mb/s eye diagrams at the sensitivity level for a bit-error rate (BER) of 10^{-9} $i_{pp}^{sens} \approx 12i_{n,rms} = 86.4 \text{ nA}_{pp}$. The eye diagram of the received photocurrent is fully closed due to ISI introduced by the LED's insufficient bandwidth. Post-equalization progressively improves eye quality, as evident by the wide opening of the simulated eye diagrams at the outputs of the TIA-TE and the 50 Ω buffer.

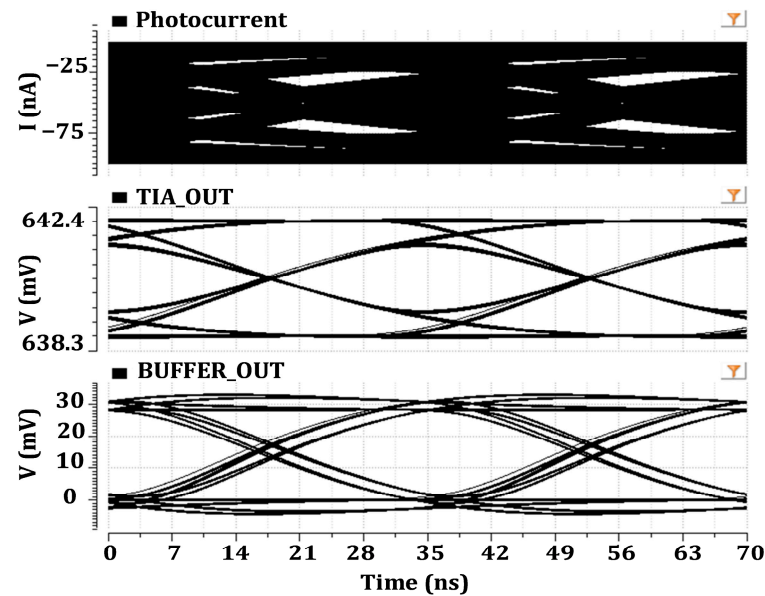
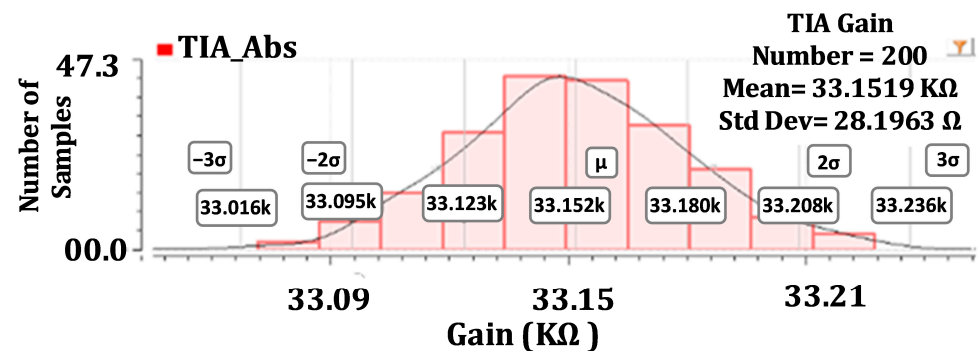
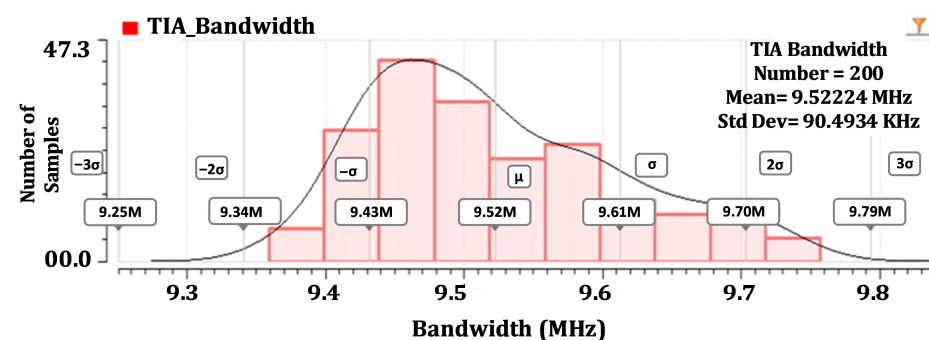


Figure 12. Simulated 28 Mb/s eye diagrams for 86.4 nA_{pp} at the input of the TIA (top), at the output of the proposed TIA-TE (middle), and at the final output (bottom).

The performance of the proposed TIA-TE in Figure 4 is evaluated under process and mismatch variations through 200 runs of Monte Carlo simulations, as shown in Figure 13. The bandwidth averages at 9.5 MHz with a standard deviation of only 90.5 kHz. The gain shows a mean value of 33.15 k Ω (90.4 dB Ω) with a standard deviation of 28.2 Ω . Monte Carlo simulations demonstrate a robust performance against process and mismatch variations compared to the nominal performance reported in Figure 8.



(a)



(b)

Figure 13. Monte Carlo simulations of the (a) gain and (b) bandwidth. The simulation is performed on the circuit in Figure 4 with nominal performance indicated in Figure 8.

Table 1 compares the proposed receiver with recently published VLC link receivers. The work in [3] utilizes post-equalization to achieve 32 Mb/s NRZ operation over a 2 m distance using an LED with a bandwidth of only 1.6 MHz. The data rate is further increased to 50 Mb/s by using blue filtering. Despite the significant bandwidth extension, the BER of the link in [3] is limited to 10^{-2} , necessitating the use of forward error correction (FEC) and receiver-side digital signal processing (DSP). Reference work [6] utilizes a two-stage CTLE at the receiver to compensate for the LED's limited bandwidth, achieving a BER of 10^{-9} at 24 Mb/s over a distance of 1.6 m with an LED modulation bandwidth of less than 3 MHz. The work in [5] combines pre-equalization, post-equalization, and blue filtering techniques to achieve a remarkable 550 Mb/s NRZ operation while employing an LED with a bandwidth of only 3 MHz. This high speed comes at the cost of reduced energy efficiency due to the use of discrete components in the transceiver circuits. The proposed receiver outperforms state-of-the-art examples in terms of noise performance. This advantage results from integrating the equalizer into the TIA, reducing the number of cascaded equalizer stages, and minimizing thermal noise sources.

Table 1. Performance comparison with recently published receivers.

	Process	LED Bandwidth	Transmission Distance	Data Rate	BER	Bandwidth Extension Tech.	Gain	Input-Ref. Noise Current	Power Dissipation
[3]	130 nm CMOS	1.6 MHz	2 m	32 Mb/s- To 50 Mb/s	10^{-2}	Post-eq (CTLE) + Blue filtering	91.16 dB Ω	65 nA _{rms}	2.4 mW
[6]	180 nm CMOS	<3 MHz	1.6 m	24 Mb/s	10^{-9}	Post-eq (two-stage CTLE)	123 dB Ω	59 nA _{rms}	2.2 mW
[5]	Discrete	3 MHz	0.6 m	550 Mb/s	2.6×10^{-9}	Pre-eq + Post-eq + Blue filtering	NA	NA	324 mW ⁽²⁾
[12]	Discrete	1 MHz	1.5 m	37 Mb/s	NA	RLC Pre-eq	AGC	NA	NA
[13]	Discrete	4.4 MHz	6 m	62.5 Mb/s	$<10^{-3}$	DSP Post-equalizer	40 dB	NA	25 mW
[14]	180 nm CMOS	NA	NA	2.6 MHz	NA	TIA, Active inductor	98 dB	7.5 pA/ $\sqrt{\text{Hz}}$	0.396 W
This work ⁽¹⁾	350 nm CMOS	3 MHz	NA Simulation	28 Mb/s	10^{-9}	Post-eq (TIA-TE + CTLE)	110 dB Ω	7.2 nA _{rms}	2.48 mW

⁽¹⁾ Post-layout simulation, excluding the 50 Ω output buffer. ⁽²⁾ The value is obtained from the datasheet of the device. NA: not available.

Table 1 provides a comprehensive comparison of the proposed receiver and representative VLC receivers spanning fully integrated CMOS implementations and discrete high-speed demonstrations. Several important observations can be drawn from this comparison. First, among fully integrated CMOS solutions targeting phosphor-converted white LEDs, the most relevant references are [3,6]. The 130 nm CMOS receiver in [3] achieves 32–50 Mb/s using post-equalization and optional blue filtering with an LED bandwidth of 1.6 MHz. While the reported bandwidth extension ($\sim 20\times$) is significant, the achieved BER is limited to 10^{-2} , which requires forward error correction (FEC) and digital signal processing for reliable communication. Moreover, the input-referred noise current is relatively high (65 nA_{rms}), reflecting the penalty associated with standalone CTLE-based cascade equalization. In contrast, the proposed receiver achieves a BER of 10^{-9} without relying on FEC, while reducing the input-referred noise current by nearly an order of magnitude (7.2 nA_{rms}). This substantial noise improvement stems directly from embedding the equalizer within the TIA feedback network, thereby eliminating noisy transconductance stages.

The 180 nm CMOS SoC in [6] demonstrates 24 Mb/s at $\text{BER} = 10^{-9}$ using a two-stage CTLE to compensate for a sub-3 MHz LED. Although [6] achieves a low BER comparable to this work, it relies on a cascaded CTLE architecture with a higher input-referred noise (59 nA_{rms}) and a higher transimpedance gain (123 dB Ω), indicating a more aggressive gain strategy to offset equalizer attenuation. In contrast, the proposed design achieves competitive BER performance with significantly lower input-referred noise and comparable power dissipation (2.48 mW vs. 2.2 mW), despite being implemented in an older 0.35 μm CMOS process. This highlights the intrinsic efficiency of the feedback-embedded equalization approach, which improves noise–bandwidth performance without requiring process scaling or large transconductance values.

Reference [5] demonstrates an impressive 550 Mb/s data rate using a 3 MHz LED; however, this performance is achieved through a combination of pre-equalization, post-equalization, blue filtering, and discrete high-speed components consuming 324 mW. The architecture sacrifices energy efficiency and integration density to reach extremely high throughput. In contrast, the proposed receiver focuses on integrated, low-power CMOS implementation (2.48 mW), targeting practical LED-limited Li-Fi front ends rather than laboratory-grade high-speed demonstrations.

The discrete implementation in [12] achieves 37 Mb/s by applying RLC pre-equalization at the transmitter, extending LED bandwidth from approximately 1 MHz to about 12 MHz. While effective, this method shifts complexity to the transmitter and does not address the receiver noise–bandwidth trade-off. The receiver TIA remains conventional, and equalization does not influence the loop dynamics of the transimpedance stage. Similarly, ref. [13] employs a limiting amplifier and DSP-based post-equalization following a TIA to achieve 62.5 Mb/s over 6 m. This cascade structure improves reach but introduces additional high-gain stages and digital complexity, increasing overall system power (~25 mW) compared to the proposed fully analog integrated solution.

Reference [14] presents a 0.18 μm CMOS TIA with ambient light rejection using an active inductor technique. While it achieves low noise spectral density (7.5 pA/ $\sqrt{\text{Hz}}$) and high gain, it does not incorporate bandwidth compensation for LED-limited channels and does not demonstrate a high-data-rate equalized operation. Therefore, it primarily addresses ambient light interference rather than LED-induced ISI.

Overall, Table 1 demonstrates that while prior works achieve either higher peak data rates (at the expense of power and discrete implementation) or a comparable BER (at the expense of higher noise and cascade complexity), the proposed receiver uniquely combines low noise, low power, full CMOS integration, and feedback-embedded equalization to optimize the noise–bandwidth–power trade-off for LED-limited VLC links.

4. Conclusions

In this paper, a novel transimpedance amplifier (TIA) architecture with an embedded T-network shunt-feedback equalizer (TIA-TE) has been introduced to address the limited modulation bandwidth in phosphor-converted white LEDs used for visible light communication (VLC). The proposed TIA incorporates a tunable high-frequency peaking directly into its frequency response, eliminating the need for power-hungry standalone equalizers. Post-layout simulations in a 0.35 μm CMOS process demonstrate that this approach extends the system bandwidth by 4.7 times, enabling 28 Mb/s NRZ data transmission. The proposed receiver achieves a high mid-band gain of 110 dB Ω and a low input-referred noise current of 7.2 nA_{rms} while consuming only 2.48 mW, making it a low-complexity, energy-efficient solution for LED-limited VLC links. Future work will include silicon measurements, BER characterization under varying ambient illumination, and robust evaluation across channel/LED variations.

Author Contributions: Conceptualization, M.A.; methodology, N.M. and M.A.; software, N.M. and D.A.; validation, N.M. and D.A.; formal analysis, N.M. and D.A.; investigation, N.M. and D.A.; resources, N.M., D.A. and M.A.; data curation, N.M. and D.A.; writing—original draft preparation, N.M. and D.A.; writing—review and editing, M.A.; visualization, N.M. and D.A.; supervision, M.A.; project administration, M.A.; funding acquisition, M.A. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the United Arab Emirates University under Grant G00004546.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

TIA	Transimpedance Amplifier
MA	Main Amplifier
CTLE	Continuous-Time Linear Equalizer
FEC	Forward Error Correction
DSP	Digital Signal Processing
LED	Light-emitting Diode
ISI	Inter-Symbol Interference

Appendix A

This Appendix A continues the noise analysis in Equation (12).

$$\overline{I_{n,TE}^2}(s) = \frac{4kT}{R_{F1}} \frac{|a_1 + b_1s + c_1s^2|^2}{|d_1 + d_2s|^2} + \frac{4kT}{R_{F2}} \frac{|a_2 + b_2s + c_2s^2|^2}{|d_1 + d_2s|^2} + \frac{4kT}{R_T} \frac{|a_3 + b_3s + c_3s^2|^2}{|d_1 + d_2s|^2} + \frac{4kT\gamma}{g_{m,TIA}(R_{F1} + R_{F2})^2} \frac{|a_4 + b_4s + c_4s^2|^2}{|d_1 + d_2s|^2}$$

The coefficients a_i , b_i , c_i , and d_i are given by

$$\begin{aligned} a_1 &= g_{m,TIA}R_{F1}, \quad a_2 = g_{m,TIA}R_{F2}, \quad a_3 = 0, \quad a_4 = 1 \\ b_1 &= C_{PD}R_{F1} + g_{m,TIA}R_{F1}C_T(R_T + R_{F2}) \\ b_2 &= C_{PD}R_{F2} + g_{m,TIA}R_{F2}C_T(R_T + R_{F2}) \\ b_3 &= C_T R_T(1 + g_{m,TIA}R_{F2}) \\ b_4 &= C_{PD}(R_{F1} + R_{F2}) + C_T(R_T + R_{F2}) \\ c_1 &= c_3 = C_T C_{PD}R_{F1}R_T, \quad c_2 = C_T C_{PD}R_{F2}(R_T + R_{F1}) \\ c_4 &= C_T C_{PD}R_{F1}R_{F2}(1 + R_T/R_{F1} + R_T/R_{F2}) \\ d_1 &= -g_{m,TIA}(R_{F1} + R_{F2}) + 1 \\ d_2 &= -g_{m,TIA}C_T R_{F1}R_{F2}(1 + R_T/R_{F1} + R_T/R_{F2}) \end{aligned}$$

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