

Article

Analysis and Control of Capacitor-Based Serial Chain-Link MMC with Reduced DC-Blocking Capacitor

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Abstract

The series-connected chain MMC with DC-blocking capacitor (C-SCMMC) is an emerging topology for HVDC tapping applications with high voltage and relatively low power capacity. However, the DC-blocking capacitor can be bulky and costly, which deteriorates its economy and flexibility. This paper investigates the feasibility of DC-blocking capacitor reduction, with special emphasis on the characteristics, control, and parameter design. The principle of C-SCMMC considering the DC-blocking capacitor dynamics is firstly modeled and analyzed, and the ripples and harmonics, as well as their influences on the external performance of the converter, are analyzed; then, improved control strategies, namely, the grid-tied harmonics suppression and current control, are proposed considering the enlarged DC-blocking capacitor voltage ripple; after that, the influence of reduced DC-blocking capacitor on the operation range and parameter design are analyzed, and the economic advantage is demonstrated via parameter design and comparison based on a typical bench mark. Analysis shows that the DC-blocking capacitor voltage ripple is coupled with other parameters, such as the arm output voltage and SM capacitance, and the advised range is from 0.1 to 0.3 p.u. at unity power factor to reduce the overall cost. In a typical design, the C-SCMMC can reduce the number of SMs by 2/3 and the capacitor energy storage capacity by 15% compared to the conventional MMC. Finally, simulation results obtained in MATLAB/Simulink 2024b are provided to verify the feasibility of the proposed converter and the correctness of the parameter design.

Keywords: capacitor-based serial chain-Link MMC; converter control; parameter design; high-voltage direct current



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1. Introduction

The high-voltage direct current (HVDC) technology is widely utilized for long-distance transmission of bulky power. China has made ambitious plans to develop solar and wind energies in the desert, Gobi, and desertification land, as well as the far-sea offshore wind power, to meet its “Carbon peak, Carbon neutrality” goals, which rely on a series of massive ultra-high voltage DC projects to transmit the generated power to its eastern and southern load centers. However, apart from the sending and receiving terminals, the HVDC projects can hardly benefit the distributed power source integration or load consumption needs along the line because of the expensive cost of the AC/DC converter station [1–3].

Therefore, the HVDC-tapping technology is proposed to extract or feed a small amount of power, typically less than 0.1 p.u., from or into the HVDC system [4]. Series and shunt tapping are the main types, and the shunt type is more favored considering its high reliability and easy integration. Meanwhile, the modular multilevel converter (MMC) technology is widely applied in high-voltage converters due to its advantages of low harmonics and switching losses, as well as high controllability and reliability [5,6]. The most commonly utilized MMC in HVDC is the three-phase parallel type, which can maximize the power conversion capacity with the limited ratings of each individual power submodule (SM) [7,8]. However, in the HVDC tapping scenarios, the converter power capacity is much smaller while the DC voltage that predominates the number of SMs remains unchanged. This would cause inadequate utilization of the SM power ratings and, therefore, high converter cost if the three-phase parallel structure is still utilized [9–11].

To reduce the number of SMs and improve the converter economy, various novel MMC topologies, as shown in Figure 1, have been extensively proposed in recent years. One solution is the hybrid topology, specifically the alternative arm multilevel converter (AAMC) proposed in [12,13]. AAMC can reduce approximately 50% SMs by combining a two-level converter and MMC, and replacing a proportion of SMs with director switches [14,15]. However, the constantly varying power path in AAMC results in more difficult inherent energy balancing and larger SM voltage fluctuation [16,17].

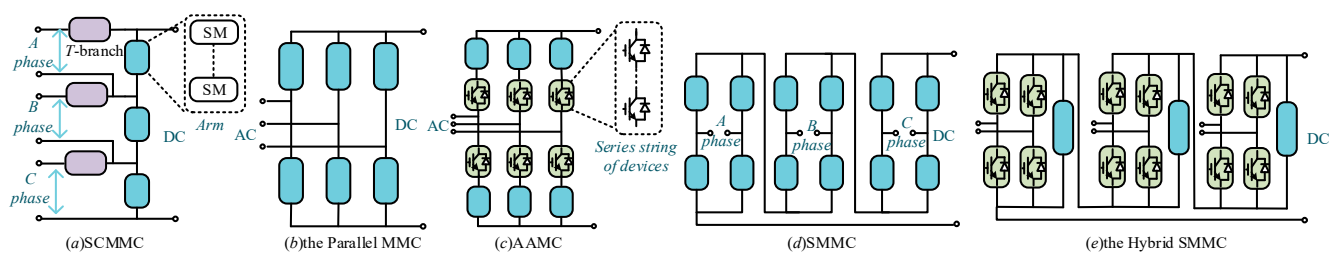


Figure 1. Circuit of the discussed topologies.

Another solution is to utilize the three-phase series structure instead of the parallel structure. The series-connected MMC (SMMC) proposed in [18–20] contains three single-phase converter units in series connection to withstand the total DC voltage, and each phase unit utilizes four SM-cascaded arms to form an H-bridge. In this way, the DC voltage across each phase unit is reduced, and therefore, the number of SMs can be reduced by one-third compared to the three-phase parallel MMC [21,22]. To further reduce the number of SMs, the Hybrid SMMC proposed in [23,24] replaces two SM-cascaded arms with an H-bridge converter formed from many serial-connected semiconductors in each phase unit. In this way, the number of SMs is further reduced by 50%, but the additional semiconductors required offset most of the savings.

The Series Chain-link MMC (SCMMC), as shown in Figure 2, is another three-phase series family that achieves a good trade-off between the SM/semiconductor and capacitor cost [25]. In the SCMMC, each phase unit contains one major SM-cascaded arm in serial connection with its two counterparts on the DC side, and each major arm withstands 1/3 of the DC voltage. Meanwhile, to eliminate the influence of the DC voltage on the AC side, each phase unit is equipped with a DC-blocking branch, also referred to as a T-branch, between its DC and AC terminals, and a series of SCMMC family members are proposed according to different T-branch structures. The active- and hybrid-SCMMC are the most extensively investigated members because of control flexibility [25,26]. The active-SCMMC utilizes another SM-cascaded arm as the T-branch, which provides the best controllability at the cost of the highest expenses. The hybrid-SCMMC replaces some of the SMs in the T-branch with a DC-blocking capacitor, but the energy balancing between the

SMs and the capacitor is tough [26–29]. The LC-SCMMC further replaces the rest of the SMs with an inductor. By properly tuning the LC parameters, the voltage drop across the LC link equals zero at the fundamental frequency, but a high-voltage inductor is also costly. On the other hand, the C-SCMMC that utilizes a pure capacitor as the T-branch attracts little attention, because it is believed that the capacitor should be sufficiently large to reduce the influences caused by voltage ripples to a negligible level [30,31]. However, the influences have never been quantitatively investigated, nor has the possibility of utilizing reduced capacitors, which will substantially improve the economic performance of the C-SCMMC. Compared to the conventional MMC, the number of SMs in C-SCMMC is decreased by 67%, which is also helpful to reduce the total energy storage capacity. Meanwhile, the C-SCMMC with the reduced DC-blocking capacitor further reduces the cost of the SMs and the capacitor in relation to the active- and hybrid-SCMMC. Consequently, the C-SCMMC with the reduced DC-blocking capacitor has the obvious economic advantage, but the influences of the ripples and harmonics on the performance of the converter are not clear.

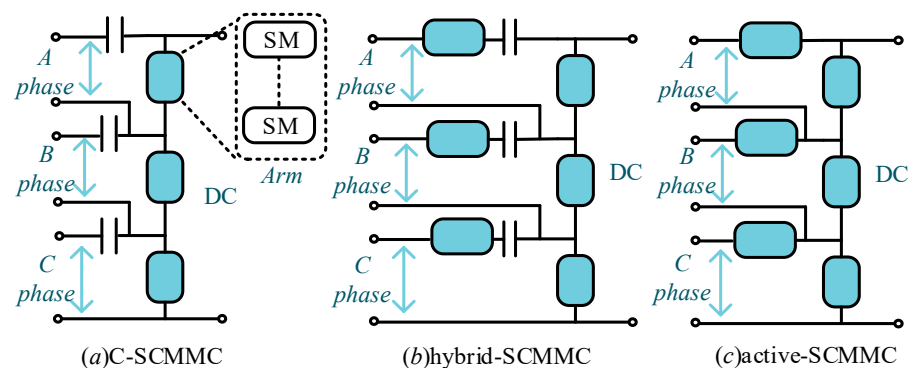


Figure 2. Circuit of the SCMMC family.

To address this issue, this paper is focused on the characteristics, control, and parameter design of the C-SCMMC with a reduced DC-blocking capacitor. The reduced DC-blocking capacitor leads to higher voltage ripples, which further influence the circuit parameter, e.g., the arm voltage and the SM capacitor voltage, and the dynamics of the AC-side current control. This paper will provide an in-depth investigation into the relationship of these parameters, and two improved current control strategies, namely, capacitor voltage feedforward and dq -axis cross-decoupling control, are proposed to guarantee the performance of the AC-side current loop. After that, the ripple/harmonic coupling mechanism in C-SCMMC is analyzed, and the grid-tied harmonics suppression current control is proposed considering the enlarged DC-blocking capacitor voltage ripple; and the economic advantage is demonstrated via parameter design and comparison based on a typical bench mark; finally, the proposed strategies and conclusions are validated by simulation conducted in MATLAB/Simulink 2024b.

The rest of the article is organized as follows. Section 2 introduces the configuration and basic model of the C-SCMMC, and Section 3 establishes the models of the ripples and harmonics. Section 4 describes the detailed control strategies to handle the harmonic suppression and current control issues. Section 5 investigates the influence of a reduced DC-blocking capacitor on parameter design and operation range. Section 6 provides simulation results to validate the C-SCMMC operation and parameter design method. Finally, Section 7 summarizes the paper.

2. Configuration and Modeling of C-SCMMC

2.1. Configuration

Figure 3 shows the configuration of C-SCMMC. The C-SCMMC comprises a transformer and three single-phase converter units. To achieve three-phase series operation, the secondary side of the transformer employs an open-delta connection, with each phase winding connected to its corresponding phase converter unit. Each single-phase converter unit consists of a DC-blocking capacitor, an SM-cascaded arm, and an inductor. The transformer can isolate the zero-sequence voltage between the grid and the C-SCMMC, and the three-phase AC-side voltages sum up to zero, which does not affect the DC-side output voltage. Therefore, the DC-side voltage and current can remain a highly stable value with extremely low ripple. Meanwhile, the DC-blocking capacitor can eliminate the DC offset produced by the corresponding arm to ensure the high-quality AC-side voltage and current. In the steady state, the three arms from different units are serially connected to share the DC voltage. Consequently, each arm only needs to output one-third of the DC voltage plus the corresponding phase AC voltage, so that the required number of SMs is reduced. The arm current comprises the DC-side current and the AC-side phase current. And the DC-blocking capacitor voltage and the SM capacitor voltage will fluctuate around their rated value due to periodically varying current through them.

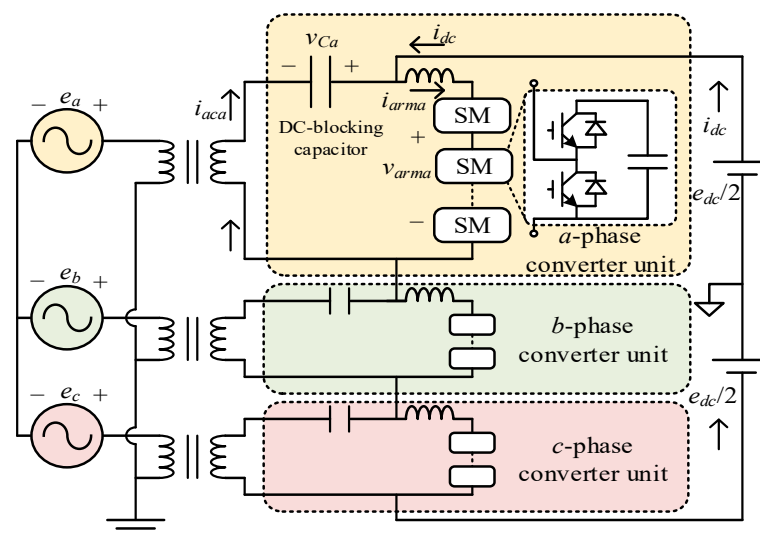


Figure 3. Topology and equivalent circuit of C-SCMMC.

2.2. Basic Model of the C-SCMMC

The Kirchhoff voltage and current equations for C-SCMMC can be formulated with the positive direction shown in Figure 3. To simplify the expression, x ($x \in \{a, b, c\}$) will be utilized to represent any phase in the rest of this paper. This section will provide an in-depth investigation into the basic model and the fundamental operating principles of C-SCMMC.

2.2.1. AC-Side Equations

In Figure 3, the Kirchhoff voltage law (KVL) equation for the converter units can be established as follows:

$$\begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix} + \begin{bmatrix} v_{Ca} \\ v_{Cb} \\ v_{Cc} \end{bmatrix} - L_T \frac{d}{dt} \begin{bmatrix} i_{aca} \\ i_{acb} \\ i_{acc} \end{bmatrix} - L_{arm} \frac{d}{dt} \begin{bmatrix} i_{arma} \\ i_{armb} \\ i_{armc} \end{bmatrix} - \begin{bmatrix} v_{arma} \\ v_{armb} \\ v_{armc} \end{bmatrix} = 0 \quad (1)$$

And the voltage and current of phase a can be expressed as follows:

$$\begin{cases} e_a = E_{ac} \cos(\omega t) \\ i_{aca} = I_{ac} \cos(\omega t - \varphi) \end{cases} \quad (2)$$

where e_x denotes the x -phase grid voltage transformed to the secondary side; E_{ac} and I_{ac} denote the amplitude of the phase voltage and line current, respectively; φ represents the power factor angle. The expressions for phase b and c can be obtained by phase-leading or lagging of $2\pi/3$ on the basis of Equation (2), respectively; v_{Cx} represents the voltage of the DC-blocking capacitor in phase x ; L_T represents the leakage inductance of the converter transformer; L_{arm} represents the arm inductance; v_{armx} represents the output voltage of the x -phase arm.

By ignoring the variation in capacitor voltages among the SMs within the same arm, v_{armx} can be expressed as follows:

$$v_{armx} = n_{SM} \cdot v_{SMx} \cdot m_x \quad (3)$$

where n_{SM} denotes the number of SMs in each arm; v_{SMx} represents the average SM capacitor voltage of the x -phase arm; m_x indicates the modulation signal for phase x .

In the steady-state, the three-phase currents sum up to zero:

$$\sum_{x=a,b,c} i_{acx} = 0 \quad (4)$$

Consequently, applying the Clarke transformation to Equation (1) yields the following:

$$\begin{bmatrix} e_\alpha \\ e_\beta \\ e_0 \end{bmatrix} + \begin{bmatrix} v_{C\alpha} \\ v_{C\beta} \\ v_{C_dc} \end{bmatrix} - L_T \frac{d}{dt} \begin{bmatrix} i_{ac\alpha} \\ i_{ac\beta} \\ i_{ac0} \end{bmatrix} - L_{arm} \frac{d}{dt} \begin{bmatrix} i_{arm\alpha} \\ i_{arm\beta} \\ i_{dc} \end{bmatrix} - \begin{bmatrix} v_{arm\alpha} \\ v_{arm\beta} \\ v_{arm_dc} \end{bmatrix} = 0 \quad (5)$$

where the subscripts α , β , and 0 denote the α -axis, β -axis, and 0-axis components of the corresponding variable; v_{arm_dc} and v_{C_dc} denote the DC component in the arm output voltage and the DC-blocking capacitor voltage, respectively. In addition, the three-phase grid voltage does not contain a common-mode (zero-sequence) component under normal operating conditions; hence, $e_0 = 0$.

For each arm, the Kirchhoff current law (KCL) equation can be expressed as follows:

$$i_{armx} = i_{acx} + i_{dc} \quad (6)$$

where i_{acx} and i_{dc} are the AC-grid-tied current of phase x and the DC-grid-tied current, respectively; i_{armx} denotes the current flowing through the arm of phase x .

According to Equation (6), i_{dc} is a common-mode component, and the α - and β -axis components of the $\{i_{arma}, i_{armb}, i_{armc}\}$ equal those of the $\{i_{aca}, i_{acb}, i_{acc}\}$, i.e.,:

$$i_{arm\alpha,\beta} = i_{ac\alpha,\beta} \quad (7)$$

Therefore, in Equation (5), the equations for α -axis and β -axis components can be formulated as follows:

$$\begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} + \begin{bmatrix} v_{C\alpha} \\ v_{C\beta} \end{bmatrix} - (L_T + L_{arm}) \frac{d}{dt} \begin{bmatrix} i_{ac\alpha} \\ i_{ac\beta} \end{bmatrix} - \begin{bmatrix} v_{arm\alpha} \\ v_{arm\beta} \end{bmatrix} = 0 \quad (8)$$

2.2.2. DC-Side Equations

The KVL equation on the DC side can be established as follows:

$$e_{dc} - L_{arm} \frac{d}{dt} \left(\sum_{x=a,b,c} i_{armx} \right) - \sum_{x=a,b,c} v_{armx} = 0 \quad (9)$$

where e_{dc} represents the DC-side voltage;

Substituting Equation (4) into Equation (9) yields the following:

$$e_{dc} - 3L_{arm} \frac{d}{dt} i_{dc} - \sum_{x=a,b,c} v_{armx} = 0 \quad (10)$$

Considering the circuit symmetry, the DC-side voltage is evenly distributed among the arms, and by ignoring the impedance voltage drop, each arm outputs one-third of the DC-side voltage in the steady state:

$$v_{arm_dc} \approx 1/3 \cdot e_{dc} \quad (11)$$

In addition, the modulation ratio ρ is expressed as follows:

$$\rho = \frac{3E_{ac}}{e_{dc}} \quad (12)$$

2.2.3. Capacitor Voltage Fluctuation Equation

The DC-blocking capacitor voltage and the SM capacitor voltage will fluctuate around their rated value due to periodically varying current through them. The dynamic model for this process can be expressed as follows:

$$C \frac{d}{dt} v_{Cx} = -i_{acx} \quad (13)$$

$$C_{SM} \frac{d}{dt} v_{SMx} = m_x i_{armx} \quad (14)$$

where C and C_{SM} denote the DC-blocking capacitance and SM capacitance, respectively.

For the SMs, the fluctuation center is the nominal SM capacitor voltage. For the DC-blocking capacitor, by combining Equations (4), (5) and (11), we have the following:

$$v_{C_dc} - L_{arm} \frac{d}{dt} i_{dc} - v_{arm_dc} = 0 \quad (15)$$

and the steady-state yields the following:

$$v_{C_dc} = v_{arm_dc} = 1/3 \cdot e_{dc} \quad (16)$$

Therefore, the DC-blocking capacitor voltages $\{v_{Ca}, v_{Cb}, v_{Cc}\}$ will fluctuate around $e_{dc}/3$.

3. Ripple/Harmonic Analysis of C-SCMMC

The inherent coupling between the capacitor voltage ripples and current harmonics is a common problem in the MMC family. Nevertheless, this issue has not been investigated in the C-SCMMC topology, and will be elaborated on in this section. Without loss of generality, this paper selects phase a as a representative case for demonstration.

Due to the ripple/harmonic coupling, the variables in C-SCMMC contain a series of frequency components, and the generalized form is as follows:

$$x = X_0 + \sum_k X_k \cos(k\omega t + \theta_k) \quad (17)$$

where x represents the original variable, e.g., i_{armx} , v_{armx} , v_{Cx} , v_{SM} , i_{acx} , e.t.c. X_0 and X_k denote the amplitude of the DC- and k th-order components, respectively; θ_k is the phase-angle of the k th-order component.

3.1. Ripple of the DC-Blocking Capacitors

For the DC-blocking capacitors, the fundamental-frequency fluctuation component is the dominant ripple, which can be obtained by substituting Equation (2) into Equation (13), as follows:

$$v_{Ca_ac} = \frac{2S \cdot \sin(\omega t - \varphi)}{3\omega C E_{ac}} \quad (18)$$

where v_{Ca_ac} is the fluctuation component of the DC-blocking capacitor voltage in phase a ; S denotes the three-phase apparent power on the AC-side.

The DC-blocking and SM capacitors should be sufficiently large to limit their voltage fluctuation within a specified range. Considering that $v_{C_dc} = e_{dc}/3$ in the steady state, for a specified relative voltage fluctuation limit ε_C , the DC-blocking capacitance should be determined as follows:

$$C = \frac{2S}{\omega \varepsilon_C E_{ac} e_{dc}} \quad (19)$$

3.2. Capacitance Design of the SM Capacitors

For the SM capacitors, according to Equation (1), by ignoring the impedance voltage drop, the output voltage of the a -phase arm can be expressed as follows:

$$v_{arma} = e_{dc}/3 + e_a + v_{Ca_ac} \quad (20)$$

Subsequently, the modulation signal can be obtained following Equation (3):

$$m_a = \frac{1}{2} + \frac{3E_{ac}}{2e_{dc}} \cos(\omega t) + \frac{3I_{ac}}{2e_{dc}\omega C} \sin(\omega t - \varphi) \quad (21)$$

The detailed expression for v_{SMa} can be obtained by substituting Equation (21) into Equation (14), which is presented in Appendix A for simplicity. v_{SMa} contains a DC, a fundamental-frequency, and a double-frequency fluctuation component, i.e.,:

$$v_{SMa} = v_{SMa_dc} + A_1 \cos(\omega t + \theta_1) + A_2 \cos(2\omega t + \theta_2) \quad (22)$$

where v_{SMa_dc} , A_1 and A_2 represent the amplitudes of the DC-, fundamental- and double-frequency components, respectively; θ_1 and θ_2 are the corresponding phase-angles. The detailed expressions of A_1 and A_2 are also provided in Appendix A.

In terms of capacitance design, further analysis shows that the amplitude of v_{SMa_ac} increases as the power factor decreases. Consequently, given the apparent power, the SM capacitance should be designed based on the operation point with the lowest power factor. Specifically, if the C-SCMMC is required to have full reactive power output capability, the SM capacitance should be determined as follows:

$$C_{SM} = \frac{n_{SM}Q}{2E_{ac}\varepsilon_{SM}\omega e_{dc}} + \frac{Qn_{SM}\varepsilon_C}{8e_{dc}E_{ac}\varepsilon_{SM}\omega} + \frac{3Qn_{SM}}{8e_{dc}^2\varepsilon_{SM}\omega} \quad (23)$$

where ε_{SM} is the required relative fluctuation limit of the SM capacitor voltage.

3.3. Harmonics in Arm Voltages and Currents

Considering the ripples in v_{SMa} , v_{arma} contains a series of frequency components, and can be expressed as follows:

$$\begin{aligned} v_{arma} &= v_{arm_dc} + v_{arma_1\omega} + v_{arma_2\omega} + v_{arma_3\omega} \\ &= e_{dc}/3 + e_a + v_{Ca_ac} + B_2 \cos(2\omega t + \phi_2) + B_3 \cos(3\omega t + \phi_3) \end{aligned} \quad (24)$$

where v_{arma_dc} , $v_{arma_1\omega}$, $v_{arma_2\omega}$ and $v_{arma_3\omega}$ represent the DC- to 3rd-order frequency components in the a -phase arm output voltage, respectively; B_2/ϕ_2 and B_3/ϕ_3 represent the amplitudes/angles of the 2nd- and 3rd-order harmonic components, respectively. By substitute Equations (21) and (22) into Equation (3), the detailed expressions of B_2/ϕ_2 and B_3/ϕ_3 can be derived, which are also presented in Appendix A for simplicity.

Similarly, the detailed expression for v_{armb} and v_{armc} can be obtained as follows:

$$\begin{cases} v_{armb_2\omega} = B_2 \cos(2\omega t + \phi_2 + 2\pi/3) \\ v_{armb_3\omega} = B_3 \cos(3\omega t + \phi_3) \end{cases} \quad (25)$$

$$\begin{cases} v_{armc_2\omega} = B_2 \cos(2\omega t + \phi_2 - 2\pi/3) \\ v_{armc_3\omega} = B_3 \cos(3\omega t + \phi_3) \end{cases} \quad (26)$$

Therefore, $v_{armx_2\omega}$ are of negative-sequence, whereas $v_{armx_3\omega}$ are of zero-sequence. To establish the model of the corresponding harmonic current, the flow path and impedance should first be determined. For the 2nd-order component, they sum up to zero:

$$\sum_{x=a,b,c} v_{armx_2\omega} = 0 \quad (27)$$

and according to Equation (9), the 2nd-order harmonic current has no influence on the DC side, and only circulates in each phase unit, as the yellow, green, and red dashed lines shown in Figure 4. The KVL equation for phase- x can be established as follows:

$$i_{armx_2\omega} = v_{armx_2\omega} / \left(j2\omega L_T + j2\omega L + \frac{1}{j2\omega C} \right) \quad (28)$$

where $i_{armx_2\omega}$ represents the 2nd-order current harmonic component of i_{armx} .

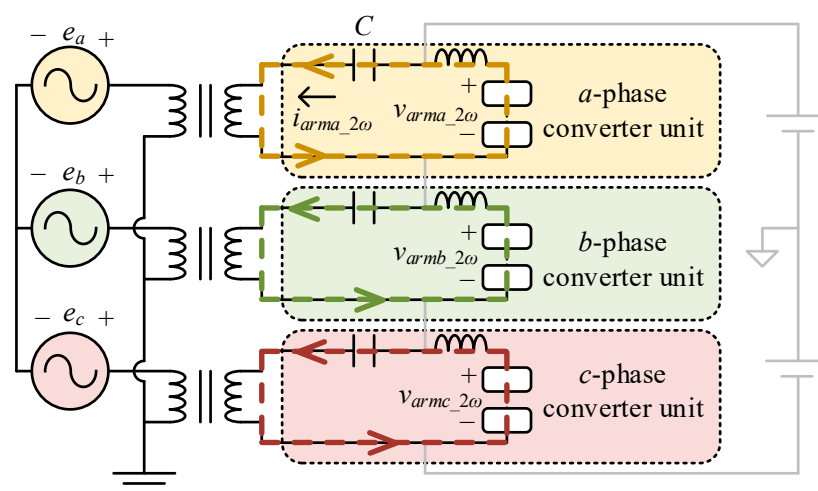


Figure 4. Negative sequence loop diagram of C-SCMMC.

For the 3rd-order component, two available paths exist, as shown in the blue dashed lines in Figure 5. The first path circulates through the AC-side of the three phase-units, while the second path flows through the DC side. The KVL equation for the two paths can be established as follows:

$$\begin{cases} 3v_{armx_{3\omega}} = j9\omega L \cdot i_{armx_{3\omega}} + \left(j9\omega L_T + \frac{1}{j\omega C}\right) i_{acx_{3\omega}} \\ 3v_{armx_{3\omega}} = j9\omega L \cdot i_{armx_{3\omega}} + R_d i_{dc_{3\omega}} \end{cases} \quad (29)$$

and the KCL equation on the DC-terminals yields the following:

$$i_{armx_{3\omega}} = i_{acx_{3\omega}} + i_{dc_{3\omega}} \quad (30)$$

where $i_{armx_{3\omega}}$ represents the triple-frequency harmonic component of the x -phase arm current; $i_{acx_{3\omega}}$ and $i_{dc_{3\omega}}$ are triple-frequency components of AC- and DC- side currents, respectively; R_d is the internal resistance of the DC-voltage source.

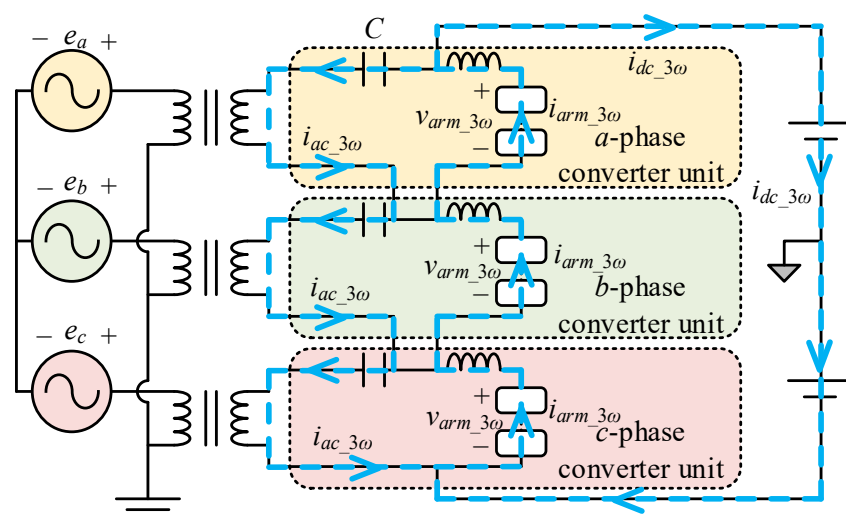


Figure 5. Zero sequence loop diagram of C-SCMMC.

According to Figures 4 and 5, all the current harmonics enter the external power grid, and should be well suppressed to guarantee good output power quality and high converter efficiency.

4. Control Design Considering Reduced DC-Blocking Capacitor

4.1. Overview of the Control System

The control system of C-SCMMC employs a hierarchy structure comprising the outer loop, the inner loop, and the modulation link, as is shown in Figure 6. Specifically, the outer loop is responsible for maintaining the energy balance of C-SCMMC, as well as external performance regulation, such as PQ control, V_f control, droop control, etc., and generates the current references for the inner loop. The inner loop ensures that the AC- and DC-grid-tied currents accurately track their corresponding references, and output the DC- and fundamental-frequency modulation signals. In addition, the suppression of the grid-tied harmonic currents roused by the inherent dynamics of C-SCMMC is also an important part, which generates several higher-order components that merge with those from the inner loop to form the final modulation signals. Finally, the modulation link generates trigger pulses for each SM considering the inner-arm SM energy balancing.

The strategies for most blocks are identical to those of other MMC topologies, except for the grid-tied current harmonic suppression. In addition, the enlarged DC-blocking

capacitor voltage ripple deteriorates the performance of the AC current control loop. These issues are discussed in this section.

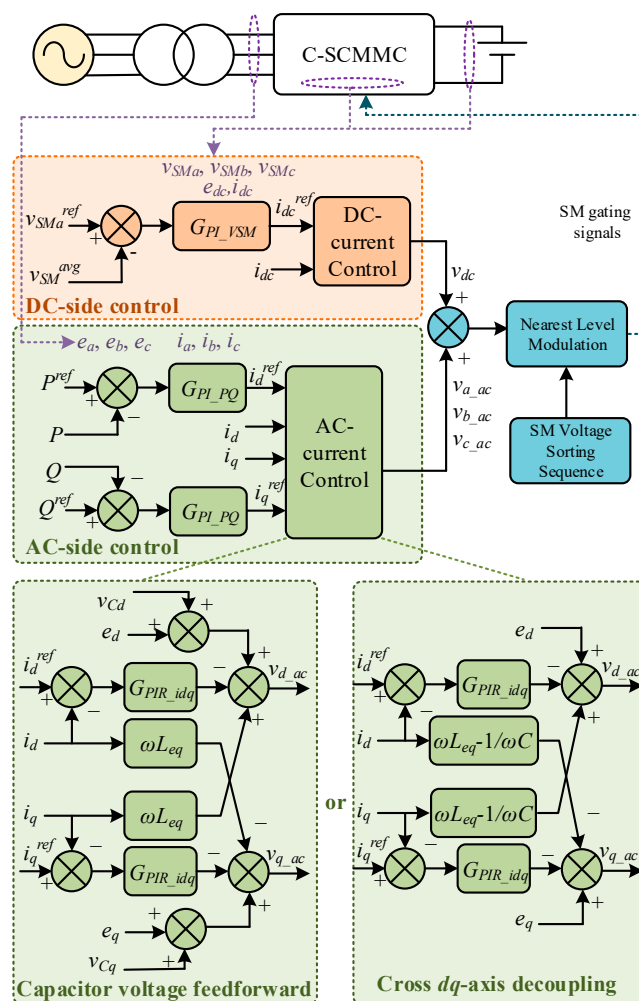


Figure 6. Control diagram of the C-SCMMC control.

4.2. Harmonic Suppression Strategy

On the DC-side, the higher-order coupling between the SM capacitor voltage ripple and the modulation signal will generate a zero-sequence current component with triple fundamental frequency. To mitigate this component, the DC-side current control is based on PI control with an additional resonant element to suppress the triple fundamental frequency harmonic current. The control equation can be expressed as follows:

$$v_{arm_dc}^{ref} = e_{dc} - G_{PIR_idc}(s)(i_{dc}^{ref} - i_{dc}) \quad (31)$$

where $v_{arm_dc}^{ref}$ denotes the reference for the DC component of the arm output voltage; $G_{PIR_idc}(s)$ denotes the transfer function of the Proportional-Integral-Resonant (PIR) controller:

$$G_{PIR_idc}(s) = K_P + K_I/s + K_R\omega_c s / (s^2 + 2\omega_c s + \omega_0^2) \quad (32)$$

where K_P , K_I , and K_R denote proportional-, integral-, and resonant- gain, respectively; ω_c and ω_0 represent resonant bandwidth and frequency.

On the AC-side, the harmonics consist of a 2ω component of negative-sequence and a 3ω component of zero-sequence. For the 3ω component, it has the same origin as the 3ω component on the DC-side. If the DC-side harmonics are well suppressed, the

3ω component on the AC-side will be simultaneously mitigated. Meanwhile, the 2ω negative-sequence component merges with the fundamental-frequency positive-sequence component, and they cannot be easily separated. After the ωt -based Park transformation, the ω component is converted to a DC component, while the 2ω component will be converted to a 3ω ripple. To achieve simultaneous control of these two components, the PIR controller in Equation (32) can also be utilized for AC-side current control.

4.3. Inner Loop Considering DC-Blocking Capacitor Voltage Ripple

According to Equation (8), the reduced DC-blocking capacitor will cause a larger voltage ripple, which influences the dynamics of the AC-side current. According to the ripple analysis in Section III, the fundamental-frequency component dominates the v_{Cx} ripple, whose influence can be gradually compensated by the integral branch of the controller. Therefore, the converter can still operate with a classic control strategy. However, the responding speed is slow due to the integral delay. To address this issue, two solutions are proposed in this section to guarantee the performance of the AC-side current loop, as shown in Figure 6.

4.3.1. Capacitor Voltage Feedforward

The first solution is to install three additional voltage sensors and utilize the sensed capacitor voltage as a feedforward component together with the grid-side voltage. The control equation can be expressed as follows:

$$\begin{cases} v_{armd_ac}^{ref} = e_d + v_{Cd} - G_{PIR_idq}(s)(i_d^{ref} - i_d) + \omega L_{eq} i_q \\ v_{armq_ac}^{ref} = e_q + v_{Cq} - G_{PIR_idq}(s)(i_q^{ref} - i_q) - \omega L_{eq} i_d \end{cases} \quad (33)$$

where $v_{armd_ac}^{ref}$, $v_{armq_ac}^{ref}$ represent the references for the dq -axis components of the AC component of the arm output voltage; v_{Cd} , v_{Cq} are the dq -components transformed from the measured $\{v_{Ca}, v_{Cb}, v_{Cc}\}$; L_{eq} denotes the equivalent total inductance of the current loop on the AC-side; $G_{PIR_idq}(s)$ denotes the transfer function of the PIR controller for the AC-side inner loop.

This method is expected to have the highest response speed at the cost of three additional voltage sensors.

4.3.2. Cross dq-Axis Decoupling

Another solution is to consider the DC-blocking capacitor in the conventional dq -axis cross-decoupling control architecture, as shown in the following equation:

$$\begin{cases} v_{armd_ac}^{ref} = e_d - G_{PIR_idq}(s)(i_d^{ref} - i_d) + (\omega L_{eq} - 1/\omega C) i_q \\ v_{armq_ac}^{ref} = e_q - G_{PIR_idq}(s)(i_q^{ref} - i_q) - (\omega L_{eq} - 1/\omega C) i_d \end{cases} \quad (34)$$

This method considers the v_{Cx} ripple as a voltage drop across a constant impedance and requires no additional hardware. Therefore, it achieves a good balance between cost and performance.

Subsequently, the references for the three-phase voltages $v_{a_ac}^{ref}$, $v_{b_ac}^{ref}$, and $v_{c_ac}^{ref}$ can be obtained by utilizing the inverse Park transform on $v_{armd_ac}^{ref}$ and $v_{armq_ac}^{ref}$.

5. Influence of Reduced DC-Blocking Capacitor on Circuit Parameter Design

This paper explores the feasibility of C-SCMMC with a reduced DC-blocking capacitor, i.e., parameter C in Figure 3. According to Equations (8), (19) and (23), the reduced DC-

blocking capacitor leads to higher v_{Cx_ac} , which further influences v_{armx_ac} and v_{SMx} . The rest of this paper will provide an in-depth investigation into these issues.

5.1. Influence on Arm Output Voltage Range and SM Count per Arm

According to Equations (1), (8) and (13), the reduced DC-blocking capacitor will cause larger v_{Cx_ac} and further influence the AC component in the arm output voltage, i.e., v_{armx_ac} . By neglecting the voltage drop across L_T and L_{arm} , the phasor version of Equation (8) can be expressed as follows:

$$v_{armx_ac} = \hat{e}_x + v_{Cx_ac} = \hat{e}_x + \frac{\hat{i}_{acx}}{j\omega C} \quad (35)$$

where $\hat{x}$ denotes the phasor associated with the variable x .

The phasor diagram of Equation (35) is illustrated in Figure 7a. Since v_{Cx_ac} always lags $\hat{i}_{acx}$ by 90 degrees, the angle between v_{Cx_ac} and $\hat{e}_x$ is determined by φ . Therefore, under given apparent power, v_{armx_ac} will move along the dashed circle with φ varying from 0 to 2π . Figure 7b–d show several special cases, i.e., $\varphi = 0$ and $\pm\pi/2$. According to Figure 7b, v_{Cx_ac} and $\hat{e}_x$ have identical angle when $\varphi = \pi/2$, resulting in the maximum amplitude of v_{armx_ac} . On the contrary, when $\varphi = -\pi/2$ in Figure 7c, v_{Cx_ac} and $\hat{e}_x$ are opposite, and the amplitude of v_{armx_ac} is the smallest. In Figure 7d, when $\varphi = 0$, v_{Cx_ac} and $\hat{e}_x$ are orthogonal, which has relative moderate impact on the amplitude of v_{armx_ac} .

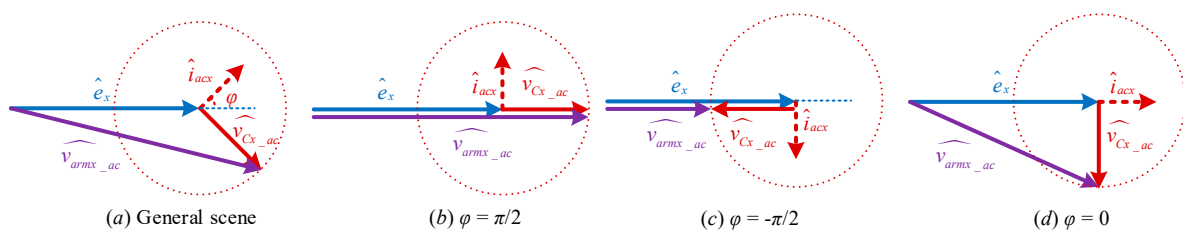


Figure 7. Vector diagram.

Figure 8 further illustrates the varying amplitude of v_{armx_ac} with various ε_C and φ . When $\varphi \in (0, \pi)$, the amplitude of v_{armx_ac} increases as ε_C increases. However, when $\varphi \in (-\pi, 0)$, the amplitude of v_{armx_ac} initially decreases but subsequently increases. Specifically, given that $\rho = 0.8$, $\varphi = 0$ and $\varepsilon_C = 0.3$, the amplitude of v_{armx_ac} will increase by 6.8%. As φ decreases, that is, when C-SCMMC absorbs reactive power, the amplitude of v_{armx_ac} will also decrease, and vice versa.

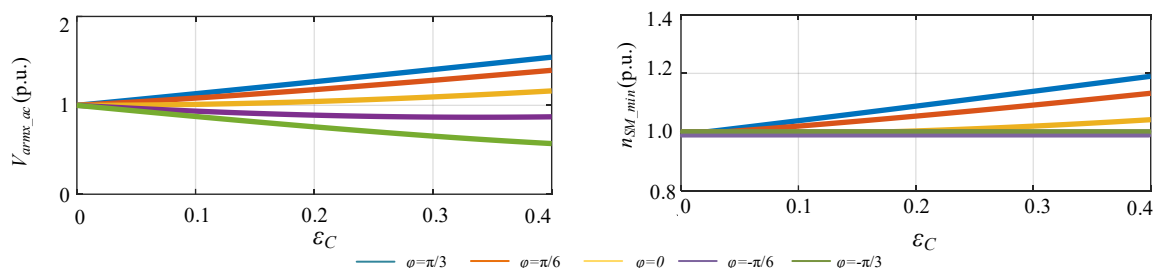


Figure 8. The change of v_{armx_ac} amplitude and n_{SM_min} with respect to φ and ε_C .

Furthermore, the arm output voltage range determines the necessary count of SMs in each arm. Ignoring the backup SMs, the necessary count of SMs can be calculated following:

$$n_{SM_min} = \frac{\max[2e_{dc}/3, (e_{dc}/3 + v_{armx_ac}) \cdot 1.1]}{v_{SM}^{ref}} \quad (36)$$

where n_{SM_min} denotes the minimum number of SMs in each arm; v_{SM}^{ref} represents the reference of the SM capacitor voltage.

Figure 8 illustrates the varying n_{SM_min} with various ε_C and φ when $\rho = 0.8$. When $\varphi \in (0, \pi)$, n_{SM_min} increases as ε_C increases. However, when $\varphi \in (-\pi, 0)$, $\varepsilon_C \in (0, 0.4)$, the reduced DC-blocking capacitor has a negligible influence on n_{SM_min} . Therefore, C-SCMMC is particularly suitable for operation with a unity power factor and reactive power absorption.

5.2. Influence on the Total Capacitive Energy Storage Capacity

According to Equation (23), C_{SM} should be enlarged to handle the larger energy fluctuation caused by higher ε_C . Therefore, the reduced DC-blocking capacitor will increase the SM capacitor. To evaluate the overall influence of the reduced DC-blocking capacitors, this paper utilizes the total energy storage capacity of the capacitors, a general criterion for the total capacitor cost, as the economic index. The total energy storage capacity can be calculated as follows for C-SCMMC:

$$W_{\Sigma} = W_{SM} + W_C \quad (37)$$

where

$$\begin{cases} W_{SM} = 3n_{SM}C_{SM}v_{SM}^2/2 \\ W_C = 3Cv_C^2/2 \end{cases} \quad (38)$$

W_{Σ} denotes the total energy storage capacity of all capacitors within C-SCMMC; W_{SM} and W_C represent the total energy storage capacities of the SM capacitor and the DC-blocking capacitor, respectively.

The quantified variations in W_{SM} and W_C with the changing ε_C are illustrated in Figure 9a. It can be observed, and also proved with the capacitance design formulas in Appendix A, that W_{SM} gently increases as ε_C increases, whereas W_C is inversely proportional to ε_C , which has a very sharp declining slope with ε_C lower than 0.05. Figure 9b further presents the curve of the W_{Σ} - ε_C relationship. W_{Σ} decreases drastically when ε_C increases from 0.0 to 0.1, and maintains a gradual decrease when $\varepsilon_C \in [0.1, 0.3]$, and finally enters the platform area where the change becomes marginal when $\varepsilon_C > 0.3$. Considering the economic cost and operation challenge with extremely large v_{Cx} ripples, the advised range of ε_C is from 0.1 to 0.3.

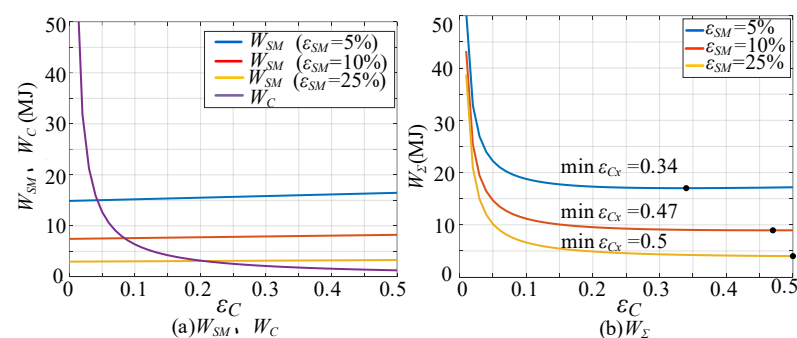


Figure 9. The change in W_{Σ} , W_{SM} , and W_C with respect to ε_{SM} and ε_C .

5.3. Case Study and Economic Comparison

This section employs a 220 kV AC/800 kV DC, 135 MVA converter station as a typical case to design the main circuit parameters of C-SCMMC. The hybrid-SCMMC is the most extensively investigated SCMMC family member, and the three-phase parallel MMC topology is widely applied in high-voltage projects. Therefore, this section compares the results with the hybrid-SCMMC and the conventional MMC parameters under the same

voltage and power capacity conditions. And ε_{SM} in each topology is set at 0.05 for a fair comparison, while ε_C is set at 0.10 and 0.25 to provide a clear demonstration of its influence. The results are presented in Table 1.

Table 1. Parameter comparison among C-SCMMC, HYBRID-SCMMC, and conventional MMC.

	C-SCMMC ($\varepsilon_C = 10\%$)	C-SCMMC ($\varepsilon_C = 25\%$)	Hybrid-SCMMC	Three-Phase Parallel MMC
number of arms	3	3	6	6
number of SMs in rela.to MMC	800 33.33%	812 33.83%	1000 41.67%	2400 100%
W_C [MJ] in rela.to MMC	6.37 Inf	2.55 Inf	1.20 Inf	0.00 100%
W_{SM} [MJ] in rela.to MMC	15.20 71.53%	15.68 73.79%	25.18 118.49%	21.25 100%
W_E [MJ] in rela.to MMC	21.57 102%	18.23 85%	26.38 124%	21.25 100%

As illustrated in Table 1, the three-phase parallel MMC requires the highest number of SMs, because the arm should withstand the whole DC voltage. In contrast, the series topologies utilize more arms to share the DC voltage, and each phase converter unit only handles one-third of the DC voltage. Therefore, the number of SMs in C-SCMMC is decreased by 67% in relative to MMC, which is also helpful to reduce the measurement, protection, and communication costs. The varying ε_C has a marginal influence on the SM capacitance of C-SCMMC, and the SM energy capacity of C-SCMMC is approximately two-thirds of MMC due to the reduced SM number, despite the fact that C-SCMMC has to employ larger capacitance in each individual SM to handle larger power fluctuation. The W_C varies a lot under different ε_C , and is the dominant factor that determines the energy capacity relationship between C-SCMMC and MMC. When $\varepsilon_C = 0.1$, their energy capacities approximately equal, and when $\varepsilon_C = 0.25$, the total energy storage capacity of C-SCMMC can be decreased by 15% in comparison to that of MMC. Compared with hybrid-SCMMC, the number of SMs and the total energy storage capacity in C-SCMMC are further reduced. In conclusion, C-SCMMC demonstrates a significant economic improvement compared to hybrid-SCMMC and conventional MMC in HVDC tapping scenarios.

To highlight the economic advantages of C-SCMMC, a quantitative comparison is provided. To simplify the calculations, the SM capacitor and DC-blocking capacitor are composed of many series- and parallel-connected capacitors (model: FFLK6NO267KJE, manufactured by KEMET, Greenville, SC, USA). For the semiconductor device, the IGBTs in C-SCMMC and the conventional MMC are respectively selected as FZ1200R45KL3_B5 (4.5 kV/1.2 kA) and FZ800R45KL3_B5 (4.5 kV/0.8 kA) from Infineon (headquartered in Neuburg, Germany) based on their nominal voltage and current. The results are presented in Table 2.

Table 2. Quantitative comparison among C-SCMMC, HYBRID-SCMMC, and conventional MMC.

Cost (Million USD)	C-SCMMC ($\varepsilon_C = 10\%$)	C-SCMMC ($\varepsilon_C = 25\%$)	Hybrid-SCMMC	Three-Phase Parallel MMC
unit SM capacitor cost	0.0115	0.0117	0.0150	0.0052
total SM capacitor cost in rela.to MMC	9.20 73.25%	9.50 75.64%	15.03 119.67%	12.56 100%
unit IGBT cost	0.0020	0.0020	0.0020	0.0018
total IGBT cost in rela.to MMC	3.17 35.98%	3.22 36.55%	3.97 45.06%	8.81 100%
unit DC-blocking capacitor cost	1.00	0.40	0.18	0.00
total DC-blocking capacitor cost in rela.to MMC	3.00 Inf	1.20 Inf	0.54 Inf	0.00 100%
overall cost in rela.to MMC	15.37 71.92%	13.92 65.14%	19.54 91.44%	21.37 100%

As illustrated in Table 2, the SM capacitor cost of C-SCMMC is approximately three-fourths of MMC due to the reduced SM number, despite the fact that C-SCMMC has larger SM capacitance and a higher unit cost. Among the compared topologies, the hybrid-SCMMC represents the most expensive option for SM capacitors due to its highest unit cost and greater quantity requirements. The unit IGBT costs in all topologies are relatively similar, and the number of IGBTs is the dominant factor that determines the total IGBT cost. Therefore, the total IGBT costs between hybrid-SCMMC and C-SCMMC have little difference, and the total IGBT cost of C-SCMMC can be decreased by 64% in comparison to that of MMC. Despite the additional cost of the DC-blocking capacitor, the C-SCMMC remains the most cost-effective, with its overall cost reduced by 35% compared to the conventional MMC.

6. Simulation Analysis

6.1. Simulation Parameters

Electromagnetic transient verification is conducted in the Matlab/Simulink environment based on the parameters listed in Table 3 to verify the accuracy of parameter design and the effectiveness of the control strategy for C-SCMMC. Specifically, four typical operation points are selected with the parameters presented in Table 4, and both steady-state and dynamic performances of C-SCMMC are analyzed.

Table 3. Bench mark parameters.

Parameter	Value	Parameter	Value
S_{VN}	135 MVA	DC voltage	800 kV
AC frequency	50 Hz	AC voltage	180 kV
SM number	267	Arm inductance	1 mH

Table 4. Operation points parameters.

Parameter	Value	Parameter	Value
Operation Point ①	$P = 135 \text{ MVA}, Q = 0, \varepsilon_C = 0.05$	Operation Point ②	$P = 135 \text{ MVA}, Q = 0, \varepsilon_C = 0.25$
Operation Point ③	$P = 0, Q = 135 \text{ MVA}, \varepsilon_C = 0.25$	Operation Point ④	$P, Q \text{ are mutated}, \varepsilon_C = 0.25$

6.2. Harmonic Current Suppression Simulation Result

Figures 10a and 11 show that without harmonic suppression, the DC-grid-tied current contains a significantly large 3rd-order harmonic component (Total Harmonic Distortion, THD = 10.26%) and the AC-grid-tied current exhibits 2nd- and 3rd-order harmonics (THD = 9.62%). According to Figures 10b and 11, after applying the harmonic current suppression method proposed in this paper, the THD values of i_{dc} and i_{acx} are effectively reduced to 1.3% and 0.6%, respectively.

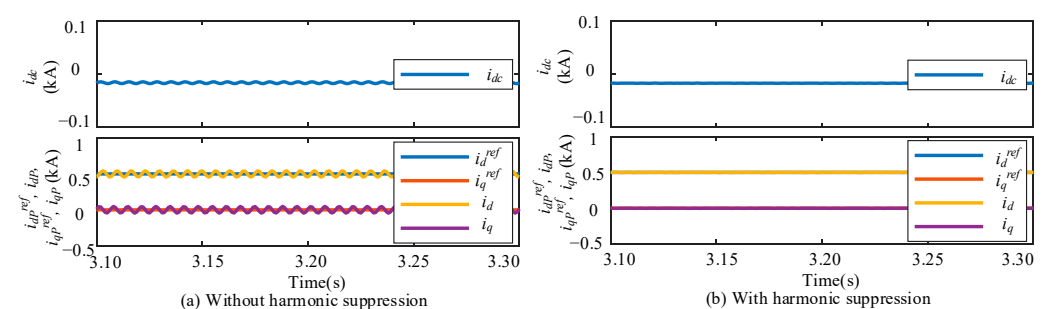


Figure 10. Harmonic suppression simulation results in Operation Point ①.

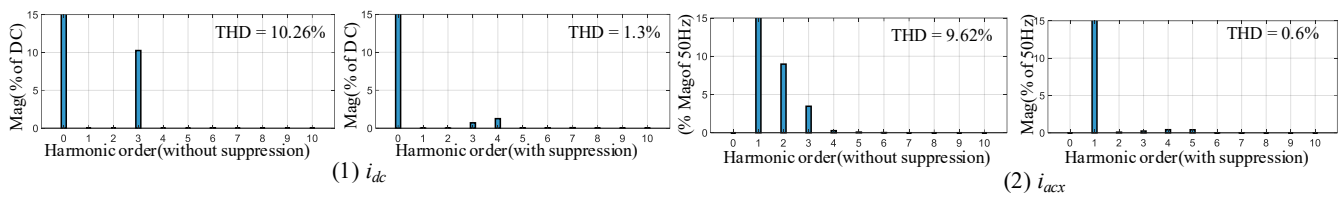


Figure 11. Spectrum of the DC and AC grid-tied current.

In conclusion, the validity and efficacy of ripple/harmonic coupling mechanism analysis and the proposed harmonic suppression strategy are well supported by the simulation results.

6.3. Steady-State and Dynamic Simulation Result

6.3.1. Operation Point ①

Figure 12 shows the waveforms at Operation Point ①. i_d , i_q and i_{dc} can consistently track their respective references, indicating that C-SCMMC can achieve precise control of active and reactive power. The voltage across the DC-blocking capacitor and the arm output voltage are both composed of a DC component of $e_{dc}/3$ and a fundamental-frequency component, which confirms the operation principle of C-SCMMC. Moreover, the phase of v_{Cx_ac} lags the corresponding grid phase voltage by 90° . This makes the AC component of the arm output voltage marginally higher than the grid voltage, which agrees with the conclusions presented in Section 5.

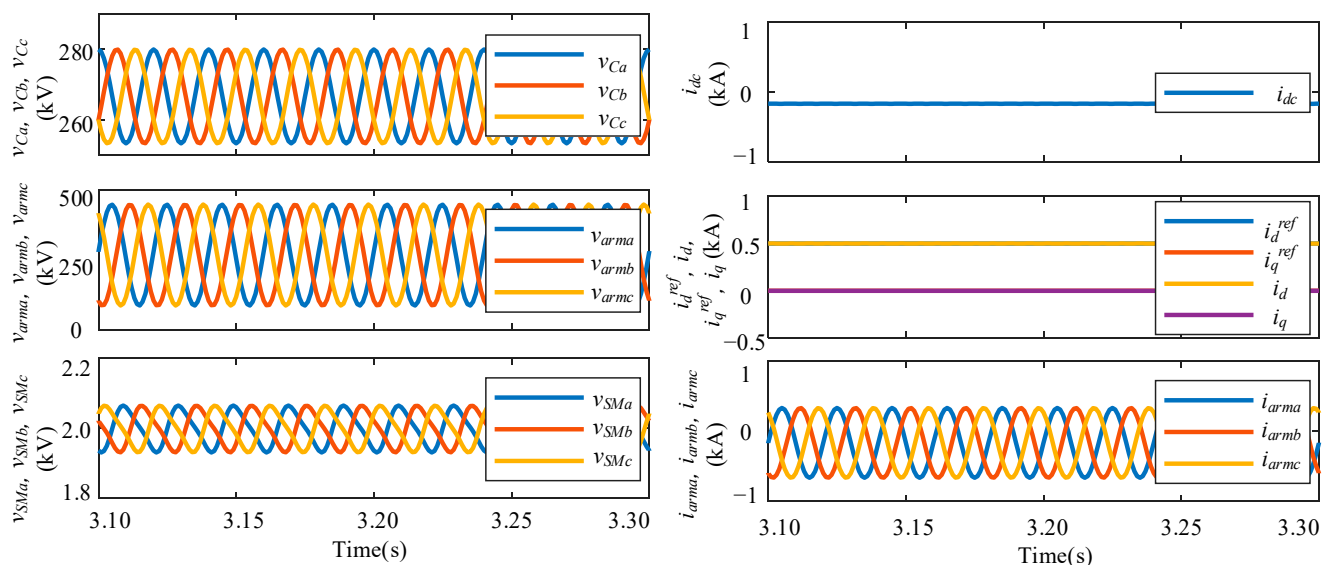


Figure 12. Steady-state simulation results in Operation Point ①.

The voltage fluctuations on the SM capacitor and the DC-blocking capacitor, respectively, remain from -3.65% to $+3.45\%$ and from -4.99% to $+4.94\%$, indicating that the C-SCMMC can maintain long-term steady operation, and its capacitances are appropriately designed.

6.3.2. Operation Point ②

The simulation waveforms of Operation Point ② are shown in Figure 13. It can be seen that C-SCMMC can still operate stably when ε_C increases to 0.25. Compared to Figure 12, v_{Cx_ac} rises from 13.275 kV to 67.3 kV, resulting in the amplitude of v_{armx_ac} increasing from 180.55 kV to 192.3 kV, which aligns with the previously discussed relationship between ε_C and v_{armx_ac} in Section 5.1. Simultaneously, the amplitude of power fluctuation in the SM has also slightly increased, and to maintain a constant voltage fluctuation across the capacitor in the SM, its capacitance must be augmented from 9.4 mF to 9.9 mF.

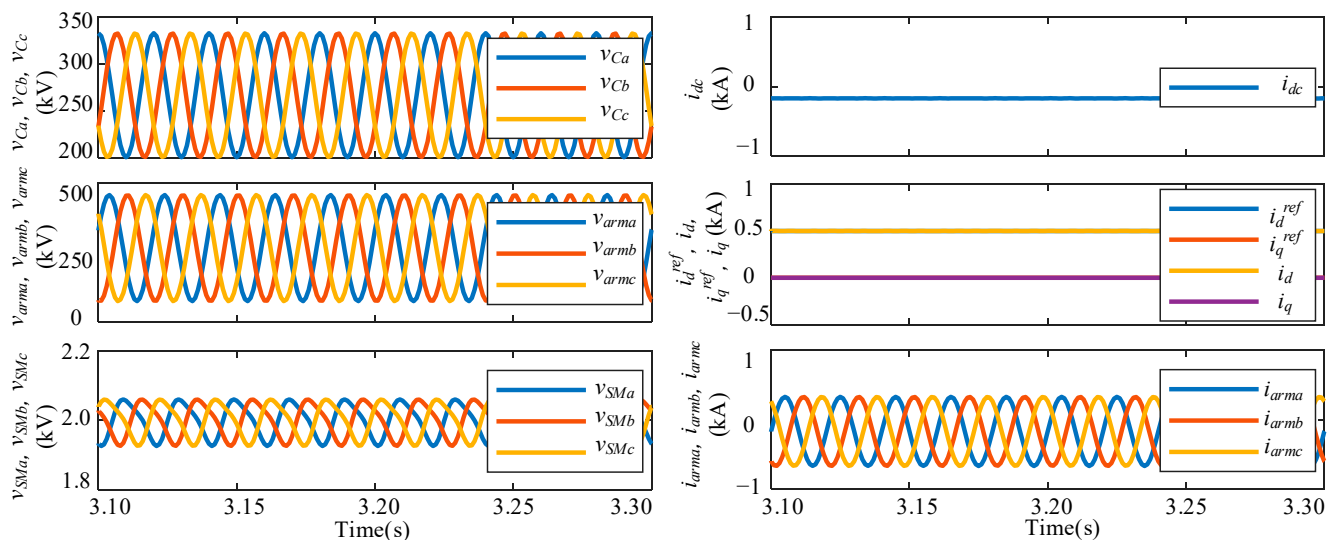


Figure 13. Steady-state simulation results in Operation Point ②.

6.3.3. Operation Point ③

The simulation waveforms for Operation Points ③ are presented in Figure 14. C-SCMMC can maintain stable operation under condition of full reactive power absorption. Compared to Figure 13, the SM capacitor voltage fluctuation has markedly increased, with an amplitude of approximately 100 V, representing a fluctuation of around 5%. This aligns with the design parameters for ε_{SM} . In Operation Point ③, v_{Cx_ac} is opposite to e_x in phase-angle, leading to a substantial decrease in v_{armx_ac} . Compared to Operation Point ②, the amplitude of v_{armx_ac} is reduced approximately from 192.3 kV to 113.7 kV. Therefore, C-SCMMC is more suitable for the reactive power absorption mode, where the arm output voltage amplitude is significantly lower.

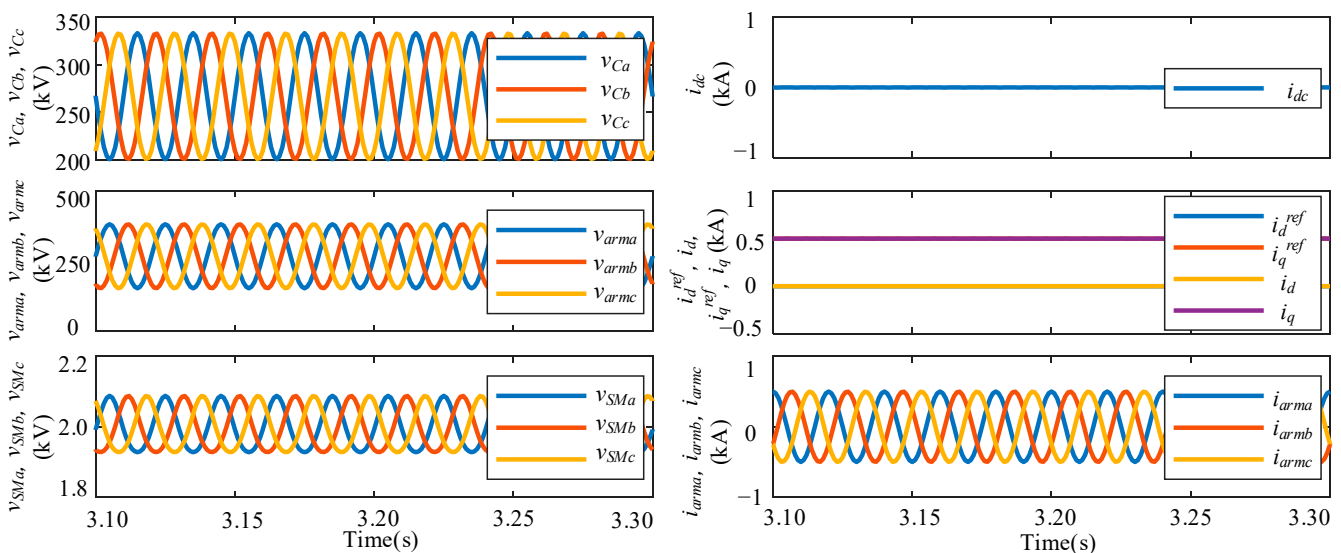


Figure 14. Steady-state simulation results in Operation Point ③.

6.3.4. Operation Point ④

Figure 15 illustrates the dynamic performance of the C-SCMMC. At $t = 3.6$ s, P and Q are step-changed from 400 MW and 300 MVA to 300 MW and 200 MVA, respectively. Notably, the tracking delay of i_d and i_q are within 0.05 s, demonstrating a high response speed. v_{Cx} and v_{SMx} have relatively longer responding delay of approximately 0.4 s. Overall, the dynamic response speed is sufficient for the general requirements of an HVDC converter station.

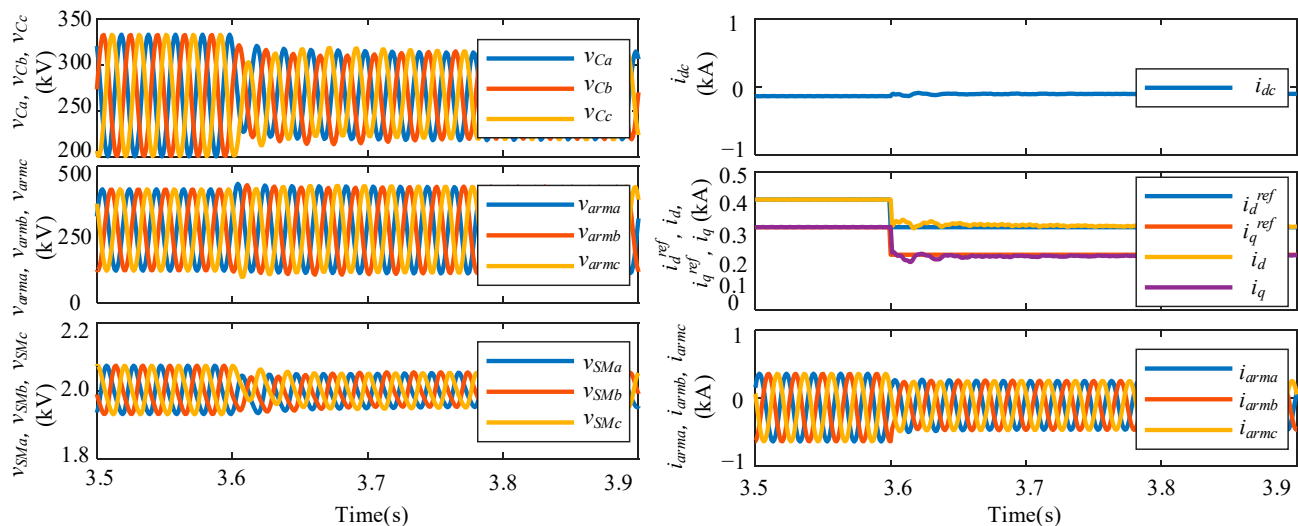


Figure 15. Dynamic simulation results in Operation Point ④.

Furthermore, Figure 16 presents dynamic performance comparisons among three control strategies: the capacitor voltage feedforward strategy (i_{d1}/i_{q1}), the cross dq -axis decoupling strategy (i_{d2}/i_{q2}), and the classic control strategy (i_{d3}/i_{q3}). Compared to the classic control strategy, the two strategies proposed in Section 4 achieve faster response speeds, with the capacitor voltage feedforward strategy exhibiting the most superior dynamic performance.

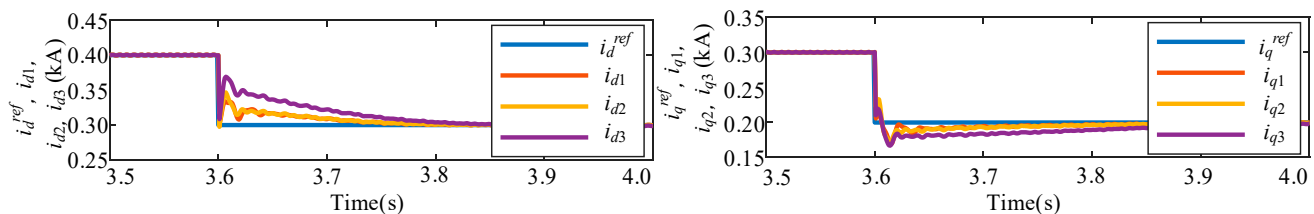


Figure 16. Dynamic simulation results comparison.

In conclusion, C-SCMMC is capable of flexible AC/DC power conversion with excellent steady-state and dynamic performance, and the validity and efficacy of the proposed parameter design method and control strategy are well supported by the simulation results.

7. Conclusions

The C-SCMMC with reduced DC-blocking capacitor is proposed in this paper for high-voltage low-power HVDC tapping applications. The principle, mathematical model, control, and parameter design are described and discussed in detail. The research conclusions are as follows:

- (1) Under normal operation, the C-SCMMC contains 2ω and 3ω harmonics on the AC-side, and 3ω harmonics on the DC side. These harmonic components can be well suppressed by introducing resonant terms in the current controllers, respectively.
- (2) By introducing the feedforward term of the DC-blocking capacitor voltage ripple in the current loop, the C-SCMMC can tolerate much higher DC-blocking capacitor voltage ripple compared with conventional cases, and therefore, the DC-blocking capacitance is much smaller.
- (3) The DC-blocking capacitor voltage ripple influences the arm voltage output voltage and SM capacitance selection. The advised range of its relative ripple amplitude is

from 0.1 to 0.3 at unity power factor, considering the overall cost. In the typical case, the C-SCMMC can reduce the capacitor energy storage capacity by 15%.

- (4) Considering the influence on the arm voltage output capability, the C-SCMMC is more suitable for operation with unity or lagging power factor, i.e., in the reactive power absorption mode.
- (5) The simulation results validate the circuit principle, control strategy and parameter design of the C-SCMMC, which also demonstrate its excellent steady-state and dynamic performance.

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Appendix A

The SM capacitor voltage fluctuation of the a -phase arm can be expressed as follows:

$$C_{SM} \frac{d}{dt} v_{SMa} = \left(\frac{3E_{ac}P}{2e_{dc}^2} - \frac{P}{3E_{ac}} + \frac{PQ}{\omega C E_{ac} e_{dc}^2} \right) \cos(\omega t) - \left(\frac{Q}{3E_{ac}} + \frac{P^2}{\omega C E_{ac} e_{dc}^2} \right) \sin(\omega t) - \left(\frac{P \cos^2 \varphi}{2e_{dc}} + \frac{2PQ}{3\omega C E_{ac}^2 e_{dc}} \right) \cos(2\omega t) + \left(\frac{P^2 - Q^2}{3\omega C E_{ac}^2 e_{dc}} + \frac{P \sin \varphi \cos \varphi}{2e_{dc}} \right) \sin(2\omega t) \quad (A1)$$

The detailed expressions of A_1 and A_2 are calculated following:

$$\begin{cases} A_1 = \frac{S}{\omega C_{SM}} \sqrt{\cos^2 \varphi \cdot \left(\frac{3E_{ac}}{2e_{dc}^2} - \frac{1}{3E_{ac}} - \frac{S \sin \varphi}{\omega C E_{ac} e_{dc}^2} \right)^2 + \left(-\frac{\sin \varphi}{3E_{ac}} + \frac{S \cos^2 \varphi}{\omega C E_{ac} e_{dc}^2} \right)^2} \\ A_2 = \frac{S}{\omega C_{SM}} \sqrt{\left(\frac{\cos \varphi}{4e_{dc}} + \frac{S \sin \varphi \cos \varphi}{3\omega C E_{ac}^2 e_{dc}} \right)^2 + \left(\frac{S \cos^2 \varphi - S \sin^2 \varphi}{6\omega C E_{ac}^2 e_{dc}} - \frac{\sin \varphi}{2e_{dc}} \right)^2} \end{cases} \quad (A2)$$

The detailed expressions of B_2 and B_3 are calculated following:

$$B_2 = \sqrt{\left(\frac{3NP^2}{2CC_{SM}e_{dc}^3\omega^2} + \frac{3NQ}{8C_{SM}e_{dc}\omega} - \frac{NS^2}{12CC_{SM}E_{ac}^2e_{dc}\omega^2} + \frac{NQ^2 - NP^2}{4CC_{SM}E_{ac}^2e_{dc}\omega^2} + \frac{NP^2Q}{C^2C_{SM}E_{ac}^3e_{dc}^3\omega^3} \right)^2 + \left(\frac{3NP}{8C_{SM}e_{dc}\omega} - \frac{9E_{ac}^2NP}{8C_{SM}e_{dc}^3\omega} + \frac{NP^3 - NPQ^2}{2C^2C_{SM}E_{ac}^3e_{dc}^3\omega^3} - \frac{3NPQ}{2CC_{SM}e_{dc}^3\omega^2} + \frac{NPQ}{2CC_{SM}E_{ac}^2e_{dc}\omega^2} \right)^2} \quad (A3)$$

$$B_3 = \sqrt{\left(\frac{NP^2 - NQ^2}{4CC_{SM}E_{ac}^2e_{dc}^2\omega^2} - \frac{3E_{ac}NQ}{16C_{SM}e_{dc}^2\omega} + \frac{3NP^2Q - NQ^3}{12C^2C_{SM}E_{ac}^3e_{dc}^3\omega^3} \right)^2 + \left(\frac{NP^3 - 3NPQ^2}{12C^2C_{SM}E_{ac}^3e_{dc}^3\omega^3} - \frac{3E_{ac}NP}{16C_{SM}e_{dc}^2\omega} - \frac{NPQ}{2CC_{SM}E_{ac}^2e_{dc}\omega^2} \right)^2} \quad (A4)$$

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