

Article

Design and Analysis of a Low-Power 30/60 GHz Dual-Band CMOS Voltage-Controlled Oscillator (VCO) Using B-to-GND-with- R_B Varactors

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Abstract

This paper presents a low-power 30/60 GHz dual-band CMOS voltage-controlled oscillator (VCO) for 5G applications. The design employs an LC-VCO core that simultaneously generates differential fundamental-frequency outputs and a single-ended second-harmonic output. To improve second-harmonic spectral purity, a second-harmonic quarter-wavelength ($\lambda/4$) transmission line is inserted in the V_{DD} bias path of the VCO core. A body-to-ground-with-resistor (B-to-GND-with- R_B) NMOS varactor configuration is adopted to provide a wide, monotonic tuning range while suppressing substrate leakage and noise coupling. In addition, a fundamental-frequency $\lambda/4$ transmission line is introduced in the control-voltage bias path to improve AC grounding of the differential varactor center node. The VCO consumes 2.19 mW and achieves a tuning range of 24.59–30.5 GHz (21.5%). At 27.48 GHz, it exhibits a phase noise of -117.69 dBc/Hz at a 10 MHz offset, corresponding to a figure of merit (FoM) of 189.72 dBc/Hz. The second-harmonic output covers 49.18–61 GHz, with the same fractional tuning range. The VCO core occupies a compact chip area of only 0.021 mm^2 .

Keywords: B-to-GND-with- R_B ; CMOS; dual band; low power; varactor; VCO

1. Introduction

A voltage-controlled oscillator (VCO)-based frequency synthesizer is a fundamental building block in modern transceiver systems, enabling frequency conversion between intermediate-frequency (IF) and radio-frequency (RF) signals. Key performance metrics of VCOs include low DC power consumption (P_{DC}), wide tuning range (TR) or fractional tuning range (FTR), and low phase noise (PN). Recently, several Ka- and V-band CMOS VCOs have been reported [1–7]; however, their performance still leaves room for improvement. For example, the VCO reported in [1], which was implemented in 22 nm fully depleted silicon-on-insulator (FDSOI) CMOS technology and designed to achieve low phase noise, operates over a fundamental frequency range of 27.67–30.12 GHz. The second-harmonic output is extracted from the tail of the cross-coupled pair using a transformer and a dedicated buffer amplifier. This design consumes 31.2 mW of DC power, achieves a relatively narrow FTR of 8.5%, and exhibits a phase noise of -119.11 dBc/Hz at a 10 MHz offset. The high power consumption and limited tuning range are mainly attributed to the large bias current under a 0.8 V supply and significant parasitic capacitances. In [3], a 37.2–42 GHz VCO fabricated in 22 nm FDSOI CMOS employs reversed varactors to achieve a constant tuning slope, thereby minimizing frequency-modulated continuous-wave (FMCW) chirp



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error. This design consumes 17.4 mW, achieves an FTR of 12.1%, and exhibits a phase noise of -117 dBc/Hz at a 10 MHz offset. The relatively high power consumption and limited tuning capability are primarily due to the high supply voltage (1.6 V) and large parasitic capacitance. In [4], a 33.6–35.9 GHz class-D VCO implemented in 65 nm CMOS utilizes a tail current source to stabilize the operating current against process, voltage, and temperature (PVT) variations, as well as supply noise. Although it achieves low power consumption (1.7 mW), it exhibits a limited FTR of 6.6%, mainly due to inherent parasitic capacitances.

This work presents a low-power 30/60 GHz dual-band CMOS VCO for 5G applications. A quarter-wavelength ($\lambda/4$) transmission line (TL), designed for a second-harmonic frequency of 56 GHz and terminated with an AC ground, is incorporated into the V_{DD} bias path of the LC-VCO core to enhance the spectral purity of the second-harmonic output. For the NMOS varactors, a body-to-ground-with- R_B (B-to-GND-with- R_B) topology is adopted instead of the conventional body-to-source (B-to-S) configuration. The body is connected to ground through a large floating resistor ($R_B = 2.17$ k Ω), enabling a monotonic and wide capacitance tuning range while suppressing substrate leakage and noise coupling. As a result, the proposed VCO achieves an enhanced tuning range. The remainder of this paper is organized as follows. Section 2 describes the VCO architecture. Section 3 presents the circuit design. Section 4 provides measurement results and comparisons with prior work. Section 5 concludes the paper.

2. VCO Architecture

Figure 1 illustrates the proposed low-power 30/60 GHz dual-band CMOS VCO and its key design features. The VCO consists of an LC-VCO core with differential fundamental outputs (f_0+ and f_0-), a single-ended second-harmonic output ($2f_0$), and two fundamental buffer amplifiers that minimize loading effects. To enhance the spectral purity of the second-harmonic output, a quarter-wavelength ($\lambda/4$) transmission line (TL) with an AC-grounded termination is incorporated into the V_{DD} bias path of the LC-VCO core. For the NMOS varactors, a body-to-ground-with- R_B (B-to-GND-with- R_B) topology is employed instead of the conventional body-to-source (B-to-S) configuration. In this topology, the body terminal is connected to ground through a large AC-floating resistor (R_B), providing a monotonic and wide capacitance tuning range while suppressing substrate leakage and noise coupling. Furthermore, an additional $\lambda/4$ TL, implemented in a spiral layout and operating at the fundamental frequency, is inserted into the control-voltage (V_{ctrl}) bias path to improve AC grounding at the center node of the differential varactor.

Figure 2a presents the circuit diagram of the proposed B-to-D-with- R_B varactor. It consists of five pairs of NMOS varactors employing the B-to-D-with- R_B topology, along with a $\lambda/4$ TL (designed for the fundamental frequency) with a good AC-grounded termination in the V_{ctrl} bias path. This configuration enhances AC grounding at the center node of the differential NMOS varactors, particularly in the presence of varactor asymmetry. This is because the input impedance of the $\lambda/4$ transmission line is approximately open-circuited at the operating frequency, resulting in negligible loading on the varactors.

The equivalent input impedance ($Z_{in,var}$) of an NMOS-based varactor can be expressed as:

$$Z_{in,var} \approx R_{s,var} + \frac{1}{j\omega C_{var}} \quad (1)$$

where $R_{s,var}$ and C_{var} denote the equivalent series resistance and equivalent capacitance, respectively. The thermal noise power contributed by the varactor to the LC tank is given by

$$V_n^2 = 4kTR_{s,var}\Delta f \quad (2)$$

where V_n is the root-mean-square (RMS) noise voltage and Δf is the noise bandwidth used in the simulation or measurement. As indicated by (2), reducing $R_{s,var}$ lowers the thermal noise contribution of the varactor, motivating the development of an NMOS-based varactor topology with a smaller equivalent series resistance.

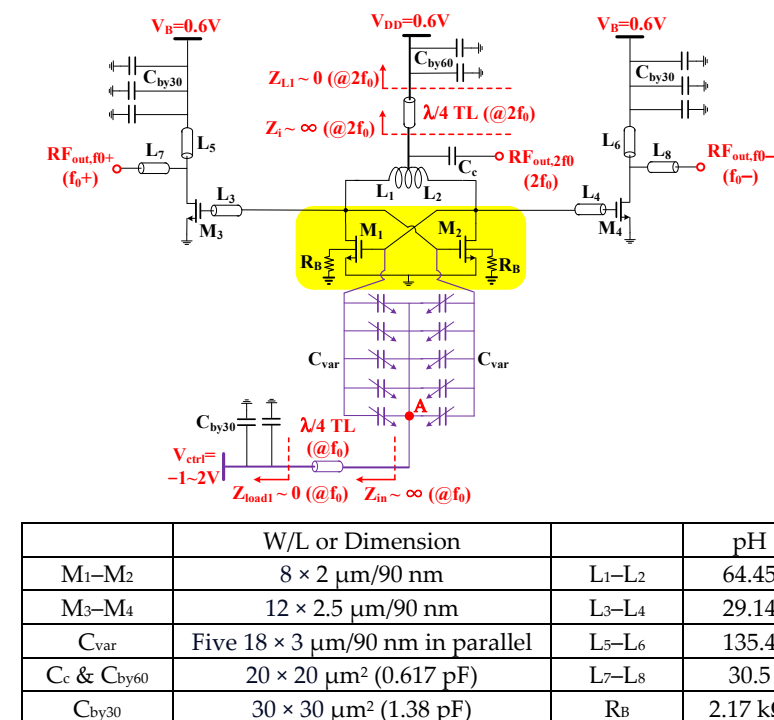


Figure 1. Circuit diagram of the proposed VCO, with key device parameters indicated.

Figure 2b shows the simulated equivalent capacitance (C_{var}) versus V_{ctrl} for the proposed B-to-GND-with- R_B varactor ($R_B = 2.17 \text{ k}\Omega$). For comparison, the simulated C_{var} characteristics of the B-to-GND varactor ($R_B = 0$) and the conventional B-to-S varactor are also included. In the conventional B-to-S topology, the capacitance tuning range is limited by the non-monotonic dependence of C_{var} on V_{ctrl} . This behavior occurs because the varactor enters the accumulation region at high V_{ctrl} values (1–3 V), where $V_{\text{GD}} = V_{\text{GS}} = -0.4$ to -2.4 V and $V_{\text{BS}} = V_{\text{BD}} = 0 \text{ V}$ for $V_{\text{DD}} = 0.6 \text{ V}$. In contrast, the proposed B-to-GND-with- R_B topology maintains in the depletion region over the same V_{ctrl} range. Under these conditions, $V_{\text{GD}} = V_{\text{GS}} = -0.4$ to -2.4 V and $V_{\text{BS}} = V_{\text{BD}} = -1$ to -3 V , indicating that the body-to-source/drain junctions remain reverse-biased. As a result, the channel remains depleted, yielding a monotonic capacitance response and a wide tuning range of 205.9–397.9 fF. Furthermore, this tuning range is slightly larger than that of the B-to-GND topology (207.4–397.9 fF). This improvement is attributed to the inclusion of R_B , which behaves as a DC short circuit due to its negligible voltage drop while acting as an AC open circuit because of its high impedance at 30 GHz. Consequently, substrate leakage and noise coupling are suppressed at high V_{ctrl} .

Figure 2c shows the simulated equivalent series resistance (R_s) as a function of V_{ctrl} for the proposed B-to-GND-with- R_B varactor, the B-to-GND varactor, and the conventional B-to-S varactor. The proposed topology achieves the lowest R_s , ranging from 2.64 to 3.46 Ω , compared with 2.64–3.59 Ω for the B-to-GND topology and 2.64–4.22 Ω for the conventional B-to-S topology. The reduction in R_s is likewise attributed to the presence of R_B , which suppresses substrate leakage and substrate coupling while maintaining AC isolation across the 30 GHz operation frequency band. Overall, as indicated by (1) and (2), the proposed B-to-GND-with- R_B varactor is the most suitable choice for VCO applications because it

simultaneously provides the lowest thermal-noise contribution and the widest capacitance tuning range.

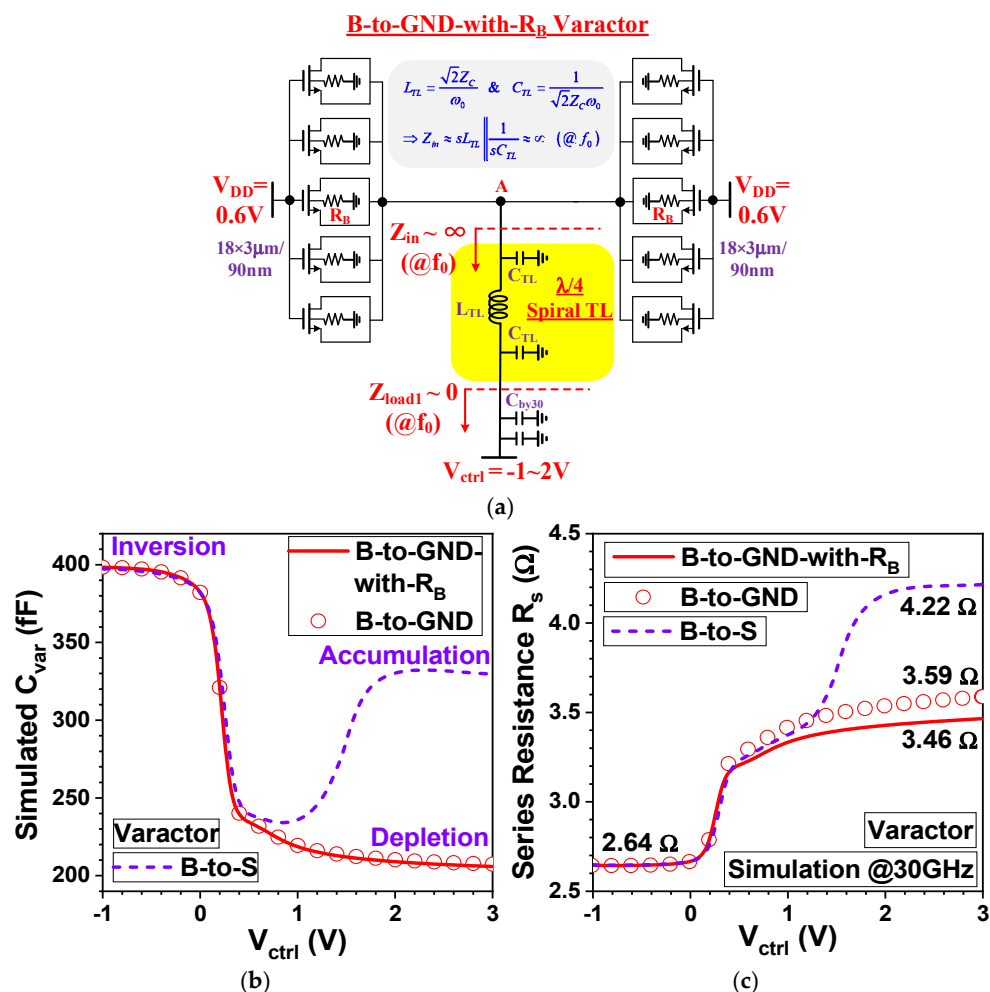


Figure 2. (a) Circuit diagram and simulated (b) equivalent capacitance (C_{var}) and (c) equivalent series resistance (R_s) as a function of V_{ctrl} for the proposed B-to-GND-with- R_B varactor.

Due to the non-negligible equivalent impedance of the V_{DD} and V_{ctrl} pads across the frequency band of interest, bypass capacitors are required to properly define the effective transmission-line length of the bias network and improve simulation accuracy. Z_{load1} denotes the equivalent load impedance at the terminal of the fundamental frequency $\lambda/4$ transmission line, which includes two parallel MIM bypass capacitors (each with dimension of $30 \times 30 \mu\text{m}^2$). Z_{in} represents the input impedance at the input of the fundamental frequency $\lambda/4$ transmission line. Figure 3a shows the simulated real and imaginary components of Z_{load1} ($\text{Re}(Z_{load1})$ and $\text{Im}(Z_{load1})$) as functions of frequency. As observed, $\text{Re}(Z_{load1})$ is approximately 0.314Ω around 30 GHz, while $\text{Im}(Z_{load1})$ approaches zero near 32.8 GHz, indicating that Z_{load1} effectively behaves as an AC ground over the 24.5–30.5 GHz fundamental frequency band of interest. Figure 3b shows the simulated magnitude of Z_{in} (i.e., $|Z_{in}|$) versus frequency. The magnitude $|Z_{in}|$ exceeds 500Ω over the 24.9–30.6 GHz range, indicating that Z_{in} effectively behaves as an AC open over the corresponding fundamental frequency band.

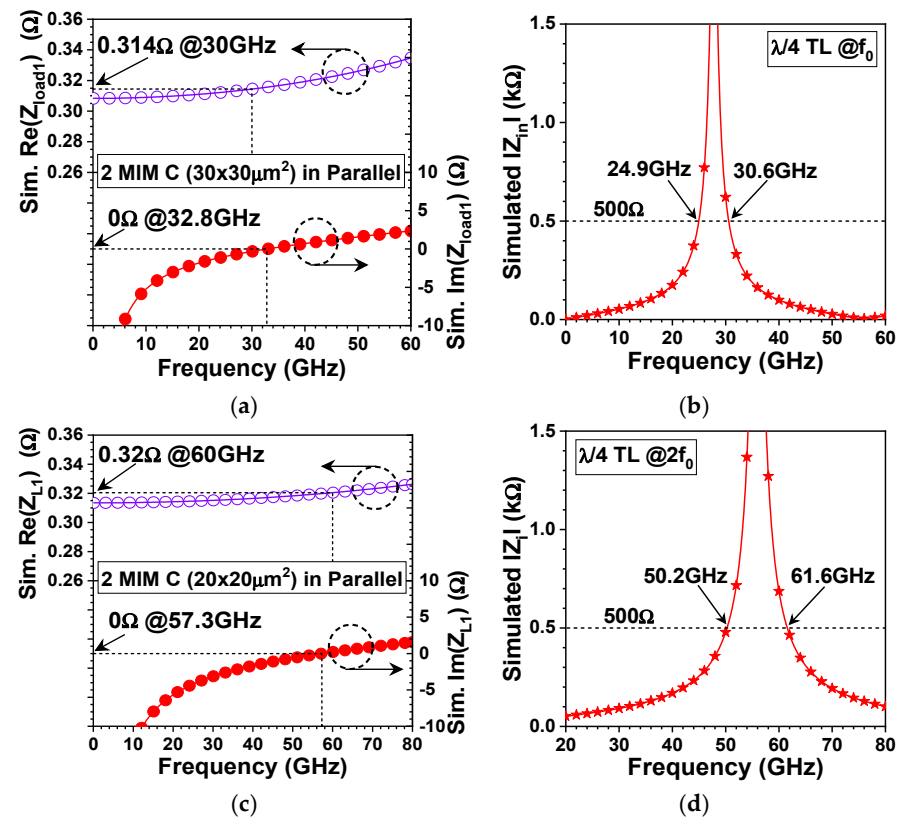


Figure 3. Simulated (a) $\text{Re}(Z_{\text{load1}})$ and $\text{Im}(Z_{\text{load1}})$, (b) magnitude of Z_{in} , (c) $\text{Re}(Z_{L1})$ and $\text{Im}(Z_{L1})$, and (d) magnitude of Z_i as functions of frequency.

Z_{L1} represents the load impedance at the terminal of the second-harmonic $\lambda/4$ transmission line, which includes two parallel MIM bypass capacitors (each with dimensions of $20 \times 20 \mu\text{m}^2$). Z_i represents the input impedance at the input of the second-harmonic $\lambda/4$ transmission line. Figure 3c shows the simulated $\text{Re}(Z_{L1})$ and $\text{Im}(Z_{L1})$ as functions of frequency. $\text{Re}(Z_{L1})$ is approximately 0.32 Ω near 60 GHz, while $\text{Im}(Z_{L1})$ approaches zero around 57.3 GHz, confirming effective AC-ground behavior across the 49–61 GHz second-harmonic frequency. $\text{Re}(Z_{L1})$ is approximately 0.32 Ω near 60 GHz, while $\text{Im}(Z_{L1})$ approaches zero around 57.3 GHz, confirming effective AC-ground behavior across the 49–61 GHz second-harmonic frequency band of interest. Figure 3d shows the simulated magnitude of Z_i (i.e., $|Z_i|$) versus frequency. The magnitude $|Z_i|$ exceeds 500 Ω over the 50.2–61.6 GHz range, indicating that Z_i effectively behaves as an AC open over the corresponding second-harmonic frequency band.

3. VCO Design

To ensure cost competitiveness, a 90 nm CMOS technology provided by a commercial foundry is adopted. The interconnection lines (ILs), inductors, and $\lambda/4$ transmission lines (TLs) are implemented on the 3.4 μm -thick top metal layer (MT₉) to minimize resistive loss. The bottom metal layer (MT₁), with a patterned density of 70%, serves as the ground plane for the ILs, inductors, and TLs. The vertical distance (D) between MT₉ and MT₁ is 6.06 μm . To prevent performance degradation, the spacing between adjacent ILs, inductors, and TLs is maintained at no less than five times D (i.e., 30.3 μm), thereby reducing mutual coupling and parasitic effects [8–11]. For example, the minimum spacing between the 28 GHz spiral $\lambda/4$ TLs (with dimensions of $67 \times 67 \mu\text{m}^2$) and adjacent conductors is 70.7 μm , while that for the 56 GHz $\lambda/4$ TLs is 127.1 μm . As a result, electromagnetic

cross-coupling and quality-factor degradation are sufficiently small and can be accurately accounted for in post-layout electromagnetic simulations.

A standard RF NMOS transistor with a threshold voltage (V_{th}) of 0.2 V is employed in the VCO design. The device exhibits a maximum oscillation frequency (f_{max}) of 150.7 GHz and a current-gain cutoff frequency (f_T) of 122.5 GHz, which are sufficient for multi-Gb/s-data-rate millimeter-wave transceiver [12] with integrated baseband circuit [13], as well as millimeter-wave transceiver array for multi-user multiple-input-multiple-output (MU-MIMO) wireless communication [14]. Therefore, the adopted 90 nm CMOS technology is also suitable for 5G millimeter-wave transceiver front-end applications.

For the LC-tank VCO shown in Figure 1, the impedance (Z_{cct}) seen looking into the cross-coupled transistors M_1 and M_2 is given by

$$Z_{cct} \approx \left(-\frac{2}{g_m} \right) \parallel \left(\frac{2}{s(C_{gs} + C_{ds})} \right) \equiv R_{nr} \parallel \frac{2}{sC_{par}} \quad (3)$$

where R_{nr} ($= -2/g_m$) represents the equivalent parallel negative resistance and is typically designed to be two to three times larger than the parallel resistance of the LC tank to ensure reliable start-up and sustained oscillation. C_{par} ($= C_{gs} + C_{gd}$) denotes the equivalent.

Single-ended parasitic capacitance. In addition, g_m is the transistor transconductance, which can be expressed as [15]:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th}) \quad (4)$$

Moreover, the fundamental oscillation frequency (f_0), theoretical tuning bandwidth (Δf_0), center oscillation frequency ($f_{0,c}$), and fractional tuning range (FTR) of the VCO are given by

$$f_0 = \frac{1}{2\pi \sqrt{(C_{par} + C_{var}) L_{eff}}} \quad (5)$$

$$\Delta f_0 = \frac{1}{2\pi \sqrt{(C_{par} + C_{var,min}) L_{eff}}} - \frac{1}{2\pi \sqrt{(C_{par} + C_{var,max}) L_{eff}}} \quad (6)$$

$$f_{0,c} = \frac{\frac{1}{2\pi \sqrt{(C_{par} + C_{var,min}) L_{eff}}} + \frac{1}{2\pi \sqrt{(C_{par} + C_{var,max}) L_{eff}}}}{2} \quad (7)$$

$$FTR = \frac{\Delta f_0}{f_{0,c}} = 2 \frac{\sqrt{\frac{C_{par} + C_{var,max}}{C_{par} + C_{var,min}}} - 1}{\sqrt{\frac{C_{par} + C_{var,max}}{C_{par} + C_{var,min}}} + 1} \quad (8)$$

where L_{eff} is the equivalent single-ended inductance and C_{var} is the single-ended variable capacitance. According to (6), the dominant factors determining the theoretical tuning bandwidth are the equivalent single-ended parasitic capacitance C_{par} ($= C_{gs} + C_{gd}$), the minimum and maximum single-ended variable capacitances $C_{var,min}$ and $C_{var,max}$, and the equivalent single-ended inductance L_{eff} . As indicated by (8), for a fixed L_{eff} , the tuning bandwidth is mainly governed by the ratio of the maximum to minimum total tank capacitance. Therefore, any inaccuracy in estimating C_{par} , $C_{var,min}$, or $C_{var,max}$ may lead to discrepancies between theoretical and simulated results. In this design, $L_{eff} = 81$ pH, $C_{par} = 125$ fF, and $C_{var} = 205.9$ – 397.9 fF (i.e., $C_{var,min} = 205.9$ fF and $C_{var,max} = 397.9$ fF). These values yield a calculated tuning bandwidth of 6.29 GHz (24.45–30.74 GHz), corresponding to an FTR of 22.8%.

For more advanced CMOS technologies (e.g., 65 nm to 22 nm nodes reported in [1–7]), a smaller transistor gate width (W) is required to achieve the same R_{nr} because the gate length (L) is reduced, as indicated by (3) and (4). Consequently, the parasitic capacitance C_{par} decreases. For a fixed $f_{0,c}$ and L_{eff} , the reduction in C_{par} allows a larger C_{var} and a wider capacitance tuning range to be utilized, as indicated by (5)–(8). As a result, a wider frequency tuning range can be achieved. In summary, further performance enhancement is expected when the VCO is implemented using more advanced CMOS technologies.

Figure 4a illustrates the simulated fundamental oscillation frequency (f_0) and single-ended output power (P_{out}) of the VCO as functions of V_{ctrl} . As V_{ctrl} varies from -1 to 2 V, the VCO achieves a tuning range of 6.2 GHz (24.47–30.67 GHz), corresponding to a fractional tuning range of 22.5%, which agrees well with the calculated tuning range of 6.29 GHz and FTR of 22.8% predicted by (3)–(6). The increase in f_0 with V_{ctrl} is attributed to a reduction in C_{var} , i.e., specifically the body–source (C_{BS}) and body–drain (C_{BD}) junction capacitances, resulting from enhanced depletion between the source/drain and the channel/body. Over the same V_{ctrl} range, the simulated P_{out} varies from -6.9 to -1.6 dBm. Figure 4b shows the simulated phase noise at the fundamental frequency, ranging from -113.6 to -117.1 dBc/Hz at a 10 MHz offset from f_0 .

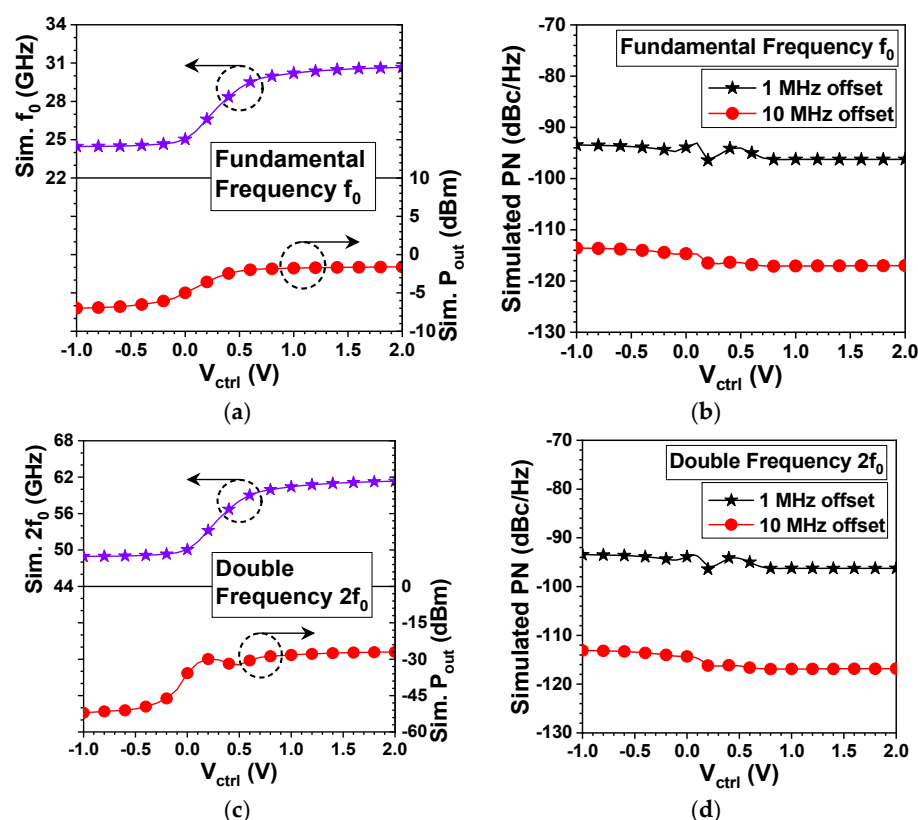


Figure 4. Simulated fundamental (a) oscillation frequency (f_0) and single-ended output power (P_{out}), and (b) phase noise; and simulated second-harmonic (c) oscillation frequency ($2f_0$) and P_{out} , and (d) phase noise of the proposed VCO.

Figure 4c presents the simulated second-harmonic oscillation frequency ($2f_0$) and single-ended output power (P_{out}) as functions of V_{ctrl} . As V_{ctrl} varies from -1 to 2 V, the VCO achieves a tuning range of 12.5 GHz (48.84–61.34 GHz), corresponding to a fractional tuning range of 22.5%. The corresponding P_{out} ranges from -52 to -27 dBm. Figure 4d shows the simulated phase noise at the second-harmonic, which ranges from -113.1 to -116.9 dBc/Hz at a 10 MHz offset from $2f_0$.

4. Measurement Results and Discussions

Figure 5 shows the chip micrograph of the VCO. The VCO core occupies a compact chip area of only $0.076 \times 0.272 \text{ mm}^2$ (0.021 mm^2). It draws a bias current of 3.65 mA from a 0.6 V supply, resulting in a power consumption of 2.19 mW. A Keysight 6629A system DC power supplies (four outputs, 0–50 V voltage range, and 0–1 A current capability) are used for DC biasing. The phase noise, output spectrum, and time-domain waveforms are measured using a Keysight N9041B UXA signal analyzer (2 Hz–110 GHz) and a Keysight DSOX3034A digital storage oscilloscope (four channels, 350 MHz bandwidth, and 4 GS/s sampling rate). De-embedding of the measurement pads was not performed because the RF pad structures were incorporated into both the design and simulation environments. Their parasitic effects were therefore included during circuit optimization and are considered an integral part of the implemented VCO. Accordingly, the reported measurement results represent the complete fabricated circuit, including the RF pads.

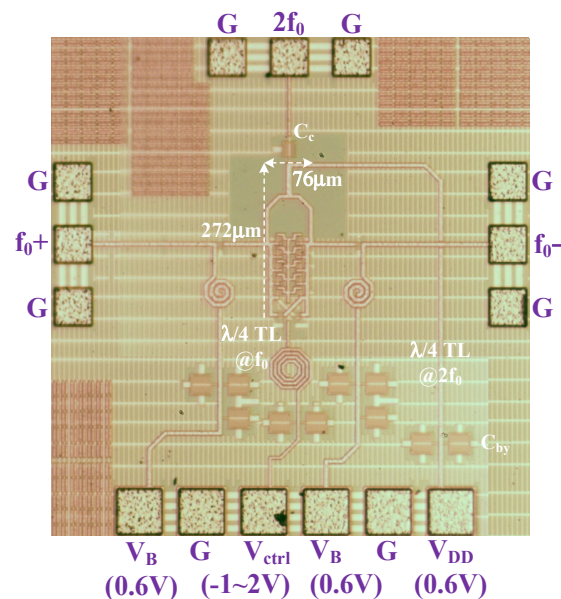


Figure 5. Chip micrograph of the proposed VCO.

Figure 6a shows the measured output spectrum for a 30 GHz input signal with an input power of 0 dBm, where the corresponding cable loss is 6.51 dB. Figure 6b shows the measured output spectrum for a 60 GHz input signal with an input power of 0 dBm, where the corresponding cable loss is 10.82 dB. Figure 6c plots the measured cable loss versus frequency, showing a variation from 6.15 to 6.51 dB over the 26–30 GHz range. Figure 6d plots the measured cable loss versus frequency, showing a variation from 9.8 to 11.67 dB over the 51–60 GHz range.

Figure 7a shows the measured and simulated fundamental oscillation frequency (f_0) as a function of control voltage (V_{ctrl}) for the proposed VCO. The measured results are in good agreement with the simulations. As V_{ctrl} varies from -1 to 2 V, the VCO achieves a measured f_0 tuning range of 5.91 GHz (24.59–30.50 GHz), corresponding to a fractional tuning range of 21.5%, which is close to the simulated tuning range of 6.20 GHz (24.47–30.67 GHz) and a fractional tuning range of 22.5%. However, the measured maximum VCO gain (K_{VCO}) is 5.8 GHz/V, which is noticeably lower than the simulated value of 8 GHz/V. The discrepancy between the simulated and measured VCO performance is primarily attributed to the following factor.

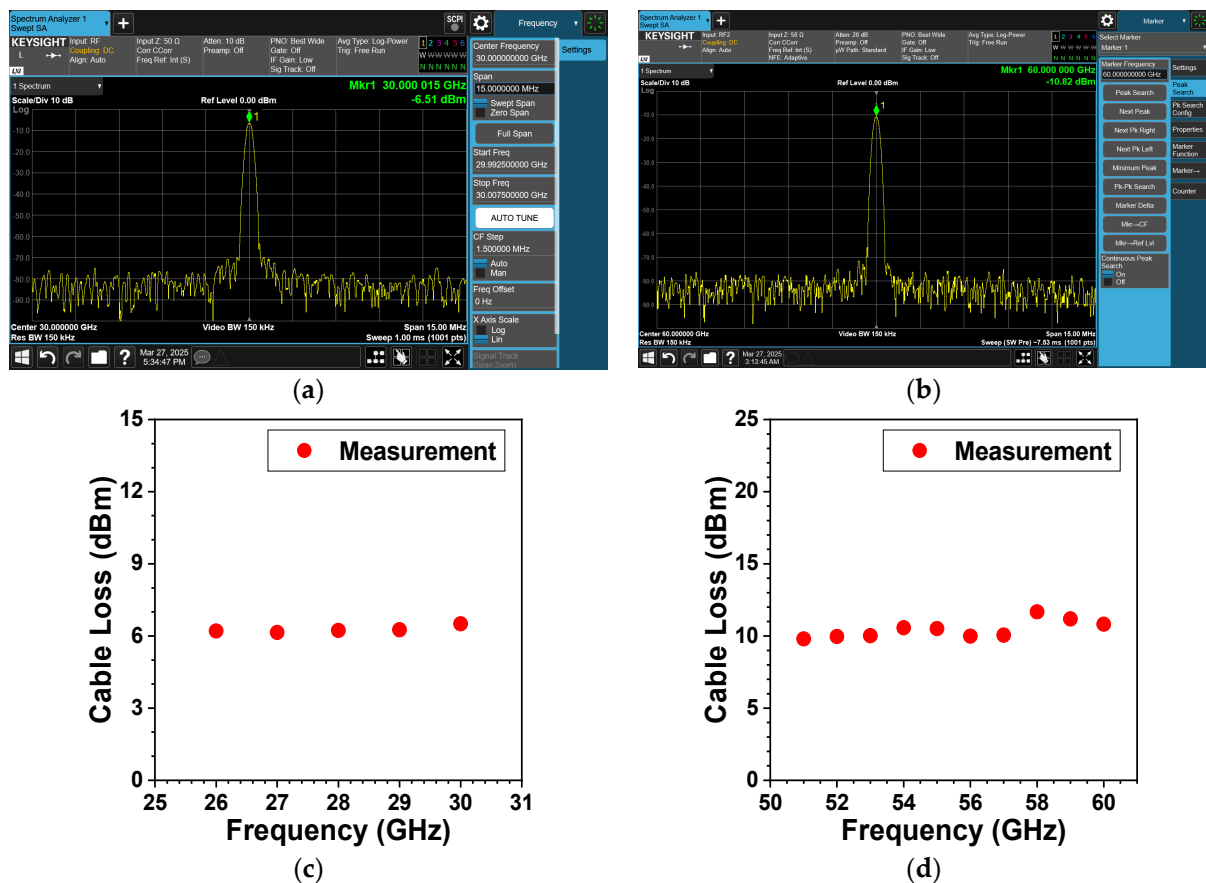


Figure 6. Measured output spectra for (a) a 30 GHz input signal and (b) a 60 GHz input signal at an input power of 0 dBm, and cable losses versus frequency at (c) the 30 GHz band and (d) the 60 GHz band.

From (5), C_{var} can be expressed as:

$$C_{var} = \frac{1}{4\pi^2 f_0^2 L_{eff}} - C_{par} \quad (9)$$

Equation (9) shows that C_{var} is a function of f_0 , L_{eff} , and C_{par} . Figure 7b presents the extracted C_{var} – V_{ctrl} characteristics obtained from the measured and simulated frequency responses in Figure 7a, assuming $L_{eff} = 81$ pH and $C_{par} = 125$ fF, where these values are determined from EM simulation, transistor models, and layout extraction. The extracted measured C_{var} ranges from 211.2 fF to 392.0 fF, while the simulated range is 207.1 fF to 397.5 fF. This close agreement between these capacitance ranges indicates that the total tank capacitance, including the extracted fixed parasitic capacitance, is accurately captured. Therefore, a substantial underestimation of C_{par} is unlikely to be the primary cause of the K_{VCO} discrepancy. Furthermore, if the measured reduction in K_{VCO} were mainly caused by an underestimated C_{par} , a corresponding shift in the overall tuning range would also be expected. However, the measured tuning range is 5.91 GHz, which agrees well with the simulated value of 6.2 GHz (4.7% difference). In contrast, the maximum slope of the extracted measured C_{var} – V_{ctrl} curve is 180.1 fF/V, compared with 242.4 fF/V in simulation, representing a 25.7% reduction. This reduction closely matches the observed 27.5% decrease in K_{VCO} (5.8 GHz/V measured versus 8.0 GHz/V simulated). These results indicate that the discrepancy originates primarily from a reduction in the local capacitance sensitivity (dC_{var}/dV_{ctrl}) of the varactor rather than from an error in the extracted fixed parasitic capacitance. Therefore, the additional analysis suggests that the measured K_{VCO}

degradation is predominantly associated with a lower-than-predicted varactor capacitance sensitivity under actual operating conditions. While extraction inaccuracies can never be completely excluded, the close agreement in both the extracted capacitance range and the overall tuning range indicates that any residual error in C_{par} is secondary and cannot account for the majority of the observed K_{VCO} reduction. Possible contributors include limitations of the varactor model under large-signal RF operation and process-induced variations affecting the $C_{\text{var}}-V_{\text{ctrl}}$ characteristic.

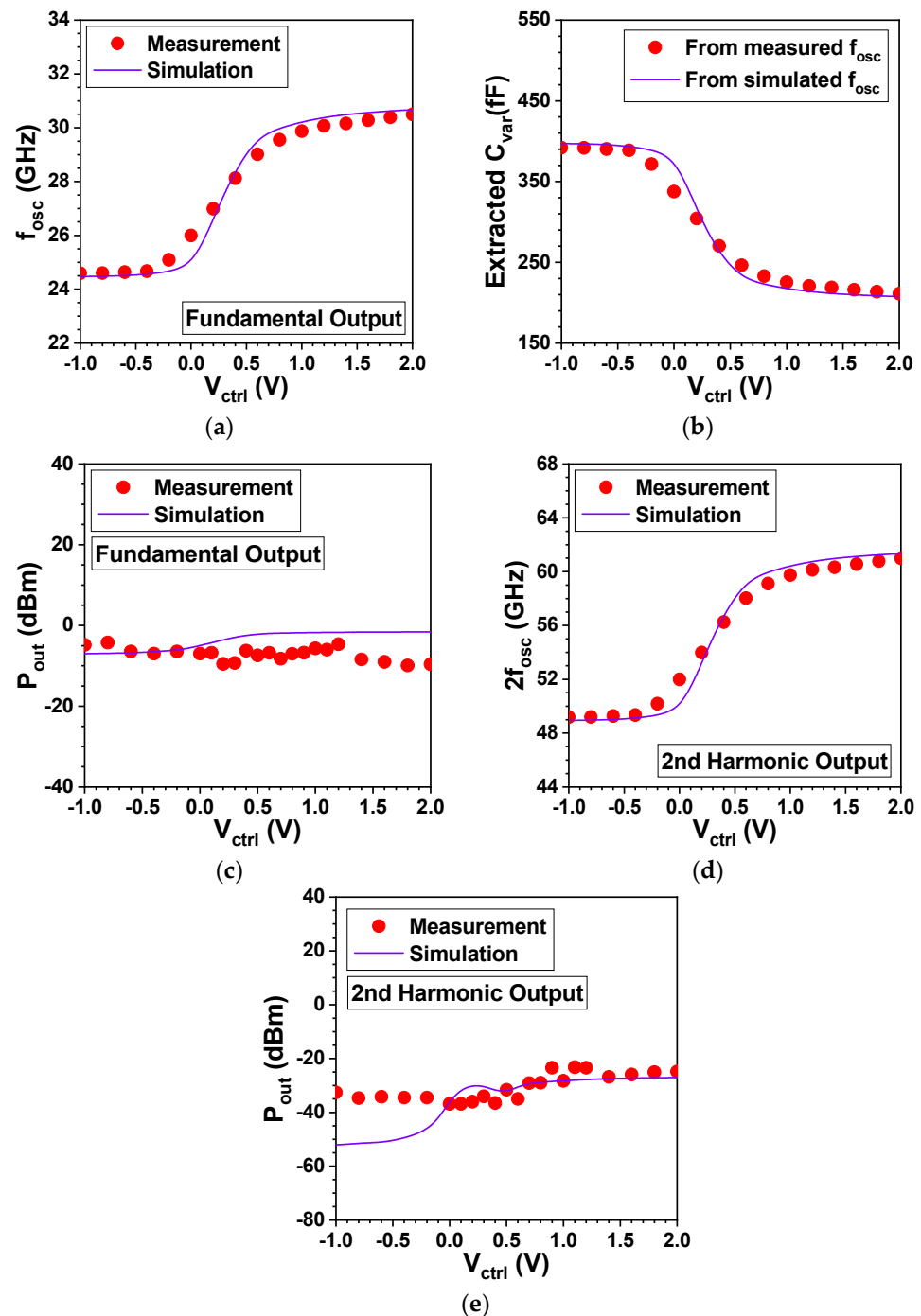


Figure 7. Measured and simulated results of the proposed VCO: (a) fundamental oscillation frequency (f_0), (b) extracted C_{var} , (c) fundamental single-ended output power (P_{out}), (d) second-harmonic oscillation frequency ($2f_0$), and (e) second-harmonic P_{out} .

Figure 7c shows the measured and simulated fundamental single-ended output power (P_{out}) versus V_{ctrl} of the VCO. The measured results closely match the simulations. As V_{ctrl} varies from -1 to 2 V, the VCO achieves a P_{out} range of -9.9 to -4.2 dBm.

Figure 7d shows the measured and simulated second-harmonic oscillation frequency ($2f_0$) versus frequency of the VCO. The measured results closely match the simulations. As V_{ctrl} varies from -1 to 2 V, the VCO achieves a tuning range of 11.82 GHz (49.18–61 GHz), corresponding to a fractional tuning range of 21.5%.

Figure 7e shows the measured and simulated second-harmonic single-ended P_{out} versus V_{ctrl} of the VCO. The measured results closely match the simulations. As V_{ctrl} varies from -1 to 2 V, the VCO achieves a P_{out} range of -36.8 to -23.2 dBm. Such power levels are insufficient to directly drive most Ka-/V-band mixers, which typically require LO input powers in the range of approximately -15 dBm to 0 dBm, depending on the mixer architecture and conversion-gain requirements. However, the objective of this work is to demonstrate the feasibility of the proposed dual-band VCO architecture rather than to realize a complete LO generation chain for a practical transceiver.

In typical 60 GHz phased-array, WiGig, and 5G transceivers, the VCO output is followed by buffer amplifiers and LO distribution networks before being applied to mixers. Furthermore, maintaining a relatively low output power at the oscillator core is often desirable because it reduces DC power consumption and minimizes load-pulling effects that can degrade phase-noise performance. In the prototype presented in this work, the generated $2f_0$ signal is directly capacitively coupled to a $50\ \Omega$ measurement load without any output buffer stage. Therefore, the measured output power reflects the intrinsic second-harmonic signal generated by the VCO core. To assess the practical feasibility of implementation, a dedicated $2f_0$ buffer amplifier was designed and simulated. Post-layout simulation results indicate that the buffer amplifier consumes 13.5 mW of DC power, occupies an area of $0.297\ \text{mm}^2$, and provides approximately 22 dB of gain at the second-harmonic frequency [16]. With this buffer stage, the expected $2f_0$ output power increases to approximately -14.8 to -1.2 dBm across the tuning range, which is sufficient to meet the LO drive requirements of typical Ka-/V-band mixer applications.

Figure 8a shows the measured output spectrum at V_{ctrl} value equal to -0.2 V for the f_0 output signal of the VCO. The VCO oscillates at 25.08 GHz with an output power of -6.44 dBm after compensating for a 6.21 dB cable loss. Figure 8b shows the measured output spectrum at V_{ctrl} value equal to 0.7 V for the f_0 output signal of the VCO. The VCO oscillates at 29.26 GHz with an output power of -8.23 dBm after compensating for a 6.26 dB cable loss.

Figure 8c shows the measured output spectrum at V_{ctrl} value equal to 2 V for the f_0 output signal of the VCO. The VCO oscillates at 30.5 GHz with an output power of -9.59 dBm after compensating for a 6.51 dB cable loss. Figure 8d shows the measured phase-noise performance of the VCO f_0 output at $V_{\text{ctrl}} = 0.3$ V. The VCO achieves phase-noise levels of -92.74 dBc/Hz and -117.69 dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively, from the 27.48 GHz carrier. These measured results agree well with the simulated phase-noise values of -95.38 dBc/Hz and -116.62 dBc/Hz at the corresponding offset frequencies. It should be noted that the phase-noise measurements were performed with the VCO chip mounted on a PCB and powered through off-chip decoupling capacitors to suppress low-frequency supply noise. Compared with the direct-powering configuration without external decoupling, this setup improves the close-in phase noise by more than 11 dB, reducing it from -81.16 dBc/Hz to -92.74 dBc/Hz at a 1 MHz offset from the 27.48 GHz carrier.

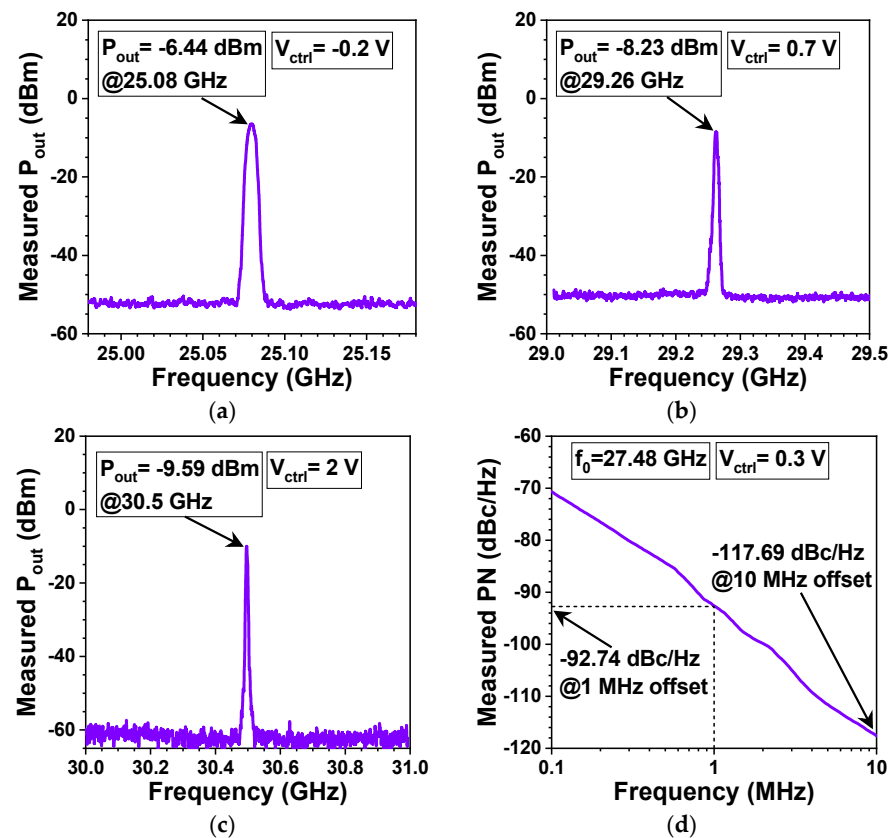


Figure 8. Measured output spectra at V_{ctrl} values equal to (a) -0.2 V, (b) 0.7 V, and (c) 2 V, along with (d) the measured phase noise at $V_{ctrl} = 0.3$ V for the fundamental (f_0) output signal of the VCO.

Figure 9a shows the measured output spectrum at V_{ctrl} value equal to -0.2 V for the $2f_0$ output signal of the VCO. The VCO oscillates at 50.18 GHz with an output power of -34.51 dBm after compensating for a 9.8 dB cable loss. Figure 9b shows the measured output spectrum at V_{ctrl} value equal to 0.7 V for the $2f_0$ output signal of the VCO. The VCO oscillates at 58.56 GHz with an output power of -28.62 dBm after compensating for a 11.67 dB cable loss. Figure 9c shows the measured output spectrum at V_{ctrl} value equal to 0.9 V for the $2f_0$ output signal of the VCO. The VCO oscillates at 59.45 GHz with an output power of -23.39 dBm after compensating for a 11.18 dB cable loss. Figure 9d shows the measured phase-noise performance of the VCO $2f_0$ output at $V_{ctrl} = 0.9$ V. The VCO exhibits phase noise levels of -88.57 dBc/Hz and -112.1 dBc/Hz at 1 MHz and 10 MHz offset frequencies, respectively, from the 59.45 GHz carrier. These measured results are in good agreement with the simulated phase noise values of -96.27 dBc/Hz and -116.90 dBc/Hz at the corresponding offset frequencies.

A figure-of-merit (FoM) suitable for evaluating the performance of a millimeter-wave CMOS VCO is given by [1]:

$$FoM(\text{dBc/Hz}) = PN(\Delta f) - 20 \log \left(\frac{f_0}{\Delta f} \right) + 10 \log \left(\frac{P_{DC}}{1 \text{ mW}} \right) - 20 \log \left(\frac{TR(\%)}{10} \right) \quad (10)$$

Table 1 summarizes the performance of the proposed VCO implemented in 90 nm CMOS, along with recently reported state-of-the-art CMOS VCOs in more advanced 22 , 28 , 40 , and 65 nm technologies [1–7]. Note that the reported results of this work are referenced to the RF pad plane and therefore include the effects of RF pad parasitics. The performance comparison in Table 1 is based on the measured results reported in the referenced publications. Since the treatment of RF pad parasitics is not always explicitly specified in the literature, the comparison should be interpreted as a benchmark of reported

measured VCO performance rather than a comparison of de-embedded intrinsic VCO-core characteristics. Despite being implemented in a less advanced technology node, the proposed VCO occupies a compact chip area while achieving low power consumption, a wide frequency tuning range, high output power, and excellent phase-noise performance. In addition, it achieves the best FoM at a 10 MHz offset among the compared works. Further performance improvements are expected if the proposed topology is implemented in more advanced CMOS technologies (e.g., 65 nm to 22 nm). These results validate the effectiveness and competitiveness of the proposed VCO architecture.

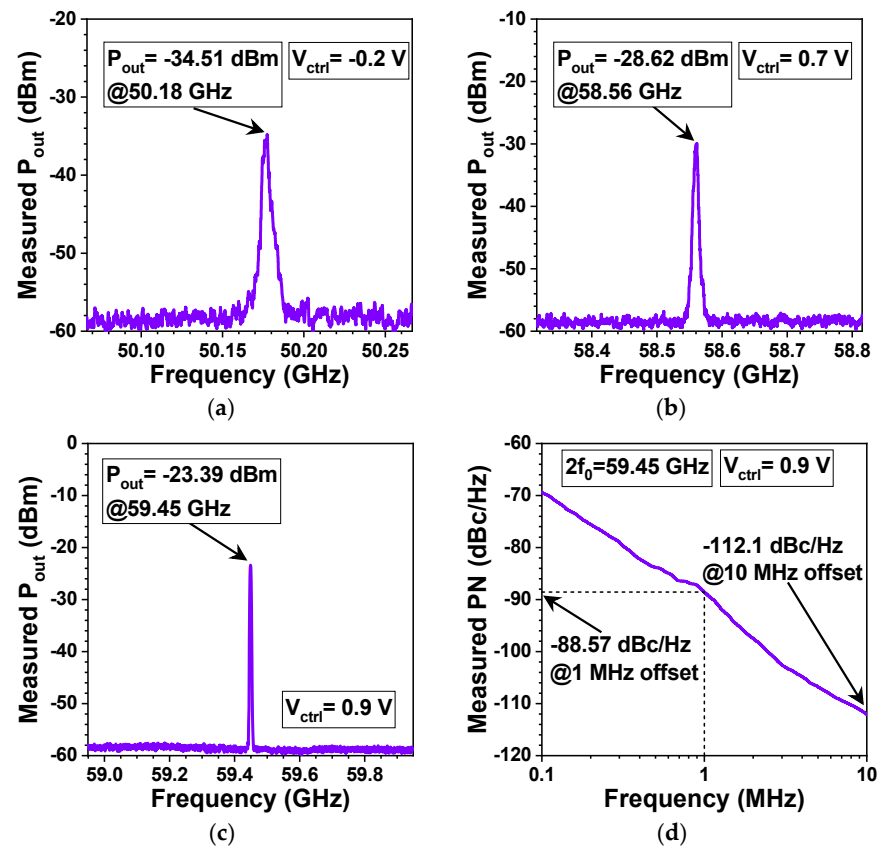


Figure 9. Measured output spectra at V_{ctrl} values equal to (a) -0.2 V, (b) 0.7 V, and (c) 0.9 V, along with (d) the phase noise at $V_{ctrl} = 0.9$ V for the second-harmonic ($2f_0$) output signal of the VCO.

Table 1. Summary of the proposed CMOS VCO and recently reported state-of-the-art CMOS VCOs with similar operation frequency.

	Topology	Freq. Range (GHz)	FTR (%)	PN@10 MHz (dBc/Hz)	P_{out} (dBm)	P_{dc} (mW)	FOM@10 MHz (dBc/Hz)	Area (mm ²)	CMOS Process
This Work	Push-Push & B-to-GND-with- R_B varactor	24.59–30.5	21.5	-117.69 $-92.74@1$ MHz	-4.2	2.19	-189.72 $-184.77@1$ MHz	0.021	90 nm
2025 GeMiC [1]	$2f_0$ from the tail of the cross-coupled pair	27.67–30.12	8.5	-119.11	-5.46	31.2	-171.95	0.018	22 nm
2023 MWTL [2]	Dual-core, class-C & switchable TF	31–46	39	-116	N/A	9.9	-189.57	0.048	28 nm
2021 EuMiC [3]	CMOS LC-tank & reversed varactors	37.2–42	12.1	-117	2.11	17.4	-178.22	0.015	22 nm
2022 APMC [4]	Class-D with average current control	33.6–35.9	6.6	-118	N/A	1.7	-182.93	0.09	65 nm

Table 1. Cont.

	Topology	Freq. Range (GHz)	FTR (%)	PN@10 MHz (dBc/Hz)	P _{out} (dBm)	P _{dc} (mW)	FOM@10 MHz (dBc/Hz)	Area (mm ²)	CMOS Process
2022 IMS [5]	TF-based Q-enhanced active Z converter	25.4–29.8	15.9	−122.7	N/A	5.1	−188.49	0.05	65 nm
2018 SSCL [6]	Switchable transformer-based tank	50.1–59.8	17.7	−111.9	−6.4	6.2	−183.71	0.065	65 nm
2018 RFIC [7]	Class-B & single varactor and inductor	31.8–40.8	24.8	−114.95	−12	20	−181.03	0.027	40 nm

5. Conclusions

This work demonstrates that the combination of $\lambda/4$ transmission-line-assisted biasing and a body-to-ground-with- R_B varactor configuration provides an effective approach for addressing several key challenges in millimeter-wave CMOS VCO design, including harmonic signal purity, AC grounding quality, substrate-noise coupling, and tuning linearity. The measured results confirm that these techniques enable a favorable trade-off among phase-noise performance, tuning range, power consumption, and chip area in a compact 30/60 GHz dual-band architecture. Beyond the specific implementation presented here, the proposed design methodology offers a scalable framework for realizing low-power fundamental- and harmonic-generation VCOs in advanced CMOS technologies. Nevertheless, realizing a complete frequency-generation block for practical mixer driving necessitates additional supporting circuitry, resulting in non-negligible power consumption and area overhead that diminish the low-power and compact advantages of the VCO core at the system level.

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