

Article

A 11-Bit Linear-Tracking Digital LDO with Variable-Step Control and Transient Enhancement for 4.4% Voltage Overshoot/Undershoot and 99.87% Peak Current Efficiency

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Abstract

This paper presents an 11-bit linear-tracking digital low-dropout (DLDO) regulator with variable step size control and transient enhancement (TE) techniques to achieve low output voltage overshoot/undershoot and high current efficiency. To address overflow issues and enable multi-step cooperative regulation, a novel feed/borrow bidirectional shift register (SR) array is proposed. Based on a standard 65 nm CMOS process, the effective core layout area is 2960 μm^2 , and post-layout simulation results show that the proposed DLDO consumes a quiescent current of 21 μA and provides a maximum load current of 15 mA, with a peak current efficiency of 99.87%. At a 1 V input and 0.9 V output, the maximum voltage overshoot/undershoot is only 40 mV under full load step change, corresponding to an overshoot/undershoot ratio of 4.4%. The DLDO is achieved with high resolution, fast transient response, low voltage ripple, and the competitive figures of merit (FOMs), which is suitable for low-power and high-precision power management applications.

Keywords: digital low-dropout regulator (DLDO); variable step size; linear tracking; overshoot/undershoot; high resolution; transient enhancement; shift register; current efficiency

1. Introduction

With the rapid development of digital and intelligent integrated circuits, stable and high-efficiency power management has become increasingly critical for system performance. Voltage regulation techniques ensure reliable operation of electronic systems and have drawn extensive research attention. Among various regulators, the linear-tracking digital low-dropout regulator (DLDO) stands out due to its high accuracy, high efficiency, low power consumption, and simple structure [1]. Moreover, the efficient integration of ultra-low power techniques and energy harvesting is crucial for the evolution of self-sufficient devices, highlighting the need for highly efficient power management solutions like the one proposed in this study [2].

Voltage regulators are core components of electronic devices, responsible for maintaining a stable output voltage to guarantee normal operation [3]. However, conventional voltage regulators suffer from output voltage fluctuations caused by input voltage variations and load changes, which degrade system stability and performance [4–6]. Linear-tracking DLDOs maintain good stability even under load variations without requiring reset operations [7]. Nevertheless, traditional linear-tracking DLDOs relying on linear search



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with fixed step size have limited resolution and lead to prolonged settling time [8]. In addition, such fixed-step structures face contradictions between adjustment speed and voltage ripple, and the shift register array is prone to overflow under extreme regulation conditions, further restricting the overall performance. In contrast, variable-step-size linear-tracking DLDOs adopt a flexible step control strategy to adapt to dynamic load and supply conditions, enabling higher resolution and faster regulation speed, thus being suitable for various operating scenarios [9]. Meanwhile, the voltage overshoot and undershoot caused by sudden load jumps remain a key challenge that must be addressed to improve system stability.

To overcome the limitations of conventional DLDOs, a linear-tracking DLDO integrated with variable step size control and transient enhancement techniques is proposed. The architecture adopts a feed/borrow bidirectional shift register array to solve the overflow problem, and uses adaptive step adjustment to balance settling time and adjustment accuracy. In addition, the transient enhancement module based on a continuous-time comparator array is introduced to quickly suppress voltage fluctuations. The proposed structure significantly improves the resolution of DLDO, reduces settling time and voltage overshoot/undershoot, enhances adaptability to load and input voltage variations, and achieves high current efficiency and compact chip area, which enables applications in low-power and high-precision on-chip power management applications.

This paper is organized as follows. An overview of the proposed DLDO architecture is provided in Section 2. The implementation of each circuit module is detailed in Section 3. The layout design and comprehensive simulation results are presented in Section 4. Finally, concluding remarks are given in Section 5.

2. Proposed Linear-Tracking DLDO

The drawbacks of conventional DLDOs are addressed, especially fixed adjustment step size and large overshoot/undershoot during load transient responses. A digital step size control algorithm is adopted to minimize settling time and reduce voltage fluctuations. Meanwhile, a transient enhancement module with additional comparison and trigger mechanisms is integrated to strengthen the transient response against sudden load and supply voltage jumps [10]. All improvements are realized with minimal hardware overhead while maintaining a clear and robust overall circuit structure.

Figure 1 shows the overall architecture of the proposed linear-tracking DLDO. It consists of five main parts: a comparator array, a step size adjustment module, a bi-directional shift register array, a transient enhancement module, and a power transistor array (adjustment MOS array).

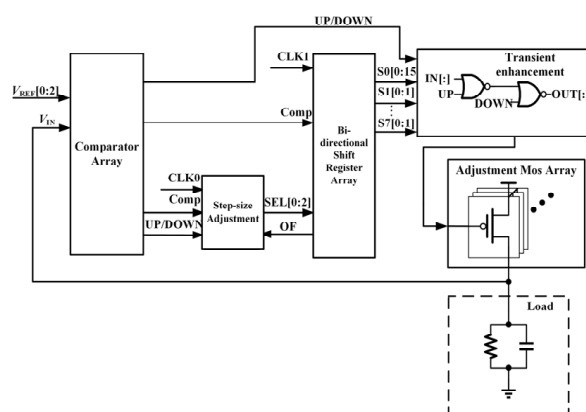


Figure 1. Block diagram of the proposed linear-tracking DLDO.

The clock signals include CLK0 (step size control clock) and CLK1 (global system clock), which are used to control the step size adjustment and the overall timing of the DLDO, respectively. The operating principle of the system is as follows: during one operating cycle of the linear-tracking DLDO, the comparator array first compares the reference voltage V_{REF} with the output voltage V_{OUT} (load input voltage). The step size control module selects the appropriate adjustment step size based on the output signals of the comparator array. The shift register control array stores the current control code of the power transistor array. When the output of the comparator array or the step size selection signal changes, the control code is updated, which ultimately adjusts the driving strength of the power transistor array. The transient enhancement module remains idle when V_{OUT} is stable near the reference voltage; once V_{OUT} deviates significantly (UP/DOWN signals are activated), the transient enhancement module temporarily takes over the control of the power transistors to limit the amplitude of V_{OUT} deviation.

3. Circuit Implementation

3.1. Comparator Array

A continuous-time comparator is adopted in the proposed DLDO to quantize the output voltage, which is a prerequisite for the normal operation of the transient enhancement module. Figure 2 shows the schematic of the continuous-time comparator, which is composed of a pre-amplification stage, an amplification stage, and a recovery stage.

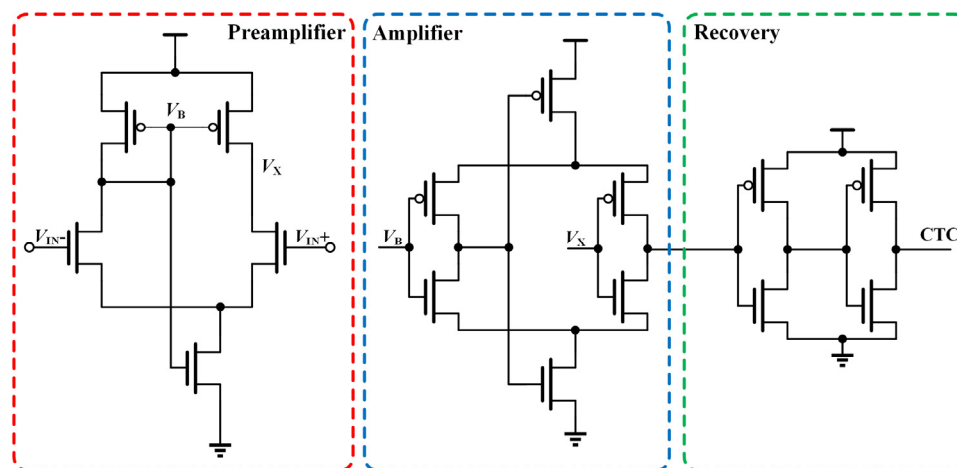


Figure 2. Schematic of the proposed continuous-time comparator.

The pre-amplifier stage is a typical single-ended output five-transistor cell amplifier structure. As shown in Figure 2, V_X is the output of the pre-amplifier stage and V_B is used for self-biasing. By optimizing the transistor size, the self-bias voltage can drive both the current-source NMOS and load PMOS transistors.

The amplification stage is a widely used amplifier structure for low-voltage and low-power design, which is considered a combination of an NMOS input pair and a PMOS input pair with mutual loading [11,12]. The inputs of the amplification stage are the two outputs of the pre-amplifier stage (V_X and V_B). V_B drives the left inverter, which in turn drives the NMOS and PMOS current sources. The feedback relationship controls the two drain voltages to make the threshold of the left inverter exactly equal to V_B . Since the left and right inverters are completely symmetrical, the flip threshold of the right inverter is also V_B , thus realizing the comparison between V_X and V_B and amplifying the signal of V_X .

The recovery stage is a buffer structure with three main functions: (1) restoring the output voltage range reduced by the structural characteristics of the amplification stage

and reducing the power consumption of subsequent circuits; (2) making up for the weak driving capability of the pre-amplification and amplification stages caused by transistor size limitations in their design; and (3) further improving the amplification gain, which is crucial for enhancing the output voltage accuracy and reducing power consumption.

Overall, the continuous-time comparator adopts a multi-stage cascade structure to obtain high amplification gain. Considering the low supply voltage, no common-source and common-gate structures are used in the circuit. In addition, the comparator can realize full self-biasing, eliminating the need for additional auxiliary biasing circuits.

The comparator array includes three continuous-time comparators of the above design, corresponding to three input reference voltages $V_{REF}[0:2]$. Figure 3 shows the distribution of the three reference voltages and their correlation with the output voltage status. The input reference voltages are $V_{REF}[0] = 0.92$ V, $V_{REF}[1] = 0.9$ V, and $V_{REF}[2] = 0.88$ V (provided externally) in descending order. Among them, $V_{REF}[1]$ is the main reference voltage that determines the ideal output voltage value; the Comp signal generated by comparing V_{OUT} with $V_{REF}[1]$ is the core control signal of the step size control module and shift register control array. $V_{REF}[0]$ and $V_{REF}[2]$ are mainly used for the transient enhancement module: the UP signal is activated when $V_{OUT} > V_{REF}[0]$, and the DOWN signal is activated when $V_{OUT} < V_{REF}[2]$. The activation of either the UP or DOWN signal will trigger the transient enhancement module to adjust V_{OUT} . When V_{OUT} is between $V_{REF}[0]$ and $V_{REF}[2]$, it indicates that V_{OUT} is close to the target reference voltage; at this time, the transient enhancement module is disabled, and the power transistor array is completely controlled by the shift register control array.

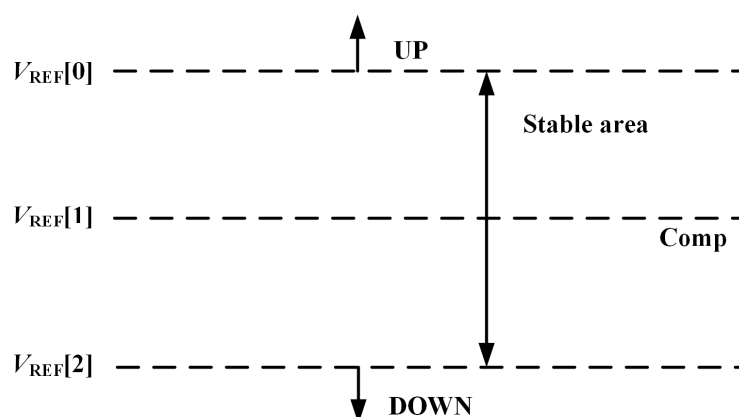


Figure 3. Relationship between reference voltages and output voltage.

3.2. Step Size Adjustment Circuit

Many conventional linear-tracking DLDOs adopt the fixed-step search method to simplify the circuit structure and minimize power consumption, but this method severely limits the resolution of DLDO. For example, a seven-bit resolution linear-tracking DLDO has 128 adjustable output ranges with a minimum search step of one, resulting in 128 adjustment cycles required for the output to change from the minimum to the maximum value, which is unacceptable for most practical applications due to the excessively long adjustment time.

There have been numerous studies on linear-tracking DLDOs with step size adjustment functions, but most of them are realized by voltage domain partitioning, leading to limited performance improvement [13,14].

A novel step size tuning design is proposed, which can significantly improve the DLDO resolution without increasing the settling time significantly, and does not require additional comparators with reference voltages or reset of control codes.

Figure 4 shows the circuit implementation of the step size adjustment module. The three-bit counter output signal SEL [0:2] indicates the currently selected step size, with eight optional levels: 000 corresponds to the maximum step size, and 111 corresponds to the minimum step size. After the minimum step size (111) is selected, the CLK terminal of the counter is locked, and the step size remains unchanged until the next step-reset signal is generated. The Comp signal from the comparator array is the core signal for the circuit to judge whether the step size needs to be adjusted. The OF signal from the shift register control array is used to indicate whether the current step size has overflowed, which will be detailed in the next section.

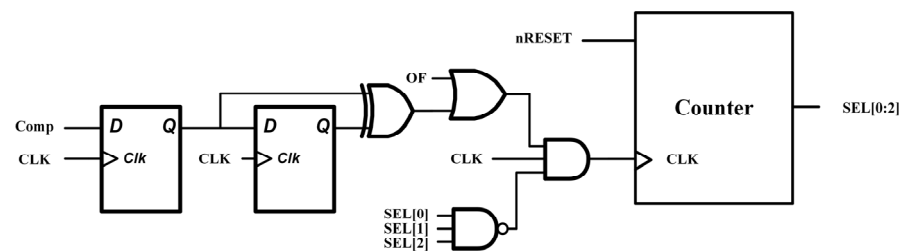


Figure 4. Circuit implementation of the step size adjustment module.

The core design idea of step size adjustment is to use a large step size when the deviation between V_{OUT} and the target value is large, and a small step size when the deviation is small. The judgment of step size adjustment is realized by comparing the Comp signals of two consecutive cycles. When V_{OUT} has a large deviation, the nRESET signal is activated to reset the counter, and the step size is restored to the maximum. In each cycle, the control code in the shift register is shifted in a specific direction according to the selected step size. At the start of a new cycle, a new Comp signal is obtained and compared with the Comp signal of the previous cycle, with the following judgment rules:

1. If the two Comp signals are the same, it means that the relative position between V_{OUT} and V_{REF} has not changed, indicating insufficient adjustment, and the large step size should be maintained continuously.
2. If the two Comp signals are different, it means that V_{OUT} crosses V_{REF} in the previous cycle, indicating that the deviation between V_{OUT} and the target value is small (less than the current step size), and the step size should be reduced at this time.

The two D flip-flops and the XOR gate on the left side of Figure 4 implement the above design idea. When V_{OUT} has a large deviation, the step size is restored to the maximum; each time V_{OUT} crosses V_{REF} , the step size is reduced once (the counter is incremented by 1) until the minimum step size is reached, after which the linear-tracking DLDO maintains the minimum step size for fine adjustment.

The nRESET signal of the counter has two trigger sources: (1) the UP/DOWN signal from the comparator array; and (2) the external global reset signal. The activation of the UP/DOWN signal indicates a significant deviation of V_{OUT} from the reference voltage, which can be regarded as a load jump, and the step size needs to be restored to the maximum for re-adjustment (this is the main trigger source of the nRESET signal). In addition, the counter is reset to the maximum step size when an external global reset is performed.

3.3. Bi-Directional Shift Register Array with Feed/Borrow Logic

To realize dynamic step size adjustment, bidirectional shift registers are adopted, which are classic core components in DLDO design [15]. Figure 5 shows the architecture of an $n + 1$ -bit bidirectional shift register applied to the k -th step size, where Q is the output of each bit, S is the shift direction control signal, and CLK is the clock signal.

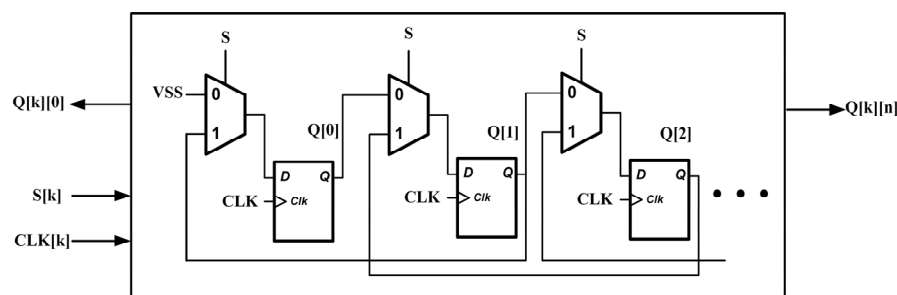


Figure 5. Schematic of the bidirectional shift register for the k -th step size.

The specific configuration of the shift register array is listed in Table 1. Three-bit step selection signals correspond to eight sets of shift registers. Among them, the largest step has 16-bit length, which corresponds to four-bit resolution when converted to binary code, while the remaining shift register sets of each step have only two-bit length, which corresponds to one-bit resolution. The total resolution of the shift register array is the sum of the resolution contributed by each step, which is 11 bit. Using the adjusting MOS cell size of the smallest step as standard, the cell size of each step is twice the next step, so as to ensure the feed/borrow logic works correctly.

Table 1. Shift register configuration and corresponding power MOS unit size.

Shift Register Number	Total Length	Adjusting MOS Unit Size
0	16 (4 bit)	$\times 128$
1	2 (1 bit)	$\times 64$
2	2 (1 bit)	$\times 32$
3	2 (1 bit)	$\times 16$
4	2 (1 bit)	$\times 8$
5	2 (1 bit)	$\times 4$
6	2 (1 bit)	$\times 2$
7	2 (1 bit)	$\times 1$

The bidirectional shift registers in the proposed DLDO have fixed 0 and 1 at the head and tail input terminals, respectively, and the stored data adopts a thermometer code format with all 0 s on the left and all 1 s on the right. A right shift in the bidirectional shift register increases the number of 0 s by one and decreases the number of 1 s by one (the total number of 1 s is reduced by one); a left shift decreases the number of 0 s by one and increases the number of 1 s by one (the total number of 1 s is increased by one). In this way, the +1 and -1 operations required for linear tracking are realized only through shift operations, eliminating the need for additional arithmetic circuits. Moreover, the data in the bidirectional shift register can directly drive the power transistor array, avoiding abrupt data changes caused by logic contention.

A shift register control array is constructed by replicating this bidirectional shift register design, with each group of shift registers corresponding to a different power transistor size. The variable-step linear tracking can be implemented without complex multi-bit shifting operations, only by selecting the appropriate group of shift registers for shift operation. The specific configuration of the shift register control array is listed in Table 1.

The three-bit step selection signal corresponds to eight groups of shift registers. Among them, the maximum step size corresponds to a 16-bit shift register (four-bit resolution when converted to binary code), and the remaining shift register groups for each step size are all two-bit (one-bit resolution for each). The total resolution of the shift register control array is the sum of the resolution contributed by each step size, reaching 11 bits. Taking the power

MOS unit size of the minimum step size as the standard, the unit size of each step size is twice of the next smaller step size, ensuring the correct operation of the feed/borrow logic.

An important challenge in the design of the multi-step shift register array is solving the overflow problem. Overflow occurs when a shift register needs to be shifted left (increased by 1) in the all-1 state or shifted right (decreased by 1) in the all-0 state (defined as positive overflow and negative overflow, respectively), at which time the shift register cannot perform effective adjustment operations. Therefore, a coordination mechanism needs to be designed to link the data of shift registers with different step sizes, avoiding control failure caused by the overflow of a single step size shift register. In addition, this coordination mechanism breaks the limitation of the small step size control by its own shift register length, greatly expanding the adjustment range of the small step size.

The feed/borrow method is adopted to solve the overflow problem of the multi-step shift register array. In binary arithmetic, the following expression can be used:

$$A_0 = A_1 + \overline{A_0} = A_2 + \overline{A_1} + \overline{A_0} = \dots \quad (1)$$

where A_0 , A_1 , and A_2 represent the 0th, 1st, and 2nd bits of the binary number from the least significant bit to the most significant bit, respectively. For the multi-step shift register array, this expression indicates that a right/left shift in the k -th-level shift register is equivalent to a right/left shift in the $(k - 1)$ -th level shift register plus a reverse shift in the k -th-level shift register.

Figure 6 shows the circuit implementation of the feed/borrow logic (taking Levels 6 and 7 as an example). When feed/borrow occurs, the circuit needs to complete two functions: (1) enabling the higher-level shift register; and (2) flipping the shift direction of the current-level shift register. The enablement of the shift register is realized by a gated clock. The left part of the logic circuit in Figure 6 is used to generate the enable signal and control the shift direction, and the right part is used to generate the feed/borrow signal.

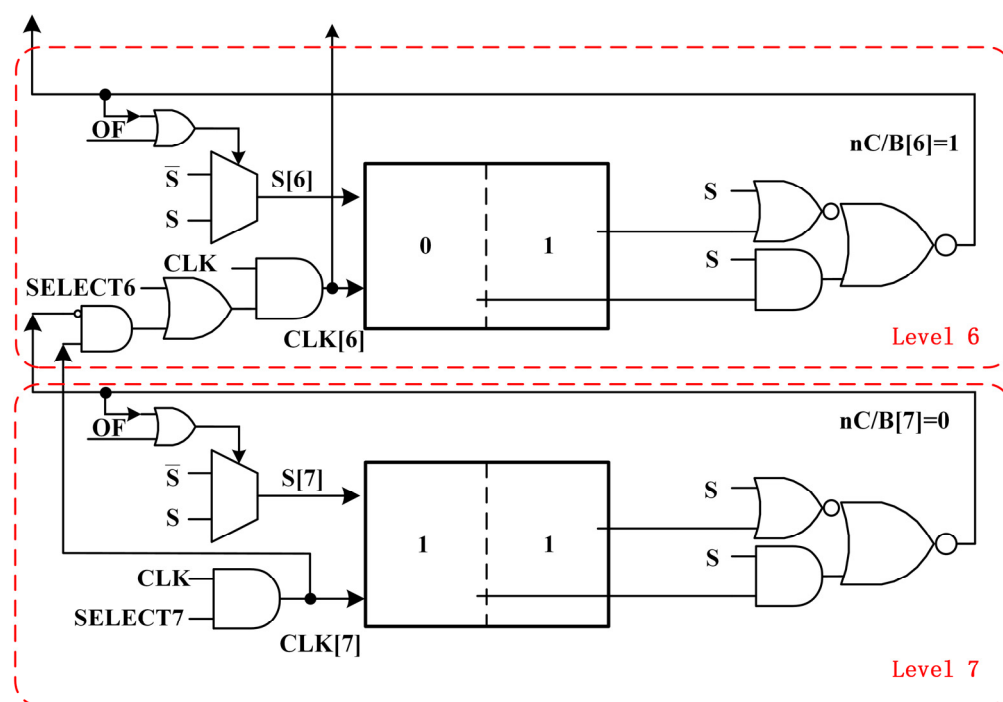


Figure 6. Circuit implementation of the feed/borrow logic (Levels 6 and 7 as an example).

First, the generation of the feed/borrow signal is explained. The $nC/B[k]$ signal is the active-low feed/borrow signal transmitted upward by the k -th-level shift register. A bidirectional shift register requires feed/borrow in two cases:

- (1) The stored data is all 0 s and needs to be shifted right.
- (2) The stored data is all 1 s and needs to be shifted left.

Since the data in the bidirectional shift register is in thermometer code format, it is only necessary to judge the leftmost bit (Q_L) or the rightmost bit (Q_R) to determine whether the data is all 0 s or all 1 s. $S = 0$ indicates a right shift and $S = 1$ indicates a left shift. The logic expression of the active-low nC/B signal is:

$$nC/B = (\overline{Q_L \cdot S}) + (\overline{Q_R + S}) \quad (2)$$

The 7th-level shift register is the minimum step size level and does not need to consider feed/borrow from other levels, so the clock signal $CLK[7]$ and shift direction signal $S[7]$ of the 7th level are:

$$CLK[7] = CLK \cdot SELECT7 \quad (3)$$

$$\text{and } S[7] = S \cdot nC/B[7] + \bar{S} \cdot \overline{nC/B[7]} \quad (4)$$

The 6th level and other higher-level shift registers need to consider the feed/borrow from the lower level. For example, when feed/borrow occurs in the 7th level, an enable signal is transmitted to the 6th level, and the shift direction of the 6th level remains the same as the original direction. If the 6th level also overflows due to feed/borrow, the 6th level transmits an enable signal to the 7th level and flips its own shift direction, thus realizing multi-level feed/borrow transmission. Taking the 6th level as an example, considering the simultaneous occurrence of feed/borrow in the 6th and 7th levels, its CLK and S signals are:

$$CLK[6] = CLK \cdot (SELECT6 + \overline{nC/B[7]} \cdot CLK[7]) \quad (5)$$

$$\text{and } S[6] = S \cdot nC/B[6] + \bar{S} \cdot \overline{nC/B[6]} \quad (6)$$

With the above design, a multi-stage transmissible feed/borrow mechanism is realized, which overcomes the problems of small search range and overflow of the multi-step shift register array.

The OF signal mentioned in the step size adjustment module indicates the overflow of the maximum step size shift register. The overflow of the maximum step size shift register means that all shift registers from the currently selected step size to the maximum step size are in the all-0 or all-1 state, indicating that the DLDO loses its adjustment capability at the current step size, and the step size needs to be reduced to expand the adjustment range. Therefore, the OF signal is also used as one of the conditions for step size reduction.

In addition, when the maximum step size shift register overflows (refer to Equation (2)), it means that the shift registers from the current step size to the sub-maximum step size are selected and shifted in the reverse direction, and the maximum step size shift register cannot complete the expected shift operation. At this time, the data in the shift register control array is shifted in the opposite direction of the expected direction. To avoid this problem, the OF signal is used as one of the conditions for shift direction reversal in Figure 6: when the OF signal is activated, the $nC/B[k]$ signal no longer flips the shift direction of the k -th level shift register.

The generation of the OF signal needs to consider two factors: whether the maximum step size shift register overflows in the current direction (i.e., whether $nC/B[0]$ is activated) and whether the maximum step size is selected (i.e., whether $CLK[0]$ is activated). To avoid

the reverse shift in other step size shift registers, the OF signal should be generated earlier than the CLK signal. And the nC/B signal can be used for judgment and derivation:

(1) When the 0th level (maximum step size) is selected, only the overflow of the 0th level itself needs to be judged:

$$OF_0 = \overline{nC/B[0]} \cdot SELECT0 \quad (7)$$

(2) When the 1st level is selected, the overflow of the maximum step size requires the simultaneous overflow of the 0th and 1st levels:

$$OF_1 = \overline{nC/B[0]} \cdot \overline{nC/B[1]} \cdot SELECT1 \quad (8)$$

(3) When the k-th level is selected, the overflow of the maximum step size requires the simultaneous overflow of the 0th to k-th levels:

$$OF_k = \overline{nC/B[0]} \cdot \dots \cdot \overline{nC/B[k]} \cdot SELECTk \quad (9)$$

The total OF signal is the OR of the OF signals of all levels. For the eight levels, the total OF signal is:

$$OF = OF_0 + OF_1 + OF_2 + OF_3 + OF_4 + OF_5 + OF_6 + OF_7 \quad (10)$$

3.4. Transient Enhancement Circuit

The control of the power transistor array by the traditional DLDO needs to be triggered by the clock signal, which limits the transient response speed and increases the output voltage overshoot/undershoot. Therefore, many DLDO designs integrate an independent transient enhancement module to assist the main control loop in regulating the output voltage [16].

Figure 7 shows the design of the transient enhancement circuit. The IN signal is the control signal from the shift register control array, and the OUT signal is the drive signal connected to the gate of the power transistors. A transient enhancement circuit is inserted between each group of IN and OUT signals. Since the power transistors are PMOS, $OUT = 1$ indicates that the PMOS is turned off, and $OUT = 0$ indicates that the PMOS is turned on. The UP and DOWN signals are generated by the comparator array; as the comparator is a continuous-time design, the UP and DOWN signals are generated instantaneously when V_{OUT} deviates from the stable region, without waiting for the clock signal. When V_{OUT} is too high ($UP = 1$, $DOWN = 0$), all OUT signals are set to 1, turning off all power transistors to reduce V_{OUT} ; conversely, when V_{OUT} is too low ($UP = 0$, $DOWN = 1$), all OUT signals are set to 0, turning on all power transistors to increase V_{OUT} .

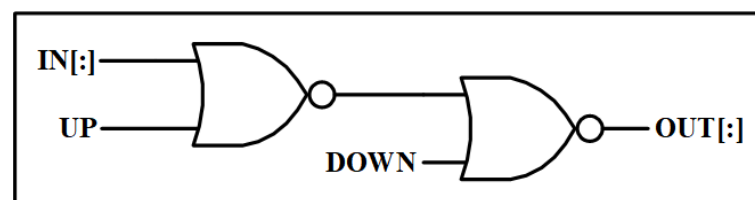


Figure 7. Circuit implementation of the transient enhancement module.

Figure 8 illustrates the operating process of the transient enhancement module. Initially, the DLDO operates in a steady state with V_{OUT} equal to $V_{REF}[1]$. When the load suddenly increases, V_{OUT} drops rapidly below $V_{REF}[2]$, triggering the activation of the DOWN signal; as a result, all power transistors are turned on to boost V_{OUT} until it exceeds

$V_{REF}[2]$. Once V_{OUT} returns to the stable region, the DOWN signal is deactivated; however, since the clock signal has not arrived, V_{OUT} drops again and reactivates the DOWN signal, forming a sawtooth voltage waveform. When the clock signal arrives, the control code of the shift register is adjusted, and the amplitude of the sawtooth waveform gradually decreases until V_{OUT} remains in the stable region, at which time the transient enhancement module is disabled. During operation, the transient enhancement module is quickly disabled after V_{OUT} enters the stable region to avoid V_{OUT} crossing $V_{REF}[1]$ due to the over-adjustment of the transient enhancement module, thus ensuring that the transient enhancement module does not interfere with the normal operation of the main control loop.

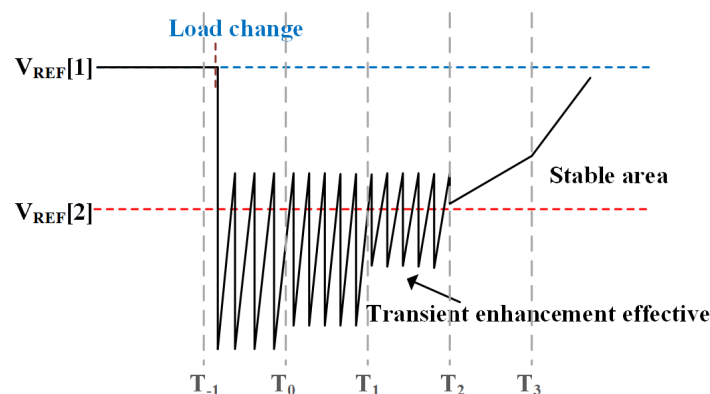


Figure 8. Functional schematic of the transient enhancement module.

4. Layout and Simulation Results

The proposed variable-step-size linear-tracking DLDO is designed using Cadence Virtuoso and implemented by a standard 65 nm CMOS process. Figure 9a shows the overall layout of the DLDO including PAD, with a total chip area of $400\ \mu\text{m} \times 400\ \mu\text{m}$. Figure 9b shows the core part of the DLDO, which is divided into three functional regions: the comparator array, the digital control circuit, and the power transistor array. The comparator array occupies an area of about $100\ \mu\text{m}^2$, the digital control circuit about $2500\ \mu\text{m}^2$, and the power transistor array about $360\ \mu\text{m}^2$. The total core area of DLDO is about $2960\ \mu\text{m}^2$.

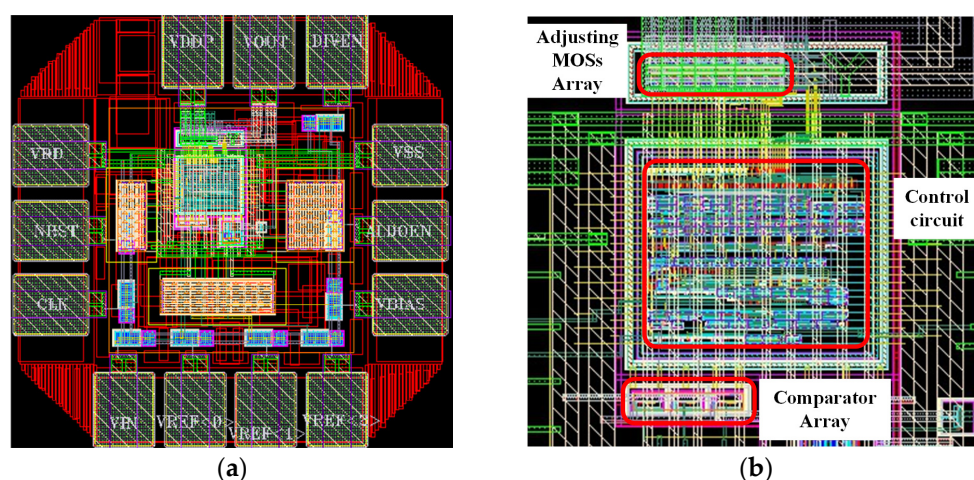


Figure 9. Layout of the proposed DLDO: (a) Total layout including PAD; (b) core part layout.

4.1. Load Transient Response

Figure 10 shows the load transient response simulation waveform of the proposed linear-tracking DLDO, which is obtained from Cadence Virtuoso simulations and processed by MATLAB R2017. The simulation conditions are set as follows: supply voltage

$V_{DD} = 1$ V, clock frequency $f_{CLK} = 20$ MHz, output capacitance $C_{OUT} = 1$ nF, reference voltages $V_{REF}[1] = 0.9$ V, $V_{REF}[0] = 0.92$ V, $V_{REF}[2] = 0.88$ V, load current switching between $50 \mu\text{A}$ and 15.05 mA with an edge time of 1 ns. Under heavy-load conditions, the maximum undershoot of V_{OUT} is 40 mV, and the settling time (from the occurrence of load jump to the stabilization of V_{OUT}) is about $1.25 \mu\text{s}$; under light-load conditions, the maximum overshoot of V_{OUT} is 34 mV, and the settling time is about $1.8 \mu\text{s}$. The longer settling time under light load is due to the small load current and the longer recovery time required for the output capacitance. In the steady state, the main control loop continues to perform fine adjustment with the minimum step size, resulting in a small amount of ripple in V_{OUT} , and the ripple is more obvious under light load than under heavy load. The 11-bit resolution power transistors are adopted, ensuring that the peak ripple of V_{OUT} is only 2.5 mV under the $50 \mu\text{A}$ light load.

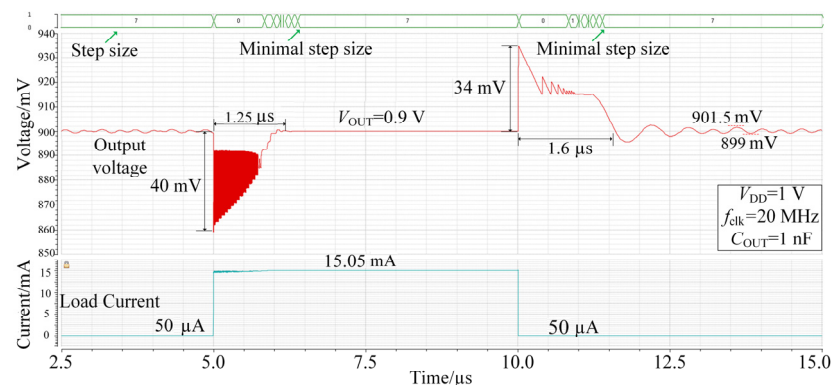


Figure 10. Load transient response simulation waveforms ($50 \mu\text{A} \leftrightarrow 15.05$ mA load jump).

Figure 11 is a partial zoom of Figure 10, focusing on the waveform details of the load switching to heavy load. This load condition requires the control code to be adjusted from the minimum to the maximum, so the effective duration of the transient enhancement module can be observed for a longer time. As the control code is gradually adjusted, the voltage spike caused by the transient enhancement module gradually attenuates. For this load current jump, the original and target control codes are at the edge of the adjustment range, so the step size adjustment is mainly realized by the overflow of the maximum step size shift register to generate the OF signal, which effectively reduces the step size.

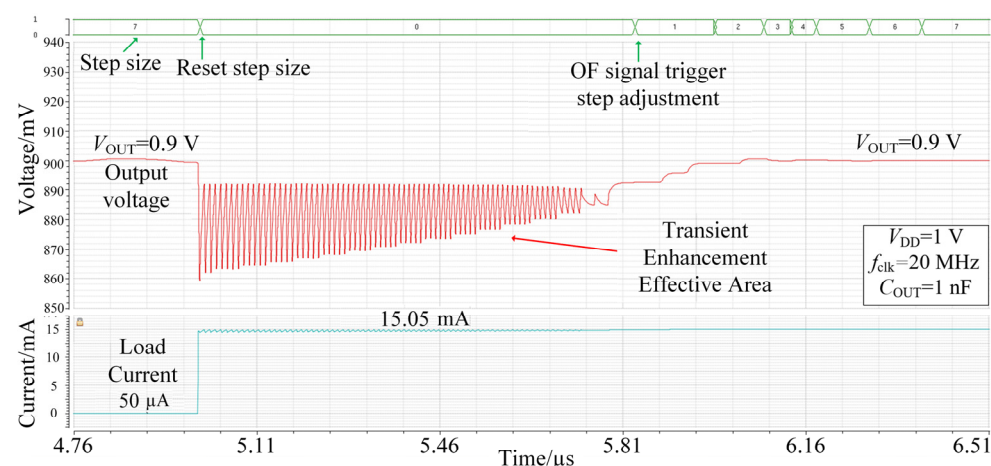


Figure 11. Zoomed view of the heavy-load transient response ($50 \mu\text{A} \rightarrow 15.05$ mA).

In some special adjustment processes, the transient enhancement module is first activated while the maximum step size is used for adjustment, then the step size is reduced

when V_{OUT} crosses the reference voltage, and the swing of V_{OUT} is continuously reduced until the steady state is reached. However, after V_{OUT} enters the stable region, the oscillation during the adjustment process may cause V_{OUT} to briefly trigger the transient enhancement module again and lead to secondary oscillation of the output, resulting in system instability. To avoid the unintended triggering of the step-reset signal by such oscillations, the proposed linear-tracking DLDO integrates a counter to limit the interval between two step-reset signals. As shown in Figure 12, the step-reset signal is prevented from being triggered by short-term voltage fluctuations, and the system stability is improved.

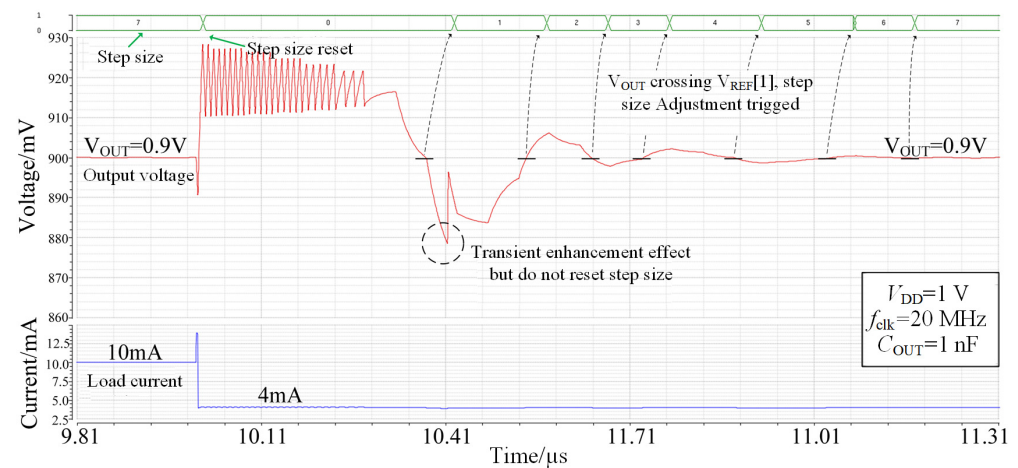


Figure 12. Zoomed view of the load transient response (4 mA → 10 mA).

4.2. Reference Voltage Tracking Response

Figure 13 shows the transient response simulation waveform of the proposed DLDO for reference voltage tracking. The simulation conditions are: $V_{DD} = 1$ V, $f_{CLK} = 20$ MHz, $C_{OUT} = 1$ nF, load current $I_{LOAD} = 7.5$ mA, and the edge time of the reference voltage is 1 ns. In the simulation, the main reference voltage $V_{REF}[1]$ switches between 0.9 V and 0.85 V, and $V_{REF}[0]$ and $V_{REF}[2]$ always keep a 20 mV interval with $V_{REF}[1]$ to track the change in the main reference voltage. The simulation results show that V_{OUT} enters the adjustment state immediately after the reference voltage changes; initially, $V_{REF}[0]$ and $V_{REF}[2]$ change and activate the transient enhancement module for a certain time, and then V_{OUT} returns to the steady state. When the reference voltage drops, the maximum overshoot of V_{OUT} is 26 mV, and the settling time is about 0.5 μ s; when the reference voltage rises, the maximum undershoot of V_{OUT} is 24 mV, and the settling time is about 0.45 μ s.

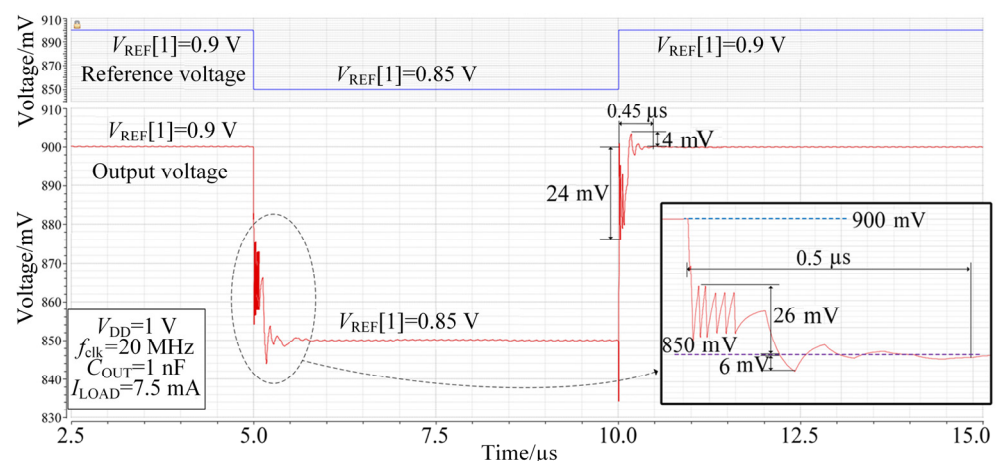


Figure 13. Reference voltage tracking simulation waveforms.

4.3. Supply Voltage Variation Response

Figure 14 shows the simulation waveform of the proposed DLDO under supply voltage variation. The simulation conditions are: reference voltage $V_{REF} = 0.8$ V, $f_{CLK} = 20$ MHz, $C_{OUT} = 1$ nF, $I_{LOAD} = 7.5$ mA, and the supply voltage switches between 0.9 V and 1 V with an edge time of 1 ns. Since the unit current of the power transistors is positively correlated with the supply voltage, V_{OUT} increases with the rise in the supply voltage (requiring the reduction in the control code), and V_{OUT} decreases with the drop of the supply voltage (requiring the increase in the control code). The simulation results show that the proposed DLDO can effectively adapt to the supply voltage variation: when the supply voltage switches between 0.9 V and 1 V, the maximum overshoot and undershoot of V_{OUT} are 39 mV and 37 mV, respectively, and V_{OUT} returns to the steady state within 0.7 μ s.

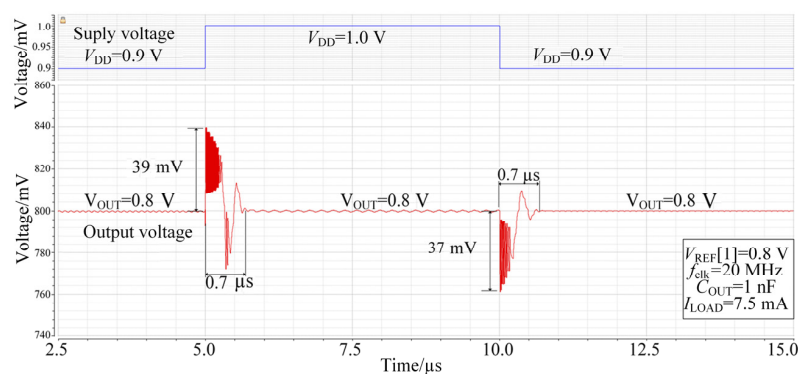


Figure 14. Supply voltage variation response simulation waveforms.

4.4. Quiescent Current and Current Efficiency

The quiescent current of the proposed DLDO is simulated, and the results show that the quiescent current remains relatively stable in the entire load range, ranging from 21 μ A to 24 μ A. The variation in the quiescent current is mainly caused by the power consumption fluctuation of the continuous-time comparator with the output voltage, and the quiescent current of the comparator is slightly higher under heavy load conditions. Figure 15 shows the current efficiency curve of the proposed DLDO which is defined as follows:

$$\eta = \frac{I_{Load}}{I_{Total}} \times 100\% = \frac{I_{Load}}{I_{Load} + I_Q} \times 100\% \quad (11)$$

where I_{Load} is the load current, I_Q is the quiescent current (control circuit current), and I_{Total} is the total supply current. When the load current is greater than 0.5 mA: the current efficiency reaches nearly 96% at the load current of 0.5 mA, and the peak current efficiency of 99.87% is achieved at the maximum load current of 15 mA.

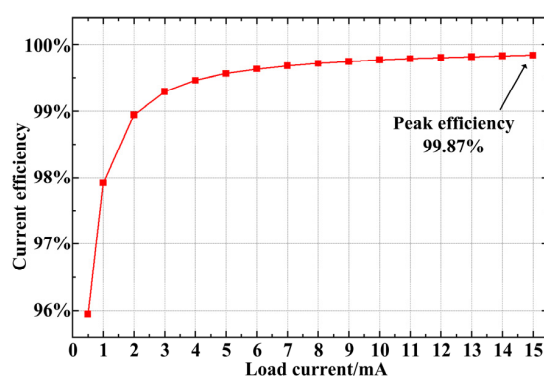


Figure 15. Current efficiency versus load current curve.

4.5. Performance Comparison

Table 2 summarizes the key performance parameters of the proposed DLDO and compares them with the State-of-the-Art DLDO designs in recent years [17–22]. A synergistic design is adopted in analog and digital LDOs, where the digital part has low resolution and the analog part dominates the overall design; although it achieves a short settling time, it has the disadvantage of a high quiescent current. The load current ranges of the designs in [17,20] are similar to that of this work, but the proposed design achieves a significantly higher resolution due to the variable-step-size design. The design in [19] proposes a clock-variable PID control with a resolution and settling time similar to this work, but the proposed design has better performance in quiescent current and output voltage overshoot/undershoot. By integrating the 11-bit high resolution and 20 MHz low operating frequency, the proposed design achieves a settling time comparable to that of the compared works, which fully reflects the advantages of the variable-step-size design. The two figures of merit (FOM1 and FOM2) of the proposed design are 4.45 ps and 0.067 pF, respectively, which are better than most of the compared works.

Table 2. Performance summary and comparison with State-of-the-Art works.

Parameters	[17] JSSC'18	[18] CICC'19	[19] JSSC'19	[20] TPE'20	[21] JSSC'21	[22] TPE'23	* This Work
Proc. (nm)	65	130	65	40	65	65	65
Topology	SAR/PD/PWM	Flash ADC	VCO-based ADC	PID	ADC+PI	CT ADC	SRs
V_{DD} (V)	0.5–1	0.83–1	0.6–1.2	1.1	1	0.6–1.2	0.6–1
V_{OUT} (V)	0.3–0.45	0.6–0.8	0.4–1.1	1	0.9	0.55–1.15	0.45–0.9
I_Q (μ A)	14	150	100–1070	10–19.6	683.1	102–167	21–24
$I_{loadmax}$ (mA)	2	26	100	20	416.7	26	15
Active area (mm ²)	0.0023	0.1178	0.056	0.18	0.0723	0.075	0.00296
Cur. Density (mA/mm ²)	869.565	220.713	1785.714	111.111	5763.485	346.667	5067.568
C_{OUT} (nF)	0.4	0.8	0.04	4.7	0.9	0.01	1
$\Delta V_{OUT@}$	40 mV@	160 mV@	108 mV@	40 mV@	94.1 mV@	140 mV@	40 mV@
ΔI_{LOAD}	1.06 mA	25 mA	50 mA	19 mA	124.2 mA	26 mA	15 mA
^b $\Delta V_{OUT,max}/V_{OUT@V_{OUT}}$	8.9%@0.45 V	20%@0.8 V	13.5%@0.8 V	8%@0.5 V	10.5%@0.9 V	23.3%@0.6 V	4.4%@0.9 V
Cur. eff.	99.8%	99.4%	99.5%	99.95%	99.8%	99.6%	99.87%
Opera. freq. (MHz)	1–240	^a N.A.	<100	100	250	20	20
Res. (bit)	7	4	10	7	9	7	11
Settling time (μ s)	0.1	0.28	1.24	1.3	0.103	0.11	1.6
^c FOM ₁ (ps)	199	30.72	1.38	10	3.75	5.49	4.45
^c FOM ₂ (pF)	0.469	0.96	0.086	0.19	0.518	0.11	0.067

^a N.A. indicates not mentioned in the literature.; ^b $\Delta V_{OUT,max}$ is the maximum over/undershoot output voltage when full load step change response occurs. ^c $FOM1 = \frac{C_{OUT} \times \Delta V_{OUT}}{\Delta I_{LOAD}} \times \frac{I_Q}{\Delta I_{LOAD}}$; $FOM2 = \frac{I_Q}{\Delta I_{LOAD}} \times \frac{\Delta V_{OUT}}{V_{OUT}} \times C_{OUT}$; The smaller the FOM value, the better. * Post simulation results.

5. Conclusions

This paper presents a high-resolution linear-tracking digital low-dropout regulator (DLDO) with variable step size control and transient enhancement techniques. The proposed design achieves excellent transient performance, low output voltage overshoot and undershoot, and fast continuous tracking capability. The variable step size adjustment mechanism effectively optimizes the regulation resolution and convergence time of the DLDO. A novel bidirectional shift register array with feed/borrow logic is proposed to implement reliable multi-step linear tracking and avoid logic conflicts and functional failure caused by shift register overflow. The integrated continuous-time transient enhancement module rapidly suppresses the maximum output voltage overshoot and undershoot un-

der large load or supply voltage step changes. Post-layout simulation results based on a standard 65 nm CMOS process demonstrate that the proposed DLDO achieves 11-bit high resolution, low quiescent current, high current efficiency up to 99.87%, small voltage overshoot/undershoot ratio of 4.4%, and competitive figures of merit (FOMs). Benefiting from the above advantages, the proposed DLDO is well suitable for low-power, high-efficiency, and high-precision on-chip power management applications in digital and intelligent integrated circuits and systems. Future work will explore the integration of this DLDO into fully self-powered energy-harvesting systems and the implementation of a fully asynchronous control loop for further power reduction. This technological trajectory is specifically targeted at enhancing the energy autonomy and performance of next-generation ultra-low-power IoT nodes, smart wearable electronics, and distributed power delivery for high-speed digital processing systems.

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