

Article

GaN HEMT-Based Frequency Quadrupler Up-Converting from S Band to X Band with Conversion Gain in Narrowband

Ainhoa Morales-Fernandez , Maria Marante-Boado , Monica Fernandez-Barciela * 
and Fernando Martin-Rodriguez 

atlanTTic Research Center for Telecommunication Technologies, Universidade de Vigo, 36310 Vigo, Spain; ainhoa.morales@uvigo.gal (A.M.-F.); maria.marante.boado@uvigo.gal (M.M.-B.); fmartin@uvigo.gal (F.M.-R.)

* Correspondence: monica.barciela@uvigo.gal

Abstract

This work presents the first design of an active frequency quadrupler based on GaN HEMTs. It is based on two cascaded frequency doubler stages that allow up-conversion from the S band to the X band, obtaining conversion gain in narrowband without the need for any additional buffer amplifier. A hybrid prototype of the quadrupler provides, at the input fundamental frequency of 2.5 GHz, a measured fourth harmonic maximum conversion gain of 13.7 dB and an output power of 23.5 dBm, with suppression of both fundamental and second harmonic above 14 dBc. To obtain these results, due to its impact in the final quadrupler behavior, a prototype of the higher frequency second stage doubler was designed and manufactured separately to assess its RF performance. The experimental results of this standalone prototype are highly competitive with the current state of the art in frequency doublers at the C band.

Keywords: frequency quadrupler; frequency doubler; gallium nitride; hybrid circuit; microwaves

1. Introduction

In general, frequency multipliers are used within mixer stages or frequency synthesizers to increase the frequency (by a multiple integer) of the signal generated by a low-frequency, high-performance local oscillator. This allows the translation of its stability and phase noise characteristics to the upper band with acceptable efficiency while providing enough output power. Different semiconductor technologies have been used over the years for their fabrication, from silicon (Si) to compound semiconductors.

Gallium nitride (GaN) transistors are showing outstanding performance over Si or gallium arsenide (GaAs)-based ones in high-frequency applications requiring high power and efficiency. GaN HEMTs, primarily used in RF power amplifiers (PAs) and power electronics, are starting to play a significant role in other areas such as renewable energy, electric vehicles, and electronics for medical applications, among others [1].

Although passive components such as Schottky barrier diodes or varactors are generally used in frequency multiplication, replacing them with active devices provides benefits in terms of conversion gain and broad bandwidth [2].

Recently, there have also been developments in the design of microwave active frequency multipliers using GaN HEMTs. These designs can benefit from the added output power and efficiency provided by GaN devices, while achieving conversion gains (G_c),



Academic Editors: Aurore Constant
and Hyon Ju Chauveau

Received: 26 May 2026

Revised: 23 June 2026

Accepted: 29 June 2026

Published: 1 July 2026

Copyright: © 2026 by the authors.

Licensee MDPI, Basel, Switzerland.

This article is an open access article distributed under the terms and conditions of the [Creative Commons Attribution \(CC BY\)](https://creativecommons.org/licenses/by/4.0/) license.

wide bandwidths, stability and output power without the need for additional amplifiers, which ultimately reduces circuit area, complexity, consumption and costs.

Regarding active frequency multipliers in hybrid technology, most published works design frequency doublers (FDs) [3–6], some triplers [3,7,8] and only a few quadruplers [3,9]. Considering those FDs with similar technologies to this work—although with higher power transistors—in [4] two FDs can be found: one using a SiC MESFET (with central frequency $f_c = 2$ GHz) and another one using a GaN HEMT ($f_c = 3.33$ GHz), both being 10 W transistors. These designs obtained a G_c of 10 dB and 14.8 dB, and an output RF power (P_{out}) of 38 dBm and 36.17 dBm, respectively, while reaching a Harmonic Rejection Ratio (HRR)@ $f_0 > 35$ dB by using $\frac{\lambda}{4}$ stub resonators. This method was also used in [5], where a FD based on a GaAs MESFET ($f_c = 4.8$ GHz) obtains a G_c of -4.9 dB and a HRR > 47 dB for both f_0 and $3f_0$. In [6] three similar FDs are presented by the authors ($f_c = 2.45$ GHz), all using the same 5 W GaN HEMT used in this work, providing more than 11 dB of G_{c2f_0} , P_{out} around 20 dBm and f_0 suppression close to or above 20 dBc.

With respect to quadrupler designs in hybrid technology, no works using GaN HEMTs have been reported so far. Only two alternative designs—based on other transistor technologies—with no conversion gain and reduced output power have been found in the literature [3,9]. The hybrid design in [3] ($f_c = 2.9$ GHz) uses a single SiGe HBT and the output frequency is above the device maximum operating frequency (10 GHz). Initially, output matching is achieved through a hairpin filter tuned to the fourth harmonic, but since it is not possible to reach the desired bandwidth, it was redesigned using two FD stages. Although the design method is not detailed, around 5 dBm of P_{out} are obtained. In [9] a one-stage hybrid quadrupler based on a GaAs pHEMT is presented, in which matching networks are optimized to achieve maximum G_{c4f_0} , resulting in a conversion gain of -0.7 dB and a HRR > 20 dB up to $6f_0$.

The majority of published quadruplers use Monolithic Microwave Integrated Circuits (MMICs) and are primarily based on other semiconductor technologies, mostly SiGe. No GaN-based MMIC quadrupler has been reported to date. These designs use a cascaded two-stage FD topology and require additional amplifying stages to improve circuit performance, but they still show no positive conversion gain nor considerable output power. A first example of this kind of quadruplers is the one in [10], which works from 2.5 to 10 GHz of input frequency (f_0), thus covering three conversion bands with the aid of passband switching filters and obtaining a HRR > 30 dB. In [11] a quadrupler is designed—but only validated in simulations—that includes amplifier stages in the input, the output and between FDs, that works in the f_0 range from 5 to 20 GHz, providing 2 dBm of maximum P_{out} . In [12], a quadrupler working in the f_0 range from 5.25 to 6.75 GHz, as part of a quadrature transmitter, shows a measured P_{out} of 0 dBm and HRR > 40 dB. In that work, Load-Pull (LP) simulation is used to simultaneously optimize the output power and the harmonic rejection for the first FD. Using FDSOI CMOS technology, the circuit designed in [13] works for a f_c of 15 GHz and includes a PA at the second FD output to compensate for a 20 dB loss.

In this work the first design of a frequency quadrupler based on GaN transistors is proposed. Designed to up-convert from the S to the X band, while presenting conversion gain in narrowband, it uses a topology consisting on two cascaded FDs without the need for any amplifier stage. A microstrip prototype was fabricated in hybrid technology using two similar GaN packaged HEMTs. The circuit design is described in Section 2, including details for the inter-stage matching network (ISMN) and the higher frequency FD stage, for which an independent prototype was manufactured. Finally, in Section 3, the FD second stage and quadrupler measured performances are shown, in small- and large-signal (LS) regimes, in comparison to simulation predictions.

2. Frequency Multiplier Design

The frequency quadrupler design in this work is based on two cascaded FD stages and does not use any amplifier stage. The first FD stage up-converts from around $f_c = 2.45$ GHz, named FD1, and the second one from around $f_c = 4.9$ GHz, named FD2. Both FD stages were designed using the packaged 5W GaN HEMT TGF2977-SM from Qorvo, as well as the ADS simulator with the Qorvo-Modelithics transistor model and Modelithics passive components models. The block diagram of the frequency quadrupler can be seen in Figure 1. Initially, the two stages were independently designed and optimized, matched to $50\ \Omega$ in the input and the output, and their target terminations and cascaded performance were also evaluated in simulation. Then the quadrupler was built partially based on those FD designs but implementing an inter-stage matching network (ISMN), matching the FD1 output with the FD2 input.

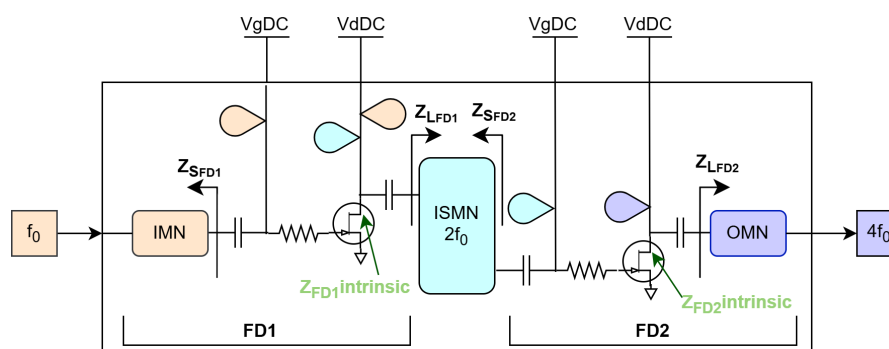


Figure 1. Frequency quadrupler block diagram consisting of two cascade frequency doublers.

A preliminary study was conducted in simulation to evaluate whether a G_{c4f_0} could be achieved with one single-stage circuit using the mentioned GaN HEMT. The maximum G_{c4f_0} obtained in simulation was below -10 dB, which could not be compensated by adding a PA working at around 10 GHz designed with the same active device, since its gain at this frequency would not overcome the single-stage quadrupler losses. However, a previous work with this transistor for a frequency doubler design at $f_0 = 2.45$ GHz [6] shows that more than 10 dB of G_{c2f_0} can be achieved. Hence, a cascade topology based on two frequency doublers is selected as the proposed solution.

2.1. Frequency Doubler Stage Design

In order to select the most appropriate HEMT bias point for each FD stage that provides the maximum G_{c2f_0} , a simultaneous sweep of the input RF power (P_{in}) and the gate DC voltage (V_{GS}), close to the threshold voltage (V_{th}), is performed with $50\ \Omega$ terminations and $Z_{L f_0}$ as a short circuit. As a result, G_{c2f_0} contours of each circuit are obtained.

Analyzing these contours it was possible to determine that the most appropriate bias point—in simulation—for both FDs was $V_{DS} = 32$ V and $V_{GS} = -3.1$ V, which corresponds to a DC drain current—in simulation—of $I_{dsDC} = 1.6$ mA. Figures 2 and 3 show the G_{c2f_0} contours as functions of P_{in} and V_{GS} at an input frequency of $f_0 = 2.45$ GHz and $f_0 = 4.9$ GHz, respectively. At this stage, it should be noted that under these load conditions ($50\ \Omega$), the maximum simulated G_{c2f_0} (6.2 dB at $f_0 = 2.45$ GHz and 1.2 dB at $f_0 = 4.9$ GHz) does not reach the expected range of values demonstrated in previous works [6]. However, when replacing the $50\ \Omega$ reference by the optimum Z_{L2f_0} that maximizes G_{c2f_0} , these values will increase considerably, as shown next.

Then, a second harmonic LP was performed, at the optimum bias settings discussed above, to replace the initial $50\ \Omega$ load for the Z_{L2f_0} that provides the maximum G_{c2f_0} . Through access to the internal nodes of the transistor compact model, and once the optimum Z_{L2f_0} are found, the corresponding second harmonic intrinsic target impedances in the

microstrip design ($Z_{2f_0}^{intrinsic}$) can be determined, which result in $Z_{2f_0}^{intrinsic} = 120 + 10j \Omega$ for FD1 and $Z_{2f_0}^{intrinsic} = 96 - 25j \Omega$ for FD2.

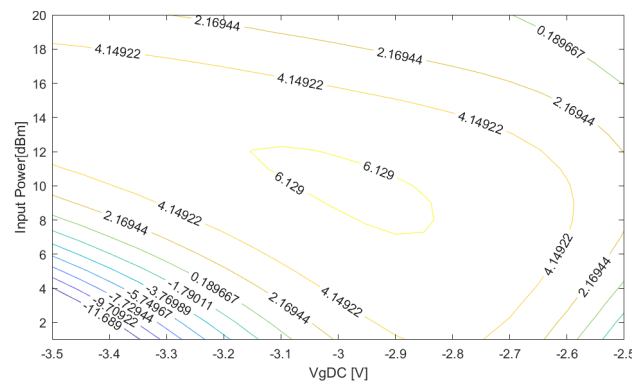


Figure 2. FD1 simulated G_{c2f_0} contours at the fundamental ($f_0 = 2.45$ GHz) vs. P_{in} and V_{GS} . The indexing variable in the curves is G_{c2f_0} [dB].

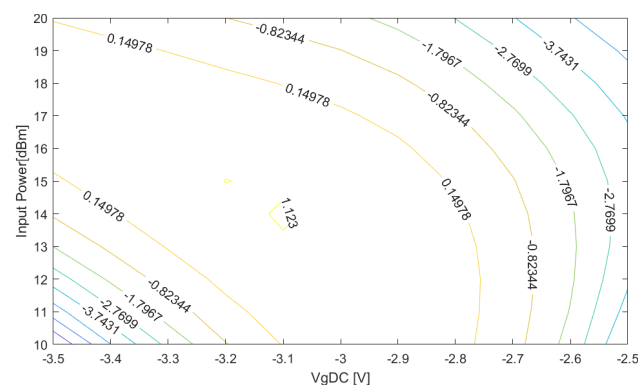


Figure 3. FD2 simulated G_{c2f_0} contours at the fundamental ($f_0 = 4.9$ GHz) vs. P_{in} and V_{GS} . The indexing variable in the curves is G_{c2f_0} [dB].

The next step was the design of the bias networks for both FDs, adding DC blocking capacitors to the circuits' input and output RF paths. Gate bias networks are based on a $\frac{\lambda_{@f_0}}{4}$ transmission line and radial stub in parallel (RF short circuit at f_0) while drain bias networks are based, correspondingly, on a $\frac{\lambda_{@2f_0}}{4}$ transmission line and radial stub in parallel (RF short circuit at $2f_0$), to drive the RF at f_0 towards each HEMT input and the RF signal at $2f_0$ towards each FD load. Moreover, in the case of FD1, it was necessary to add a second radial stub in the drain bias network to allow short circuiting the intrinsic Z_{f_0} when designing the output matching network. On the other hand, to filter out low-frequency undesired signals, RC filters were added in parallel in these networks.

To ensure HEMTs unconditional stability at small-signal conditions, a series resistor was added to each transistor gate, with the value of 5.6Ω for FD1 and 3Ω for FD2, since working at higher frequencies implies higher losses, which allowed the reduction in the FD2 stability resistor.

Figure 4 highlights the FD2 final bias and stabilization networks, along with input and output matching networks detailed next.

To reject the RF signal at f_0 at each FD output, a stub $\frac{\lambda_{@f_0}}{4}$, as shown in Figure 4, was added in the drain to short circuit $Z_{f_0}^{intrinsic}$. In addition, in FD1, it was necessary to include a transmission line before the stub to help achieve the target $Z_{f_0}^{intrinsic}$.

Now, the required Z_{L2f_0} was recalculated in order to provide the target $Z_{2f_0}^{intrinsic}$ for each FD, obtaining $Z_{LFD1} = 11 - 40j \Omega$ and $Z_{LFD2} = 30 - 30j \Omega$. Finally, the optimum source impedance (Z_S) for each FD was computed, forcing conjugate matching for maximum

power transfer ($Z_S = Z_{in}^*$), obtaining $Z_{S_{FD1}} = 10 - 8.5j \Omega$ and $Z_{S_{FD2}} = 14 + 27j \Omega$. To synthesize these impedances, output matching networks (OMNs) and input matching networks (IMNs) are designed in order to reduce reflections at desired frequencies when attaching 50Ω RF connectors.

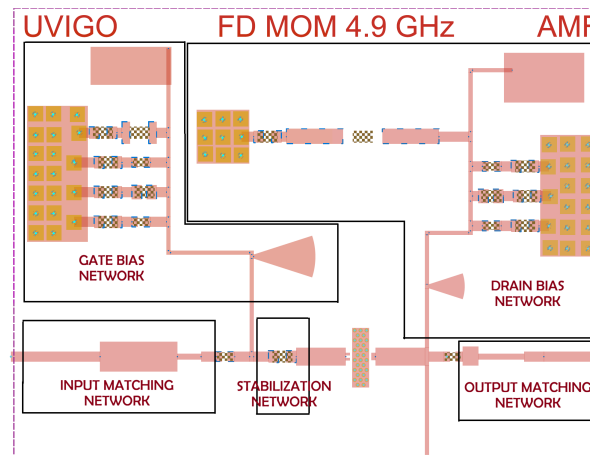


Figure 4. Layout of the FD2 with the different networks identified.

The FD1 IMN was obtained from a single microstrip transmission line with characteristic impedance $Z_0 = 20 \Omega$ showing transmission losses of less than 0.1 dB, and good return losses. Similar designs of FD1 using the same active device were carried out previously by the group [6] providing satisfactory results in terms of G_{c2f_0} and P_{out} , although adding circuit modifications to improve fundamental signal rejection. Therefore, its separate fabrication is not deemed necessary, since comparable performance is expected. Consequently, there is no need to design the FD1 OMN. However, the design of the FD2 was conducted from scratch, motivating the manufacturing and measurements of a FD2 prototype standalone, prior to its integration into the quadrupler. The IMN and OMN in FD2 are designed following the same methodology: using a transmission line to remove the reactive impedance component ($Z_0 = 24 \Omega$ at FD2 IMN and $Z_0 = 50 \Omega$ at FD2 OMN), and a $\frac{\lambda}{4}$ transformer with $Z_0 = 67 \Omega$ at FD2 IMN and a $\frac{\lambda}{4}$ transformer with $Z_0 = 78 \Omega$ at FD2 OMN.

Figure 5a includes the results of the P_{in} sweep simulations for FD1, including the IMN but directly specifying the optimum $Z_{L_{FD1}}$ previously computed. It shows an expected performance of more than 8 dB of maximum G_{c2f_0} and high suppression for f_0 and $3f_0$ signals, while not forcing suppression of the $4f_0$ component, the target signal at the output of the frequency quadrupler. In Figure 5b, the FD2 P_{in} sweep simulation results are shown. The expected maximum G_{c2f_0} exceeds 5 dB and presents a minimum fundamental suppression of 15 dB. The FD2 measured performance is analyzed in the next section.

2.2. Quadrupler Design

Once the FD2 has been manufactured and measured, showing a suitable performance in accordance with the one expected from simulations, the next step was the design of the complete quadrupler, taking into account the preliminary work carried out while designing each FD independently. Since the quadrupler topology implies cascading the two FD stages, an inter-stage matching network ISMN needs to be designed. Because the FD1 output and FD2 input operate at the same frequency ($f_c = 4.9$ GHz), a similar matching procedure as the one usually applied for cascaded PAs [14] was used.

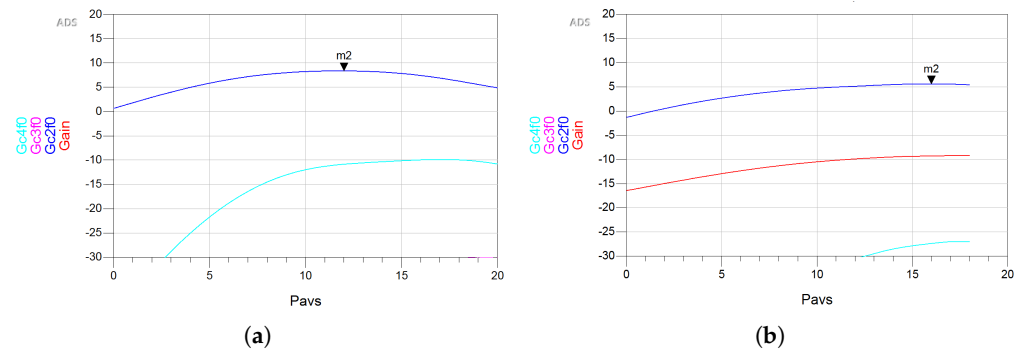


Figure 5. Simulated conversion gain up to the 4th harmonic vs. P_{in} (a) at f_0 2.45 GHz for FD1 design and (b) at f_0 4.9 GHz FD2 design. Curves not shown imply their value is below -30 dB.

Ideally, for maximum power transfer $Z_{OUT_{FD1}} = Z_{IN_{FD2}}^*$ is needed, so the inter-stage matching network is optimized as much as possible to reach that goal as well as minimizing the losses. The designed ISMN, whose schematic is shown in Figure 6, includes two microstrip transmission lines of which the simulated S-parameters are displayed in Figure 7, showing transmission losses at $f_0 = 4.9$ GHz of only 0.2 dB, and good return losses.

After placing the ISMN between FD1 and FD2, the impedances presented by this network to each FD can be computed in ADS and, as revealed in Figure 8, they are very close to the desired ones. Adjusting these impedances to more accurate values was a non-trivial optimization, since the approximation to the target $Z_{L_{FD1}}$ caused $Z_{S_{FD2}}$ to move away from the target value, and vice versa. Thus, when both the simulated frequency quadrupler inter-stage impedances were close to the target ones and the simulated performance showed higher G_{c4f_0} and P_{out} than the state-of-the-art proposals, the design procedure was concluded.

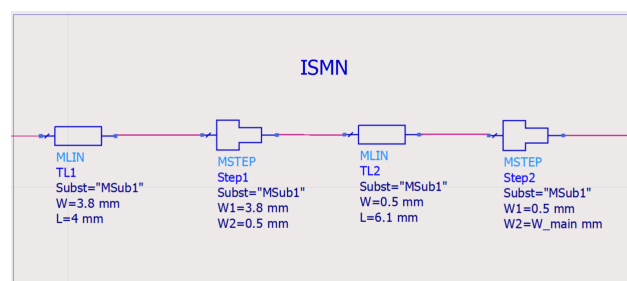


Figure 6. Quadrupler ISMN ADS schematic.

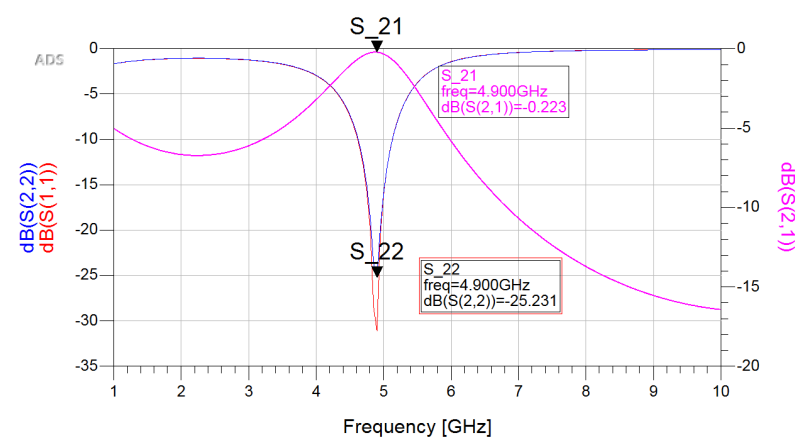


Figure 7. Simulated quadrupler ISMN S_{11} (red), S_{21} (magenta) and S_{22} (blue) S-parameters.

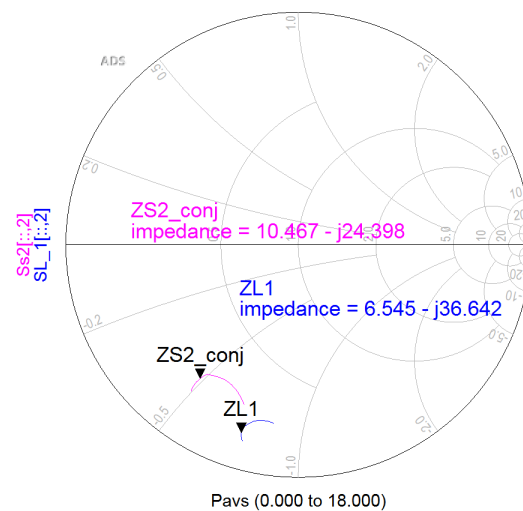


Figure 8. Impedances shown by the ISMN, in simulation, within the quadrupler circuit, pointing out where G_{c4f_0} is maximum.

3. Frequency Multipliers Prototypes RF Performance and Discussion

In Figure 9, photographs of the hybrid microstrip FD2 (dimensions 59.3 mm × 45.5 mm) and frequency quadrupler (dimensions 100 mm × 55 mm) prototypes are shown. The substrate used in both cases was 20 mil RO4003C, processed using laser milling, on which the GaN HEMT and the SMD passive components were assembled. Prototypes were mounted on a Cu heat-sink to reduce transistor heating. Both circuits were tested under small- and large-signal excitations, using corresponding test benches, at different bias points and fundamental frequencies.

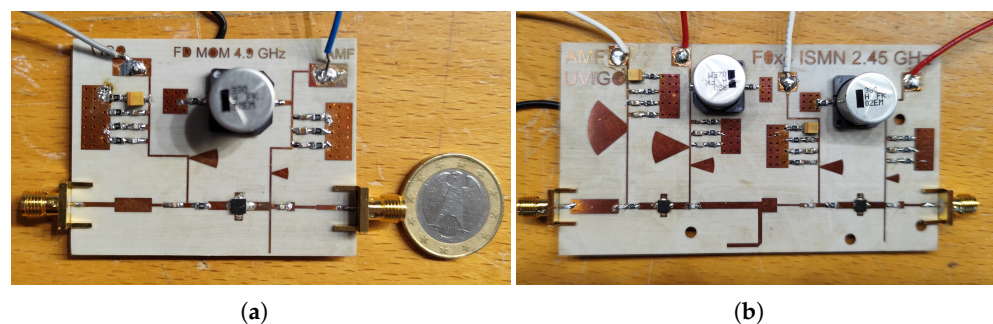


Figure 9. (a) Photograph of the hybrid FD2 microstrip prototype. (b) Photograph of the hybrid frequency quadrupler microstrip prototype.

To bias the HEMTs of the FD2 and the quadrupler while on the test bench, a two-channel DC power supply (Keithley 2602B) was used. From the discussion in Section 2, this allowed both HEMTs of the quadrupler prototype to be biased at the required, same, quiescent bias point.

Both prototypes were measured in small-signal regime using a test bench based on a vector calibrated VNA (P9377B) that allows the evaluation of the prototypes' S-parameters. Figure 10 shows the setup for large-signal (LS) measurements, consisting of a signal generator (E8257D: from 250 kHz to 20 GHz) to set the input fundamental frequency and RF power, and a spectrum analyzer (CXA N9000A: from 9 kHz to 26.5 GHz) that measures the received signal at fundamental and harmonics up to the fourth, in the case of the FD2 prototype, and up to the eighth in the case of the quadrupler, while performing a *Pin* sweep. In Figure 11 a diagram of the LS measurement system is included for clarity.

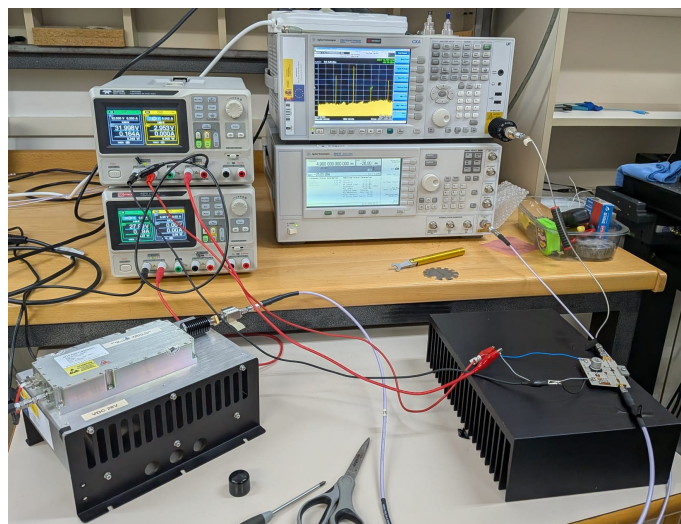


Figure 10. Large-signal microwave test bench used in this work.

The LS test bench includes a 50 dB gain driver amplifier, to increase the input signal power level to the desired level, since E8257D maximum power supplied is 15 dBm. A 6 dB attenuator and a circulator were added at the output of the driver amplifier to protect and enhance the driver amplifier performance. Moreover, a 30 dB attenuator at the input of the CNA decreases the DUT output signals so their level does not exceed the CNA maximum input power. The LS measurement system was calibrated at different frequencies and power levels by characterizing the gain of the input path and the attenuation of the output path. These calibration factors were subsequently applied so the prototypes' figures of merit were computed at DUT reference planes.

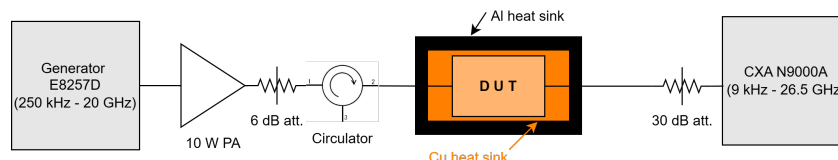


Figure 11. Diagram of the large-signal system used in this work for prototype measurements.

3.1. FD2 Prototype Measurements

The frequency doubler FD2 prototype was measured at a class B bias point, with $V_{DS} = 32$ V and $V_{GS} = -2.95$ V, corresponding to a I_{dDC} of around 1 mA. Figures 12 and 13 show the measured S_{11} and S_{21} S-parameters compared to the simulated values, respectively. These figures reveal a good matching performance, with a slight frequency deviation between measurements and simulations in the S_{21} response at 4.9 GHz, which may cause less suppression than expected. The circuit achieves almost -7 dB of input return losses at $f_0 = 4.9$ GHz and output suppression in that band, as intended by design.

Large-signal measurements were conducted by sweeping the P_{in} at the FD2 input. Figure 14a shows the measured and simulated transducer power gain at the fundamental frequency and the second harmonic conversion gain. It presents a maximum value of $G_{c2f_0} = 4.8$ dB, a measured higher fundamental frequency suppression than expected in the simulation and satisfactory results for conversion gain. Figure 14b presents the measured and simulated RF output power up to the fourth harmonic, revealing the same trends as in simulations, with a maximum measured P_{out} close to 25 dBm at $2f_0$ and 18 dBc of fundamental tone suppression, being higher at higher harmonics.

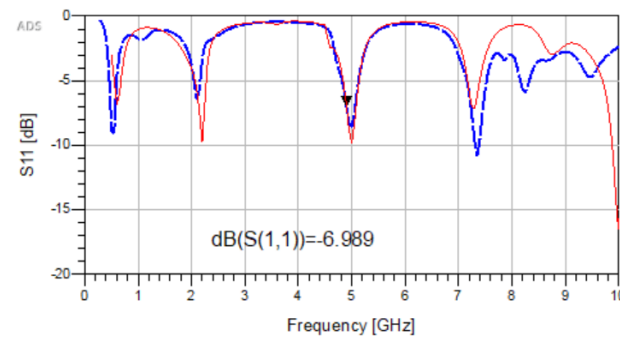


Figure 12. FD2 prototype simulated (continuous line) and measured (dashed line) small-signal S_{11} [dB] vs frequency [GHz].

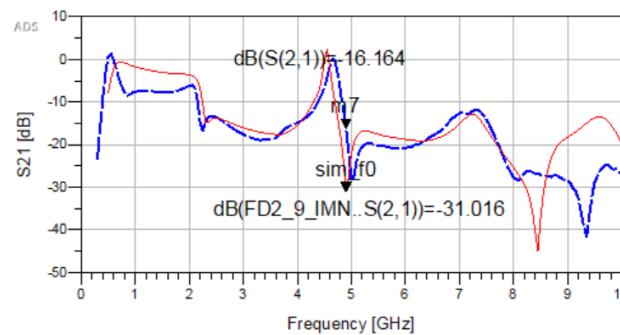


Figure 13. FD2 prototype simulated (continuous line) and measured (dashed line) small-signal S_{21} [dB] vs frequency [GHz].

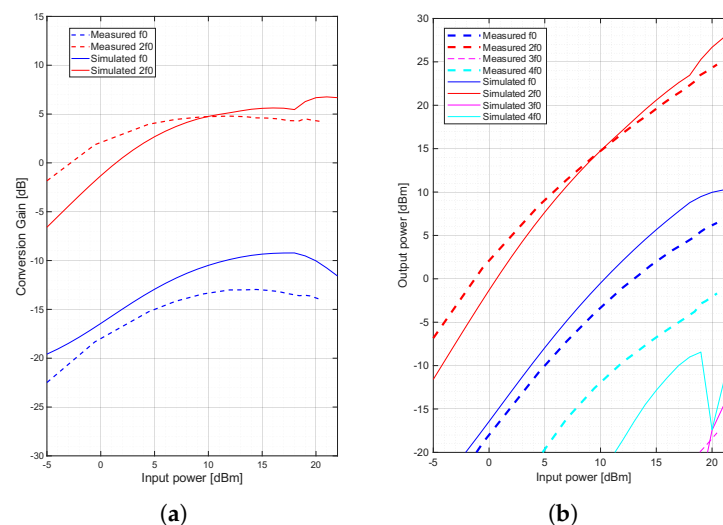


Figure 14. (a) FD2 prototype simulated (continuous line) and measured (dashed line) conversion gain (G_c) vs. P_{in} for the fundamental ($f_0 = 4.9$ GHz) and the second harmonic. (b) FD2 prototype simulated (continuous line) and measured (dashed line) P_{out} vs. P_{in} at the fundamental ($f_0 = 4.9$ GHz).

The higher measured fundamental suppression than expected from simulations can be attributed to several factors. First, the performance of the frequency multiplier is highly sensitive to the bias conditions of the transistor, and the bias point used in measurements can slightly differ from that in simulations. In addition, fabrication and component tolerances may contribute to observed discrepancies. Moreover, the nonlinear transistor model was not specifically optimized for the operating conditions associated with frequency multiplication. Nevertheless, the transistor model provides a sufficiently accurate representation

of the device behavior, enabling reliable prediction of the overall circuit performance and serving as a valuable design tool.

Finally, the DC drain current consumption of FD2 vs. P_{in} is shown in Figure 15, matching the simulation results, and with a maximum measured value of almost 200 mA at the highest measured input RF power.

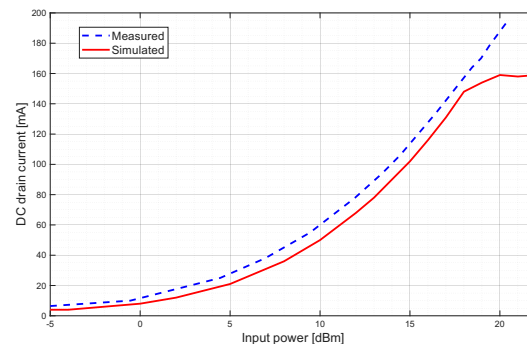


Figure 15. FD2 prototype simulated (continuous line) and measured (dashed line) I_{dDC} vs. P_{in} at the fundamental ($f_0 = 4.9$ GHz).

Table 1 compares the measured performance of the FD2 to the reported state-of-the-art hybrid frequency doublers. The designed frequency doubler in this work naturally does not reach the output power levels reported by other designs at lower f_0 and utilizing higher power transistor devices [4], though it exhibits positive conversion gain and a fivefold increase in output power over previous designs—based on GaAs—operating in the C band. Regarding harmonic suppression, it is important to note that this design prioritized maximizing output power and conversion gain over harmonic filtering. Consequently, while harmonic suppression is subject to optimization in future design iterations, the current results validate the design approach and the outstanding capabilities of GaN technology.

Table 1. Comparison of state-of-the-art hybrid frequency doublers from different technologies.

Refs.	[4]	[6] ⁽¹⁾	[4]	[5]	This Work
Transistor	SiC MESFET 10 W (CRF24010)	GaN HEMT 5 W (TGF2977-SM)	GaN HEMT 10 W (CH40010F)	GaAs MESFET (CFY25-20P)	GaN HEMT 5 W (TGF2977-SM)
ine f_c [GHz]	2	2.45	3.33	4.8	4.9
ine Max. Conversion Gain [dB]	~11	12.2	~15	-	4.79
Pout [dBm]	38	20.5	36.17	5	25
Min. Harmonic Suppression [dBc]	39.5	24.2	26.17	47	17.5

⁽¹⁾ Results from prototype C of the publication.

3.2. Frequency Quadrupler Prototype Measurements

Figure 16 shows the frequency quadrupler measured input return losses vs. frequency compared to simulated predictions, showing good agreement. At $f_0 = 2.45$ GHz, -22.2 dB of input return losses was obtained. Figure 17 shows the quadrupler measured S_{21} in dB, exhibiting frequency suppression in the 2.45–2.9 GHz band as well as around 4.9–5 GHz band, since the goal was also to minimize as much as possible the RF power of those unwanted signals.

It is important to note that the quadrupler prototype was tested at the same nominal bias point as in simulation, in addition to other close bias points, all around V_{th} . Due to the high sensitivity of active frequency multipliers—quadruplers in particular—to the active device bias point and V_{th} tolerances across packaged transistor lots, differences between the optimum bias point in measurements and simulation were expected. The best measured results were obtained for $V_{DS} = 32$ V and $V_{th} = -3$ V, which provided a $I_{dDC} = 0.5$ mA. The next figures show the results in large-signal regime using this optimum bias point.

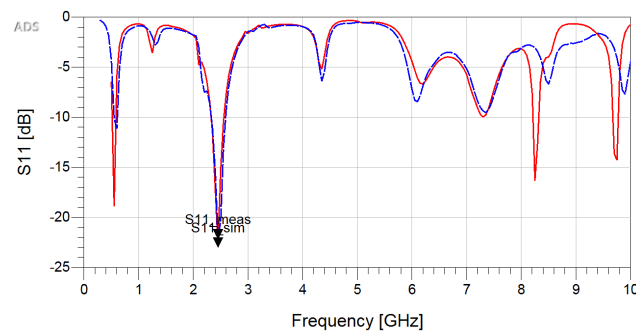


Figure 16. Quadrupler prototype simulated (red continuous line) and measured (blue dashed line) small-signal S_{11} [dB] vs. frequency [GHz].

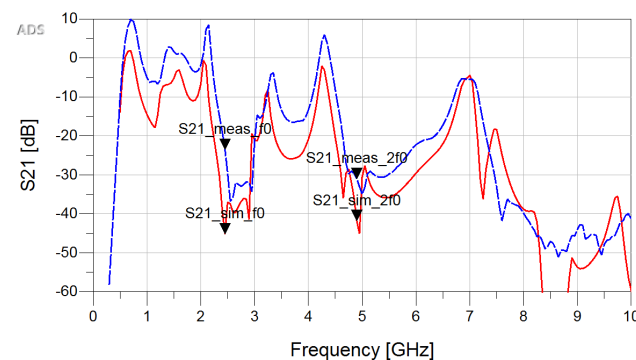


Figure 17. Quadrupler prototype simulated (red continuous line) and measured (blue dashed line) small-signal S_{21} [dB] vs frequency [GHz].

Figure 18a shows the G_c up to the fifth harmonic. At $f_0 = 2.45$ GHz, the maximum measured G_{c4f_0} was 10.75 dB which, although lower than predicted by simulations, is higher than the predictions obtained—in simulation—when designing a one-stage quadrupler with the same GaN HEMT; second harmonic suppression was 5.3 dBc. Figure 18b shows good suppression for the other undesired harmonics, above 15 dBc for $f_0 = 2.45$ GHz and above 20 dBc for the rest of measured harmonics. The maximum measured output power for the fourth harmonic reaches up to 26 dBm, slightly below the predicted value in simulation.

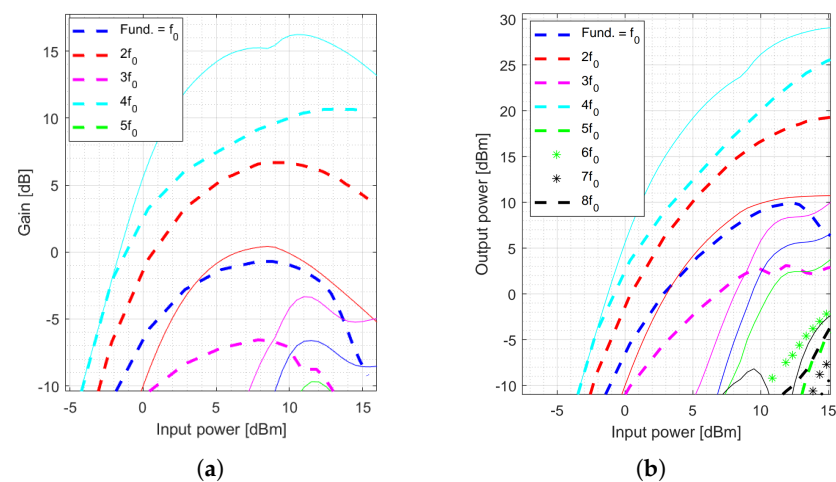


Figure 18. (a) Quadrupler prototype simulated (continuous line) and measured (dashed line) conversion gain (G_c) vs. P_{in} up to the fifth harmonic at the fundamental ($f_0 = 2.45$ GHz). (b) Quadrupler prototype simulated (continuous line) and measured (dashed line) P_{out} vs. P_{in} at the fundamental ($f_0 = 2.45$ GHz).

At $f_0 = 2.5$ GHz, the measured G_{c4f_0} improves by 3 dB with respect to the previous case, and second harmonic suppression reaches up to 14 dBc, hence closer to simulations, as can be seen in Figure 19a. Moreover, as shown in Figure 19b, 23.5 dBm of fourth harmonic output power are obtained and good harmonic suppression is achieved at higher order harmonics. Finally, the DC current consumption of both HEMTs in the quadrupler vs. P_{in} is shown, at $f_0 = 2.45$ GHz (Figure 20a) and $f_0 = 2.5$ GHz (Figure 20b), in this last case almost matching the predictions in simulation.

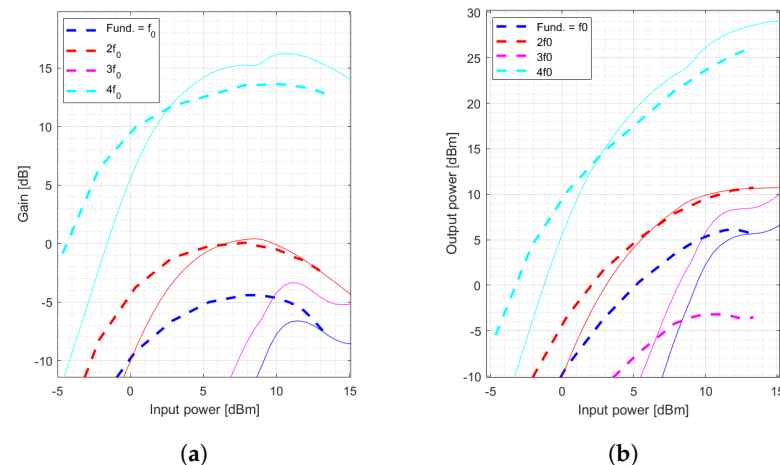


Figure 19. (a) Quadrupler prototype simulated (continuous line) and measured (dashed line) conversion gain (G_c) vs. P_{in} , up to the fourth harmonic, at the fundamental ($f_0 = 2.5$ GHz). (b) Quadrupler prototype simulated (continuous line) and measured (dashed line) P_{out} vs. P_{in} at the fundamental ($f_0 = 2.5$ GHz).

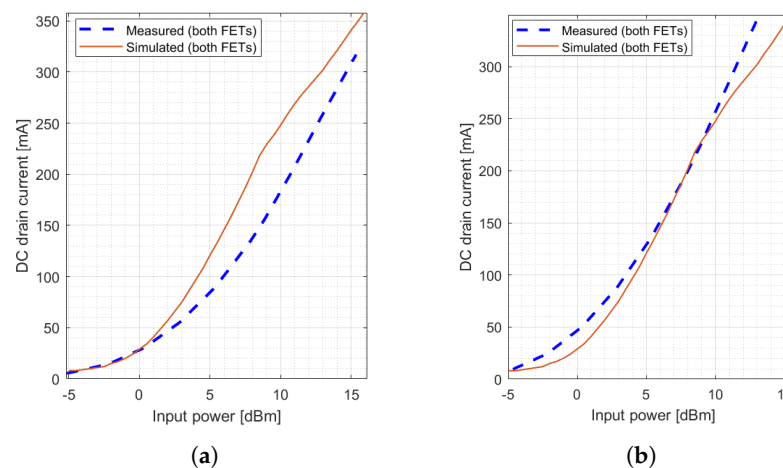


Figure 20. (a) Quadrupler prototype simulated (continuous line) and measured (dashed line) I_{dDC} (adding both HEMTs DC currents) vs. P_{in} at the fundamental frequency (a) $f_0 = 2.45$ GHz and (b) $f_0 = 2.5$ GHz.

Table 2 presents the measured performance of the quadrupler in this work in comparison to the state-of-the-art designs reported in the literature. This quadrupler exhibits a maximum positive conversion gain of 13.7 dB and an output power of 23.5 dBm at that P_{in} point, while measuring a maximum of 26 dBm of P_{out} at higher P_{in} . Notably, these results represent an improvement in output power compared to alternative semiconductor technologies, without requiring additional buffer amplification stages. Harmonic suppression—treated as a secondary metric during the design—is not yet optimal and remains subject to future inclusion of filtering structures, as the core objective at this stage was to maximize conversion gain and output power.

Table 2. Comparison of state-of-the-art frequency quadruplers from different technologies.

Refs.	[10]	[12]	[13]	[3]	[9]	This Work
Technology	MMIC	MMIC	MMIC	HMIC	HMIC	HMIC
Transistor	SiGe BiCMOS	SiGe BiCMOS	FD SOI	SiGe Bipolar (BFP740)	GaAs pHEMT (CE3520K3)	GaN HEMT (TGF2977-SM)
f_0 [GHz]	[2.5, 10]	[5.25, 6.75]	[13.72, 16.43]	[2.6, 3.2]	5	2.5
Stages	2	2	2	2	1	2
Buffer PA	Yes	Yes	Yes	No	No	No
Max Conversion Gain [dB]	0	<0	<0	<0	−0.7	13.7
Pout [dBm]	[−8, 1]	0	−	−	4.3	23.5
Min. Harmonic Suppression [dBc]	30	40	22.5	−	22	14

4. Conclusions

In this work an active frequency quadrupler based on GaN HEMTs is presented for the first time. Using packaged transistors and two cascaded frequency doubler stages without requiring any additional amplification stages, the designed hybrid microstrip quadrupler performs up-conversion in narrowband from the S band to the X band. The fabricated prototype shows positive fourth harmonic conversion gain ($G_{c_4f_0}$) in narrowband, reaching up to 13.7 dB at an input f_0 of 2.5 GHz as well as 23.5 dBm of output power, with $2f_0$ signal suppression of 14 dBc and fundamental f_0 suppression of 18 dBc. While the suppression of the fundamental frequency—which was not the primary focus of this work—could be further improved through the incorporation of additional filtering structures, such as band-pass or high-pass filters, or by employing additional harmonic control stubs, the proposed designs exhibit substantially superior output power and conversion gain compared to the state of the art. We believe that these performance improvements represent a meaningful contribution and demonstrate the strong potential of GaN HEMTs as a highly competitive technology for high-power, high-frequency and high even-order multiplication applications.

To achieve these quadrupler results, a careful design of an inter-stage matching network between the cascaded frequency doublers was conducted. Due to its critical impact on the final quadrupler performance, a standalone prototype of the second-stage doubler (FD2) was independently manufactured and measured as well, obtaining comparable results to the state-of-the-art frequency doublers and delivering five times more output power than other alternatives based on other semiconductor technologies in the C band.

It should be noted that, in all this work, a compact HEMT nonlinear model (HMT_QOR_TGF2977_SM_001) was used. Although this model is not originally optimized for this specific application and bias points, it performed quite well at high input power levels and the experimental results obtained from both prototypes successfully validate the proposed design approach.

Author Contributions: Conceptualization, A.M.-F. and M.F.-B.; methodology, A.M.-F.; validation, A.M.-F. and M.M.-B.; formal analysis, A.M.-F.; investigation, A.M.-F.; resources, A.M.-F. and F.M.-R.; data curation, A.M.-F.; writing—original draft preparation, A.M.-F.; writing—review and editing, M.F.-B., M.M.-B. and F.M.-R.; visualization, M.M.-B.; supervision, M.F.-B.; project administration, M.F.-B.; funding acquisition, M.F.-B. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by MICIU/AEI/10.13039/501100011033 under grants PID2020-116569RB-C33 and PID2023-147653OB-C33, the last one also funded by ERDF/EU.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Acknowledgments: The authors would like to thank Qorvo and Modelithics for the active and passive components models (under the University License Program) and the University of Cantabria for their collaboration on PCB processing.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

ADS	Advanced Design System
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CMOS	Complementary Metal Oxide Semiconductor
Cu	Copper
dB	Decibel
DC	Direct Current
DUT	Device Under Test
FD	Frequency Doubler
FDSOI	Fully Depleted Silicon On Insulator
GaN	Gallium Nitride
GaAs	Gallium Arsenide
G_c	Conversion Gain
GHz	Giga-Hertz
HBT	Heterojunction Bipolar Transistor
HEMT	High-Electron Mobility Transistor
HMIC	Hybrid Microwave Integrated Circuit
HRR	Harmonic Rejection Rate
IMN	Input Matching Network
ISMN	Inter-Stage Matching Network
LS	Large-signal
LP	Load-Pull
MESFET	Metal-Semiconductor Field-Effect Transistor
MMIC	Monolithic Microwave Integrated Circuits
OMN	Output Matching Network
PA	Power Amplifier
pHEMT	Pseudomorphic High-Electron-Mobility Transistor
P_{in}	Input Power
P_{out}	Output Power
RF	Radio-frequency
Si	Silicon
SiC	Silicon Carbide
SiGe	Silicon-Germanio
SMD	Surface-Mount Device
V_{DS}	Drain voltage
V_{GS}	Gate voltage
V_{th}	Threshold Voltage
VNA	Vector Network Analyzer
W	Watt

References

1. Satyam; Mritunjay, A.; Kumar, M.; Kumar, S.; Utkarsh; Islam, A. Emerging Potential of GaN HEMTs: Advancements, Challenges, and Future Prospects. In Proceedings of the 2025 International Conference on Communication and Smart Devices (ICCoSD), Ranchi, India, 25–26 July 2025; pp. 1–6. <https://doi.org/10.1109/ICCoSD66074.2025.11348371>.
2. Maas, S.A. *Nonlinear Microwave and RF Circuits*, 2nd ed.; Artech: Norwood, MA, USA, 1988.
3. López, Á.D.; Guardado, A.H.; Ambrojo, J.C.P. Frequency Multipliers Based on Hybrid Technology with High Harmonic Suppression. In Proceedings of the 2018 48th European Microwave Conference (EuMC), Madrid, Spain, 25–27 September 2018; pp. 1333–1336. <https://doi.org/10.23919/EuMC.2018.8541617>.

4. Yuk, K.; Branner, G.R.; Wong, C. High power, high conversion gain frequency doublers using SiC MESFETs and AlGaIn/GaN HEMTs. In Proceedings of the 2010 IEEE MTT-S International Microwave Symposium, Anaheim, CA, USA, 23–28 May 2010; pp. 1008–1011. <https://doi.org/10.1109/MWSYM.2010.5517565>.
5. Srivastava, S.; Gaddam, V.R.; Dhar, J.; Rao, C.V.N. Active Frequency Doubler at X-Band. In Proceedings of the 2022 IEEE Microwaves, Antennas, and Propagation Conference (MAPCON), Bangalore, India, 12–16 December 2022; pp. 272–276. <https://doi.org/10.1109/MAPCON56011.2022.10047101>.
6. Morales-Fernandez, A.; Marante-Boado, M.; Toimil-Cornado, P.; Fernandez-Barciela, M.; Martin-Rodriguez, F.; Tasker, P.J. Single-Ended and Balanced Frequency Doublers 2.45 to 4.9 GHz Using GaN FETs. In Proceedings of the 2024 54th European Microwave Conference (EuMC), Paris, France, 24–26 September 2024; pp. 1042–1045. <https://doi.org/10.23919/EuMC61614.2024.10732057>.
7. Yuk, K.; Wong, C.; Branner, G.R. Design of a high power x-band frequency tripler using a AlGaIn/GaN HEMT device. In Proceedings of the 40th European Microwave Conference, Paris, France, 28–30 September 2010; pp. 612–615. <https://doi.org/10.23919/EUMC.2010.5616156>.
8. Wang, F.; Clark, C.J.; Le, D.C. Design of a GaN HEMT High Efficiency High Power Frequency Tripler Using a Class-F Technique. In Proceedings of the 2020 IEEE Aerospace Conference, Big Sky, MT, USA, 7–14 March 2020; pp. 1–6. <https://doi.org/10.1109/AERO47225.2020.9172514>.
9. Zdemir, O.; Kartal, M. Design and Implementation of a K-Band Active Frequency Quadrupler with Low DC Power Consumption. In Proceedings of the 2022 FORTEI-International Conference on Electrical Engineering (FORTEI-ICEE), Riau, Indonesia, 11–12 October 2022; pp. 22–25. <https://doi.org/10.1109/FORTEI-ICEE57243.2022.9972929>.
10. Chung, H.; Ma, Q.; Rebeiz, G.M. A 10–40 GHz frequency quadrupler source with switchable bandpass filters and > 30 dBc harmonic rejection. In Proceedings of the 2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Honolulu, HI, USA, 4–6 June 2017; pp. 49–52. <https://doi.org/10.1109/RFIC.2017.7969014>.
11. Sokol, M.; Galajda, P.; Jurik, P.; Pospisil, M. Frequency Quadrupler for Ultra-Wideband mm-Wave M-Sequence Transceiver. In Proceedings of the 2023 33rd International Conference Radioelektronika (RADIOELEKTRONIKA), Pardubice, Czech Republic, 19–20 April 2023; pp. 1–5. <https://doi.org/10.1109/RADIOELEKTRONIKA57919.2023.10109061>.
12. Ozdag, C.; Paidimarri, A.; Yoshiyama, M.; Yamaguchi, Y.; Tojo, Y.; Sadhu, B. A 21–27-GHz Frequency Quadrupler in 0.13 μm SiGe BiCMOS with 0-dBm POUT and 40-dBc HRR for Wideband 5G Applications. In Proceedings of the 2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Washington, DC, USA, 16–18 June 2024; pp. 55–58. <https://doi.org/10.1109/RFIC61187.2024.10599982>.
13. Darban, M.S.; Ha, D.S.; Walling, J.S. Low-Power mm-Wave Frequency Quadrupler Using Deep Class-C Doublers. In Proceedings of the 2024 19th European Microwave Integrated Circuits Conference (EuMIC), Paris, France, 23–24 September 2024; pp. 391–394. <https://doi.org/10.23919/EuMIC61603.2024.10732574>.
14. Abkenari, M.R.; Tayarani, M.; Abdipour, A.; Kiumarsi, H. A Novel Method to Design Interstage Matching Network in the Smith Chart. In Proceedings of the 2006 IEEE International Conference on Semiconductor Electronics, Kuala Lumpur, Malaysia, 29 November–1 December 2006; pp. 776–780. <https://doi.org/10.1109/SMELEC.2006.380742>.

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.