

Article

A Novel High-Frequency Simulation Methodology for IBIS Models Utilizing Verilog-AMS Dynamic Parameter Compensation

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Abstract

Conventional I/O Buffer Information Specification (IBIS) models often suffer from reduced fidelity in high-speed signaling because their static table-lookup mechanism cannot accurately reproduce complex transient I/O-buffer dynamics. To address this limitation, this study proposes a Verilog-AMS-based dynamic parameter compensation method. First, the conventional IBIS model is reformulated into a three-layer architecture comprising a data interface layer, an intermediate variable computation layer, and a port response synthesis layer. Then, based on Kirchhoff's current law (KCL), the monotonic dependence of the output voltage on the pull-up and pull-down driving factors, k_{pu} and k_{pd} , is analytically derived to provide a directional criterion for parameter correction. Building on this criterion, a pulse-width-driven compensation algorithm is developed by constructing a pulse-width-indexed dual-factor empirical adjustment matrix and detecting the pulse width of the input bitstream in real time during transient simulation. The detected pulse width is then used to dynamically update k_{pu} and k_{pd} , enabling the IBIS response to converge toward the transistor-level SPICE reference waveform. Three representative device models were evaluated at 666 Mbps and 1.302 Gbps using pseudo-random binary sequence excitation, and the model fidelity was quantified using the normalized mean square error (NMSE). The proposed method reduced the NMSE from -6.73 to -1.03 dB before compensation to -54.79 to -44.19 dB after compensation, demonstrating a substantial improvement in high-frequency IBIS modeling fidelity and confirming the robustness and adaptability of the pulse-width-aware dynamic compensation strategy under random high-speed excitation.

Keywords: IBIS model; Verilog-AMS; high-frequency signal integrity; dynamic driving-factor correction; pulse-width identification



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1. Introduction

As clock frequencies and integration densities continue to increase, signal-integrity (SI) issues—such as signal distortion, timing jitter, electromagnetic coupling, reflections, crosstalk, and inter-symbol interference (ISI)—have become major constraints on the performance and reliability of high-speed electronic systems [1]. Modern interfaces, including PCI Express, USB, and DDR5, commonly operate at gigabit-per-second data rates, where even small modeling errors can degrade eye-diagram opening and increase the bit error rate (BER) [2,3]. Above 20 Gb/s, conventional board- and package-level SI analysis methods have been reported to struggle to maintain sufficient accuracy [4]. Because input/output

(I/O) buffers form the electrical interface between the silicon die and the external channel, accurate modeling of their transient behavior is essential for credible system-level SI simulation [5–7].

The I/O Buffer Information Specification (IBIS) has become a widely used behavioral modeling format for board-level SI analysis because it offers low computational cost, protects device-level intellectual property, and supports multi-vendor simulation workflows [8]. Since its ratification in 1993, the IBIS standard has evolved to include constructs such as Series MOSFET and Composite Current for complex signaling modes, including differential signaling and dynamic on-die termination (ODT) [9,10]. In applications such as DDR4 interface simulation, IBIS models can provide error margins within 2% while running approximately an order of magnitude faster than full SPICE simulations. However, conventional IBIS models are built primarily on static current-voltage (I-V) and voltage-time (V-T) lookup-table interpolation. Consequently, they cannot adequately capture frequency-dependent parasitics, nonlinear overshoot, carrier transit delays, gate-charge redistribution, or substrate coupling effects at gigabit-per-second data rates [11–13]. This limitation increasingly separates the IBIS response from the physical device response, particularly above the Gb/s range [14,15].

Several approaches have been proposed to improve IBIS accuracy under high-frequency or overclocked conditions. Early methods added passive filters or empirical delay elements to the IBIS periphery, but they relied heavily on parameter tuning and provided limited physical insight [9,16]. Wideband behavioral models based on frequency-domain fitting, including vector fitting (VF), can approximate driver output impedance but may introduce causality or passivity issues in time-domain simulation [16,17]. Hybrid IBIS-SPICE macromodels can improve fidelity, yet stitching table-based and transistor-level representations without artifacts remains challenging [5,7,12,13]. HDL-based reconstruction offers another route for extending IBIS behavior, but its correction mechanism still needs to remain compatible with standard EDA workflows [18,19].

Representative studies include the two-port grey-box and aliasing-abstraction models reported by Dghais et al., [9,11] the pre-delay compensation workflow for SDRAM interfaces proposed by Liu et al. [20], and the slew-rate or driving-factor correction strategies reported by Ding and co-workers [21,22]. Artificial-neural-network-based I/O-buffer models have also been investigated [23]. Recent signal-integrity studies have further emphasized data-driven and system-level modeling, such as complex-valued neural-network surrogate models for SI applications [24] and multimodal machine-learning-based surrogate modeling for high-speed link systems [25]. Collectively, these studies show that IBIS and high-speed signal-integrity modeling have evolved from conventional static table lookup toward mixed-signal abstraction, delay- and slew-rate-aware correction, data-driven surrogate modeling, and system-level prediction. These developments indicate that further enhancement of IBIS-based I/O-buffer models requires a modeling framework capable of incorporating both analog transient behavior and event-dependent parameter updates.

Verilog-AMS provides a suitable framework for enhancing IBIS models because it supports both continuous-time analog dynamics and discrete digital events [19]. Its mixed-signal modeling capability allows differential-algebraic relationships, event-triggered operations, and nonlinear time-varying effects to be directly incorporated into behavioral models, thereby reducing reliance on static lookup-table approximations. Since IBIS Version 4.1, Verilog-AMS and VHDL-AMS have been incorporated into the extensible IBIS framework, allowing conventional table-based models to be enhanced while preserving the computational efficiency and intellectual-property protection advantages of IBIS [8]. In I/O-buffer modeling, Verilog-AMS is therefore well suited for describing edge-rate degradation, power-supply-noise-induced effects, and gate modulation behavior [26].

Although previous Verilog-AMS-based studies have made important contributions to enhancing the behavioral expressiveness and physical interpretability of IBIS models, the pulse-width-dependent distortion occurring under arbitrary random bit-stream excitation still requires further investigation. Ning et al. demonstrated that a Verilog-AMS-centered optimization strategy can improve IBIS overlocking simulation by explicitly defining circuit-level variables within the IBIS structure and constructing a more physically grounded behavioral model, achieving a 21.7% improvement in overlocked simulation accuracy with only a 2.2% increase in CPU time [18]. Recent Verilog-AMS behavioral modeling studies have also shown its usefulness in analog/mixed-signal virtual testing and system-level verification, where parameterized behavioral models are used to represent circuit-level behavior before physical-chip validation [27]. These studies confirm the effectiveness of introducing Verilog-AMS into IBIS model enhancement. However, in random bit streams, the effective pulse width varies continuously with the local bit pattern, and narrow pulses may induce different degrees of amplitude collapse, overshoot, undershoot, edge delay, and recovery distortion. These distortions are device-dependent and may require different correction directions and magnitudes for the pull-up and pull-down paths under different pulse widths and transition polarities. Therefore, how to associate correction coefficients with real-time pulse-width information and transition polarity during transient simulation remains a key issue for high-frequency IBIS model compensation.

Accordingly, this paper proposes a Verilog-AMS-based dynamic parameter compensation method for high-fidelity IBIS simulation. The conventional IBIS model is first reconstructed into three functional layers: a data interface layer, an intermediate variable computation layer, and a port response synthesis layer. The monotonic dependence of the output voltage waveform on the key driving factors k_{pu} and k_{pd} is then analytically derived and used to determine the direction of parameter correction. Based on this criterion, a pulse-width-aware adaptive tuning mechanism is developed. During transient simulation, the pulse width of the input bit stream is detected in real time and used to retrieve pre-calibrated coefficients for in situ correction of the driving factors, thereby driving the IBIS transient response toward the transistor-level SPICE reference.

Compared with existing methods, the proposed approach offers four main advantages. First, the compensation logic is embedded directly in the Verilog-AMS description of the IBIS model and does not require modifications to the simulator kernel or external co-processing modules. Second, the correction direction is guided by monotonicity analysis, reducing reliance on heuristic or blind parameter searches. Third, real-time pulse-width detection allows the method to adapt to arbitrary random bit sequences rather than predefined excitation patterns or specific interface standards. Fourth, the dual-factor co-regulation mechanism enables stronger correction of nonlinear distortion under ultra-narrow pulse conditions. Simulation experiments on three functionally distinct integrated circuit devices show that the proposed method substantially improves IBIS simulation accuracy while maintaining low implementation complexity.

2. Traditional Methods

Architecture of the Conventional IBIS Model

The conventional IBIS model is a quasi-static, table-based behavioral model used to describe the external electrical response of an I/O buffer. Instead of solving transistor-level semiconductor equations, it approximates buffer behavior by interpolating pre-characterized current-voltage (I-V) and voltage-time (V-T) data. Therefore, its simulation accuracy depends strongly on how well these lookup tables capture the steady-state and switching characteristics of the relevant circuit branches.

As shown in Figure 1A, the conventional IBIS topology is centered on the output pad node, which is connected to four nonlinear I-V branches: [Pullup], [Pulldown], [Power Clamp], and [GND Clamp]. The model also includes the equivalent die capacitance [C_comp] and the package parasitic resistance–inductance–capacitance (RLC) network. These elements jointly define the external electrical behavior of the I/O buffer and provide the structural basis for IBIS behavioral modeling, in which lookup-table-derived data are mapped onto the corresponding branch characteristics. Specifically, [Pullup] and [Pulldown] describe the source and sink drive strengths, [Power Clamp] and [GND Clamp] characterize electrostatic discharge clamp paths, [Ramp] defines the logic transition rate, and [Rising Waveform] and [Falling Waveform] describe the transient profiles of the output edges. The figure also denotes the reference potentials associated with each branch (P_{Uref} , P_{Dref} , P_{Cref} , G_{Cref}), which determine the biasing conditions applied to the corresponding port voltages.

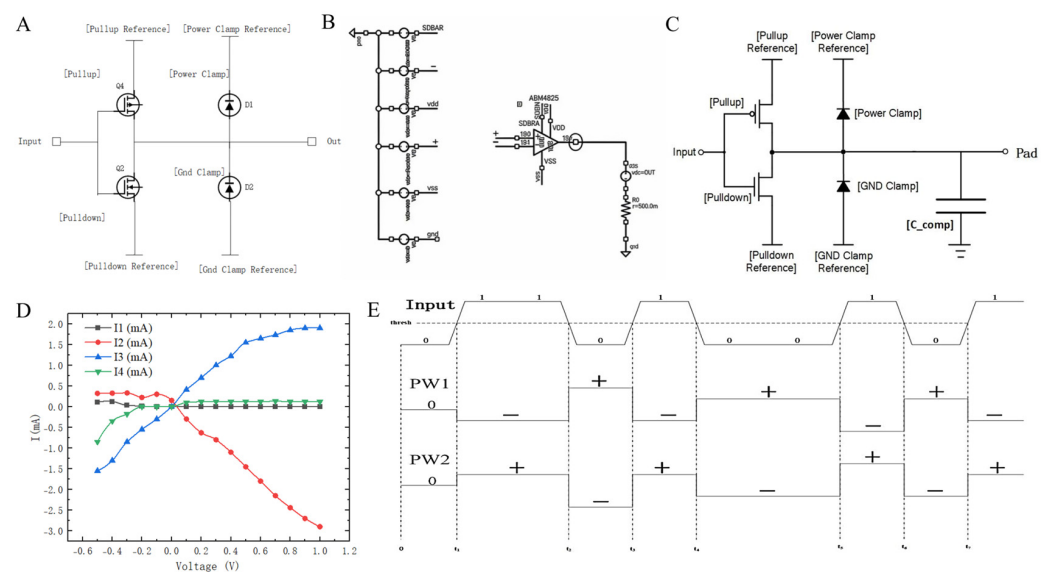


Figure 1. (A) Constituent Components of the Conventional IBIS Model; (B) Circuit Diagram for Measuring [GND Clamp] I-V; (C) Conceptual Diagram of Verilog-AMS-Based IBIS Model; (D) Data Points for Device 1 Keywords; (E) Timing Diagram Illustrating Input Bitstream and the Associated Pulse Width Detection Logic.

During IBIS simulation, the simulator continuously monitors the port voltage and uses it as the index for I-V table lookup. The corresponding branch currents are obtained by linear interpolation, while the switching behavior is described by the [Ramp] and [Waveform] data. These branch currents are then assembled into the output-node equation according to Kirchhoff's current law, and the node voltage is solved iteratively. In this way, the conventional IBIS workflow can be summarized as a voltage-to-table-to-current loop: operating condition setting, port-voltage monitoring, table lookup, branch-current interpolation, KCL equation formulation, and output-voltage solving. This mechanism provides high computational efficiency, but its reliance on static lookup data limits its ability to represent high-frequency dynamic effects.

The main IBIS tables are typically extracted from transistor-level SPICE simulations. The [GND Clamp] I-V data are obtained by applying a DC sweep to the output terminal while the driver is disabled or placed in a high-impedance state, so that the measured current mainly reflects the ESD clamp path. To cover both overshoot and undershoot conditions, the sweep range generally extends from $-V_{DD}$ to $2V_{DD}$, as illustrated in Figure 1B. By contrast, the [Pullup] and [Pulldown] tables are extracted by forcing the buffer into a defined output state and sweeping the pad voltage. For [Pulldown] extraction,

the output is set to the low state and the sink current is measured as the pad voltage increases (Figure S1A). For [Pullup] extraction, the output is set to the high state and the source current is recorded as the pad voltage approaches VDD; the shunt current from the power-clamp branch should be subtracted to obtain the intrinsic pull-up characteristic (Figure S1B). Finally, [C_comp] is determined from AC simulation by calculating the equivalent input capacitance from the imaginary component of the measured current, the AC excitation frequency, and the excitation amplitude.

$$C_{comp} = C_{IN} - C_{Package} \quad (1)$$

$$C_{comp} = -\frac{(\text{Im}_{I_{ac}})}{2 \times \pi \times f \times V_{AC}} \quad (2)$$

In the formula, $\text{Im}_{I_{ac}}$ represents the imaginary part of the measured current, f represents the frequency of the AC power source, and V_{AC} represents the amplitude of the AC power source.

Collectively, these extracted I-V, V-T, and capacitance parameters form the basis of conventional IBIS behavioral simulation. However, because they are derived from static or pre-characterized conditions, they cannot fully capture pulse-width-dependent nonlinear effects under high-frequency excitation. This limitation motivates the subsequent monotonicity analysis and dynamic parameter compensation strategy developed in this work.

3. Innovative Method

3.1. Verilog-AMS-Based IBIS Model

To enable dynamic parameter compensation while preserving the computational efficiency of conventional IBIS simulation, the original IBIS model was reconstructed within a Verilog-AMS framework. As shown in Figure 1C, the reconstructed model comprises three functional layers with a clear data flow: the data interface layer, the intermediate variable computation layer, and the port response synthesis layer. The data interface layer maps the discrete I-V/V-T lookup tables in the IBIS file into Verilog-AMS array structures and provides continuous interpolation through the *\$table_model* function. The intermediate variable computation layer dynamically solves the pull-up and pull-down driving factors (k_{pu} and k_{pd}), using transient response equations under two load conditions. The port response synthesis layer then integrates the current contributions of all branches according to Kirchhoff's current law (KCL) to generate the output waveform. In addition, pulse-width detection and adaptive coefficient-update modules are incorporated into the framework to enable real-time adjustment of the driving factors during transient simulation. This layered design balances model accuracy and simulation efficiency while providing the structural basis for subsequent parameter adjustment.

3.1.1. Data Interface Layer

This layer is responsible for mapping the discrete data tables described in the IBIS text into multidimensional array structures compatible with Verilog-AMS and provides continuous interpolation services to the upper layers through the *\$table_model* system function. Taking the [POWER Clamp] keyword as an example, the voltage and current data are stored as V_{pc} data and I_{pc} data, respectively. The branch current can then be obtained using the function call *\$table_model* ($V(pc)$, V_{pc} data, I_{pc} data, "1L"), where the parameter "1L" indicates linear interpolation within the query boundaries and linear extrapolation outside the boundaries. For other key data tables such as [Pullup], [Pulldown], and [GND Clamp], the same array mapping and interface encapsulation strategy is adopted.

3.1.2. Intermediate Variable Calculation Layer

The parameters k_{pu} and k_{pd} quantify the nonlinear current transport capabilities of the pull-up and pull-down driver networks, respectively, and are core regulating factors influencing the dynamic evolution of the waveform. Their values can be obtained by solving circuit constraint equations under two different load conditions. As shown in Figure 1C, by switching the far end of the reference resistor R to the P_{Uref} potential (Condition 1) and the P_{Dref} potential (Condition 2), the corresponding transient output voltages $V_{out1} = V_1(t)$ and $V_{out2} = V_2(t)$ can be observed, thereby constructing a system of equations:

$$I_{out1} = k_{pu} \cdot I_{pu1} + k_{pd} \cdot I_{pd1} + I_{pc1} + I_{gc1} \quad (3)$$

$$I_{out2} = k_{pu} \cdot I_{pu2} + k_{pd} \cdot I_{pd2} + I_{pc2} + I_{gc2} \quad (4)$$

where I_{out1} , I_{pu1} , I_{pd1} , I_{pc1} , and I_{gc1} denote the branch currents under Load Condition 1; I_{out2} , I_{pu2} , I_{pd2} , I_{pc2} , and I_{gc2} denote the corresponding currents under Load Condition 2. The circuit used for calculating k_{pu} and k_{pd} is shown in Figure 1C, where R is a load with known impedance. V_f is set to P_{Uref} corresponding to Load Condition 1, and V_f is set to P_{Dref} corresponding to Load Condition 2. Therefore,

$$I_{out1} = \frac{V_{out1} - P_{Uref}}{R} \quad (5)$$

$$I_{out2} = \frac{V_{out2} - P_{Dref}}{R} \quad (6)$$

Let $V_{out1} = V_1(t)$, $V_{out2} = V_2(t)$, where $V_1(t)$ and $V_2(t)$ are functions of time t with known forms. The remaining current values in the two equations can all be obtained using the *\$table_model* function.

After solving the equations, we obtain:

$$k_{pu} = g(t) \quad (7)$$

$$k_{pd} = h(t) \quad (8)$$

3.1.3. Port Response Synthesis Layer

At the output pad node, according to Kirchhoff's Current Law, the branch currents satisfy:

$$I(pc) + I(pu) - I(pd) - I(gc) = 0 \quad (9)$$

In the Verilog-AMS syntax environment, the current contributions of each branch are described as:

$$I(pc) < + - \$table_model(V(pc), Vpc_data, Ipc_data, "1L") + C_comp_pc * ddt(V(pc)) \quad (10)$$

$$I(pu) < + - k_{pu} * \$table_model(V(pu), Vpu_data, Ipu_data, "1L") + C_comp_pu * ddt(V(pu)) \quad (11)$$

$$I(pd) < + - k_{pd} * \$table_model(V(pd), Vpd_data, Ipd_data, "1L") + C_comp_pd * ddt(V(pd)) \quad (12)$$

$$I(gc) < + - \$table_model(V(gc), Vgc_data, Igc_data, "1L") + C_comp_gc * ddt(V(gc)) \quad (13)$$

where $<+$ is the symbol used in Verilog-AMS language for assigning current or voltage quantities, and $ddt()$ represents taking the derivative of the function inside the parentheses with respect to time t . The terms [C comp pc], [C comp pu], [C comp pd], and [C comp gc] represent the capacitance components assigned to the power-clamp, pull-up, pull-down,

and ground-clamp branches, respectively. The simulation output $V(\text{Pad})$ is implicitly solved from Kirchhoff's current law.

$$I(pc) + I(pu) - I(pd) - I(gc) = 0 \quad (14)$$

$$V(pc) = pcref - V(pad) \quad (15)$$

$$V(pu) = puref - V(pad) \quad (16)$$

3.2. Analysis of Key Parameters Exhibiting Monotonic Relationship with Output Waveform

To avoid empirical blind searching, this method performs a rigorous monotonicity analysis as the basis for the compensation strategy. To establish the quantitative relationship between the output waveform and the key parameters k_{pu} and k_{pd} , function fitting is first performed on the I-V characteristics of each branch in the IBIS model. For the data tables in [Power Clamp], [Pullup], [Pulldown], and [GND Clamp], let their voltage columns and current columns be x_i and y_i , respectively. The least squares method is used to fit and obtain the functional relationships h_1, h_2, h_3, h_4 :

$$I_{pc} = h_1(V(pc)) \quad (17)$$

$$I_{pu} = h_2(V(pu)) \quad (18)$$

$$I_{pd} = h_3(V(pd)) \quad (19)$$

$$I_{gc} = h_4(V(gc)) \quad (20)$$

According to Kirchhoff's Current Law, the output node satisfies:

$$I(pc) + I(pu) - I(pd) - I(gc) = 0 \quad (21)$$

Substituting the expressions for each branch current and considering the influence of the compensation capacitor C_{comp} , the differential equation for the output voltage $V = V(\text{Pad})$ can be obtained:

$$C \frac{dV}{dt} = h_1(PC_{ref} - V) - k_{pu}h_2(PU_{ref} - V) - k_{pd}h_3(V - PD_{ref}) - h_4(V - GC_{ref}) \quad (22)$$

where $C = C_{comp_pc} + C_{comp_pu} + C_{comp_pd} + C_{comp_gc} > 0$.

For specific devices, linear approximation of the I-V data can be performed to simplify the analysis. Taking Device 1 (TPS53317) as an example, the data points of [Power Clamp], [Pullup], [Pulldown], and [GND Clamp] are plotted in a coordinate system (Figure 1D).

In the range of 0~0.5 V, each curve approximates a straight line, and the fitting yields:

$$I_1 \approx 0 \quad (23)$$

$$I_2 \approx -3V(pu) \quad (24)$$

$$I_3 \approx 3V(pd) \quad (25)$$

$$I_4 \approx 0 \quad (26)$$

Substituting into Equations (3)–(21) and solving the differential equation, under the approximation that $C \approx 0$, we obtain:

$$V \approx V_0 \frac{x}{x+y} \quad (27)$$

Further, the partial derivatives are obtained:

$$\frac{\delta V}{\delta x} = \frac{V_0 y}{(x + y)^2} > 0 \quad (28)$$

$$\frac{\delta V}{\delta y} = \frac{V_0 y}{(x + y)^2} < 0 \quad (29)$$

Therefore, for Device 1, the output voltage V is a monotonically increasing function of k_{pu} and a monotonically decreasing function of k_{pd} . This monotonicity conclusion provides a clear direction for parameter adjustment: if the IBIS output is higher than the SPICE reference, k_{pu} should be decreased or k_{pd} increased; conversely, k_{pu} should be increased or k_{pd} decreased. The same derivative-based procedure is used for other devices to determine the sign of compensation before coefficient calibration, avoiding blind empirical search.

The $C \approx 0$ approximation is used only to derive a local monotonicity criterion and is not used in the actual Verilog-AMS transient simulation, where the Ccomp-related ddt() terms are retained. This approximation introduces a quasi-static error by neglecting the capacitive current and package RLC-induced dynamic effects. As the pulse width becomes ultra-narrow, the increased dV/dt amplifies this error, so the simplified expression can no longer accurately predict the correction magnitude or convergence speed. It is therefore used only to determine the initial correction direction, whereas the final compensation coefficients are obtained through SPICE-referenced pulse-width calibration. This also explains why dual-factor co-regulation is required when single-parameter correction becomes insufficient under very short pulse excitation.

3.3. Empirical Parameter Adjustment Based on Single Pulse

The single-pulse unit is used for coefficient calibration, with Type-010 and Type-101 pulses treated separately. Pulse Width (PW) is defined as the duration for which the high or low level is maintained. For a specific pulse width PW, SPICE reference simulation and unoptimized IBIS simulation are run separately to obtain comparative waveforms W_{SPICE} and W_{IBIS} . Based on the relative amplitude relationship between the two, combined with the monotonicity criterion determined in Section 3.2, eight parameter correction strategies can be summarized, as listed in Table 1. In the table, x denotes k_{pu} , and y denotes k_{pd} . Operations such as $x \times \alpha$ indicate multiplicative scaling, whereas $x + \beta$ denotes additive offset compensation ($0 < \alpha < 1$, $\beta > 0$).

Table 1. Independent Variable Adjustment Methods.

Transition Condition	$W_{IBIS} > W_{SPICE}$	$W_{IBIS} < W_{SPICE}$
$\frac{\delta V}{\delta x} > 0, \frac{\delta V}{\delta y} > 0$	$x \rightarrow \alpha_1 x$ $y \rightarrow \alpha_2 y$	$x \rightarrow x + \beta_1$ $y \rightarrow y + \beta_2$
$\frac{\delta V}{\delta x} > 0, \frac{\delta V}{\delta y} < 0$	$x \rightarrow \alpha_1 x$ $y \rightarrow y + \beta_2$	$x \rightarrow x + \beta_1$ $y \rightarrow \alpha_2 y$
$\frac{\delta V}{\delta x} < 0, \frac{\delta V}{\delta y} > 0$	$x \rightarrow x + \beta_1$ $y \rightarrow \alpha_2 y$	$x \rightarrow \alpha_1 x$ $y \rightarrow y + \beta_2$
$\frac{\delta V}{\delta x} < 0, \frac{\delta V}{\delta y} < 0$	$x \rightarrow x + \beta_1$ $y \rightarrow y + \beta_2$	$x \rightarrow \alpha_1 x$ $y \rightarrow y + \beta_2$

By iteratively executing IBIS simulation and fine-tuning coefficients at different pulse width PW values until $W_{IBIS} \approx W_{SPICE}$ is satisfied, and recording the corresponding values of α_1 , α_2 , β_1 , β_2 , an empirical adjustment matrix indexed by pulse width with correction coefficients as output responses can be formed. The general matrix structures are shown in Tables S1–S4.

When the pulse width is compressed to a certain extent, and single-factor adjustment is insufficient to fully compensate for waveform distortion, a dual-factor co-regulation mechanism must be initiated. The critical pulse width thresholds and specific combined adjustment modes are detailed in Tables S5–S12.

3.4. Real-Time, In Situ Pulse Width Detection

To enable adaptive dynamic parameter compensation, a robust pulse-width detection logic block is embedded directly in the Verilog-AMS transient analysis kernel. As illustrated in Figure 1E, the input excitation signal $V(in)$ is continuously compared with a predefined decision threshold $thresh$, which is conventionally defined as the arithmetic mean of the high and low logic levels. The native cross event-triggering function is configured to detect both positive-going rising-edge and negative-going falling-edge threshold crossings, and the corresponding absolute simulation timestamps are recorded. Specifically, by capturing the successive rising-edge timestamp t_{rise1} , the subsequent falling-edge timestamp t_{fall} , and the next rising-edge timestamp t_{rise2} , the Type-010 pulse width $PW1$, defined as the duration of the high-level plateau, and the Type-101 pulse width $PW2$, defined as the duration of the low-level plateau, can be calculated in real time as $PW1 = t_{fall} - t_{rise1}$ and $PW2 = t_{rise2} - t_{fall}$, respectively. For subsequent coefficient indexing, only positive and non-zero pulse-width measurements are retained as valid operational data. Because this detection logic is fully encapsulated within the analog event scheduler of the Verilog-AMS simulation engine, it operates autonomously without external digital processing, thereby enabling real-time pulse-width-aware parameter compensation.

3.5. Adaptive Compensation Framework for Arbitrary Binary Sequences

Recognizing that any arbitrarily complex digital bitstream can be uniquely decomposed into an alternating sequence of fundamental Type-010 and Type-101 pulse primitives, the coefficient adjustment matrices calibrated for isolated single-pulse excitations (as described in Section 3.4) are inherently extensible to arbitrary waveform contexts. Within the iterative loop of the Verilog-AMS transient simulation, upon the successful identification and validation of each complete pulse event, the measured pulse duration is employed as a query key. This key is used to index the pre-calibrated empirical correction matrix via the $\$table_model$ function, retrieving the corresponding set of optimal correction coefficients. The dynamic factors k_{pu} and k_{pd} are then instantaneously updated with these retrieved values:

$$k_{pu} \leftarrow \alpha_1 \cdot k_{pu} \gg \partial \quad k_{pu} \leftarrow k_{pu} + \beta_1 \quad (30)$$

$$k_{pd} \leftarrow \alpha_2 \cdot k_{pd} \gg \partial \quad k_{pd} \leftarrow k_{pd} + \beta_2 \quad (31)$$

The specific adjustment modality invoked is contingent upon both the measured pulse width interval and the governing monotonicity conditions derived in Section 3.2. To streamline the implementation, the $\$table_model$ system function can be leveraged to establish a direct functional mapping between the extracted pulse width and the corresponding adjustment coefficient set, as conceptually illustrated below:

$$\alpha_1 = \$table_model(PW, T_array, A1_array, "1L") \quad (32)$$

In this construct, the array T_array stores the discretized pulse width values, and the array $A1_array$ holds the associated, pre-calibrated α_1 coefficients. Through this mechanism, dynamic, on-the-fly parametric correction is seamlessly achieved throughout the transient simulation, compelling the IBIS-generated output waveform to converge in real-time toward the high-fidelity SPICE reference.

The applicability of the calibrated coefficient matrices is governed primarily by the calibrated pulse-width range and the validity of the monotonicity-guided correction criterion, rather than by a universal data-rate threshold. The local linearized I-V analysis is used only to determine the correction direction of k_{pu} and k_{pd} , whereas the actual Verilog-AMS simulation retains the original table-based I-V interpolation and the final coefficients are obtained through full-waveform SPICE-referenced calibration. Therefore, when the detected pulse width falls outside the calibrated range, or when the sensitivity relationship between the output waveform and k_{pu}/k_{pd} changes significantly, the coefficient matrices should be recalibrated before further application. For the present devices and PRBS excitation conditions, the method has been experimentally validated up to 1.302 Gbps.

4. Experimental Validation and Results Analysis

4.1. Experimental Configuration

To rigorously and systematically assess the efficacy of the proposed optimization framework, three functionally diverse semiconductor devices manufactured by Texas Instruments were selected as representative test vehicles: the TPS53317 (an integrated power management unit), the BUF20800-Q1 (a programmable gamma buffer), and the TPS22986 (a multi-channel load switch). The simulation testbed was established within the Cadence Virtuoso design environment. For each device, the corresponding foundry-provided transistor-level SPICE model simulation served as the definitive “gold standard” reference for accuracy benchmarking.

The input excitation was uniformly defined as a 10-bit pseudo-random binary sequence (PRBS), specifically “0110100101”. In this work, the two PRBS excitation conditions are denoted as 666 Mbps and 1.302 Gbps for consistency with the simulation setup. These labels refer to the repetition conditions of the complete 10-bit PRBS pattern rather than the duration of an isolated single bit. Accordingly, for the 10-bit pattern used here, the effective single-bit pulse widths are approximately 150 ps and 76.8 ps, respectively. These two excitation conditions were selected to provide two levels of narrow-pulse high-frequency stress and to evaluate whether the pulse-width-aware compensation remains effective when the calibrated Type-010 and Type-101 single-pulse coefficients are extended to random multi-pulse excitation. It should be noted that the coefficient lookup is based on the effective pulse width measured from threshold-crossing events of the analog input waveform, rather than directly on the excitation-condition labels themselves. Therefore, each detected high- or low-level pulse segment is indexed to the corresponding pre-calibrated coefficient entry, while pulse segments falling within the no-correction range retain the nominal parameters.

Quantitative assessment of model fidelity was performed using the Normalized Mean Square Error (NMSE) metric, defined mathematically as:

$$NMSE = 10 \lg \left[\frac{\sum_{i=1}^n [Z(n) - Z_o(n)]^2}{\sum_{i=1}^n [Z(n)]^2} \right] \text{ (dB)} \quad (33)$$

In this expression, $Z(n)$ represents the discrete-time output voltage sequence generated by the IBIS model under evaluation, $Z_o(n)$ denotes the corresponding SPICE reference sequence, and N is the total number of temporal sampling points. A more negative NMSE value is indicative of a reduced discrepancy between the model output and the reference waveform, signifying superior model fidelity.

4.2. Single-Pulse Calibration Experiments and Result Analysis

As an initial calibration step, isolated Type-010 and Type-101 single-pulse excitations were applied to each of the three test devices. The output waveforms before and after compensation are compared in Figures 2–4.

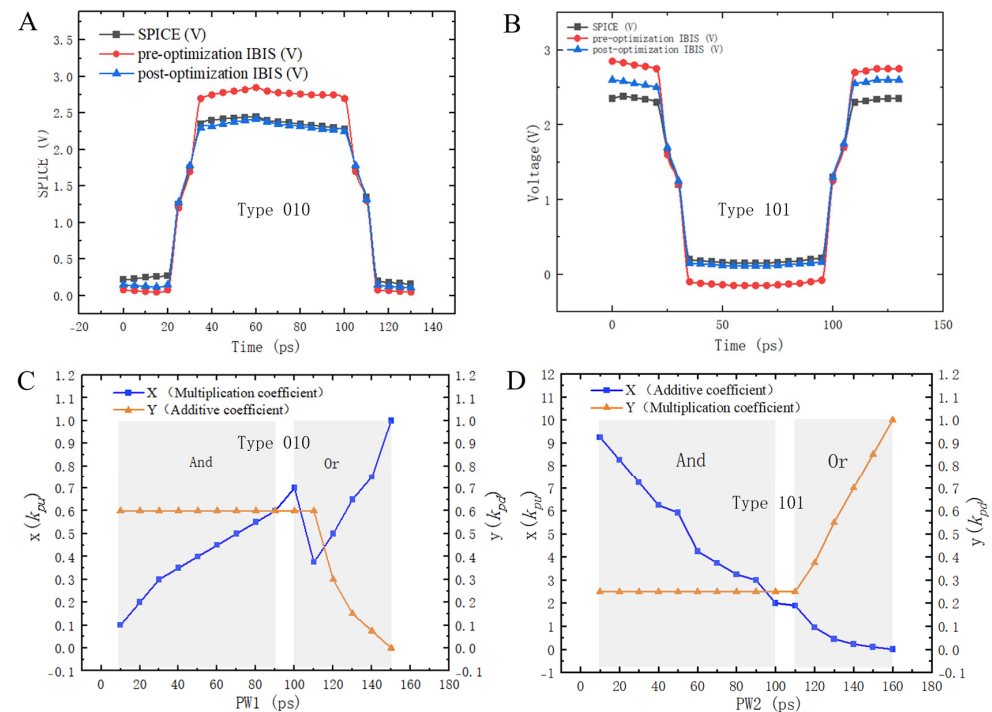


Figure 2. Optimization results for Device 1: (A) under Type-010 single-pulse excitation, (B) under Type-101 single-pulse excitation; empirically calibrated adjustment coefficients for Device 1: (C) under PW1 waveform excitation, (D) under PW2 waveform excitation.

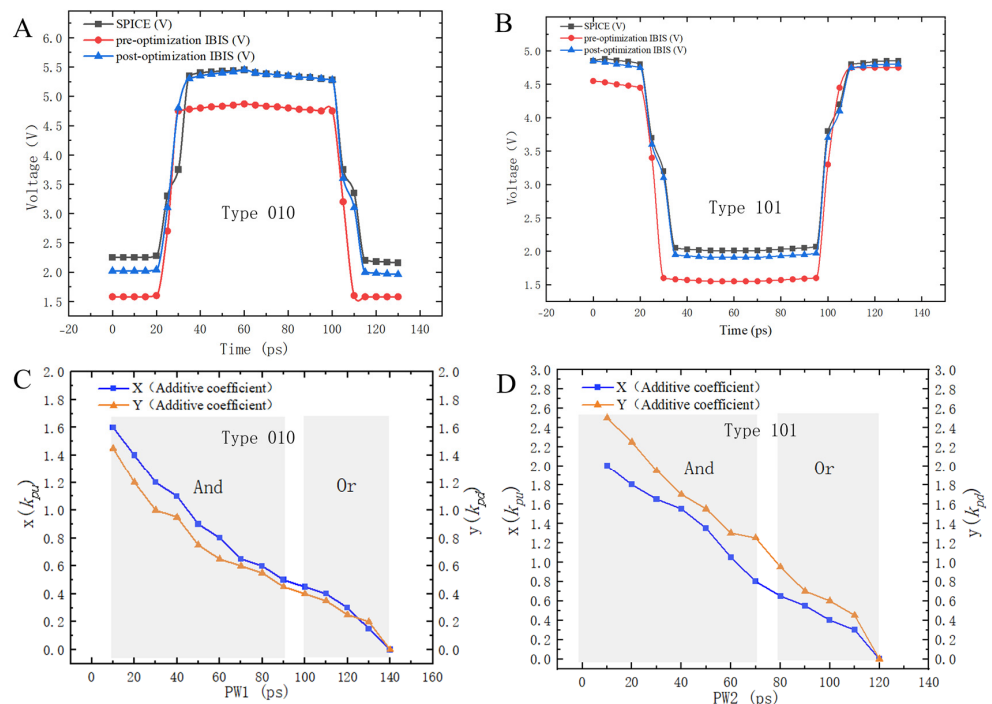


Figure 3. Optimization results for Device 2: (A) under Type-010 single-pulse excitation, (B) under Type-101 single-pulse excitation; empirically calibrated adjustment coefficients for Device 2: (C) under PW1 waveform excitation, (D) under PW2 waveform excitation.

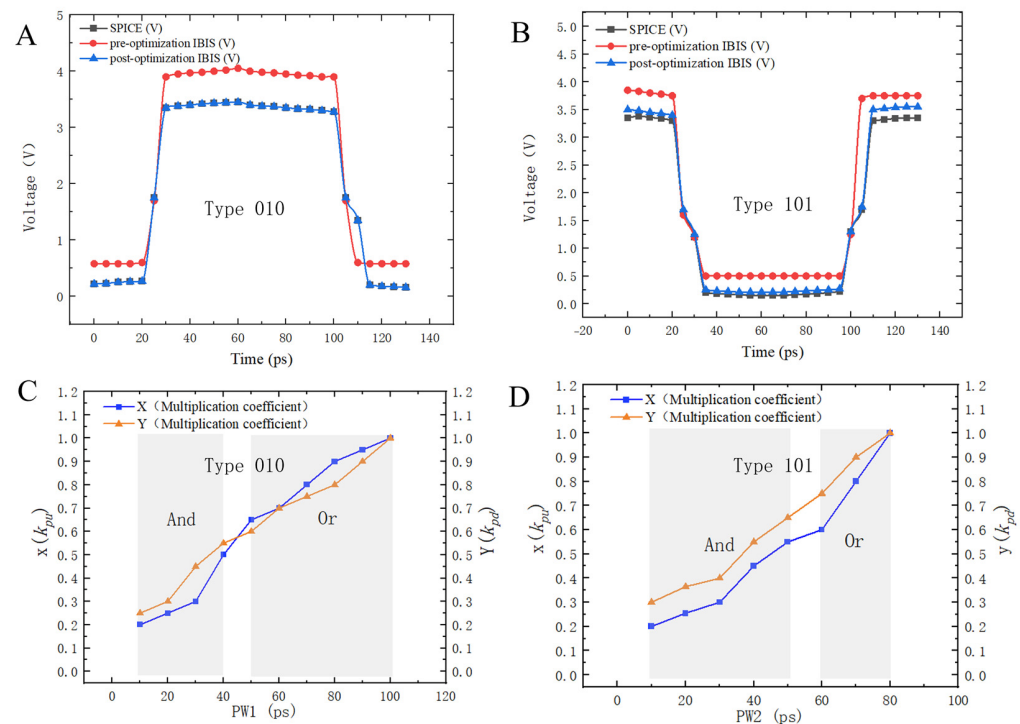


Figure 4. Optimization results for Device 3: (A) under Type-010 single-pulse excitation, (B) under Type-101 single-pulse excitation; empirically calibrated adjustment coefficients for Device 3: (C) under PW1 waveform excitation, (D) under PW2 waveform excitation.

4.2.1. Device 1 (TPS53317)

For Device 1 (TPS53317), the unmodified IBIS waveform exhibited clear deviations from the SPICE reference, mainly in the pulse plateau and baseline regions (Figure 2A,B). Under Type-010 excitation, the pre-compensation IBIS waveform showed a noticeable voltage sag at the pulse apex, with an amplitude deficit of approximately 0.2 V relative to the SPICE reference. After dynamic compensation, the optimized waveform closely matched the SPICE reference, and the flatness of the pulse plateau was markedly improved. Under Type-101 excitation, the unoptimized waveform exhibited an undesired upward shift at the pulse base, accompanied by pronounced overshoot during the falling-edge transient. After compensation, both the baseline voltage and the overshoot amplitude were effectively corrected and brought into close agreement with the SPICE reference.

The adjustment coefficients used for Device 1 were obtained from the empirical calibration results shown in Figure 2C,D, where PW1 and PW2 denote the high-level and low-level durations, respectively. Detailed coefficient values are provided in the Supporting Information. As a representative example, for PW1 = 100 ps, the prescribed adjustment involves multiplying k_{pu} by 0.7 and additively increasing k_{pd} by 0.6. These results indicate that parameter adjustment guided by the analytically derived monotonicity criterion can effectively reduce waveform distortion.

For Type-010 excitation (Figure 3A), no correction was required when $PW1 \geq 150$ ps, indicating that the native IBIS model provided sufficient accuracy under relatively wide-pulse conditions. In the PW1 range of 140–110 ps, single-parameter correction was sufficient, either by multiplicatively reducing $x(k_{pu})$ from $\times 0.75$ to $\times 0.375$ or by additively increasing $y(k_{pd})$ from +0.075 to +0.6 (Figure 3C). When $PW1 \leq 100$ ps, single-parameter correction became insufficient, and simultaneous dual-parameter compensation was required. Specifically, x was attenuated from $\times 0.7$ to $\times 0.1$, whereas y was maintained at a constant additive offset of +0.6. For example, at PW1 = 100 ps, the prescribed correction was $x \rightarrow \times 0.7$ and $y \rightarrow +0.6$. These results indicate that stronger attenuation of x is required as the pulse width

decreases, whereas the additive compensation applied to y reaches a stable value in the narrow-pulse regime.

In the case of Type-101 excitation (Figure 2B,D), no parameter correction was required when $PW2 \geq 160$ ps. Within the $PW2$ range of 150–110 ps, single-parameter adjustment was sufficient, either by additively increasing x from +0.1 to +1.9 or by multiplicatively reducing y from $\times 0.85$ to $\times 0.25$. When $PW2 \leq 100$ ps, simultaneous dual-parameter compensation became necessary: x was additively increased from +2 to +9.25, whereas y was fixed at a multiplicative scaling factor of $\times 0.25$. For instance, at $PW2 = 100$ ps, the corresponding correction was $x \rightarrow +2$ and $y \rightarrow \times 0.25$.

Compared with the Type-010 case, the compensation strategy under Type-101 excitation showed a similar structural pattern, but the correction direction and coefficient magnitudes were asymmetric. This asymmetry reflects the distinct nonlinear electrical characteristics of the pull-up and pull-down paths. Overall, the results demonstrate that the monotonicity-guided parameter correction strategy can effectively determine the direction and magnitude of compensation and reduce waveform distortion in conventional IBIS models under narrow-pulse high-frequency excitation.

4.2.2. Device 2 (BUF20800-Q1)

The single-pulse calibration results for Device 2 (BUF20800-Q1) are presented in Figure 3A,B. The pre-compensation IBIS waveform was systematically lower than the SPICE reference, indicating an overall amplitude deficit in the native model. After applying the proposed dynamic compensation strategy, this amplitude discrepancy was substantially reduced, and the optimized waveform showed improved agreement with the SPICE reference. Under Type-010 excitation, the native IBIS waveform remained consistently below the SPICE reference, with an amplitude deviation of approximately 0.15 V at the pulse plateau and a noticeably delayed rising edge. After compensation, the waveform amplitude was elevated to the SPICE reference level, and the rising-edge slew rate was also well aligned with the reference. Under Type-101 excitation, the unoptimized waveform exhibited excessive undershoot during the low-level sustain period, together with a prolonged recovery process. After compensation, the undershoot was effectively suppressed, resulting in a waveform that closely matched the SPICE reference.

The monotonicity analysis of Device 2 further indicates that its output voltage responds to the key adjustment parameters in a well-defined direction. Unlike Device 1, Device 2 primarily required additive enhancement of the adjustment parameters, which is consistent with the systematic amplitude deficiency observed in its native IBIS waveform. Figure 3C presents the empirically calibrated coefficients for Type-010 single-pulse excitation, where $PW1$ denotes the high-level duration. When $PW1 \geq 140$ ps, the nominal parameters were retained without correction, suggesting that the native IBIS model remained sufficiently accurate under relatively wide-pulse conditions. Within the $PW1$ range of 130–100 ps, single-parameter compensation was sufficient, either by additively increasing x (k_{pu}) from +0.15 to +0.45 or by additively increasing y (k_{pd}) from +0.2 to +0.4. When $PW1 \leq 90$ ps, simultaneous enhancement of both x and y was required, with x increasing from +0.5 to +1.6 and y increasing from +0.45 to +1.45. These results show that the required additive compensation increased monotonically as the pulse width decreased, indicating that the drive-strength deficiency of the native IBIS model became more pronounced under narrow-pulse high-frequency conditions.

Figure 3D presents the calibrated coefficients for Type-101 single-pulse excitation, where $PW2$ denotes the low-level duration. No correction was required when $PW2 \geq 120$ ps. Within the $PW2$ range of 110–80 ps, single-parameter compensation was sufficient, either by additively increasing x from +0.3 to +0.65 or by additively increas-

ing y from +0.45 to +0.95. When $PW2 \leq 70$ ps, simultaneous additive enhancement of both parameters became necessary, and the required compensation increased further as the pulse width decreased. For example, at $PW2 = 70$ ps, the prescribed correction was $x \rightarrow +0.8$ and $y \rightarrow +1.25$, whereas at $PW2 = 10$ ps, the correction increased to $x \rightarrow +2$ and $y \rightarrow +2.5$. Therefore, Figure 3C,D demonstrates that Device 2 consistently benefited from additive compensation under both Type-010 and Type-101 excitations. This behavior reflects the insufficient effective drive strength of its native IBIS model and further confirms that the monotonicity-guided compensation strategy can adapt to device-specific error characteristics and improve waveform fidelity under high-frequency narrow-pulse excitation.

4.2.3. Device 3 (TPS22986)

The single-pulse compensation results for Device 3 (TPS22986) are presented in Figure 4A,B, and the corresponding pulse-width-dependent calibration coefficients are summarized in Figure 4C,D. Detailed coefficient values are provided in the Supporting Information. In contrast to Devices 1 and 2, Device 3 exhibited an over-driven native IBIS response, as the unoptimized IBIS waveform consistently exceeded the SPICE reference amplitude. Under Type-010 excitation, the original IBIS waveform showed pronounced overshoot at the pulse peak, approximately 0.25 V higher than the SPICE reference, together with post-transition ringing. After applying dynamic compensation, the overshoot and ringing were effectively suppressed, and the optimized waveform nearly overlapped with the SPICE reference. Under Type-101 excitation, the unmodified waveform displayed a distinct low-level tail lasting up to 0.5 ns after the falling-edge transition, whereas the SPICE reference recovered more rapidly. After compensation, this tailing artifact was substantially eliminated, and the transient response was brought into close agreement with the SPICE reference.

The calibration results further clarify why Device 3 required a compensation strategy different from those used for Devices 1 and 2. For Type-010 excitation, no parameter correction was required when $PW1 \geq 100$ ps. As $PW1$ decreased to the 90–50 ps range, single-parameter multiplicative attenuation was sufficient, either by reducing x (k_{pu}) from $\times 0.95$ to $\times 0.65$ or by reducing y (k_{pd}) from $\times 0.9$ to $\times 0.6$. When $PW1$ was further reduced to 40 ps or below, single-parameter correction was no longer sufficient, and simultaneous attenuation of both parameters was required. Specifically, the correction changed from $x \rightarrow \times 0.5$ and $y \rightarrow \times 0.55$ at $PW1 = 40$ ps to $x \rightarrow \times 0.2$ and $y \rightarrow \times 0.25$ at $PW1 = 10$ ps. This progressive decrease in the scaling factors indicates that stronger suppression of the effective driving strength is needed as the pulse width becomes narrower.

For Type-101 excitation, no correction was required when $PW2 \geq 80$ ps. Within the $PW2$ range of 70–60 ps, unilateral multiplicative attenuation remained applicable, either by reducing x from $\times 0.8$ to $\times 0.6$ or by reducing y from $\times 0.9$ to $\times 0.75$. When $PW2 \leq 50$ ps, simultaneous attenuation of both parameters became necessary. For example, the correction changed from $x \rightarrow \times 0.55$ and $y \rightarrow \times 0.65$ at $PW2 = 50$ ps to $x \rightarrow \times 0.2$ and $y \rightarrow \times 0.3$ at $PW2 = 10$ ps. These results show that Device 3 consistently required multiplicative attenuation for both pulse polarities, indicating that the native IBIS model overestimated the effective drive response under narrow-pulse excitation. In addition, the different critical thresholds for $PW1$ and $PW2$ suggest asymmetric nonlinear responses between the pull-up and pull-down paths. Overall, the results for Device 3 demonstrate that the proposed dynamic compensation strategy can adapt to device-specific nonlinear error characteristics and select the appropriate transition from single-parameter correction to dual-parameter co-regulation, thereby improving the waveform fidelity of the conventional IBIS model under narrow-pulse high-frequency excitation.

The pulse-width-dependent compensation behavior can be attributed to the high-frequency limitation of conventional IBIS models. Although standard IBIS models include lumped parasitic elements such as C_{comp} and package RLC parameters, the core buffer response is still mainly represented by pre-characterized static I-V tables and V-T waveforms. Under narrow-pulse excitation, the output transition becomes strongly history dependent because the output node and the pull-up/pull-down networks may not fully recover before the next switching event. Under such conditions, residual node charge, C_{comp} -related capacitive current, package parasitic response, load-dependent recovery, and edge-rate-dependent nonlinear behavior may jointly contribute to the discrepancy between the static IBIS response and the transistor-level SPICE reference.

It should be noted that the proposed method does not explicitly model each of these physical effects separately. Instead, it treats their combined influence on the output waveform as an equivalent pulse-width-dependent drive-strength error. The detected pulse width is therefore used as an event-dependent descriptor of local switching history, and k_{pu}/k_{pd} are dynamically adjusted to correct the effective pull-up and pull-down drive strengths according to the SPICE-referenced calibration results. This explains why additive enhancement, multiplicative attenuation, or dual-factor co-regulation is required under different device-specific and pulse-width-dependent error patterns.

Collectively, the single-pulse calibration results show that the proposed method can select device-specific correction directions and compensation magnitudes according to pulse-width-dependent distortion behavior. The corresponding distortion patterns, dominant compensation modes, and electrical interpretations are summarized in Table 2.

Table 2. Electrical summary of waveform distortion and compensation.

Device	Native IBIS Error Pattern	Dynamic Feature Before Compensation	Main Compensation Mode	Electrical Interpretation
Device 1 TPS53317	Plateau sag/base shift, asymmetric Type-010/Type-101 distortion	Pull-up and pull-down mismatch; different PW1/PW2 thresholds	Asymmetric k_{pu}/k_{pd} correction	pull-up/pull-down paths have different nonlinear recovery behavior
Device 2 BUF20800-Q1	IBIS waveform lower than SPICE; amplitude deficit	Insufficient effective drive strength; delayed rising edge	Additive enhancement of k_{pu} and/or k_{pd}	Native IBIS underestimates effective drive under narrow pulses
Device 3 TPS22986	Over-driven amplitude, overshoot/ringing/tailing	Excessive effective drive; non-monotonic transitions	Multiplicative attenuation	Native IBIS overestimates drive response under compressed pulses

4.3. Fidelity Validation Under Random Sequence Excitation

The proposed compensation strategy was further evaluated under random multi-pulse excitation to determine whether the calibrated pulse-width-dependent coefficients could be extended beyond isolated single-pulse conditions. A 10-bit pseudo-random binary sequence (PRBS), “0110100101”, was applied to the three test devices at two data rates, 666 Mbps and 1.302 Gbps. The resulting waveforms were compared with the transistor-level SPICE reference to assess the practical effectiveness of the proposed method under more realistic high-speed switching conditions.

For Device 1, the unoptimized IBIS model accumulated both timing and amplitude errors under PRBS excitation, particularly during consecutive transitions. At 666 Mbps, these errors appeared as inconsistent pulse plateau levels and clear deviations from the

SPICE reference. After compensation, the optimized waveform closely followed the SPICE waveform across different bit positions (Figure 5A). When the data rate was increased to 1.302 Gbps, the native IBIS model exhibited more pronounced amplitude collapse and inter-symbol interference, especially near narrow-pulse regions. In contrast, the optimized model maintained good tracking fidelity, with only minor residual deviations at the most compressed pulse segments (Figure 5B).

For Device 2, the random-sequence response further confirmed the need for adaptive compensation. At 666 Mbps, the unoptimized waveform exhibited level drift after consecutive logic “1” states, and the rising-edge monotonicity was visibly degraded. After optimization, the output level became more stable, and the edge transitions were sharper and better aligned with the SPICE reference (Figure 5C). At 1.302 Gbps, the native IBIS model showed more pronounced overshoot and ringing, with pulse-amplitude distortion exceeding 20% in some segments. Through dynamic adjustment of the driving factors, the proposed method restored both the peak and baseline voltage levels of individual pulses, leaving only slight discrepancies at the fastest transition edges (Figure 5D).

For Device 3, the unoptimized waveform showed a different error pattern under PRBS excitation. At 666 Mbps, the native IBIS response displayed asymmetric rise and fall transitions, especially in alternating “010” segments. After compensation, the waveform symmetry was substantially improved (Figure 5E). At 1.302 Gbps, the unoptimized model exhibited severe non-monotonic edge behavior, which could lead to inaccurate logic-level interpretation in high-speed simulation. The optimized waveform not only recovered the expected amplitude level but also restored monotonic transition behavior (Figure 5F). This improvement is consistent with the single-pulse calibration results in Section 4.2, where Device 3 required dual-factor co-regulation under narrow-pulse conditions.

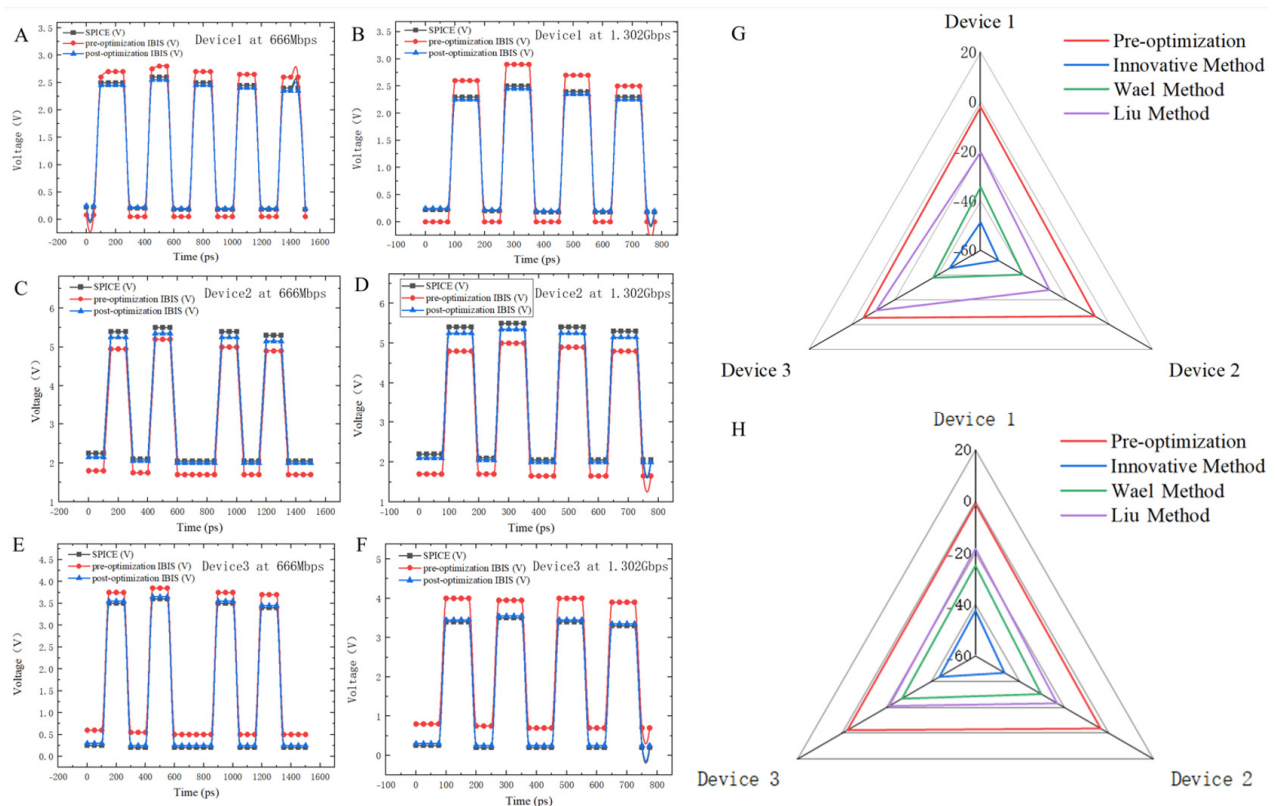


Figure 5. Validation of the Proposed Method With Pseudo-Random Binary Sequence (PRBS) Excitation for Device 1 (A,B), Device 2 (C,D), and Device 3 (E,F). Radar chart comparison of NMSE performance across different methods at two data rates: (G) 666 Mbps; (H) 1.302 Gbps (Unit: dB).

The random-sequence simulations achieved consistent waveform recovery across all three devices, confirming that the pulse-width-indexed lookup-table compensation mechanism can be extended from isolated single-pulse calibration to random multi-pulse excitation. With real-time pulse-width detection and dynamic updating of the driving factors, k_{pu} and k_{pd} , the optimized IBIS models remained closely aligned with the SPICE reference waveforms at both 666 Mbps and 1.302 Gbps. These results demonstrate that the proposed Verilog-AMS-based compensation framework improves waveform fidelity under random high-speed excitation and is applicable to high-frequency signal-integrity simulation.

4.4. Quantitative Comparative Assessment of Fidelity Enhancement

The modeling fidelity was quantitatively assessed using NMSE. The proposed method was compared with the unoptimized IBIS model and two representative published methods, referred to here as the Wael Method [9] and the Liu Method [20]. Table 3 summarizes the NMSE values for the three devices at 666 Mbps and 1.302 Gbps, and Figure 5G,H presents the same comparison using radar charts. Because NMSE is expressed in decibels, more negative values indicate lower modeling error.

Table 3. NMSE comparison of different methods at two data rates (dB).

Device	Data Rate	Before Optimization	Proposed Method	Wael Method	Liu Method
Device 1	666 Mbps	−2.13	−47.62	−34.47	−20.34
	1.302 Gbps	−1.03	−44.19	−24.88	−18.34
Device 2	666 Mbps	−6.73	−54.79	−40.30	−27.89
	1.302 Gbps	−3.72	−46.71	−30.42	−23.27
Device 3	666 Mbps	−5.36	−46.21	−37.82	−11.25
	1.302 Gbps	−2.33	−46.08	−26.93	−21.15

At 666 Mbps, the unoptimized IBIS model produced NMSE values ranging from −6.73 dB to −2.13 dB, indicating substantial deviation from the SPICE reference. The Wael Method reduced the NMSE to the range of −40.30 dB to −34.47 dB, whereas the Liu Method achieved NMSE values between −27.89 dB and −11.25 dB. By comparison, the proposed method achieved NMSE values from −54.79 dB to −46.21 dB across the three devices. For Device 2, for example, the proposed method achieved an NMSE of −54.79 dB, which was 14.49 dB lower than that of the Wael Method and 26.90 dB lower than that of the Liu Method. These results demonstrate that the proposed method provides higher modeling accuracy at the lower tested data rate and establish a baseline for evaluating its robustness under more demanding signaling conditions.

When the data rate was increased to 1.302 Gbps, the performance gap became more pronounced. The unoptimized IBIS model deteriorated further, with NMSE values ranging from −3.72 dB to −1.03 dB. The Wael Method and the Liu Method also showed reduced performance compared with their 666 Mbps results, yielding NMSE ranges of −30.42 dB to −24.88 dB and −23.27 dB to −18.34 dB, respectively. In contrast, the proposed method retained NMSE values between −46.71 dB and −44.19 dB, showing only limited degradation relative to the lower data rate. For Device 1, the proposed method achieved an NMSE of −44.19 dB, which was 19.31 dB lower than that of the Wael Method. These results indicate

that the proposed dynamic compensation mechanism is more robust against data-rate increases than the comparative methods.

To further clarify the methodological novelty, a qualitative comparison with representative IBIS, high-speed I/O-buffer, and SI/link surrogate modeling approaches is provided in Table 4. Compared with existing delay-based, slew-rate-based, and data-driven surrogate modeling approaches, the proposed method integrates real-time pulse-width detection, monotonicity-guided correction, and pull-up/pull-down dual-factor regulation into a Verilog-AMS-reconstructed IBIS model, thereby enabling more explicit compensation of pulse-width-dependent waveform distortions under random PRBS excitation.

The present compensation framework is mainly robust against pulse-width-dependent distortions, including amplitude collapse, overshoot, undershoot, edge-delay error, and incomplete recovery, because these effects are reflected in the detected pulse width and corrected through dynamic k_{pu} and k_{pd} updates. However, disturbances dominated by power-supply noise, simultaneous switching noise, crosstalk, package resonance, or PVT drift may change the branch-current relationship independently of pulse width. In such cases, the current PW-indexed matrix should be extended to a multi-dimensional matrix including supply voltage, temperature, package condition, or noise descriptors.

Table 4. Comparison with representative IBIS, high-speed I/O-buffer, and SI/link surrogate modeling methods.

Method Category	Representative Studies	Main Idea	Random PRBS Support	Pulse-Width Awareness	Interpretability	Need Training Data	Compatibility
Conventional IBIS	Fernando [8]	Static I-V/V-T lookup	Limited	No	Medium	No	High
Two-port/grey-box model	Dghais et al. [9,16,17]	Pre-driver/output-stage behavioral abstraction	Partial	No explicit PW matrix	Medium	No	Medium
Mixed-signal overclocked model	Dghais/Ning et al. [11,18]	Hybrid automaton/mixed-signal abstraction	Partial	No explicit PW indexing	Medium	No	Medium
Pre-delay compensation	Liu et al. [20]	Delay and waveform smoothing	Interface-specific	No	Medium	No	High
Slew-rate correction	Ding et al. [21]	Correct edge-rate mismatch	Partial	No	High	No	High
ANN/surrogate model	Varma/Zhu et al. [12,13,23]	Data-driven nonlinear mapping	Possible	Implicit	Low	Yes	Medium
Recent ML-based SI/link surrogate model	Akinwande/Wu et al. [24,25]	ML-based SI/link surrogate modeling	Possible	Implicit	Medium	Yes	Medium
Proposed method	This work	Real-time PW detection + k_{pu}/k_{pd} dynamic correction	Yes	Yes	High	No training, needs calibration	High

From a practical viewpoint, the proposed method is intended to serve as an enhanced behavioral-modeling flow for high-speed electronic systems. Chip vendors or model developers can use transistor-level SPICE simulations or measured reference waveforms

to calibrate the coefficient matrices, while system-level signal-integrity engineers can subsequently use the calibrated Verilog-AMS-enhanced IBIS model for faster board-level simulations. This makes the method potentially useful for pre-layout and post-layout verification of high-speed digital links, mixed-signal interfaces, and compact embedded systems where full SPICE simulation is computationally expensive or not suitable for model distribution.

The same interface-level modeling requirement also exists in emerging sensor and intelligent sensing systems [28,29], where sensing units are increasingly integrated with readout circuits, data converters, microcontrollers, and wireless or high-speed digital communication modules. The proposed method does not model the sensing material or gas-sensing mechanism itself; instead, it can support more accurate signal-integrity prediction for the electrical readout and data-transmission interfaces associated with such systems.

Overall, the quantitative and qualitative results support two main conclusions. First, static table-based IBIS models exhibit rapidly increasing errors under narrow-pulse and high-data-rate conditions. Second, the proposed Verilog-AMS compensation framework substantially reduces these errors by linking real-time pulse-width detection with monotonicity-guided k_{pu}/k_{pd} correction. The consistent NMSE reduction across three functionally distinct devices and two representative PRBS excitation conditions confirms the effectiveness of the proposed framework within the tested scope. These results, together with the qualitative comparison in Table 4, demonstrate that the proposed method provides a more explicit pulse-width-aware compensation mechanism than conventional delay-based, slew-rate-based, and data-driven modeling approaches.

5. Conclusions

This work proposes a Verilog-AMS-based dynamic parameter compensation method to improve the high-frequency fidelity of conventional IBIS models. By reconstructing the IBIS model into three functional layers, deriving the monotonic relationship between the output voltage and the driving factors k_{pu}/k_{pd} , and introducing real-time pulse-width-indexed coefficient adjustment, the proposed framework enables adaptive compensation of pulse-width-dependent waveform distortion.

Experiments on three representative semiconductor devices show that the proposed method can adapt to different native IBIS error patterns and switch from single-parameter correction to dual-factor co-regulation under narrow-pulse excitation. Random-sequence validation at 666 Mbps and 1.302 Gbps further confirms that the optimized IBIS models remain closely aligned with transistor-level SPICE references, achieving NMSE values below -40 dB for all tested devices and data rates. These results demonstrate the effectiveness of the method for high-frequency signal-integrity simulation and its potential use in board-level verification of high-speed digital links, mixed-signal interfaces, compact embedded systems, and advanced sensor-interface applications.

These results also provide a basis for further extension of the proposed framework. In the present study, the compensation coefficients were calibrated using SPICE reference waveforms, and the validation was conducted on three device models under two representative PRBS excitation conditions. Future work will further evaluate the method across broader device families, loading conditions, PVT corners, interference scenarios, and longer random bitstream patterns. Automated coefficient extraction and extension from a pulse-width-indexed matrix to a multi-dimensional disturbance-aware compensation framework will also be investigated.

Supplementary Materials: The following supporting information can be downloaded at: <https://www.mdpi.com/article/10.3390/electronics15132906/s1>.

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