

Article

A Design of Active Gate Driver for Reducing Surge Voltage During Turn-Off Transient of SiC MOSFET in Boost Converter

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Abstract

This paper proposes an Active Gate Driver (AGD) for a DC–DC boost converter based on Silicon Carbide (SiC) power devices, in which surge voltage and ringing arise from their fast-switching characteristics. In this work, a practical and simple 4-bit logic AGD was proposed to adjust the gate resistance during the Miller interval of the SiC MOSFET. This helps suppress these effects and lowers the surge voltage and ringing stress on the power device. Experimental results demonstrate that the voltage overshoot decreases from 52 V to 22 V, corresponding to a reduction from 52% to 22% under a 100 V output condition, while the peak drain–source voltage decreases from 152 V to 122 V. The turn-off energy increases from 60.2 μ J to 76.9 μ J due to the slightly reduced switching speed. This trade-off represents the improvement in the comparison between transient suppression and switching loss. In addition, the voltage ringing is significantly attenuated. Although the modified switching strategy slightly increases switching loss, it effectively improves waveform quality and reduces voltage stress. These results confirm that the proposed AGD provides a simple and effective solution for improving the switching robustness and reliability of SiC-based DC–DC boost converters.

Keywords: active gate driver; DC–DC boost converter; SiC MOSFET; surge voltage; electric vehicle

1. Introduction

Recent surveys consistently report a clear trend toward adopting wide-bandgap (WBG) semiconductor devices, in particular SiC MOSFETs, SiC diodes, and gallium nitride (GaN) FETs for high-power DC–DC converters in electric vehicle (EV), as shown in Figure 1 [1–3]. SiC MOSFETs, as wide-bandgap (WBG) power devices, are particularly well suited for DC–DC converters [4–7]. From a material perspective, SiC has a bandgap energy of approximately 3.26 eV (compared with 1.1 eV for Si), a breakdown electric field of about 3×10^6 V/cm (roughly an order of magnitude higher), and a thermal conductivity of about 3.7 W/cm·K (nearly 2.5 times the 1.5 W/cm·K of Si) [8,9]. These physical parameters enable a thinner drift layer while maintaining the voltage-blocking capability for ratings from 1.2 kV to 3.3 kV. Consequently, the specific on-state resistance R_{on} decreases significantly, and conductance losses at the same power level are much lower compared with Si-based MOSFETs and IGBTs [10,11].



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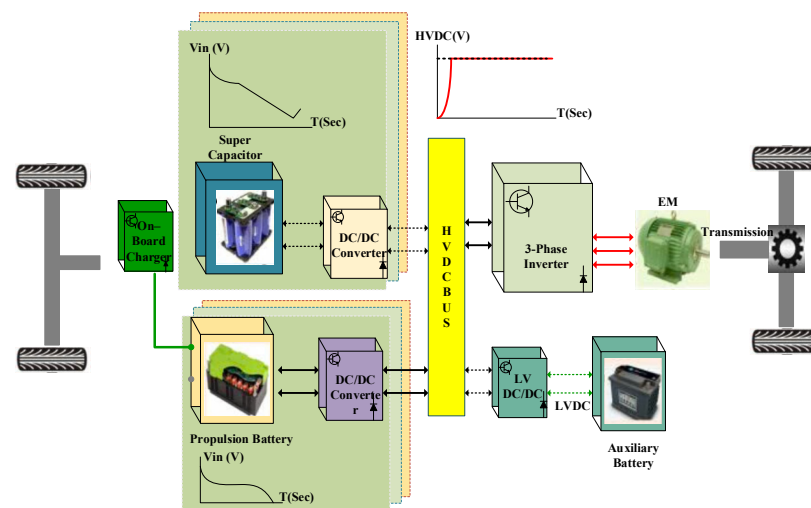


Figure 1. Block diagram of an electric vehicle powertrain [1].

However, the very fast switching behavior of SiC MOSFETs introduces several challenges in the power circuit. Therefore, the current design trend involves adopting AGD techniques, in which the gate-source voltage waveform is shaped for each switching phase to actively set dv/dt , di/dt , and the I-V trajectory within a desired operating region [12,13]. The fast-switching process, combined with parasitic inductance and capacitance in the power and gate loops, can easily lead to overvoltage, ringing, and self-turn-on (false turn-on or crosstalk) phenomena in power converters, which can be controlled using AGD [14–17]. Compared with AGD, fixed gate-driver circuits (a single RG value and a single VGS level) are no longer sufficient to fully exploit the potential of SiC MOSFETs in high-power converters [18,19]. To reduce voltage overshoot and enhance switching performance across various operating conditions, further studies investigated feedback-based AGD schemes [20]. Building on this idea, subsequent studies investigated various AGD methods, such as switching-trajectory optimization and stage-wise gate control, to achieve more accurate control of switching transients [21,22]. Other AGD implementations were further developed to improve the switching performance while, in turn, mitigating the voltage overshoot and switching losses [23,24]. In the meantime, various gate-driver topologies and design approaches were investigated to improve transient behavior and ensure reliable operation under high (dv/dt) conditions [25,26]. To balance surge voltage suppression and converter efficiency, programmable and digital AGD solutions were also documented in [27–29]. It shows that AGD technology for SiC MOSFET applications is still evolving. However, this programmable IC, which is just in the laboratory, is not yet suitable for industrial applications. On the other hand, the closed-loop gate-sensing and feedback-based AGD approaches have been developed in [30,31] to dynamically control switching transients and improve the trade-off between voltage-overshoot suppression and switching losses. The summary and comparison of the development and challenges of the previous study on AGD are presented in Table 1. Numerous AGD techniques have been proposed to improve the switching performance of SiC MOSFETs with complicated control.

However, most studies have focused on inverter applications or require relatively sophisticated control structures. Furthermore, it lacks study on developing suitable AGD for DC–DC boost converter, where the high switching speed of SiC MOSFETs can still result in significant surge voltage and ringing due to the parasitic inductances in the power loop during turn-off transitions. In our work, the feasibility of an Active Gate Driver for mitigating these effects was verified through simulation studies [32]. Building upon this foundation, the present work develops and experimentally validates a practical AGD

hardware system based on active gate-resistance control for reducing turn-off surge voltage and improving the operating performance of a DC–DC boost converter.

Table 1. Comparison of Representative AGD Techniques for SiC MOSFET Applications.

AGD Approach	Sensor/Feedback	Control Complexity	Main Achievement	Main Limitation
Adaptive multi-level AGD [12]	Yes	High	Dynamic dv/dt control and switching optimization	Requires sensing and adaptive control circuits
AGD for current-sharing improvement [13]	Yes	High	Improved current balancing of parallel SiC modules	Additional sensing hardware required
Closed-loop AGD [14]	Yes	High	Voltage-spike suppression	Increased implementation complexity
Three-level gate driver [15]	No	Medium	Reduced overshoot and switching loss	Additional gate-driving stages required
Negative-feedback AGD [20]	Yes	High	Suppressed crosstalk and parasitic oscillation	Feedback circuitry increases complexity
Partial active gate control [29]	No	Medium	Improved surge-voltage/efficiency tradeoff	Digital implementation required
Gate-sensing AGD with closed-loop timing control [30]	Yes	High	Real-time transient regulation	Complex IC architecture
Real-time transient-feedback AGD [31]	Yes	High	Adaptive switching optimization	High control and sensing complexity

The rest of this paper is organized as follows. Section 2 describes the analysis of the gate driver for the SiC MOSFET in a DC–DC boost converter. The principles of the gate driver and surge voltage are analyzed. Section 3 presents simulation and experimental results of a DC–DC boost converter using SiC MOSFETs. Section 4 shows the simulation and experimental results. Section 5 discusses research results and related requirements. Finally, Section 6 concludes the paper with key findings and future research directions.

2. Analysis Turn-Off Transient of SiC MOSFET

In boost-type converters, as shown in Figure 2a, high switching speed causes parasitic L-C elements and the MOSFET capacitances, which generate surge voltage and resonant ringing. Therefore, the SiC MOSFET switching transient was divided into characteristic time intervals. Based on this segmentation, the dependence of the switching speed on the AGD control parameters was analyzed. This relationship provides the foundation for designing and optimizing the gate-control strategy. This should provide a concise and precise description of the experimental results, their interpretation, and the experimental conclusions. The MOSFET's turn-off process can be divided into characteristic time intervals, as illustrated in Figure 2b.

- (1) $t_1 - t_2$ is the turn-off delay time. During this interval, the circuit discharges the input capacitance C_{iss} from its initial value down to the Miller level. The gate–source voltage V_{GS} starts to decrease from V_{dron} but remains higher than V_{miller} . The drain current and drain–source voltage stay almost unchanged: $I_{DS} \approx I_0$, $V_{DS} \approx V_{on}$.
- (2) $t_2 - t_3$ is the onset of the Miller plateau (turn-off). In this interval, the drain–source voltage V_{DS} begins to increase from $I_D \times R_{DS(on)}$ toward ten percentage of its high value. The gate current primarily charges/discharges the Miller capacitance, C_{GD} , while the drain current, I_{DS} , remains approximately equal to the load current. The

gate–source voltage V_{GS} reaches the Miller level V_{miller} and enters the turn-off Miller plateau. Immediately after this point, C_{GD} starts to discharge, and V_{DS} starts to rise.

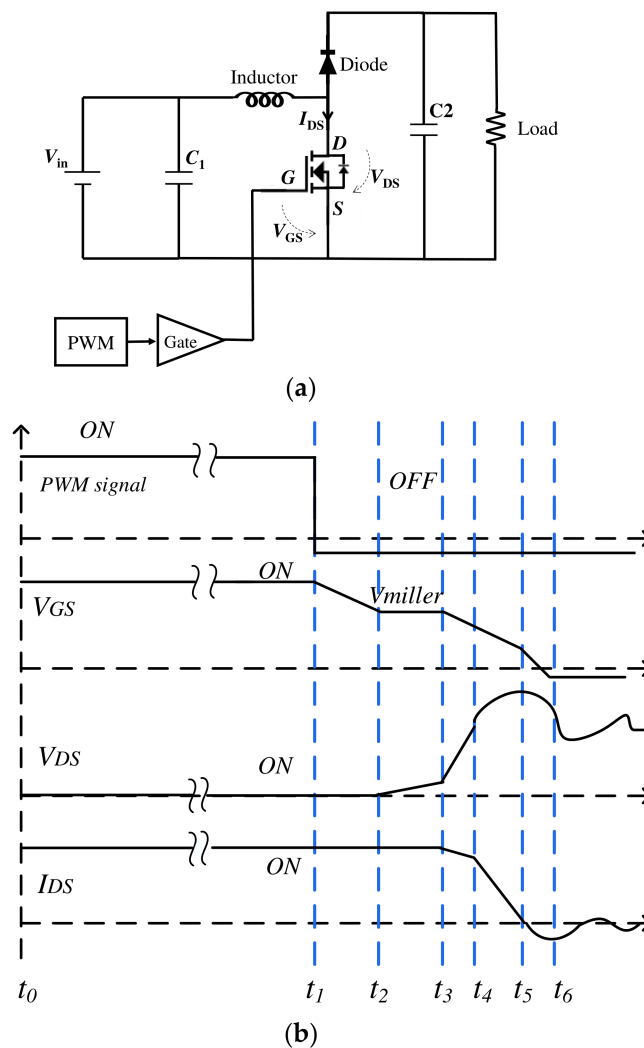


Figure 2. Switching behavior of the SiC MOSFET: (a) DC–DC Boost converter; (b) corresponding switching waveforms.

- (3) $t_3 - t_4$ is the drain–source voltage rise time region. This interval corresponds to the rising edge of V_{DS} and is used to determine the turn-off dv/dt . The drain–source voltage increases from V_{on} to a value close to V_{bus} , while the drain current remains approximately constant ($I_{DS} \approx I_0$). The gate–source voltage V_{GS} stands around the Miller plateau V_{miller} . During this interval, V_{DS} increases from low to high, which is used to calculate the turn-off dv/dt as in (1).
- (4) $t_4 - t_5$ is the drain current fall time region. At t_4 , V_{DS} has already risen to a high level. Then, V_{GS} drops toward the threshold voltage V_{th} , which leads the drain–source current I_{ds} to begin decreasing to a low level. During this interval, I_{DS} falls from I_0 to 0, and this segment is used to calculate the turn-off di/dt as in (2).

$$\frac{dv}{dt} = \frac{I_G(t_3-t_4)}{C_{GD}} = \frac{(V_{dr_on} - V_{miller})}{C_{GD}R_G + (C_{DS} + C_{GD} + C_L)/2g_{fs}} \quad (1)$$

$$\frac{di}{dt} = \frac{g_{fs}I_G(t_4-t_5)}{C_{GD} + C_{GS}} = \frac{(0.5V_{miller} + 0.5V_{th} - V_{dr_off})g_{fs}}{(C_{GD} + C_{GS})R_G + Lg_{fs}} \quad (2)$$

- (5) $t_5 - t_6$ is the final turn-off region. The drain current is essentially zero ($I_{DS} \approx 0$), and the device is almost completely turned off. The gate-source voltage V_{GS} continues to discharge toward V_{doff} (0 V or a negative value), completing the turn-off process.

The SiC MOSFET switching edge rate is governed by gate-driver parameters, including the gate current I_G , the parasitic capacitances C_{GD} and C_{GS} , the external gate resistance R_G , and the driver voltage levels (V_{dron} , V_{doff}). Among these factors, changing R_G before and during the Miller interval provides the most practical and widely adopted control handle, since it can be tuned directly at the circuit level without altering the device structure or redesigning the gate driver.

3. Proposed Active Gate Driver for SiC MOSFET

In this study, the switching speed is regulated using a time-varying gate resistance rather than a fixed resistor. As shown in Figure 3, the proposed Active Gate Driver is configured with multiple parallel resistor branches, which are selectively activated during both the turn-on and turn-off transitions depending on the V_{GS} condition. The proposed AGD method for a DC–DC boost converter does not employ a high gate resistance throughout the entire turn-off process as a conventional fixed gate resistor. Instead, the gate resistance is switched only for a short time during the Miller interval, when voltage overshoot is primarily generated. This achieves a better trade-off between voltage overshoot suppression and switching losses than a conventional fixed gate resistor.

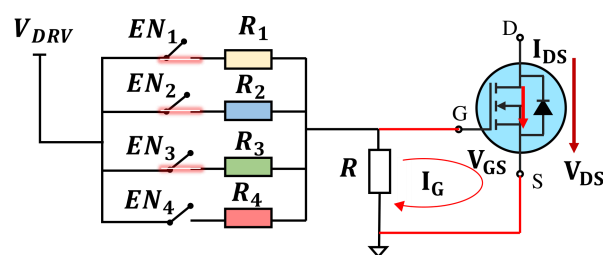


Figure 3. Proposed circuit of the Active Gate Driver method.

Figure 4 shows the MOSFET with parasitic inductance and capacitance elements. When V_{GS} enters the Miller plateau region, where dv/dt and di/dt exhibit the highest sensitivity to the gate-driving strength, the effective gate resistance R_G is intentionally increased to slow down the switching transition. In this manner, voltage overshoot is mitigated, and ringing is suppressed. Outside the Miller interval, R_G is decreased to enhance the gate driving capability, thereby shortening the switching transient and reducing the switching energy losses E_{on} and E_{off} .

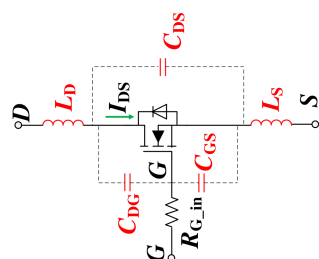


Figure 4. The switching waveforms of a variable gate resistance AGD.

Figures 5 and 6 conceptually compare the conventional fixed- R_{G-on} gate drive with the proposed AGD approach, in which the effective turn-on resistance is stepwise adjusted via $(R_{on1} \dots R_{on-m})$ according to the control states ($x_1 \sim x_m$) to shape the switching transient. Table 2 lists the 16 gate-resistance combinations of the 4-bit Active Gate Driver. These

combinations are selected and scheduled to optimize the MOSFET switching transient by shaping the gate current I_G . The proposed AGD control is implemented by sequentially activating the resistor branches through the enable signals EN1–EN4 according to the gate-voltage operating regions of the SiC MOSFET. During the initial switching interval, a lower equivalent gate resistance is selected to provide a higher gate current and accelerate the switching process. As the gate voltage approaches the Miller plateau region, the equivalent gate resistance is increased to limit the gate current, thereby reducing dv/dt , di/dt , and the associated voltage overshoot. The gate resistance is lowered once again to finish the switching transition as quickly as possible after the Miller interval. Through this time-varying gate-resistance profile, the proposed AGD achieves a balance between surge-voltage suppression and switching-loss reduction.

Table 2. Switching configurations and corresponding gate resistance values of the 4-bit Active Gate Driver.

IN1	IN2	IN3	IN4	Level	R_G
0	0	0	1	15	R_4
0	0	1	0	14	R_3
0	0	1	1	13	$R_4 // R_3$
0	1	0	0	12	R_2
0	1	0	1	11	$R_2 // R_4$
0	1	1	0	10	$R_2 // R_3$
0	1	1	1	9	$R_2 // R_3 // R_4$
1	0	0	0	8	R_1
1	0	0	1	7	$R_1 // R_4$
1	0	1	0	6	$R_1 // R_3$
1	0	1	1	5	$R_1 // R_3 // R_4$
1	1	0	0	4	$R_1 // R_2$
1	1	0	1	3	$R_1 // R_2 // R_4$
1	1	1	0	2	$R_1 // R_2 // R_3$
1	1	1	1	1	$R_1 // R_2 // R_3 // R_4$
0	0	0	0	0	0

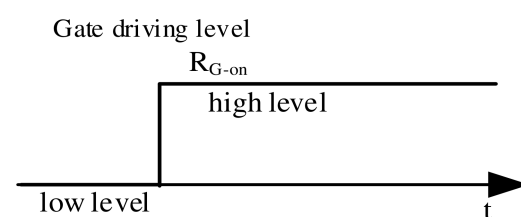


Figure 5. Normal gate drive.

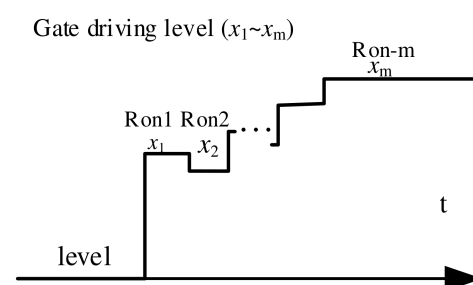


Figure 6. Active gate drive (AGD).

4. Simulation and Experimental Results

To verify the effectiveness of the proposed AGD technique, this section presents a comparative analysis between a conventional gate driver and the AGD implementation in a high-efficiency DC–DC boost converter, using simulation and experiment. Table 3 lists the power components in simulation and experiment.

Table 3. Components in simulation, experiment.

Component Name	Specifications
SiC MOSFET	650 V
Inductor	350 μ H
Diode	650 V

4.1. Simulation Results

Table 4 displays the detailed parameters of the test bench and measurement equipment used in the test. The DC–DC boost converter increases the input voltage from 200 V to the output voltage of 400 V. Switching frequency is 100 kHz. Figure 7 shows the waveform representation under the conventional scheme. In this baseline case, the external gate resistance over the range $R_G = 10.8$ to 100 Ω was applied while keeping the gate command (0–15 V) and the power-stage parameters unchanged. V_{GS} , V_{DS} , and I_{DS} around the turn-on/turn-off commutation intervals were extracted. As shown in Figure 8, the LTspice schematic is used for simulation. Figures 9–11 and Table 4 confirm that a conventional fixed- R_G gate drive imposes an inherent and unfavorable trade-off. As the gate resistance R_G increases from 10.8 Ω to 100 Ω , the conventional fixed- R_G gate drive significantly suppresses the switching slew rates during both turn-on and turn-off transitions. Specifically, dv/dt (on) decreases from 6.94 to 2.08 V/ns, while dv/dt (off) is reduced more sharply from 17.9 to 3.5 V/ns.

Table 4. Boost DC–DC circuit specifications.

Boost DC–DC Converter Parameters	Value	Unit
Input Voltage (V_{in})	200	V
Output Voltage (V_{out})	400	V
Switching Frequency (f_s)	100	kHz
Output Current (I_{out})	10	A
Efficiency	97	%

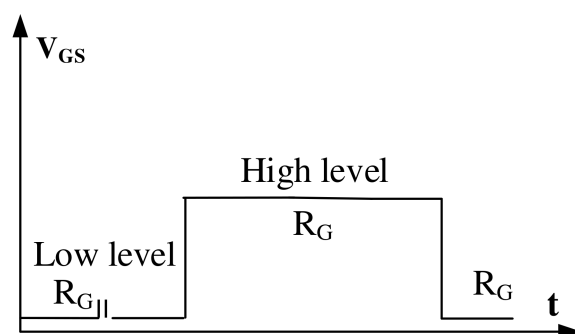


Figure 7. Conventional PWM control.

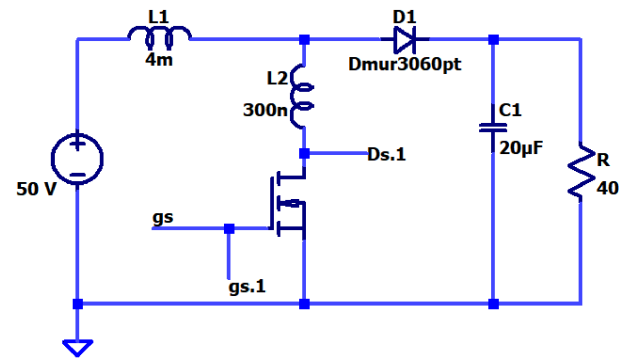


Figure 8. LTspice schematic used for simulation.

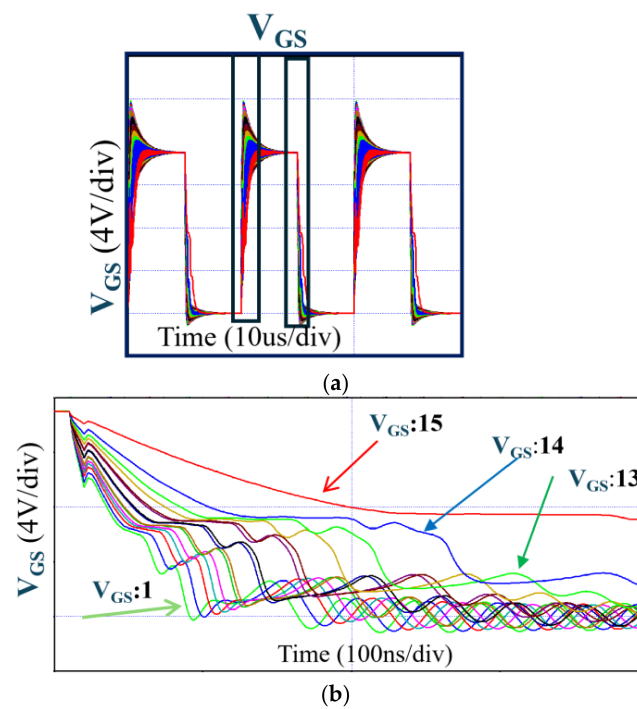


Figure 9. V_{GS} waveforms for conventional fixed- R_G drive: (a) gate-source voltage V_{GS} ; (b) V_{GS} zoomed-in turn-off transient.

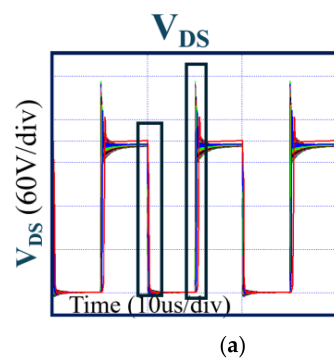
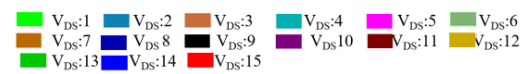


Figure 10. Cont.

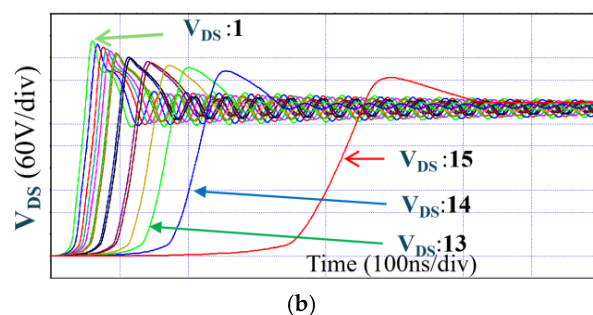


Figure 10. V_{DS} waveforms for conventional fixed- R_G drive: (a) drain–source voltage V_{DS} ; (b) V_{DS} zoomed-in turn-off transient.

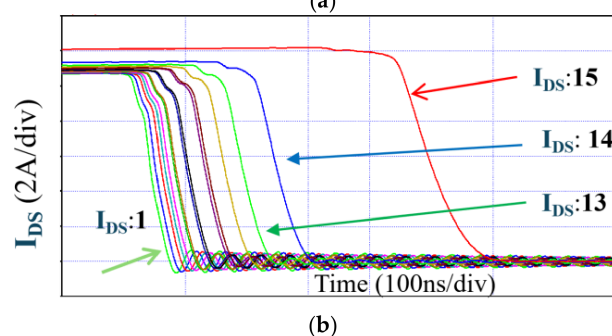
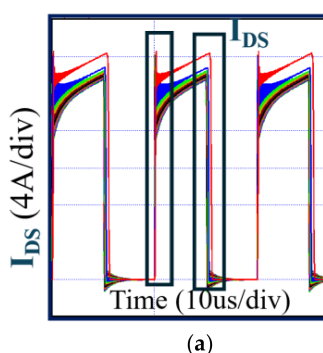


Figure 11. I_{DS} waveforms for conventional fixed- R_G drive: (a) drain–source current I_{DS} ; (b) I_{DS} zoomed-in turn-off transient.

Table 5 shows the summary of the effects of R_G on switching characteristics when changing fixed gate resistance. Despite this pronounced reduction in dv/dt , the peak V_{DS} overshoot is only moderately mitigated, decreasing from 585.6 V to 486.7 V (approximately 16.9%). However, this comes at the cost of substantially prolonged switching intervals (t_{off} : 85.2 $\rightarrow$ 441.9 ns) and a dramatic increase in switching energy. Notably, at $R_G \approx 21.9 \Omega$, dv/dt is already reduced (turn-on 18.9%, turn-off 31.6%), and overshoot decreases by 7.35%, yet E_{sw} increases by 43.8%, indicating that slowing the device throughout the entire transient using a larger fixed R_G is energetically inefficient.

Instead of using a single gate resistance, AGD selectively intervenes around the Miller/voltage-transition interval by dynamically switching the effective gate resistance over time. Specifically, a strong drive level with $R_{G,low} \approx 10.8 \Omega$ was applied to preserve fast gate-charge transfer and limit E_{on}/E_{off} , then temporarily switch to $R_{G,Miller} \approx 21.9 \Omega$ during the Miller plateau to reduce dv/dt , suppress V_{DS} overshoot, and damp commutation-loop ringing. After the Miller interval, the gate resistance returns to $R_{G,low}$ for the remaining switching stages, as shown in Figure 12. Therefore, the increased gate resistance is applied

only during the critical transition interval, limiting the increase in switching loss while preserving the surge-voltage suppression capability of the proposed AGD.

Table 5. Summary of the effects of R_G on switching characteristics when changing fixed gate resistance.

Level	R_G (Ω)	V_{DS} Speak (V)	E_{on} (μJ)	E_{off} (μJ)	dv/dt (On) V/ns	dv/dt (Off) V/ns	t_{on} (ns)	t_{off} (ns)
1	10.8	585.6	122.9	262.5	6.94	17.9	51.9	85.2
2	12.1	576.8	130.5	281.5	6.77	17.1	54.3	94.6
3	13.8	571	137.7	294.4	6.53	15.9	56.4	101.2
4	14.9	565.6	143.6	306.6	6.34	15.3	57.7	104.6
5	15.9	558.9	148.5	319.4	6.23	14.7	59.1	112.1
6	17.5	554.3	155.9	338.2	6.02	13.7	82.5	120.9
7	17.7	550.9	157.9	346.7	5.96	13.6	87.9	122.8
8	21.3	542.6	173.7	380.4	5.63	12.3	92.5	135.1
9	21.9	538.6	176.9	389.2	5.57	12.1	94.8	146.2
10	27	529.9	202.7	443.6	5.14	10.6	102.2	160.2
11	28.1	526.9	207.6	453.7	5.05	10.4	104.2	169.8
12	33.3	519.1	234.1	514.7	4.67	9.1	137.3	185.3
13	39	512.8	263.2	575.3	4.33	7.9	145.7	219.9
14	50	504.3	325.9	693.8	3.67	6.6	186.9	257.4
15	100	486.7	658.7	1285	2.08	3.5	425.7	441.9

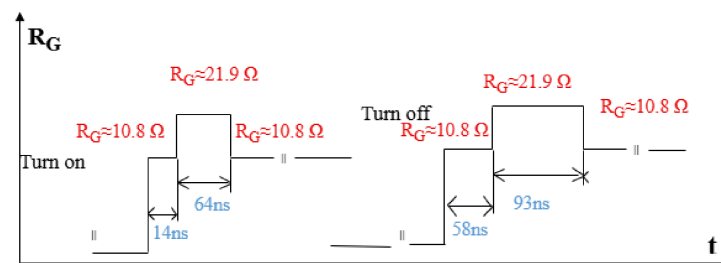


Figure 12. Gate control patterns used in simulations.

Based on the identified Miller-region, the simulation scenario was conducted following the principle of intervening only during the voltage-transition interval. The Miller interval is first identified from the measured V_{GS} waveform and then used to define the switching schedule of the proposed AGD. During this interval, the gate charge is predominantly transferred into C_{GD} , and V_{DS} changes rapidly. Consistent with the V_{DS} waveforms, this time window corresponds to the steep V_{DS} rising/falling edges and the most pronounced propensity for ringing. Accordingly, the AGD does not employ a fixed R_G ; instead, it time-variably switches the effective gate resistance. At the beginning of the transition, a low gate resistance was applied ($R_{G,low} \approx 10.8 \Omega$) to accelerate gate-charge injection, maintain a short switching interval, and avoid excessive growth of E_{on} upon entering the marked Miller window, it temporarily switch to a higher resistance ($R_{G,Miller} \approx 21.9 \Omega$) to soften the voltage transition, thereby reducing dv/dt , lowering V_{DS} overshoot, and damping switching-loop ringing. After the device exits the plateau, the AGD returns to $R_{G,low}$ for the remaining sub-stages to prevent unnecessary prolongation of the turn-on/turn-off process. In Figure 13, the V_{GS} waveforms confirmed that the AGD intervenes only within the Miller window (i.e., the nearly flat plateau) by temporarily switching to $R_{G,Miller} \approx 21.9 \Omega$. Then

it returns to a low gate resistance for the remaining sub-stages. When the AGD is activated within the Miller window, it clearly softens the V_{DS} transition, as shown in Figure 14. During turn-on, the dv/dt decreases from 6.82 to 5.56 V/ns ($\approx 18.5\%$), and the V_{DS} ringing amplitude is reduced from 22.6 to 15.9 V ($\approx 30\%$). During turn-off, the improvement is more pronounced: the dv/dt decreases from 18.06 to 12.42 V/ns ($\approx 31\%$), the peak V_{DS} drops from 581.52 to 534.6 V, resulting in a 26% reduction in the surge voltage from 181.5 V to 134.6 V. In addition, the ringing amplitude decreases from 90.43 to 61.69 V ($\approx 32\%$).

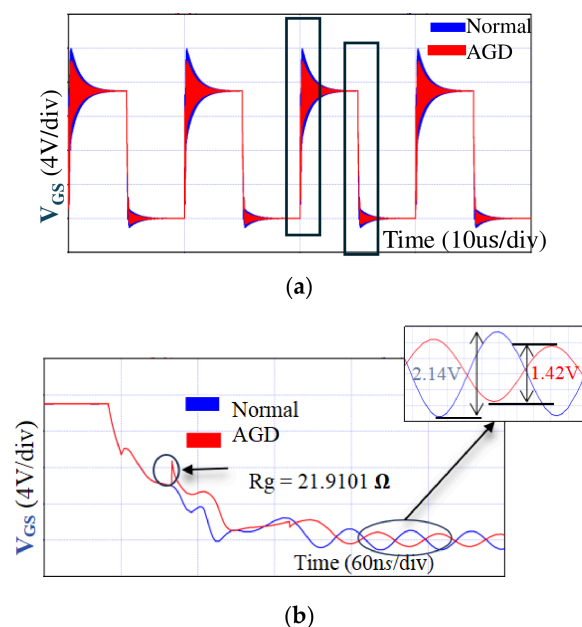


Figure 13. Comparison of V_{GS} waveforms between the conventional gate drive and the AGD: (a) gate-source voltage V_{GS} ; (b). V_{GS} zoomed-in turn-off transient.

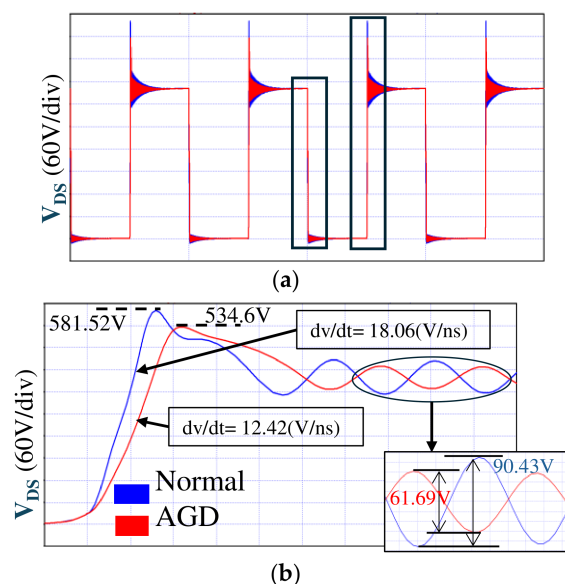


Figure 14. Comparison of V_{DS} waveforms between the conventional gate drive and the AGD: (a) drain-source voltage V_{DS} ; (b). V_{DS} zoomed-in turn-off transient.

As shown in Figure 15, the current response reflects the reduced switching aggressiveness achieved by the proposed AGD. During turn-on, the AGD reduces di/dt from 0.722 to 0.564 A/ns ($\approx 22\%$) and decreases the I_{DS} ringing amplitude from 7.64 to 5.36 A ($\approx 30\%$). During turn-off, the I_{DS} ringing amplitude is further reduced from 2.2 to 1.5 A ($\approx 32\%$),

while di/dt changes only slightly from 0.379 to 0.355 A/ns ($\approx 6\%$). These results confirm that the AGD effectively suppresses current oscillations while maintaining a comparable switching speed.

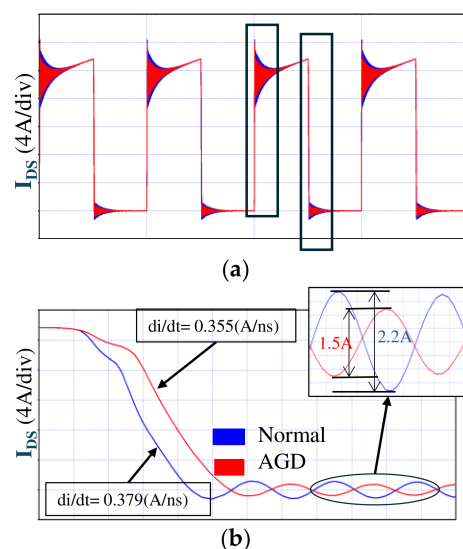


Figure 15. Comparison of I_{DS} waveforms between the conventional gate drive and the AGD: (a) drain–source current I_{DS} ; (b). I_{DS} zoomed-in turn-off transient.

The simulation results show that activating the AGD specifically within the Miller window (temporarily increasing R_G to approximately $21.9\ \Omega$ while maintaining a low R_G outside the Miller interval) selectively softens the switching transition. As a result, the AGD reduces dv/dt and di/dt and markedly suppresses overshoot and ringing in both V_{DS} and I_{DS} , with the most pronounced improvement during turn-off.

The switching loss and transition-time comparison between the fixed gate resistance method and the proposed AGD is presented in Figure 16. With a fixed gate resistance ($R_G = 10.79\ \Omega$), the device exhibits faster switching, with shorter turn-off ($t_{off} \approx 89.1\text{ ns}$), resulting in lower switching losses ($E_{off} = 268.39\ \mu\text{J}$). However, as discussed previously, this fast transition leads to significant voltage overshooting and ringing.

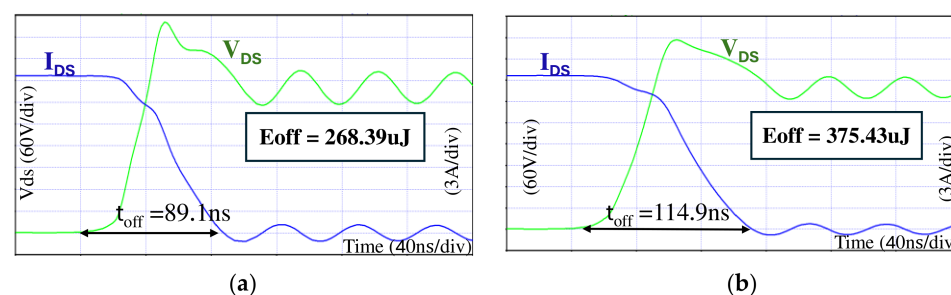


Figure 16. Comparison of SiC MOSFET switching losses under fixed gate resistance and two-step AGD control: (a) fixed gate resistance ($R_G = 10.8\ \Omega$); (b) two-step AGD control.

In contrast, the proposed AGD adaptively modifies the gate resistance during the switching process. The transitions are intentionally slowed ($t_{off} \approx 114.9\text{ ns}$), leading to higher switching losses ($E_{off} = 375.43\ \mu\text{J}$). Nevertheless, the reduced dv/dt and di/dt effectively suppress overshoot and oscillations. These results highlight a clear trade-off between switching loss and waveform quality, where the AGD improves stability of the power converter.

4.2. Experimental Results

A boost-converter test bench is configured as shown in Figure 17. The operating condition is summarized in Table 6. The converter is operated at $V_{in} = 50\text{ V}$ ($\pm 1\%$), $f_s = 100\text{ kHz}$, and $D = 50\%$ to obtain $V_{out} \approx 100\text{ V}$ with a $100\ \Omega$ load ($\approx 1\text{ A}$). These settings provide a consistent baseline for evaluating the impact of AGD on switching transients and device stress. To assess the impact of gate-driving methods on switching characteristics, the experimentally implemented approaches, including constant and two-level-gate resistance, are illustrated in Figure 18.

The experimental turn-off results of the SiC MOSFET demonstrate that Miller-region gate-resistance modulation provides a noticeable improvement in voltage stress and switching ringing compared with the conventional fixed-resistance gate driver. Figure 19 shows the experimental turn-off waveforms of the SiC MOSFET under a 50 V input and 100 V output condition. With the conventional gate driver ($R_G = 10.8\ \Omega$), the drain–source voltage rises rapidly during turn-off. It reaches a peak value of 152 V . Since the steady-state blocking voltage is approximately 100 V , the corresponding voltage overshoot is about 52 V . A relatively large ringing amplitude is also observed after the switching transition.

To reduce the surge voltage, the proposed AGD temporarily increases the gate resistance to $21.9\ \Omega$ during the Miller interval. As shown in Figure 19b, the peak V_{DS} decreases to 122 V , corresponding to an overshoot of 30 V . Compared with the conventional gate driver, the overshoot is reduced by 57.7% . The waveform indicates a smoother turn-off process when the proposed AGD is applied. However, the slower voltage transition increases turn-off energy. The measured E_{off} increases from $60.2\ \mu\text{J}$ to $76.9\ \mu\text{J}$. This result is expected because a larger gate resistance slows down the switching transition. Although E_{off} increases, the reduction in voltage overshoot and dv/dt helps reduce the electrical stress on the device.

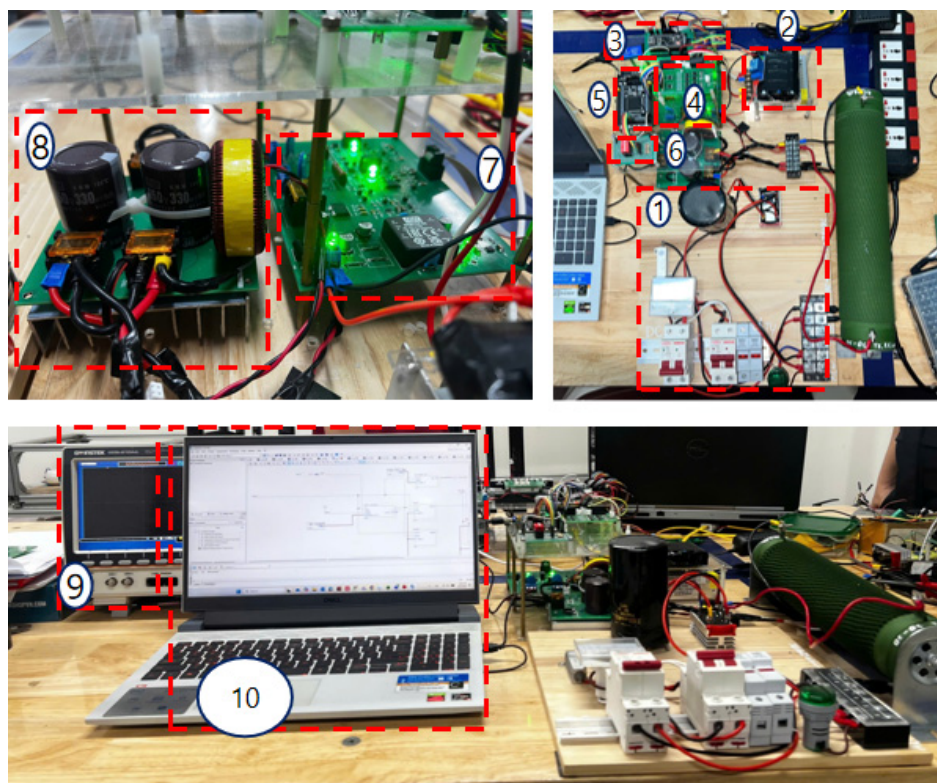
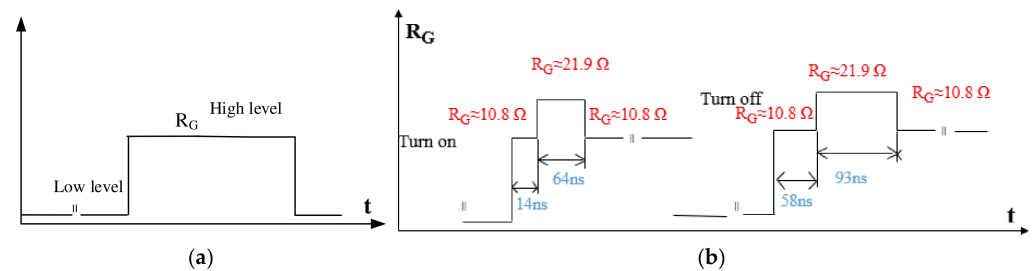
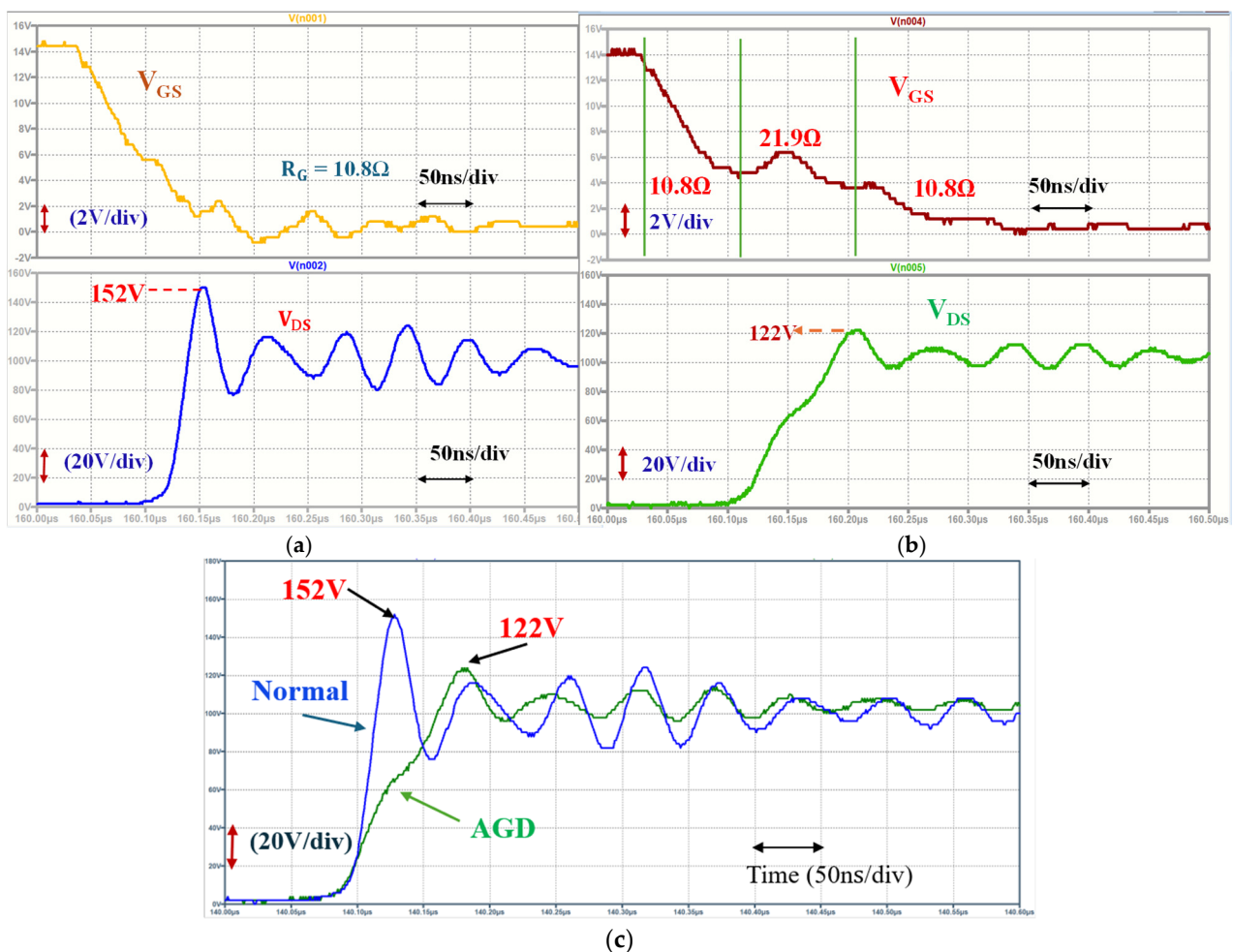


Figure 17. Experimental system: (1) rectifier circuit; (2) 5 V-AGD power supply circuit; (3) MCU; (4) AGD circuit; (5) FPGA; (6) DIP switch circuit; (7) boost converter; (8) measurement circuit; (9) oscilloscope; (10) computer.

Table 6. Components of experiment.

Experiment Parameters	Value	Unit
Input Voltage (V_{in})	100	V
Output Voltage (V_{out})	200	V
Switching Frequency (f_s)	100	kHz
Efficiency	97	%
Current Probe CWTUM/06, Bandwidth	30	MHz
Isolated Voltage Probe (DP10013), Bandwidth	100	MHz

**Figure 18.** Gate pattern for switching control in experiment: (a) normal gate using fixed gate resistance; (b) gate pattern in proposed AGD control.**Figure 19.** Comparison of SiC MOSFET switching waveforms under fixed gate resistance and two-step AGD control: (a) under fixed gate resistance ($R_G = 10.8 \Omega$); (b) two-step AGD control; (c) drain-source voltage comparison between two gate drivers.

These results confirm that increasing gate resistance during the Miller region is an effective way to suppress the turn-off transient. The proposed method reduces voltage overshoot and ringing without requiring additional sensors or complex control circuits.

5. Discussion

The simulation results at an output of 400 V showed that the proposed AGD can reduce the surge voltage during the turn-off transient. By adjusting the switching speed at the Miller interval, the peak VDS drops from 581.52 V to 534.6 V, reducing the surge voltage by 26%, from 181.5 V to 134.6 V. In addition, the ringing amplitude decreases from 90.43 V to 61.69 V ($\approx 32\%$). During the Miller interval, the proposed AGD temporarily increased R_G to approximately 21.9 Ω while maintaining a low R_G outside of that. Therefore, the AGD achieved softens the switching transition. As a result, the AGD reduces dv/dt and di/dt and markedly suppresses overshoot and ringing in both V_{DS} and I_{DS} , with the most pronounced improvement during turn-off. In addition, the switching loss and transition time comparison between the fixed gate resistance method and proposed AGD was provided. With a fixed gate-resistance ($R_G = 10.79 \Omega$), the device exhibits faster switching, with shorter turn-off ($t_{off} \approx 89.1$ ns), resulting in lower switching losses ($E_{off} = 268.39 \mu J$). However, as discussed previously, this fast transition leads to significant voltage overshooting and ringing. The proposed AGD adaptively modifies the gate resistance during the switching process. The transitions are intentionally slowed ($t_{off} \approx 114.9$ ns), leading to higher switching losses ($E_{off} = 375.43 \mu J$). It shows that there is a compensation between switching loss and surge voltage.

Furthermore, the experimental results indicate that the proposed AGD can effectively suppress surge voltage in comparison to the conventional fixed gate resistance approach, reducing the overshoot from 52 V to 22 V for the peak drain–source voltage from 152 V to 122 V. This strengthens the novelty of the paper in designing a 4-bit logic AGD and applying it to a DC–DC boost converter as the main contribution. The behavior is mainly attributed to the application of the proposed AGD during the Miller interval, which reduces surge voltage and limits the excitation of parasitic resonances. As a result, the peak voltage stress and oscillation amplitude are both reduced. The experimental waveforms also show a smoother turn-off current transition. However, the slower switching transition increases the turn-off energy from 60.2 μJ to 76.9 μJ . This result reflects the trade-off between transient suppression and switching loss. Overall, the proposed AGD balances switching loss and voltage stress by combining a standard gate driver integrated circuit (IC) with a 4-bit logic of variable resistors in a practical implementation. The experiment was conducted at 100 V due to the equipment's current-conditioning limitations, but it confirmed the behavior and effectiveness of the proposed AGD, consistent with the simulation and theory.

Since the optimal gate resistance depends on the power converter's operating conditions, particularly the switching current, the proposed AGD method is incorporated into the multiple gate-resistance method to provide the flexibility needed for different operating conditions. In this work, the gate-resistance values were predetermined to experimentally validate the proposed AGD hardware with an operating condition of the DC–DC boost converter. By measuring V_{GS} , the Miller interval can be specified to tune the optimal gate pattern for each load condition. In addition, the switching current of the power converter will be measured under closed-loop control to verify optimal AGD values across different operating conditions to continue developing this research in the future.

As discussed above, the proposed AGD focused on a short time around the Miller interval. However, some very fast-switching SiC MOSFETs with very small input gate-source capacitance have a very short Miller interval. Even if there is still has a chance for AGD during a short window before the Miller interval, AGD faces challenges in effectively

affecting that window. It requires high accuracy and bandwidth, which may limit its application. This point needs further investigation into the next research.

It should be noted that the magnitude of voltage overshoot is strongly influenced by the parasitic inductance of the power loop. Therefore, different converter layouts and soldering may exhibit different absolute overshoot levels. Since the proposed AGD is applied during the Miller interval, the surge-voltage suppression mechanism remains effective under different parasitic inductance conditions with a suitable optimal gate pattern. The effectiveness of the proposed AGD depends on the appropriate selection of gate-resistance combinations and switching schedules. These parameters may require re-optimization when the converter operating conditions, device ratings, or parasitic parameters change. Furthermore, the proposed AGD introduces additional switching elements compared with a conventional fixed-resistance gate driver, providing flexibility for combining software and hardware solutions.

6. Conclusions and Future Work

This paper proposed a 4-bit logic Active Gate Driver with variable gate resistance for improving the switching behavior of SiC MOSFETs in a DC–DC boost converter. By adjusting the gate resistance during only a short-time Miller interval, the proposed method effectively suppresses voltage overshoot and switching oscillations. Both simulation and experimental results demonstrate improved switching performance and reduced voltage stress across the power devices. In simulation, the surge voltage decreased from 581.52 V to 534.6 V, resulting in a 26% reduction from 181.5 V to 134.6 V. The ringing amplitude decreased from 90.43 V to 61.69 V ($\approx 32\%$). Under the experimental condition of a 50 V input and 100 V output boost converter, the proposed AGD reduced the peak drain–source voltage from 152 V to 122 V, corresponding to the overshoot reduction from 52% to 22% (52 V to 22 V). In addition, it resulted in a noticeable attenuation of voltage ringing. These results confirm the effectiveness of the proposed gate-resistance modulation strategy.

Compared with the conventional fixed gate resistance method, the proposed AGD suppresses surge voltage by intentionally increasing the gate resistance only during the Miller interval, thereby slightly reducing switching speed during this critical period. The proposed AGD achieves smoother switching transitions and lower voltage stress. Although the turn-off energy increases from 60.2 μJ to 76.9 μJ due to the reduced switching speed, this trade-off is acceptable considering the significant improvement in comparison between transient suppression and switching loss. Overall, the proposed AGD method provides a practical compromise between switching performance, voltage reliability, and switching loss for SiC-based power converters. It provides a simple, effective solution for enhancing the reliability and robustness of high-speed power electronic systems.

In future work, this research will continue to develop a closed-loop control to verify the proposed AGD for variable operating conditions. The optimal AGD that maintains high switching performance while reducing the surge voltage can be discussed and confirmed using feedback control.

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Abbreviations

The following abbreviations are used in this manuscript:

AGD	Active Gate Driver
WBG	Wide Bandgap
SiC	Silicon Carbide
EV	Electric Vehicle
DC–DC	Direct Current–Direct Current

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