

Article

Impact of Metal-Gate-Induced Stress on Device- and Circuit-Level Performance of GAAFET CMOS Inverters

Subin Lim ¹, Jaehyuk Lim ^{2,3}, Donghwan Han ^{1,4}, Myongjin Kim ¹ and Changhwan Shin ^{1,*} 

¹ School of Electrical Engineering, Korea University, Seoul 02841, Republic of Korea; imsubinssy@korea.ac.kr (S.L.); ianhan@korea.ac.kr (D.H.); btmj0218@korea.ac.kr (M.K.)

² Research Institute of Semiconductor Technology, Korea University, Seoul 02841, Republic of Korea; jaehyuklim@korea.ac.kr

³ The Process Architecture Team, Foundry Division, Samsung Electronics, Hwaseong 18448, Republic of Korea

⁴ Logic Technology Development Team, Semiconductor R&D center, Samsung Electronics, Hwaseong 18448, Republic of Korea

* Correspondence: cshin@korea.ac.kr; Tel.: +82-2-3290-3226

Abstract

Gate-all-around field-effect transistors (GAAFETs) are promising candidates for next-generation CMOS technology because they satisfy both low-power and high-performance requirements. However, their nanoscale geometry makes them highly sensitive to intrinsic stress generated during gate formation, which can affect both device characteristics and circuit operation. In this study, the effects of metal-gate-induced intrinsic stress on GAAFET-based CMOS inverters were systematically investigated with respect to nanosheet width (W_{NS}). Sentaurus TCAD simulations were performed to analyze stress distributions, threshold voltages, saturation currents, and effective currents in NMOS and PMOS devices. In addition, circuit characteristics, including voltage transfer curves, noise margins, fan-out-of-three delay times, overshoot/undershoot voltages, switching energy, and energy-delay product, were evaluated. The results show that NMOS and PMOS devices exhibit opposite current variations under identical stress conditions, which may lead to current imbalance and operational asymmetry in CMOS circuits. Furthermore, W_{NS} was identified as an important parameter governing stress sensitivity. Smaller W_{NS} values increased variations in device characteristics, whereas larger W_{NS} values showed greater delay sensitivity to stress. These findings demonstrate that W_{NS} is a critical design factor for improving performance balance and reliability in stress-aware GAAFET circuit design.

Keywords: CMOS inverter; gate-all-around FET (GAAFET); metal gate intrinsic stress; nanosheet width; TCAD simulation



Academic Editors: Yi Gu, Slawomir Sujecki, Tao Wang, Zhaoyang Fan, Giovanna Mura and Wenrui Zhang

Received: 15 May 2026

Revised: 3 July 2026

Accepted: 7 July 2026

Published: 9 July 2026

Copyright: © 2026 by the authors.

Licensee MDPI, Basel, Switzerland.

This article is an open access article distributed under the terms and conditions of the [Creative Commons Attribution \(CC BY\)](https://creativecommons.org/licenses/by/4.0/) license.

1. Introduction

The semiconductor industry's growth has been driven for decades by continuous transistor downsizing and increased integration density, serving as key enablers of Moore's law. The International Roadmap for Devices and Systems (IRDS) documents how CMOS technology has undergone successive structural innovations whenever scaling approaches its limits. This evolution has progressed from planar MOSFETs to FinFETs [1,2], and most recently to gate-all-around field-effect transistors (GAAFETs) at the 3 nm technology node [3]. The GAAFET architecture, which completely surrounds the channel with gate material, provides superior electrostatic control and is regarded as one of the most promising device architectures for meeting both low-power and high-performance requirements [4].

The gate-all-around (GAA) structure features a unique geometry in which the physical properties of the gate material can affect the channel more directly than in conventional transistor architectures [5]. As a result, intrinsic stress induced during gate formation can strongly influence device characteristics and circuit responses through channel strain modulation. While previous studies have predominantly focused on substrate stress or epitaxial strain effects [6–8], the impact of intrinsic stress originating from the metal gate itself has received comparatively limited attention [9].

In next-generation circuits requiring ultralow power consumption and high-speed operation, even subtle variations in process or structural parameters can significantly affect device performance and overall circuit response. At the nanometer scale, material interactions and structural changes can induce variations in electrical characteristics [10–12], potentially degrading circuit uniformity and operational stability. Although numerous studies have examined the effects of scaling-induced structural or process variations on device characteristics, comprehensive investigations of how process-induced stress propagates to circuit operation remain limited.

System-level reliability requires a clear understanding of how device- and process-induced variations propagate to actual circuit behavior. Small structural changes, such as variations in nanosheet width (W_{NS}) or channel length, combined with internal stress states and material properties, can influence critical inverter performance metrics including delay time, voltage swing, and noise margins.

In this work, we investigate the effects of metal-gate-induced intrinsic stress on GAAFET-based CMOS inverters using Sentaurus TCAD simulations. This stress can arise as an inherent consequence of metal-gate material properties and process conditions. Particular attention is given to W_{NS} -dependent stress sensitivity at both device and circuit levels. The results provide insights into stress-aware circuit design and demonstrate the importance of W_{NS} as a structural parameter for managing stress-induced variability in advanced GAA CMOS technologies.

2. Simulation Setup

2.1. Device Structure and Parameters

To analyze the effect of the metal-gate stress on the electrical characteristics of a GAA-based CMOS inverter, a quantitative analysis was performed using the simulation software Sentaurus TCAD (V-2024.03). The device structure was created using the TCAD Sentaurus Process (SProcess), and device simulations were conducted using the Sentaurus Device (SDevice) [13].

Our investigation focused on GAAFETs with a multibrIDGE channel (MBC) structure. While we applied identical structural parameters to both NMOS and PMOS devices, we configured their channel materials and gate metals differently. Figure 1 presents both a 3D bird's-eye view and cross-section of the baseline device ($W_{NS} = 15$ nm, stress = 0 GPa). The NMOS device utilizes a silicon channel with a TiAlC metal gate, while the PMOS incorporates $\text{Si}_{0.5}\text{Ge}_{0.5}$ source/drain regions, corresponding to a Ge concentration of 50%, with a TiN metal gate. In the baseline configuration, W_{NS} was set to 15 nm under zero-stress conditions. This baseline served as our reference point for evaluating characteristic variations with respect to W_{NS} and metal-gate stress.

The TCAD model parameters used in this work were based on a previously calibrated simulation framework [12], whose calibration was performed using experimental Intel 10 nm FinFET $I_{DS}-V_{GS}$ characteristics reported in [14], as shown in Figure 2. The inherited model framework was then adapted to the present 14 nm GAAFET structure by adjusting the gate work-functions to align the baseline NMOS and PMOS threshold voltages (V_{th}) to 0.28 V at $W_{NS} = 15$ nm under zero-stress conditions.

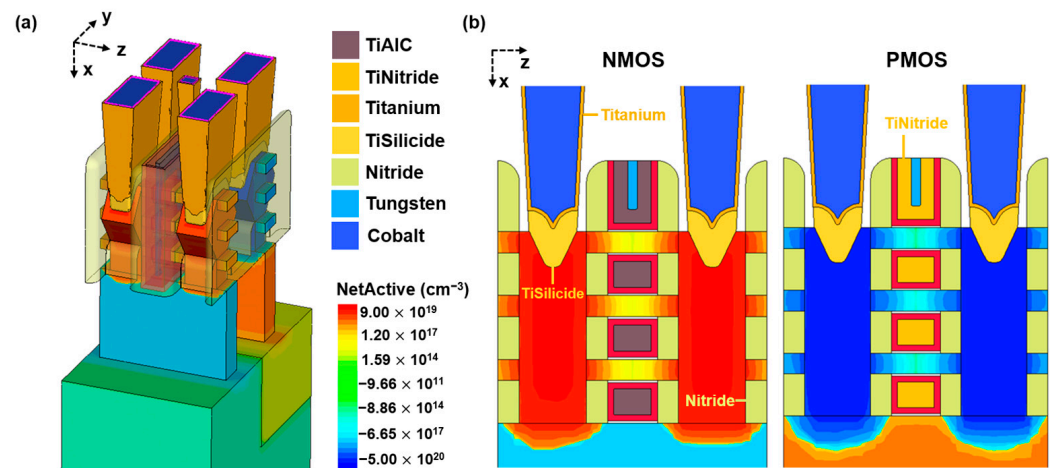


Figure 1. (a) Bird's-eye view of GAAFET CMOS inverter, (b) cross-sectional view of GAAFET inverter along the X–Z plane.

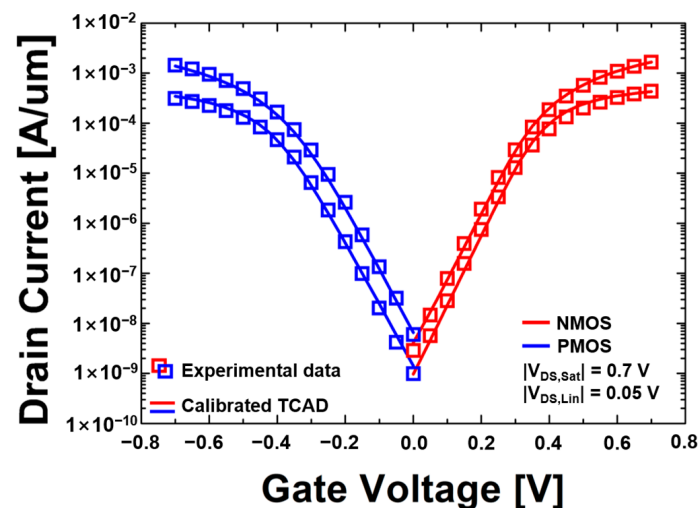


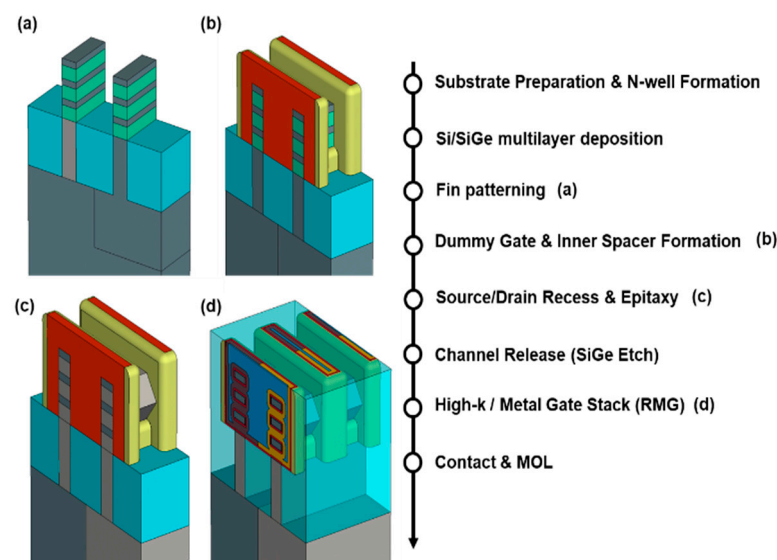
Figure 2. Calibration of the TCAD framework using experimental Intel 10 nm FinFET $I_{\text{DS}}-V_{\text{GS}}$ characteristics.

Although the experimental calibration was originally based on a FinFET benchmark and then applied to the present GAAFET structure, all metal-gate stress and WNS conditions were evaluated using the same calibrated TCAD framework. Therefore, this work focuses on the relative stress-induced trends and WNS-dependent design implications obtained under consistent simulation conditions.

We set W_{NS} values at 7, 15, 30, and 50 nm, while varying the applied metal-gate stress linearly from -2 to $+2$ GPa in 1 GPa increments. The intrinsic stresses of metal-gate films vary with material properties and deposition conditions, typically ranging from sub-GPa levels to several gigapascals in both tensile and compressive regimes [15–17]. Based on this empirical evidence, the -2 to $+2$ GPa range was selected as a representative intrinsic-stress range for sensitivity analysis in advanced CMOS gate-stack technologies. Table 1 summarizes the detailed structural parameters and baseline electrical characteristics, while Figure 3 schematically illustrates the major process steps used to construct the simulated device.

Table 1. Device parameters and baseline electrical characteristics used in the simulation.

Symbol	Parameter	Value
L_G	Gate length	14 nm
N_{CH}	Number of channel stacks	3
W_{NS}	Nanosheet width	7, 15, 30, 50 nm
T_{NS}	Nanosheet thickness	6 nm
T_{SUS}	Channel spacing	12 nm
T_{GLE}	Gate line end thickness	15 nm
L_{SP}	Spacer length	6 nm
T_{IL}	Interfacial SiO ₂ thickness	0.6 nm
T_{HK}	High-K (HfO ₂) thickness	1.7 nm
H_G	Gate height	20 nm
$N_{SD,N}$	Source/Drain doping concentration (NMOS)	10^{20} cm^{-3}
$N_{SD,P}$	Source/Drain doping concentration (PMOS)	$5 \times 10^{20} \text{ cm}^{-3}$
C_{PP}	Contacted poly pitch	45 nm
W_{FN}	Gate-metal work-function (NMOS)	4.43 eV
W_{FP}	Gate-metal work-function (PMOS)	4.80 eV
SS_N	Baseline NMOS subthreshold swing	68.0 mV/dec
SS_P	Baseline PMOS subthreshold swing	72.1 mV/dec
$DIBL_N$	Baseline NMOS DIBL	34.2 mV/V
$DIBL_P$	Baseline PMOS DIBL	42.8 mV/V

**Figure 3.** Schematic process flow to fabricate GAAFET CMOS inverter. (a) fin patterning; (b) dummy gate and inner spacer formation; (c) source/drain recess and epitaxy; (d) high-k/metal gate stack formation using the replacement metal gate (RMG) process.

2.2. Simulation Methodology

We evaluated electrical characteristics using a drift–diffusion transport framework applied to the process-based GAAFET structures described in Section 2.1. Our simulations solved Poisson and continuity equations while incorporating a density gradient quantum potential model. We modeled carrier mobility degradation due to doping concentration using the BalMob mobility model, while accounting for high-field velocity saturation with the high-field saturation model. Additionally, we corrected mobility reduction in ultrathin channels using a thin-layer mobility model (IALMob). The mobility model also included normal-field-dependent mobility degradation and ballistic-mobility correction within the drift–diffusion framework. At $L_G = 14$ nm, quasi-ballistic transport may influence the

absolute magnitude of the simulated stress sensitivity; therefore, the reported quantitative values should be understood in the context of the selected drift–diffusion-based transport model. Self-heating effects were not explicitly included in the present simulations; therefore, the reported results should be interpreted under isothermal simulation conditions.

Carrier generation and recombination processes were modeled using Shockley–Read–Hall (SRH) and Auger recombination models, while band-to-band tunneling under high electric fields was represented by the Hurkx band-to-band tunneling model. For Si and SiGe channels, we employed the AutoOrientation-based density gradient model to accurately capture quantum confinement effects.

We incorporated applied metal-gate stress conditions through multivalley mobility and piezo mobility models to reflect changes in effective mass, band structure, and carrier mobility. Additional consideration of the deformation potential accounted for strain-induced modifications in the electronic structure [13]. Therefore, the stress-dependent simulations considered coupled mobility, multivalley, deformation-potential, and quantum-confinement-related effects within the TCAD framework. In addition, the source/drain epitaxy was modeled as an idealized defect-free structure, and defect- or dislocation-induced stress relaxation near the inner spacers was not explicitly considered. The extracted channel stress should therefore be interpreted under this idealized epitaxial-stress assumption.

The analysis primarily focused on quantitatively evaluating stress-induced variations as functions of metal-gate stress and nanosheet width (W_{NS}). At the device level, stress sensitivity was analyzed using threshold voltage (V_{th}), saturation current (I_{dsat}), and effective current (I_{eff}). I_{dsat} was extracted at fixed V_{DD} conditions ($V_{GS} = V_{DS} = V_{DD} = 0.7$ V). The effective current (I_{eff}) was calculated using the standard definition:

$$I_{eff} = \frac{I_H + I_L}{2} \quad (1)$$

where I_H is the drain current at $V_{GS} = V_{DD}$ and $V_{DS} = V_{DD}/2$, and I_L is the drain current at $V_{GS} = V_{DD}/2$ and $V_{DS} = V_{DD}$. For PMOS devices, the current magnitude was used in the calculation.

At the circuit level, CMOS inverter characteristics were evaluated using voltage transfer characteristics (VTCs) and noise margins (NM_H and NM_L). Transient simulations were further performed for a fan-out-of-three (FO3) inverter to compare the stress sensitivities of the high-to-low propagation delay (t_{pHL}), low-to-high propagation delay (t_{pLH}), overshoot voltage (V_{OV}), and undershoot voltage (V_{UND}). Switching energy and energy-delay product (EDP) were also extracted from the transient-current response to evaluate the dynamic energy-delay behavior of the FO3 inverter.

These analyses provide a comprehensive understanding of how W_{NS} and metal-gate stress affect circuit-level operation.

3. Results and Discussion

3.1. Channel Stress and Device-Level Electrical Variability

In the GAA architecture, intrinsic stress applied to the metal gate is transferred to the channel along the length, width, and thickness directions, creating a complex stress state that differs fundamentally from conventional uniaxial stress. This multidirectional stress distribution influences carrier-transport properties and band structure, thereby inducing variations in device electrical characteristics. In the following stress-profile analysis, the stress components shown in Figure 4 were extracted along the channel-center line from the redistributed stress field in the simulated device structure after intrinsic stress was applied to the metal-gate region. This stress-transfer behavior is consistent with previous reports

showing that metal-gate-induced stress can additionally modulate channel stress in GAA nanosheet and nanowire channels [9,18].

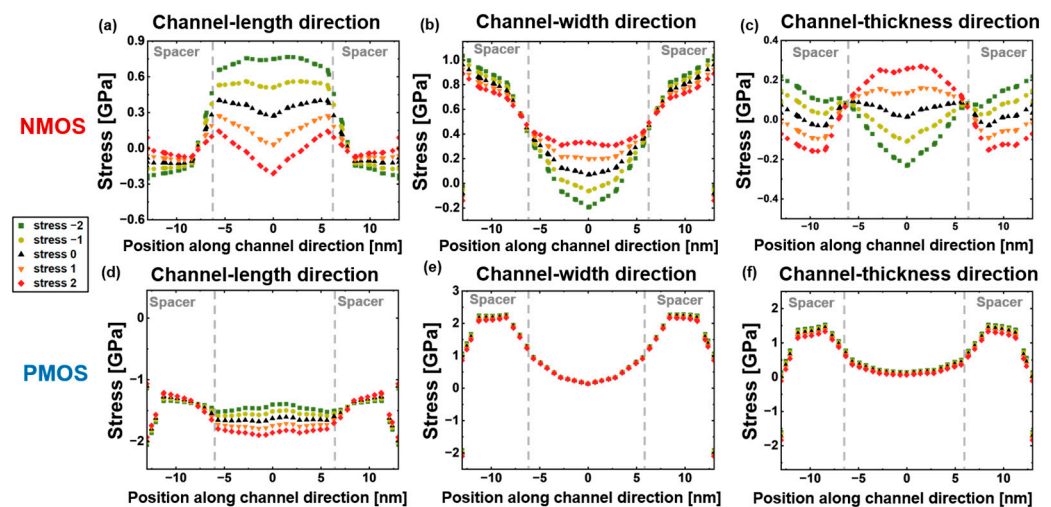


Figure 4. Channel-center stress distributions of the GAAFET CMOS inverter with $W_{NS} = 15$ nm under intrinsic metal-gate stress: (a–c) NMOS and (d–f) PMOS components along the length, width, and thickness directions.

Our simulation results revealed distinct stress-transfer patterns in NMOS devices: tensile metal-gate stress induces compressive stress along the channel length while developing tensile stress along both thickness and width directions. Conversely, compressive metal-gate stress results in tensile stress in the length direction and compressive stress in thickness and width directions. Figure 4a–c confirm these multidirectional stress-transfer patterns through channel-center stress distributions. This composite stress configuration increases the conduction-band edge, leading to increased threshold voltage (V_{th}) and decreased saturation current (I_{dsat}). Figure 5a–c consistently demonstrate this behavior, showing how tensile stress significantly increases V_{th} , delays inversion layer formation, and reduces inversion charge (Q_{inv}) at the same gate voltage, resulting in pronounced degradation of both I_{dsat} and I_{eff} [19,20].

To clarify the physical mechanism of metal-gate stress transfer, the stress response should be interpreted in terms of the multi-axial stress state formed in the nanosheet channel. The intrinsic stress applied to the surrounding metal gate is not transferred to the channel as a purely uniaxial stress. Instead, it induces coupled stress components along the channel-length, -width, and -thickness directions. Therefore, the electrical response is not determined solely by the channel-length-direction stress component, but is also affected by the stress-induced modulation of the channel band profile and electrostatic potential.

This coupled mechanism is important for understanding the stress-dependent current response. From a simplified uniaxial piezoresistance viewpoint, tensile and compressive metal-gate stress would be expected to induce opposite channel-length-direction stress components and therefore opposite mobility-driven current responses. However, in the simulated NMOS device, I_{dsat} decreases under both stress polarities, indicating that the channel-length-direction stress component alone is not sufficient to fully explain the observed trend. Instead, the multi-axial stress state modifies the band and electrostatic conditions of the channel and contributes to the positive V_{th} shift observed under both tensile and compressive metal-gate stress conditions.

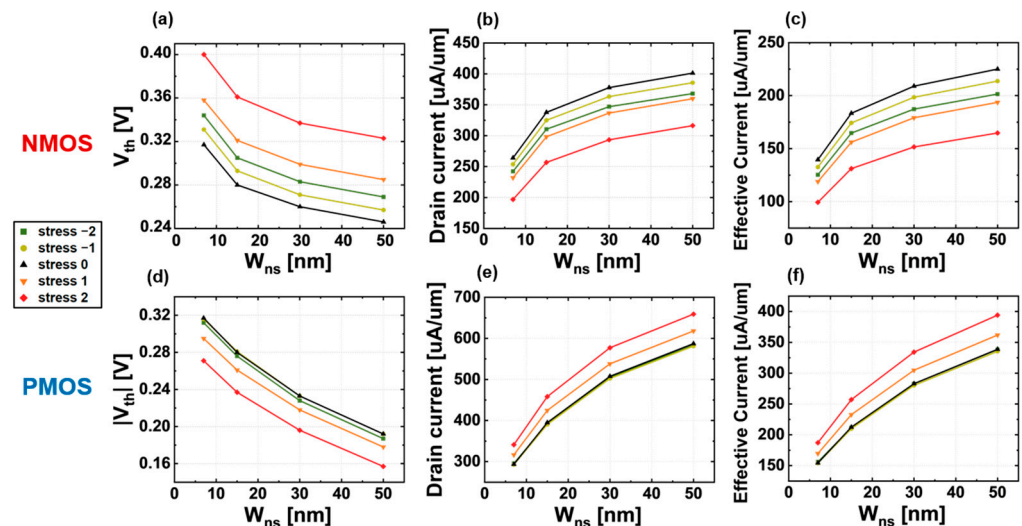


Figure 5. Electrical characteristics under intrinsic metal-gate stress across various W_{NS} values, for (a) NMOS threshold voltage (V_{th}), (b) NMOS drain current, (c) NMOS effective current, (d) PMOS threshold voltage (V_{th}), (e) PMOS drain current, and (f) PMOS effective current.

To support this interpretation, spatial profiles of the conduction-band energy, electrostatic potential, and total current density were extracted along the channel-center cutline, as shown in Figure 6a. The conduction-band-energy and electrostatic-potential profiles were extracted under the high-drain off-state condition to examine stress-induced channel-barrier modulation, whereas the total current-density distribution was extracted under the on-state saturation condition corresponding to the I_{dsat} evaluation condition. As shown in Figure 6b, the conduction-band-energy profile exhibits an upward shift in the channel region under both -2 GPa and $+2$ GPa stress conditions compared with the zero-stress case, with the largest shift observed under $+2$ GPa. The electrostatic-potential profile in Figure 6c also shows stress-dependent modulation in the same channel region. Consistently, the total current-density magnitude in Figure 6d decreases under both stress polarities, following the same trend as the extracted I_{dsat} degradation.

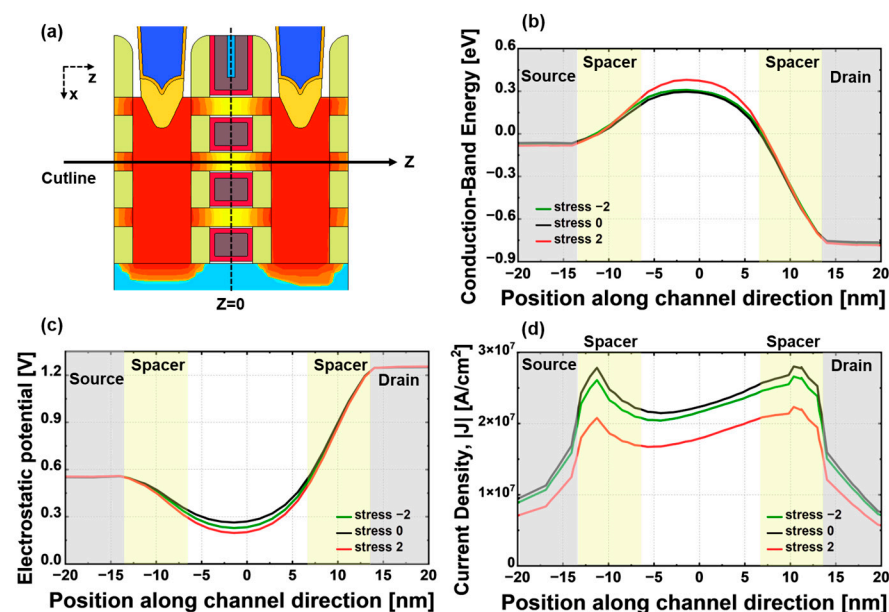


Figure 6. NMOS channel-center cutline profiles with $W_{NS} = 15$ nm under -2 , 0 , and $+2$ GPa metal-gate stress. (a) Cutline location. (b) Conduction-band energy and (c) electrostatic potential extracted at $V_{GS} = 0$ V and $V_{DS} = V_{DD}$. (d) Total current-density magnitude extracted at $V_{GS} = V_{DS} = V_{DD}$.

Taken together, these spatial profiles show that metal-gate-induced stress affects the device response through a coupled mechanism involving multi-axial stress transfer, channel-band/electrostatic modulation, and reduction in channel current flow. This coupled stress-induced band modulation explains the non-monotonic electrical trends observed in Figure 5a–c, where both tensile and compressive gate stress reduce the NMOS current-related characteristics relative to the zero-stress baseline.

For PMOS devices, the channel-direction stress-transfer behavior was similar to that of NMOS devices, as shown in Figure 4d. Tensile gate stress induced compressive channel stress, whereas compressive gate stress induced tensile channel stress. However, the overall PMOS channel stress is mainly governed by the pre-existing compressive stress originating from the SiGe source/drain epitaxy [7]. In this stress state, the intrinsic stress in the metal-gate stack further modifies the pre-existing compressive stress in the PMOS channel. Consequently, the additional stress variations induced by the metal gate in the width and thickness directions remain relatively small, as shown in Figure 4e,f. Under tensile gate stress, the enhanced channel compressive stress slightly raises the valence-band profile and modulates the electrostatic potential in the channel region, consistent with reduced $|V_{th}|$ and increased I_{dsat} and I_{eff} [20]. Figure 5d–f show these effects becoming more pronounced with increasing tensile stress, while changes under compressive stress remain smaller and relatively gradual.

Figure 7 presents the PMOS channel-center cutline profiles of the valence-band energy, electrostatic potential, and total current-density magnitude under -2 , 0 , and $+2$ GPa metal-gate stress conditions. The PMOS valence-band and electrostatic-potential profiles exhibit relatively small but consistent stress-dependent modulation in the channel region. Correspondingly, the total current-density magnitude increases under tensile gate stress, which is consistent with the reduced $|V_{th}|$ and increased I_{dsat} and I_{eff} observed in Figure 5d–f. This asymmetric valence-band/electrostatic modulation explains why the PMOS electrical characteristics do not follow a simple monotonic dependence on the nominal metal-gate stress.

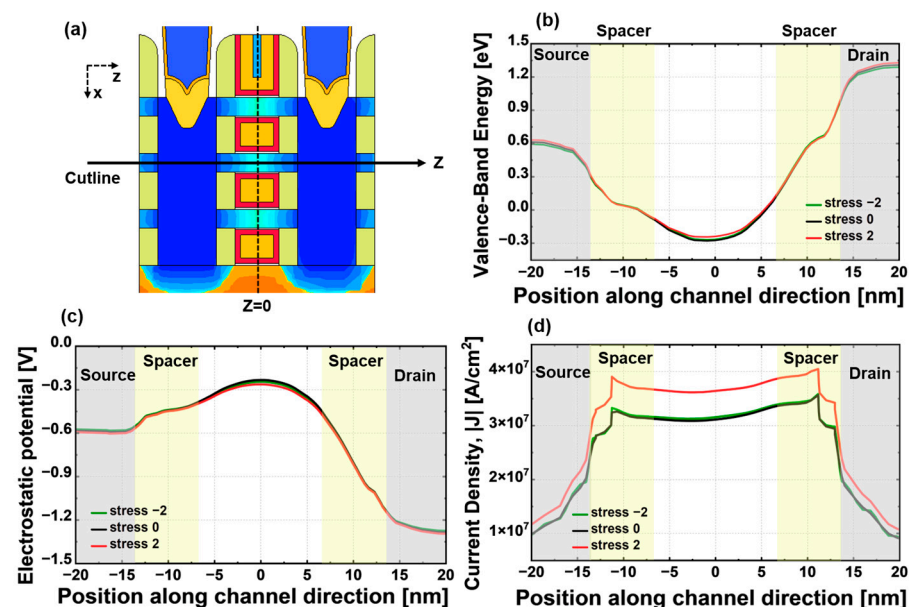


Figure 7. PMOS channel-center cutline profiles with $W_{NS} = 15$ nm under -2 , 0 , and $+2$ GPa metal-gate stress. (a) Cutline location. (b) Valence-band energy and (c) electrostatic potential extracted at $V_{GS} = 0$ V and $|V_{DS}| = V_{DD}$. (d) Total current-density magnitude extracted at $|V_{GS}| = |V_{DS}| = V_{DD}$.

Although NMOS and PMOS devices exhibit similar stress-transfer mechanisms, the resulting electrical characteristic changes (V_{th} , I_{dsat} , and I_{eff}) occur in opposite directions.

These opposite responses potentially cause device-level imbalances under identical stress conditions. Such imbalance increases electrical variability at the device level and can induce skew and delay variations in circuit implementations such as CMOS inverters. We examine these circuit-level implications in detail in subsequent sections, but first investigate the potential of adjusting nanosheet width as a structural design parameter to mitigate imbalances and tune device sensitivity.

Based on these device-level trends, metal-gate intrinsic stress can be considered not only as a process-induced variation source but also as a potentially controllable process parameter for improving PMOS/NMOS drive-current balance. Since NMOS and PMOS employ different gate-metal materials, partially independent stress tuning may be achievable through separate optimization of the deposition conditions. As indicated by the PMOS trend in Figure 5, a moderately tensile PMOS gate-metal stress could selectively enhance PMOS drive current, while the NMOS gate-metal stress could be maintained near zero, providing an additional degree of freedom beyond conventional work-function engineering. It should be noted, however, that these drive-current variations reflect combined contributions of stress-induced V_{th} shift and mobility modulation under fixed- V_{DD} conditions.

Although intentional stress tuning may offer practical benefits, uncontrolled metal-gate stress variation can also lead to device variability. Therefore, the following analysis evaluates the W_{NS} -dependent sensitivity to metal-gate stress variation.

Figure 8 presents the W_{NS} -dependent variations in electrical characteristics under metal-gate stress. For NMOS devices, I_{dsat} changes under compressive stress remained limited to approximately -8% , with minimal W_{NS} dependence. However, as tensile stress increased, I_{dsat} and I_{eff} decreased substantially relative to the corresponding 0 GPa case, with smaller W_{NS} values amplifying sensitivity. PMOS devices showed a similar W_{NS} -dependent sensitivity: under compressive stress, changes were limited to $\pm 1\%$, while tensile stress increased I_{dsat} by up to $+16\%$, with greater variations again observed for smaller W_{NS} values. This phenomenon arises because narrow-channel structures experience less effective stress relaxation with more localized effects [21], and the increased gate-to-channel interface ratio amplifies conduction- and valence-band edge shifts.

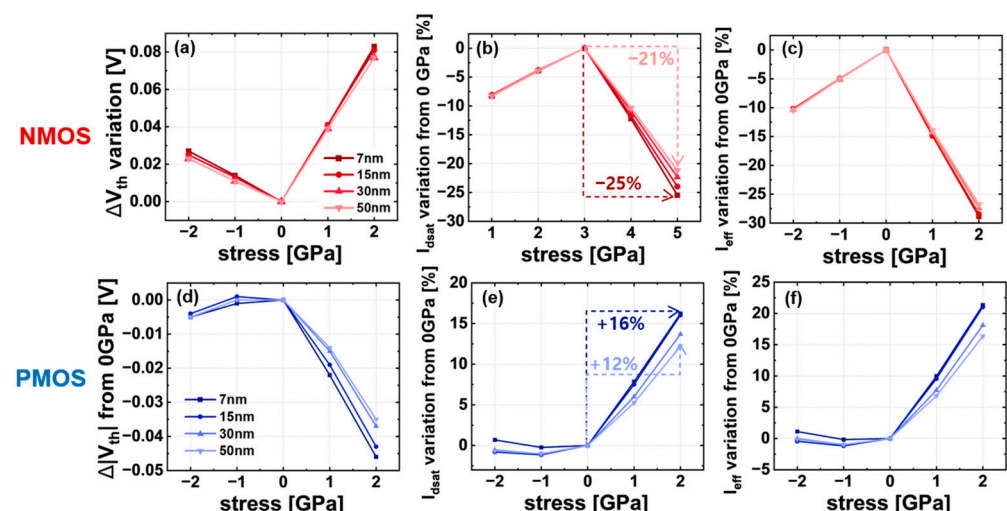


Figure 8. Variations in electrical characteristics relative to the 0 GPa case under intrinsic metal-gate stress for different W_{NS} values: absolute V_{th} change for (a) NMOS and (d) PMOS, percentage I_{dsat} change for (b) NMOS and (e) PMOS, and percentage I_{eff} change for (c) NMOS and (f) PMOS.

These results indicate that smaller W_{NS} values lead to more efficient stress transfer from the metal gate at the device level, thereby increasing electrical variability. Consequently, in GAA architectures, W_{NS} should be regarded not merely as a structural dimen-

sion but as a critical design parameter for controlling stress-induced changes and electrical characteristic variability.

To evaluate the effect of local metal-gate stress fluctuation, the local metal-gate stress was assumed to vary around the nominal 0 GPa condition following a Gaussian distribution:

$$S_{MG} \sim N(0, (0.25 \text{ GPa})^2) \quad (2)$$

where S_{MG} denotes the local metal-gate stress. The assumed distribution is centered at 0 GPa with a standard deviation of 0.25 GPa. The stress-dependent I_{eff} response was obtained from local stress simulations at -0.5 , -0.25 , 0 , $+0.25$, and $+0.5$ GPa. This response was then used to estimate the distribution of I_{eff} variation relative to the corresponding zero-stress value, $I_{eff,0}$, for each W_{NS} .

Figure 9 shows the estimated distributions of I_{eff} variation for NMOS and PMOS devices. The x-axis represents the percentage change in I_{eff} relative to $I_{eff,0}$. Thus, negative and positive values correspond to a decrease and an increase in I_{eff} from the zero-stress value, respectively.

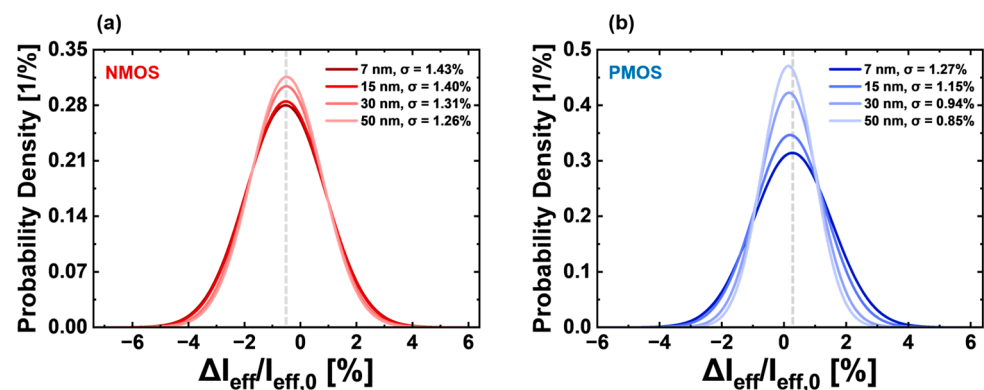


Figure 9. Estimated distributions of I_{eff} variation induced by Gaussian local metal-gate stress fluctuation for (a) NMOS and (b) PMOS devices with different W_{NS} values. The gray dashed line marks the center of the estimated distributions in each panel, highlighting the shift of the distributions from 0% I_{eff} variation.

For NMOS devices, the calculated standard deviations of the I_{eff} -variation distributions were 1.43%, 1.40%, 1.31%, and 1.26% for $W_{NS} = 7$, 15, 30, and 50 nm, respectively. For PMOS devices, the corresponding values were 1.27%, 1.15%, 0.94%, and 0.85%. These larger standard deviations in NMOS indicate that the estimated I_{eff} -variation distributions are broader for NMOS than for PMOS under the assumed local metal-gate stress fluctuation.

Although the assumed local metal-gate stress distribution is centered at 0 GPa, the estimated I_{eff} distributions are not exactly centered at 0%. The NMOS distributions are slightly shifted toward negative I_{eff} variation, whereas the PMOS distributions are shifted toward positive I_{eff} variation. This indicates that the I_{eff} changes induced by positive and negative local metal-gate stress are not identical in magnitude within the investigated stress range.

In both NMOS and PMOS devices, the distribution width decreases as W_{NS} increases. This result indicates that wider nanosheets reduce the I_{eff} variation caused by local metal-gate stress fluctuation. This W_{NS} -dependent trend is consistent with the deterministic device-level analysis, where smaller W_{NS} values showed larger stress-induced changes in electrical characteristics.

3.2. Circuit-Level Impact of Stress and WNS Scaling

This section quantitatively evaluates how device-level electrical characteristic variations analyzed previously impact circuit operation. Considering that opposite stress sensitivities of NMOS and PMOS devices can induce skew or delay imbalance in CMOS inverters, we conducted circuit-level simulations based on inverter structures. Our circuit-level analysis employed two complementary approaches:

(1) From a DC perspective, we extracted switching voltage (V_M) and noise margins (NM_H and NM_L) from voltage transfer characteristics to analyze how metal-gate stress and W_{NS} variation affect circuit static operating characteristics.

(2) From an AC perspective, we applied pulse inputs to FO3 inverter chains and quantitatively evaluated the stress sensitivities of delay times (t_{pHL} and t_{pLH}), overshoot/undershoot voltages (V_{OV} and V_{UND}) [22], and transient-current-based dynamic energy-delay metrics.

Metal-gate stress and WNS variations affect not only device-level current characteristics but also static operating characteristics of circuits, including CMOS inverter VTCs. Figure 10a illustrates VTC curves for various stress conditions under the baseline configuration ($W_{NS} = 15$ nm), showing rightward shifts in switching threshold voltage (V_M) with increasing stress. As discussed in Section 3.1, NMOS devices exhibited increased V_{th} and decreased I_{dsat} under both tensile and compressive stresses, leading to overall pull-down capability reduction. This effect becomes more pronounced under tensile stress, while PMOS devices are strengthened, causing the inverter's overall current balance point to shift toward the PMOS side.

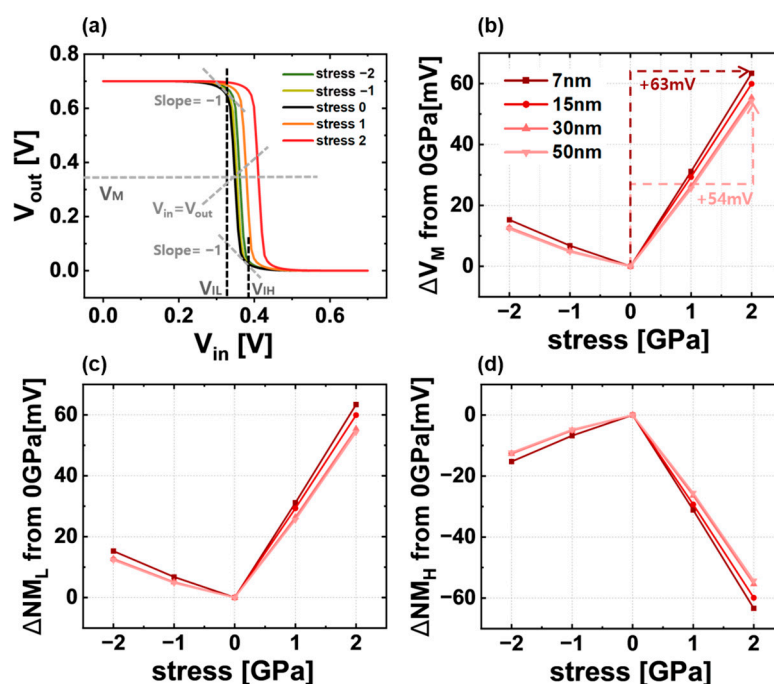


Figure 10. VTC and noise-margin characteristics of the GAAFET CMOS inverter under intrinsic metal-gate stress: (a) VTC curves for $W_{NS} = 15$ nm and variations relative to the 0 GPa case for (b) ΔV_M , (c) ΔNM_L , and (d) ΔNM_H with different W_{NS} values.

These changes also impact noise-margin characteristics: as V_M increases, NM_H decreases, while NM_L increases, resulting in asymmetric variation. Notably, under tensile stress, ΔV_M reached +63 mV, with the most pronounced asymmetry observed in NM_H and NM_L . This behavior represents a VTC shift toward the PMOS side, reducing voltage margin in the pull-down region while increasing it in the pull-up region. These results directly

reflect the influence of device-level current-characteristic variations on circuit operation and carry significant implications for switching stability in digital circuits.

Furthermore, the stress-sensitivity analysis with respect to W_{NS} variation in Figure 10b–d shows that smaller W_{NS} values result in larger stress-induced shifts in V_M , NM_H , and NM_L . This occurs because narrower channels transfer metal-gate stress more effectively, making current imbalance between devices more strongly reflected in circuit voltage characteristics. Conversely, larger W_{NS} values produce a relatively relaxed strain distribution, resulting in smaller voltage characteristic variations under stress.

We analyzed circuit dynamic characteristics using an FO3-configured CMOS inverter chain with key evaluation metrics shown in Figure 11a. The effective load capacitance in the FO3 configuration was determined by the gate capacitance of the following inverter stages. Figure 11b shows t_{pHL} and t_{pLH} for different stress conditions under the baseline configuration ($W_{NS} = 15$ nm). The t_{pHL} value generally increased with increasing stress, showing an approximately +16% increase in delay under tensile stress. This behavior stems from upward shifts of the NMOS conduction-band edge and delayed inversion layer formation, which slows current conduction in the pull-down path. In contrast, t_{pLH} exhibits negligible changes under compressive stress but decreases sharply by approximately 12% with increasing tensile stress, which is attributed to enhanced PMOS performance leading to faster current delivery in the pull-up path.

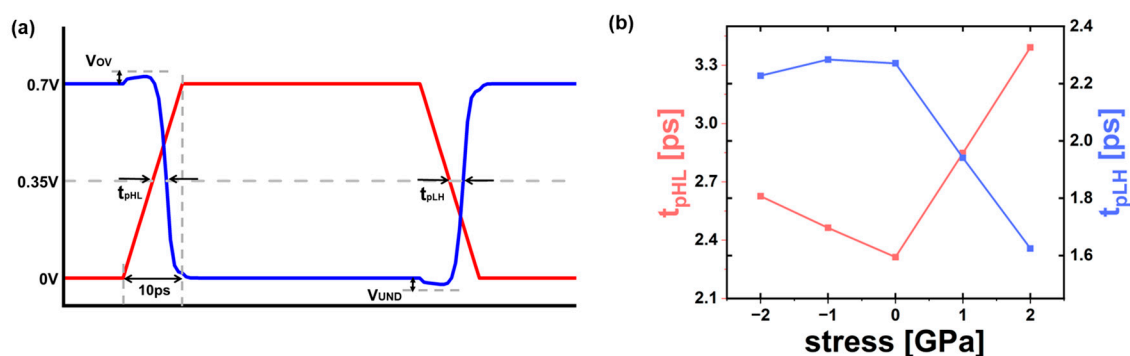


Figure 11. (a) Input waveform of a GAAFET CMOS inverter, with four extracted parameters (t_{pHL} , t_{pLH} , V_{OV} , and V_{UND}). The red and blue lines represent the input and output voltage waveforms, respectively. (b) t_{pHL} and t_{pLH} under intrinsic metal-gate stress in a GAAFET CMOS inverter with $W_{NS} = 15$ nm.

Figure 12a,b quantitatively compare delay sensitivity with respect to W_{NS} variation. The delay sensitivity was quantified as the percentage variation in t_p with respect to the corresponding 0 GPa case for each W_{NS} :

$$\Delta t_p(W_{ns}, \sigma)(\%) = \frac{t_p(W_{ns}, \sigma) - t_p(W_{ns}, 0)}{t_p(W_{ns}, 0)} \times 100 \quad (3)$$

where t_p represents either t_{pHL} or t_{pLH} , and σ denotes the applied metal-gate stress. As shown in Figure 12a,b, both t_{pHL} and t_{pLH} exhibit stronger stress-induced variations at larger W_{NS} values, although the polarity of the variation differs between the pull-down and pull-up transitions. This trend is distinct from the static voltage characteristics discussed above, where smaller W_{NS} values showed larger stress sensitivity.

Voltage swing characteristics were also sensitive to both metal-gate stress and W_{NS} variation. Figure 12c,d show the stress sensitivity of overshoot voltage (V_{OV}) and undershoot voltage (V_{UND}). With increasing metal-gate stress, V_{OV} shifted toward higher values while V_{UND} shifted toward lower values. These changes became more pronounced for smaller W_{NS} values, whereas larger W_{NS} values showed negligible stress-induced voltage

response variations. This behavior stems from more concentrated stress transfer in narrower channels, which amplifies drive-current imbalance between pull-up and pull-down transistors. Consequently, the difference between rising- and falling-edge transition speeds increases, leading to larger overshoot/undershoot voltages and greater circuit voltage response asymmetry. These results indicate that overshoot/undershoot characteristics exhibit directional trends similar to static characteristics, with smaller W_{NS} values showing higher stress sensitivity.

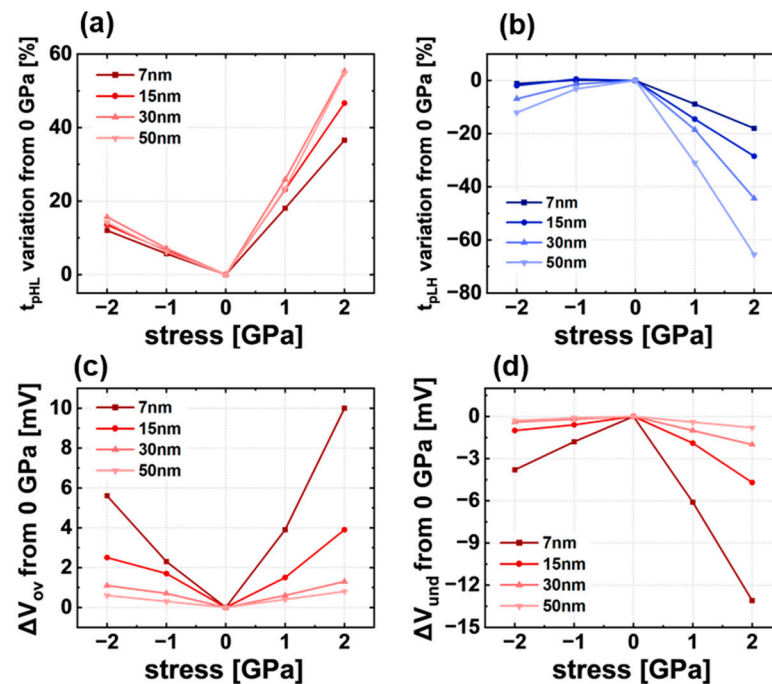


Figure 12. Variations in transient inverter characteristics relative to the 0 GPa case under intrinsic metal-gate stress for different W_{NS} values: (a) t_{pHL} , (b) t_{pLH} , (c) ΔV_{OV} , and (d) ΔV_{UND} .

In addition to the timing and voltage response metrics shown in Figure 12, the transient supply-current waveform was used to extract switching energy and evaluate the dynamic energy-delay response of the FO3 inverter. The switching energy was calculated by integrating the supply current over one FO3 input cycle:

$$E_{sw} = \int_{t_0}^{t_0+T} V_{DD} I_{DD}(t) dt \quad (4)$$

where $I_{DD}(t)$ denotes the positive supply current drawn from the voltage source during one FO3 input cycle. The average propagation delay and energy-delay product (EDP) were defined as

$$t_{pd} = \frac{t_{pHL} + t_{pLH}}{2} \quad (5)$$

$$EDP = E_{sw} \times t_{pd} \quad (6)$$

Figure 13 shows the FO3 dynamic energy-delay response under metal-gate stress. Figure 13a shows the switching-energy versus average propagation-delay trade-off at 0 GPa. As W_{NS} increases, t_{pd} decreases because of the enhanced drive capability. However, E_{sw} increases because the larger nanosheet width increases the gate capacitance and the effective FO3 capacitive load. Therefore, increasing W_{NS} does not simply improve inverter operation in an energy-efficient manner, but introduces a speed-energy trade-off at the loaded inverter stage.

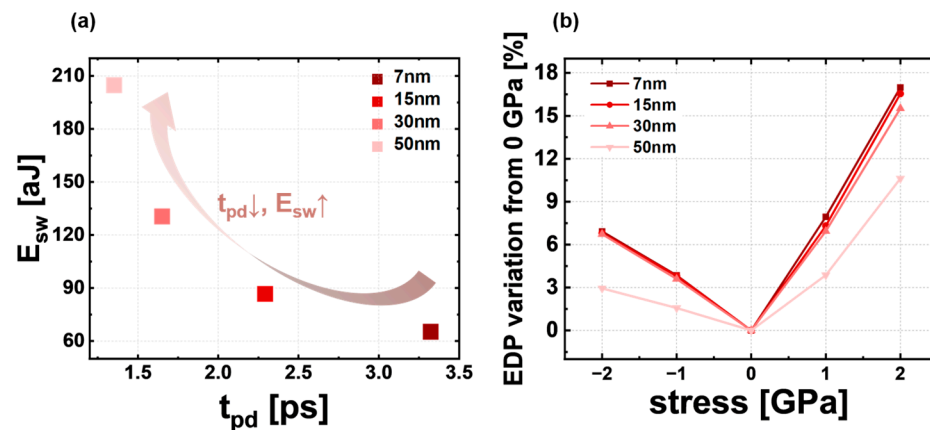


Figure 13. FO3 dynamic energy-delay response under metal-gate stress: (a) switching-energy versus average propagation-delay trade-off at 0 GPa, where the arrow indicates the direction of decreasing t_{pd} and increasing E_{sw} ; and (b) stress-induced EDP variation relative to the corresponding 0 GPa case for different W_{NS} values.

Figure 13b shows the stress-induced EDP variation with respect to the corresponding 0 GPa case. For $W_{NS} = 7, 15$, and 30 nm, the EDP increases significantly under tensile stress, indicating that metal-gate stress produces a dynamic energy-delay penalty in the loaded inverter stage. In contrast, the EDP variation is relatively smaller at $W_{NS} = 50$ nm, although its absolute switching energy is the largest. These results indicate that the stress-induced energy-delay response is strongly dependent on W_{NS} , reflecting the combined effects of capacitive loading, drive-current modulation, and propagation-delay variation.

The delay time can be approximated as

$$Delay \propto \frac{C_{load} \cdot V_{DD}}{I_{drive}} \quad (7)$$

To interpret the W_{NS} -dependent dynamic timing and energy-delay responses, channel resistance (R_{ch}) and C_{gg} were compared in Figure 14. Here, C_{gg} denotes the inverter gate capacitance extracted from the C–V characteristics and is used as an effective capacitive-loading metric for the FO3 inverter chain. In the FO3 configuration, the load capacitance, C_{load} , is directly related to the input gate capacitance of the following inverter stages. Therefore, an increase in C_{gg} leads to an increase in the effective C_{load} [23,24].

As shown in Figure 14, R_{ch} decreases for both NMOS and PMOS as W_{NS} increases, indicating improved drive capability. At the same time, C_{gg} increases with W_{NS} , thereby increasing the effective FO3 capacitive load and switching energy. This result explains why wider nanosheets reduce propagation delay but require larger switching energy, as shown in Figure 13a. Therefore, the dynamic circuit response should not be attributed solely to either drive-current enhancement or capacitance increase. Instead, it should be interpreted as a net loaded-stage response determined by the competition among improved drive capability, increased capacitive loading, stress-dependent drive-current modulation, and dynamic switching behavior.

Accordingly, stress sensitivity varies with the performance metric, resulting in different optimal W_{NS} scaling directions depending on the characteristics of interest. Specifically, static and quasi-static parameters (V_M , N_{MH} , and N_{ML}) exhibited greater stress sensitivity at smaller W_{NS} values, while dynamic delay metrics (t_{pHL} and t_{pLH}) showed greater stress sensitivity for larger W_{NS} values. In contrast, overshoot/undershoot voltages followed patterns similar to static characteristics, with smaller W_{NS} values exhibiting more pronounced asymmetric responses. The dynamic energy-delay analysis further shows that W_{NS} scaling introduces a trade-off between reduced propagation delay and increased switching

energy, while the stress-induced EDP variation reflects the combined timing and energy response of the FO3 inverter. These opposing tendencies reflect the combined effects of device-level stress-transfer characteristics, circuit RC trade-offs, fan-out conditions, and dynamic energy-delay behavior.

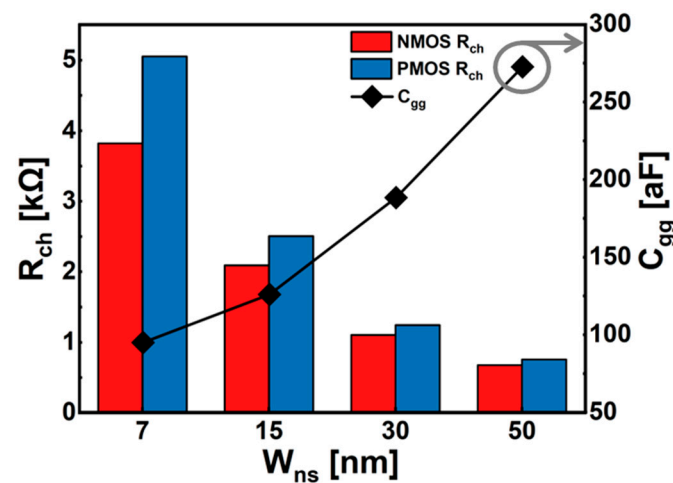


Figure 14. NMOS and PMOS channel resistance (R_{ch}) and inverter gate capacitance (C_{gg}) at 0 GPa stress for different W_{NS} values. The arrow indicates the right y-axis for C_{gg} .

Overall, the results of this section demonstrate that W_{NS} serves as a pivotal parameter for modulating stress-induced electrical variability at the device level and translating these effects into circuit-level performance in GAA-based CMOS inverters. This role of W_{NS} is consistent with a key advantage of GAA nanosheet FETs, where nanosheet-width engineering provides an additional design degree of freedom for tuning effective channel width and drive capability within the nanosheet process architecture [3,5,25]. Through appropriate W_{NS} selection, skew and delay variations arising from metal-gate intrinsic stress can be mitigated, supporting strategies for managing variability and maintaining consistent device-circuit performance. In addition, stress-induced changes in threshold voltage and carrier transport may also become relevant to reliability degradation mechanisms such as bias temperature instability (BTI) and hot-carrier effects.

Furthermore, if metal-gate intrinsic stress can be precisely controlled during fabrication, it may be considered not only as a source of process-induced variation but also as an additional process-design parameter for tuning PMOS/NMOS drive-current balance and inverter-level metrics such as the switching point, noise-margin symmetry, and propagation-delay asymmetry. In this context, intentional metal-gate stress engineering, together with W_{NS} -based sensitivity management, should be further explored as a potential future direction for process/device co-optimization.

4. Conclusions

This study investigated the impact of metal-gate-induced intrinsic stress on GAA-based CMOS inverters using process-based TCAD simulations. Identical metal-gate stress conditions induced different current responses in NMOS and PMOS devices, leading to current imbalance and asymmetric inverter operation. These device-level variations were also reflected in inverter-level circuit behavior.

Nanosheet width (W_{NS}) was identified as a key design parameter for controlling stress sensitivity. Because individual threshold-voltage calibration for every stress condition is difficult in practical fabrication environments, W_{NS} tuning provides a practical approach for mitigating device-level imbalance and improving circuit uniformity. The results also reveal a metric-dependent trade-off: larger W_{NS} values reduce voltage response sensitivity,

whereas smaller W_{NS} values reduce delay sensitivity. However, uncontrolled W_{NS} variation or nonuniform stress distribution may still cause unexpected skew and performance deviations, requiring reliability-oriented design considerations.

Overall, this work provides a device-to-circuit analysis framework for the effects of metal-gate-induced stress in GAAFET CMOS inverters. The results emphasize the role of W_{NS} as a stress-aware structural parameter for managing metal-gate stress-induced device imbalance and inverter-level performance variation. Future work may extend this framework to larger logic blocks, ring oscillators, and SRAM stability analysis.

Author Contributions: Conceptualization, S.L. and J.L.; methodology, S.L. and J.L.; software, S.L. and J.L.; validation, S.L. and J.L.; formal analysis, S.L. and J.L.; investigation, S.L. and J.L.; resources, S.L. and J.L.; data curation, S.L. and J.L.; writing—original draft preparation, S.L.; writing—review and editing, S.L., J.L., D.H., M.K. and C.S.; visualization, S.L.; supervision, C.S.; project administration, C.S.; funding acquisition, C.S.; S.L. and J.L. contributed equally to this study. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by the Technology Innovation Program (P0023718) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea). This work was also supported by K-CHIPS (Korea Collaborative & High-tech Initiative for Prospective Semiconductor Research) (2410012306, 02305570, 25069-15FC) funded by the Ministry of Trade, Industry & Energy (MOTIE, Korea).

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Acknowledgments: The EDA tool, Sentaurus TCAD, was supported by the IC Design Education Center (IDEC), Republic of Korea.

Conflicts of Interest: Author Jaehyuk Lim was employed by the Foundry Division, Samsung Electronics, Hwaseong, Republic of Korea. Author Donghwan Han was employed by the Semiconductor R&D Center, Samsung Electronics, Hwaseong, Republic of Korea. All authors declare that there are no other commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Cheng, Y.; Chen, K.; Imai, K.; Hu, C. A unified MOSFET channel charge model for device modeling in circuit simulation. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **1998**, *17*, 641–644. [\[CrossRef\]](#)
2. Xu, C.; Kolluri, S.K.; Endo, K.; Banerjee, K. Analytical thermal model for self-heating in advanced FinFET devices with implications for design and reliability. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2013**, *32*, 1045–1058. [\[CrossRef\]](#)
3. Bae, G.; Bae, D.-I.; Kang, M.; Hwang, S.; Kim, S.; Seo, B.; Kwon, T.; Lee, T.; Moon, C.; Choi, Y. 3nm GAA technology featuring multi-bridge-channel FET for low power and high performance applications. In Proceedings of the 2018 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 1–5 December 2018; pp. 28.7.1–28.7.4.
4. Mohan, C.; Choudhary, S.; Prasad, B. Gate all around FET: An alternative of FinFET for future technology nodes. *Int. J. Adv. Res. Sci. Eng.* **2017**, *6*, 563–569.
5. Mukesh, S.; Zhang, J. A review of the gate-all-around nanosheet FET process opportunities. *Electronics* **2022**, *11*, 3589. [\[CrossRef\]](#)
6. Zhu, C.; Zhu, X.; Yu, S.; Zhang, D.W. Process-dependent Evolution of Channel Stress and Stress-induced Mobility Gain in FinFET, Normal-and Si/SiGe Hybrid Channel GAAFET. *IEEE Access* **2025**, *13*, 21600–21609. [\[CrossRef\]](#)
7. Reboh, S.; Coquand, R.; Barraud, S.; Loubet, N.; Bernier, N.; Audoit, G.; Rouviere, J.-L.; Augendre, E.; Li, J.; Gaudiello, J. Strain, stress, and mechanical relaxation in fin-patterned Si/SiGe multilayers for sub-7 nm nanosheet gate-all-around device technology. *Appl. Phys. Lett.* **2018**, *112*, 051901. [\[CrossRef\]](#)
8. Mohapatra, E.; Jena, D.; Das, S.; Maiti, C.; Dash, T. Design and optimization of stress/strain in GAA nanosheet FETs for improved FOMs at sub-7 nm nodes. *Phys. Scr.* **2023**, *98*, 065919. [\[CrossRef\]](#)
9. Singh, N.; Fang, W.; Rustagi, S.; Budharaju, K.; Teo, S.H.; Mohanraj, S.; Lo, G.; Balasubramanian, N.; Kwong, D.-L. Observation of Metal-Layer Stress on Si Nanowires in Gate-All-Around High- κ /Metal-Gate Device Structures. *IEEE Electron Device Lett.* **2007**, *28*, 558–561. [\[CrossRef\]](#)
10. Wu, Y.-S.; Su, P. Sensitivity of gate-all-around nanowire MOSFETs to process variations—A comparison with multigate MOSFETs. *IEEE Trans. Electron Devices* **2008**, *55*, 3042–3047. [\[CrossRef\]](#)

11. Nam, H.; Lee, Y.; Park, J.-D.; Shin, C. Study of Work-Function Variation in High- κ /Metal-Gate Gate-All-Around Nanowire MOSFET. *IEEE Trans. Electron Devices* **2016**, *63*, 3338–3341. [[CrossRef](#)]
12. Lim, J.; Han, D.; Seon, S.; Baac, H.W.; Shin, C. Design for variability: Counter-doped source/drain epitaxy pockets in gate-all-around FET. *IEEE Trans. Electron Devices* **2023**, *71*, 400–405.
13. Guide, T.S.U. *TCAD Sentaurus User Guide*; Synopsys, Inc.: Mountain View, CA, USA, 2019.
14. Auth, C.; Aliyarukunju, A.; Asoro, M.; Bergstrom, D.; Bhagwat, V.; Birdsall, J.; Bisnik, N.; Buehler, M.; Chikarmane, V.; Ding, G. A 10nm high performance and low-power CMOS technology featuring 3rd generation FinFET transistors, Self-Aligned Quad Patterning, contact over active gate and cobalt local interconnects. In Proceedings of the 2017 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 2–6 December 2017; pp. 29.2.1–29.2.4.
15. Kang, D.; Kim, Y.S.; Kim, J.N.; Park, I.K. Characteristics of TiN thin films deposited by substrate temperature variables using scanning acoustic microscopy. *Appl. Sci.* **2022**, *12*, 3571. [[CrossRef](#)]
16. Shen, Y.; Mai, Y. Crystallization-induced stress in tungsten nitride thin films. *J. Mater. Sci. Lett.* **2000**, *19*, 1941–1943. [[CrossRef](#)]
17. Machunze, R.; Ehasarian, A.; Tichelaar, F.; Janssen, G. Stress and texture in HIPIMS TiN thin films. *Thin Solid Films* **2009**, *518*, 1561–1565. [[CrossRef](#)]
18. Reboh, S.; Coquand, R.; Loubet, N.; Bernier, N.; Augendre, E.; Chao, R.; Li, J.; Zhang, J.; Muthinti, R.; Boureau, V. Imaging, modeling and engineering of strain in gate-all-around nanosheet transistors. In Proceedings of the 2019 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 7–11 December 2019; pp. 11.5.1–11.5.4.
19. Lim, J.-S.; Thompson, S.E.; Fossum, J.G. Comparison of threshold-voltage shifts for uniaxial and biaxial tensile-stressed n-MOSFETs. *IEEE Electron Device Lett.* **2004**, *25*, 731–733. [[CrossRef](#)]
20. Thompson, S.; Sun, G.; Wu, K.; Lim, J.; Nishida, T. Key differences for process-induced uniaxial vs. substrate-induced biaxial stressed Si and Ge channel MOSFETs. In Proceedings of the IEDM Technical Digest. IEEE International Electron Devices Meeting, 2004, IEDM Technical Digest, San Francisco, CA, USA, 13–15 December 2004; pp. 221–224.
21. Liu, Y.-Y.; Lu, H.; Wang, Z.; Zeng, L.; Deng, H.-X.; Wei, Z.; Wang, L.-W.; Luo, J.-W.; Wang, R. Strain-and dipole-induced interface states in gate-all-around transistors: Properties and implications for application. *Phys. Rev. Appl.* **2025**, *23*, 034020. [[CrossRef](#)]
22. Lim, J.; Han, D.; Sung, J.; Yoon, S.; Kang, S.; Kim, G.; Baac, H.W.; Shin, C. Device Design Guidelines to Boost up AC Performance of CFET (Complementary Field-Effect-Transistor)-Based Inverter. *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2025**, *44*, 3189–3196. [[CrossRef](#)]
23. Wei, L.; Boeuf, F.; Skotnicki, T.; Wong, H.-S.P. Parasitic capacitances: Analytical models and impact on circuit-level performance. *IEEE Trans. Electron Devices* **2011**, *58*, 1361–1370. [[CrossRef](#)]
24. Sarker, S.; Kumar, A.; Ehteshamuddin, M.; Dasgupta, A. Compact modeling of parasitic capacitances in GAAFETs for advanced technology nodes. *IEEE J. Electron Devices Soc.* **2023**, *11*, 510–517. [[CrossRef](#)]
25. Loubet, N.; Hook, T.; Montanini, P.; Yeung, C.-W.; Kanakasabapathy, S.; Guillom, M.; Yamashita, T.; Zhang, J.; Miao, X.; Wang, J. Stacked nanosheet gate-all-around transistor to enable scaling beyond FinFET. In Proceedings of the 2017 Symposium on VLSI Technology, Kyoto, Japan, 5–8 June 2017; pp. T230–T231.

Disclaimer/Publisher’s Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.