

Article

A DC-DC Converter Reuse-Based Double-Line Frequency Ripple Suppression Method for Substation Uninterruptible Power Supply Systems

Sigun Sun ^{1,2}, Khalil Yiming Wang ³, Yifeng Chen ², Qiuxue Wang ⁴ and Yuanxi Chen ^{1,*} 

¹ College of Information Science and Engineering, Huaqiao University, Xiamen 361021, China; sunsg@evadaups.com

² Xiamen EVADA Electronics Co., Ltd., Xiamen 361000, China; cyf@evadaups.com

³ Department of Engineering Science, Macau University of Science and Technology, Macau 999078, China; 1240009839@student.must.edu.mo

⁴ School of Intelligent Manufacturing Engineering, Liming Vocational University, Quanzhou 362000, China; 20231005@lmu.edu.cn

* Correspondence: yuanxi.chen@hqu.edu.cn

Abstract

As a critical device for ensuring stable operation in power substations, an Uninterruptible Power Supply (UPS) plays a vital role in maintaining a continuous power supply, improving power quality, and enhancing system reliability. However, startup inrush current and backflow ripple voltage significantly impact the stability of DC power supply equipment. This paper proposes a DC-DC circuit-reuse method with double-line frequency ripple suppression for substation UPS systems. This approach utilizes a boost converter to transfer the double-line frequency pulsation from the DC input to the bus capacitor side, thereby reducing the double-line frequency components at the input. Notably, this Boost converter simultaneously serves as part of the power factor correction (PFC) circuit connecting the grid and DC bus, achieving functional integration that significantly reduces system costs. A 3 kVA UPS experimental platform was constructed to validate the proposed method. The test results demonstrate that while the bus voltage exhibits slight pulsation at double-line frequency, the input current transforms into an approximate DC quantity. This second-harmonic ripple suppression method effectively improves key performance indicators: Startup inrush current decreases by 38% compared to conventional designs, and backflow ripple voltage amplitude is suppressed below 0.5% of the nominal DC voltage. The proposed topology demonstrates superior compatibility with existing substation DC systems and provides a cost-optimized solution for power quality enhancement in critical infrastructure applications.



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1. Introduction

Uninterruptible Power Supply (UPS) systems have zero-interruption power switching and multi-dimensional power purification capabilities. UPS can simultaneously perform voltage regulation, harmonic suppression, and transient surge protection, mitigating frequency drift, electromagnetic noise, and other power quality disturbances in the grid [1,2], and the detailed operation principles and control strategies of UPS systems are discussed. As the central hub of critical infrastructure, UPS systems have been extensively deployed to ensure data integrity, enhancing the reliability of life-support systems and enabling

high-precision industrial control applications. As a critical power infrastructure, substation power systems are typically equipped with battery banks as backup power sources to ensure power supply reliability [3,4], and they analyze the resilience and coordinated energy management of such DC power infrastructures. Consequently, substation UPS systems do not require additional energy storage devices. Instead, they draw power directly from the DC distribution panel and convert it through an inverter to supply energy to the load, as illustrated in Figure 1 [5,6], where high-performance online UPS architectures are introduced.

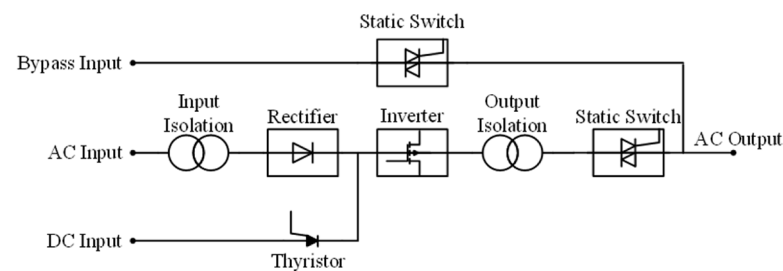


Figure 1. Structure of an Uninterruptible Power Supply.

The frequency of the output voltage and output current is 50 Hz, resulting in an instantaneous output power pulsation at 100 Hz (twice the rated condition) when the UPS serves as the inverter. According to the principle of power conservation, the current or voltage on the DC side will also exhibit a pulsation at twice the fundamental frequency on the AC side [7]. When the UPS is powered by a switching power supply, the DC voltage is regulated but contains low-frequency, high-peak ripple pulsations. This not only affects the stability of the switching power supply but also leads to increased heat generation and reduced lifespans [8,9], where the DC-link current and voltage ripple are rigorously analyzed. In parallel, advanced magnetic structures and control strategies for power electronic converters have been extensively investigated for high-performance DC–DC conversion [10–12], as well as sophisticated grid-synchronization and control schemes such as SOGI-based PLLs [13]. These techniques are closely related to the high-performance implementation of UPS and DC–DC stages.

Regardless of whether the DC power source is a switching power supply or a battery, it fails to meet the substation UPS requirements for low startup currents and low back-feed ripple voltages. As a result, the suppression of second-harmonic ripple has remained a critical research focus and technical challenge in the industry. To address this issue, researchers have conducted extensive research on second-harmonic suppression.

Current methods for suppressing second-harmonic ripple can be broadly categorized into three types: passive filtering, active power decoupling, and dedicated auxiliary converters. The first type, passive filtering, involves adding passive power components to reduce or absorb the low-frequency voltage/current ripple, such as introducing inductors and increasing the bus capacitor [14]. This method is simple and widely used in substation UPS products, but it leads to bulky and costly passive components and still provides limited suppression, especially at high power levels. The second type is active power decoupling based on improved modulation or control strategies. For example, ref. [15] injects specific harmonics into the SPWM modulation wave to suppress the second harmonic, while refs. [16,17] estimate or control the second-harmonic component of the DC bus to mitigate low-frequency ripple. Although these methods can reduce the required passive component size, they usually introduce additional control complexity and may affect the output power quality, which restricts their application in industrial UPS systems. The third type employs dedicated auxiliary converters connected to the DC bus to buffer the double-

line frequency power. Typical examples include parallel-connected DC–DC converters for ripple suppression [18,19] and switched-capacitor-based UPS topologies [20]. These solutions effectively attenuate the second-harmonic ripple but increase system complexity and hardware cost, which is not attractive for compact and cost-sensitive substation UPS applications. Although these solutions effectively attenuate the second-harmonic ripple, they increase system complexity and hardware costs, and sometimes, they still require further validation for practical substation applications. In addition, for complex power electronic systems such as substation UPS, identifying the root causes of multiport instability [21] and improving fault diagnosis capabilities for multi-switch topologies [22] are also important to ensure overall system reliability and robustness in smart grid applications.

However, existing solutions still suffer from one or more of the following drawbacks in substation UPS applications: (i) bulky and expensive passive components, (ii) additional power stages and semiconductor devices, and (iii) increased control and implementation complexity with limited compatibility with existing PFC front-ends. To address the aforementioned issues, this paper proposes a DC–DC converter reuse-based second-harmonic ripple suppression method, in which the existing boost converter in the PFC stage is reused for both PFC and double-line frequency ripple suppression without adding extra power stages. By detecting AC input abnormalities and dynamically switching the boost converter between AC/DC and DC/DC modes, the proposed method not only maintains excellent power factor correction (PFC) performance and low current harmonic distortion but also effectively suppresses second-harmonic ripples. By integrating the PFC and ripple suppression control loops without adding extra system costs, this method fully meets the performance requirements of substation UPS systems.

The main contributions of this work are given as follows:

- (1) A converter-reuse topology that shares a single boost stage for both PFC and DC-side ripple suppression in substation UPS systems.
- (2) A unified dual-loop control strategy that enables seamless mode switching while maintaining low DC-side ripples and high input power factors.
- (3) Comprehensive simulation and 3 kVA experimental validation under realistic operating conditions, including quantitative comparisons with conventional DC input connection schemes.

2. Analysis of Second-Harmonic Ripple in UPS Applications

We assume that the Uninterruptible Power Supply (UPS) inverter output voltage u_o and output current i_o are ideal without harmonics, and they are defined as follows:

$$u_o = U_o \sin(t) \quad (1)$$

$$i_o = I_o \sin(t) \quad (2)$$

where ω_o is the operating angular frequency of the system, equaling $2\pi f$.

For the UPS application, f is 50 Hz, and U_o is 220 V. When the UPS has a resistive load, the instantaneous output power is given by Equation (3). This resistive-load assumption is adopted here only as a modeling simplification to clearly illustrate the double-line frequency component in the output power.

$$P_o = u_o i_o = U_o \sin(\omega_o t) \cdot I_o \sin(\omega_o t) = \frac{1}{2} U_o I_o - \frac{1}{2} U_o I_o \cos(2\omega_o t) \quad (3)$$

As given in Equation (3), the instantaneous output power oscillates at twice the fundamental frequency, the output power fluctuates at a frequency of $2\omega_o$, and the total power oscillates within the range of $[0, U_o I_o]$.

Assuming a regulated DC output u_{dc} from the substation's DC switch-mode power supply and neglecting energy conversion efficiency, the DC input current i_{dc} can be expressed as follows:

$$i_{dc} = \frac{P_o}{u_{dc}} = \frac{U_o I_o}{2u_{dc}} - \frac{U_o I_o \cos(2\omega_o t)}{2u_{dc}} = I_{dc} - i_{2nd} \quad (4)$$

Based on Equation (4), the average value of the DC input current is I_{dc} , which reaches its maximum when the minimum current i_{2nd} is 0. Conversely, the current i_{dc} reaches its peak value when i_{2nd} reaches its minimum value, and it is defined as follows. For non-unity power factor loads, the instantaneous power expression becomes more complex, but the DC-side current still contains a dominant second-harmonic component, and the design requirement for ripple suppression remains unchanged.

$$I_{max} = \frac{U_o I_o}{u_{dc}} = 2I_{dc} \quad (5)$$

Combining Equations (4) and (5), the DC input current oscillates at a frequency of $2\omega_o$, with a peak-to-peak value of I_{max} . Under ideal conditions, the UPS output voltage U_o and bus voltage U_{dc} are stable. Therefore, as the inverter output current I_o increases, the ripple amplitude of the DC input current also increases.

According to the latest standard, DL/T 1074-2019: Integrated DC and AC Uninterruptible Power Supply for Power Applications [23], the DC input of a UPS must meet two core criteria: the inrush current ratio and the back-feed ripple voltage coefficient. The inrush current ratio is defined as the maximum transient power during cold start, with the ratio of the maximum inrush current to the steady-state current not exceeding 150% under the rated DC input voltage, rated output voltage, and rated load conditions. The back-feed ripple voltage coefficient refers to the ratio of the RMS value of ripple voltage to the average DC voltage, which should not exceed 0.5% when the UPS is operating under rated DC voltage and load conditions.

In this work, the inrush current ratio is measured as

$$I_{ratio} = \frac{I_{max}}{I_{dc}} \quad (6)$$

where I_{max} is the maximum DC input current observed during the cold-start transient, and I_{dc} is the average DC input current after the UPS reaches a steady state under rated conditions.

The back-feed ripple voltage coefficient is measured as

$$\delta_{RSM} = \frac{U_{RMS}}{U_{dc}} \times 100\% \quad (7)$$

where U_{RMS} represents the effective value of ripple voltage, while U_{dc} denotes the average value of DC voltage.

$$\frac{I_{max}}{I_{dc}} = 2 > 1.5 \quad (8)$$

From Equation (8), it can be concluded that neither battery nor switching power supplies directly connected to the bus can meet the required standards. When the DC input is powered by a battery, the absence of voltage regulation causes both the battery voltage and current to fluctuate during inverter operation, resulting in a back-feed ripple voltage coefficient that fails to meet the standard requirements. Hence, the suppression of the second harmonic is one of the necessary issues that need to be solved in UPS applications.

3. Control Technique Design and Configuration

To address the issue of second-harmonic ripples in the direct bus connection approach, a boost circuit is added between the DC input and the bus [15]. This configuration transfers the second-harmonic ripple of the DC input to the bus capacitor side, ensuring that the DC input current remains stable and free from ripples. Furthermore, to avoid increasing system complexity and reducing costs, the DC input and PFC module share the same boost circuit. A hybrid control strategy combining PFC and second-harmonic ripple suppression is employed. The system power topology is shown in Figure 2.

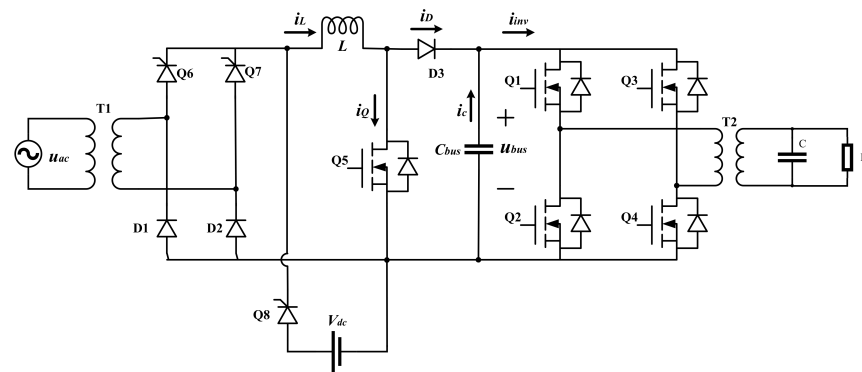


Figure 2. System configuration of the boost converter reuse-based Uninterruptible Power Supply.

When the AC input is normal, Q6 and Q7 are turned on, while Q8 is turned off, and the UPS operates in PFC rectification and inversion modes. When the AC input is abnormal, Q6 and Q7 are turned off, and Q8 is turned on, causing the UPS to operate in the DC boost inversion mode. Since Q6, Q7, and Q8 are all semi-controlled devices, the inverter's output energy is provided by the bus capacitor during mode switching.

3.1. DC Boost Inversion Mode

The input current of the inverter can be equal to a DC source and a second-harmonic current source according to Equation (4), when the UPS operates in the DC boost inversion mode. The system configuration under this condition is shown in Figure 3 [16]. The second-harmonic component of the inverter input current is caused by both the boost inductor and the bus capacitor. Based on Equation (3), the ripple of the output is defined as follows, with the ripple power distribution factors α and β , where $\alpha + \beta = 1$:

$$P_r = \frac{1}{2} U_o I_o \cos(2\omega_o t) = \alpha P_r + \beta P_r \quad (9)$$

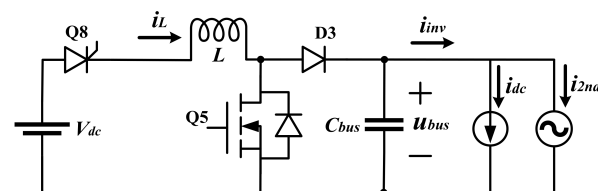


Figure 3. Equivalent circuit of the DC boost inverter.

Here, α represents the ripple power associated with the boost inductor, while β corresponds to the ripple power of the bus capacitor.

To enhance the energy conversion efficiency of the DC input source and meet the voltage requirements of the substation UPS, the inductor current i_L should maintain the stability of the DC side. This results in a reduction in the second-harmonic ripple power

component αP_r in the boost inductor and increases the second-harmonic ripple power component βP_r in the bus voltage. Ideally, the bus capacitor should absorb the entirety of the second-harmonic ripple power required by the inverter output.

According to the operating principle of the boost converter, when Q5 is on, the inductor L stores energy, with $i_L = i_Q$, $i_D = 0$. When Q5 is off, the DC source and the stored energy in L both supply power to the bus capacitor and load, with $i_L = i_D$ and $i_Q = 0$. Over a switching cycle, the average currents through diode D3 and switching transistor Q5 can be expressed as

$$\begin{cases} i_D = i_L(1 - d) \\ i_Q = i_L - i_D \end{cases} \quad (10)$$

where d is the duty ratio of the switching transistor, expressed as

$$d = 1 - \frac{V_{dc}}{u_{bus}} \quad (11)$$

The second-harmonic ripple in the DC bus voltage cannot be eliminated totally based on Equation (3). In addition, according to Equation (11), the duty cycle d also exhibits a second-harmonic component. Since the duty cycle d is positively correlated with the current i_Q , reducing the second-harmonic content in the input current i_L can be achieved by decreasing the second-harmonic ripple current in the diode current i_D . Similarly, controlling the ripple current i_D can be accomplished by regulating the duty cycle and the bus voltage level.

In the DC boost inverter mode of the UPS, the dual-loop control framework for second-harmonic ripple suppression is shown in Figure 4. The control strategy adopts a dual-loop scheme, where the inner loop is the second-harmonic current loop, and the outer loop is the bus voltage loop. In the diagram, $G_v(s)$ represents the voltage controller, which regulates the bus voltage to track the reference value. $G_i(s)$ is the current controller, where the reference value is the output of the voltage controller, and the feedback is the inductor current, ensuring that the inductor current remains a stable DC component. The output of the current loop serves as the modulation signal to drive the power switch Q5. Physically, the outer voltage loop regulates the average DC bus voltage to its reference. The inner current loop shapes the inductor current into a nearly constant DC quantity so that the second-harmonic power pulsation is mainly absorbed by the bus capacitor instead of the DC source.

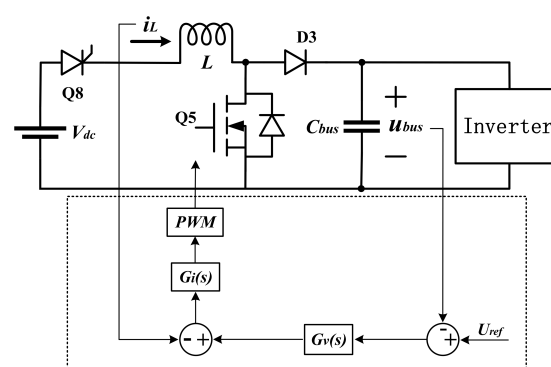


Figure 4. Double loop control diagram for second-harmonic ripple suppression.

From the viewpoint of small-signal dynamics, the boost converter in the DC-side inversion mode can be described by the standard averaged model, where the inductor current and bus voltage are the main state variables, and the duty cycle is the control input. Based on this model, the controller is designed using a classical dual-loop approach. The

inner current loop is tuned first, with a relatively high bandwidth so that the inductor current can quickly follow its reference and reject low-frequency disturbances. Then, the outer voltage loop is tuned with a bandwidth roughly one order of magnitude lower than that of the current loop so that the bus voltage changes more slowly and the two loops do not interfere with each other. In practice, proportional integral (PI) controllers are used for both loops, and their gains are adjusted to achieve a sufficient phase margin and an acceptable settling time of the bus voltage under the tested operating conditions.

3.2. Power Factor Correction Control

For substation UPS, the key performance indicators for AC input are power factor (PF) and total harmonic distortion of current (THD). Therefore, the power factor correction (PFC) function must not only regulate the bus voltage to a specified value but also ensure that the AC input current remains in phase with the AC input voltage. When the UPS operates in rectification-inversion mode, the dual-loop control framework for power factor correction is shown in Figure 5.

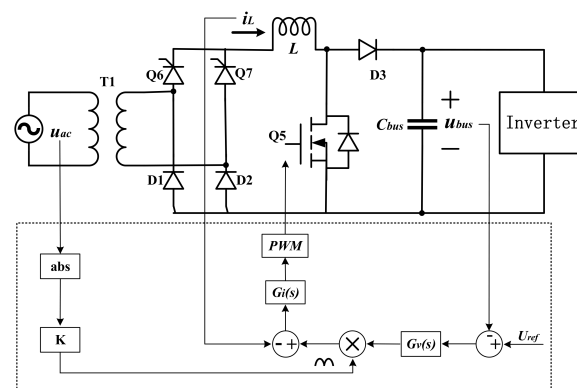


Figure 5. Double loop control structure diagram of the power factor correction circuit.

The digital PFC control principle is identical to that of analog control [18], adopting the same dual-loop strategy. The inner current loop regulates the AC half-wave current, while the outer voltage loop controls the bus voltage. In the diagram, $G_v(s)$ represents the voltage controller, which ensures that the bus voltage follows the reference value. $G_i(s)$ is the current controller, where the reference value is the product of the voltage controller's output and the AC half-wave input voltage. The feedback signal is the inductor current, which is controlled to remain in phase with the AC input voltage. The output of the current loop serves as the modulation signal to drive the power switch $Q5$. In this case, the outer voltage loop sets the required input power by regulating the bus voltage, while the inner current loop shapes the inductor current to follow the rectified AC voltage, thus achieving a high power factor.

3.3. Hybrid Control for the Boost Converter Reuse-Based Uninterruptible Power Supply

Both the double-line frequency ripple suppression control and power factor correction (PFC) control adopt a dual-loop control strategy, with the outer voltage loop regulating the bus voltage and the inner inductor current loop serving different physical control objectives. However, since both modes involve inductor current regulation, they can share the same control loop. In both modes, the outer loop keeps regulating the bus voltage, whereas the inner current loop either suppresses the second-harmonic ripple by maintaining a nearly constant inductor current (DC boost inversion mode) or performs power factor correction by shaping a sinusoidal current (PFC rectification mode). The UPS operating mode can be switched based on the detected power quality of the AC input. The dual-loop hybrid

control framework is illustrated in Figure 6. Since Q8 is a semi-controlled device, ensuring reliable turn-off requires that the peak value of the rectified AC input voltage u_{rec} is greater than the DC bus voltage V_{dc} . When the AC input returns to normal operations, a soft-start signal is sent to turn on Q6 and Q7. After completing the soft start, these switches remain continuously on, forming an uncontrolled rectifier circuit together with D1 and D2. When the condition $u_{rec} > V_{dc}$ is met, a turn-off signal is sent to Q8, and the control loop switches to PFC operation. Conversely, when an AC input anomaly occurs, a turn-off signal is sent to Q6 and Q7. At most, after half of a power frequency cycle, the AC input is fully disconnected, triggering Q8 to turn on, and the control loop transitions into the boost-mode double-line frequency ripple suppression state.

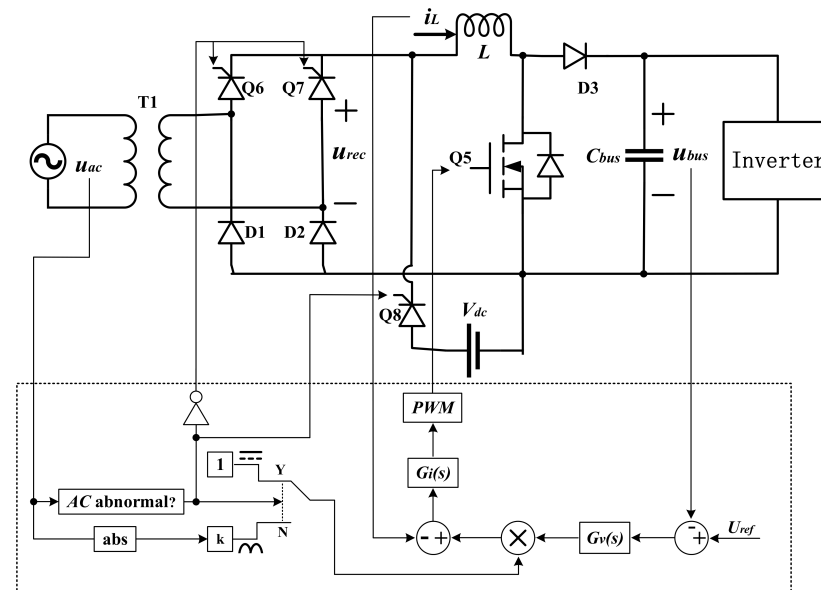


Figure 6. Hybrid control diagram of PFC and secondary ripple suppression.

4. Simulation Comparison and Verification

To verify the effectiveness of the proposed method, a comprehensive simulation model was developed. The system parameters match the experimental prototype, featuring an AC input of 190 Vac, a DC input of 220 Vdc, a 550 μ H inductor, and a 3540 μ F bus capacitor, operating at a switching frequency of 20 kHz.

4.1. Steady-State Performance Comparison

The steady-state performance of the proposed DC-DC converter-reuse method (Model 3) was compared against traditional direct-bus connection (Model 1) and series-inductor topologies (Model 2).

As illustrated in Figure 7, when the battery is directly connected to the bus voltage or connected via a series inductor, the bus voltage aligns closely with the battery voltage. Consequently, the second-harmonic ripple from the instantaneous inverter output power is significantly reflected on the DC side. Fast Fourier Transform (FFT) analysis reveals that the direct connection configuration suffers from a massive DC ripple, with the total harmonic distortion (THD) reaching 101.98%. While the series-inductor method provides limited mitigation, reducing the current ripple THD to 24.15%, it remains insufficient for strict substation standards and causes larger bus voltage drops. Conversely, the proposed boost topology actively boosts the bus voltage to 250 Vdc. By isolating the DC input from the pulsating bus power, the proposed method effectively suppresses the double-line frequency ripple, smoothing the DC input current to an approximate pure DC quantity. Under the

proposed control, the DC input current THD drops dramatically to merely 1.45%, and the DC voltage ripple is suppressed to 0.06%, providing ample margin for the DL/T 1074-2019 standards. These quantitative results confirm that the proposed method reduces the DC input current THD from 101.98% (direct connection) and 24.15% (series inductor) down to 1.45% while keeping the DC voltage ripple at only 0.06%.

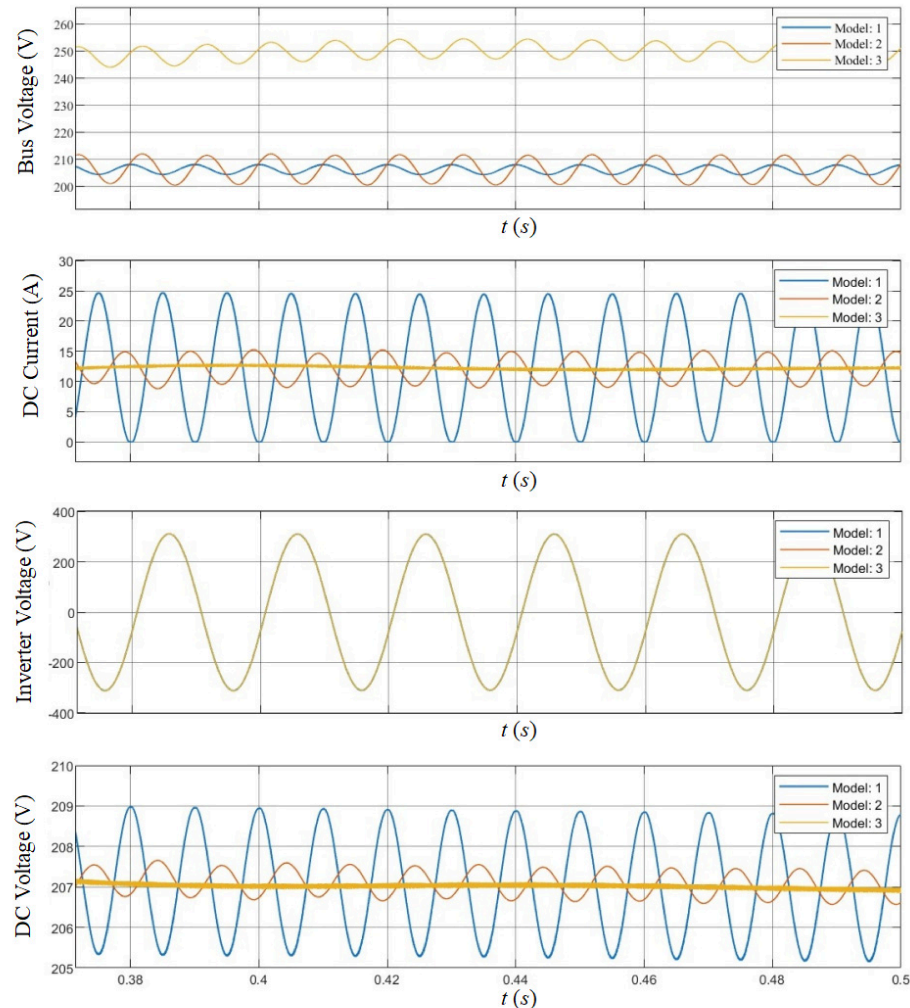


Figure 7. Steady-state waveforms of the three different DC input connection topologies. The corresponding THD of the DC input current is 101.98%, 24.15%, and 1.45% for Model 1, Model 2, and Model 3, respectively.

4.2. Dynamic Response During Mode Transitions

A critical requirement of the proposed topology is the smooth transition between the power factor correction (PFC) mode and the DC-side inversion mode during grid faults.

Figure 8 demonstrates the system's dynamic tracking capability. Initially operating in PFC mode, the bus voltage is tightly regulated at 300 Vdc. When an AC input failure occurs at 0.4 s, the system swiftly switches to the double-line frequency ripple suppression mode. The bus voltage reference steps down to 250 Vdc, and the controller tracks this transition with minimal overshoot. During this period, the DC input current dynamically ramps up from 0 A to carry the load, maintaining an exceptionally low ripple profile. Upon the restoration of the AC grid at 0.8 s, the system seamlessly reverts to PFC operation, ramping the bus voltage back to 300 Vdc while the DC smoothly returns to zero.

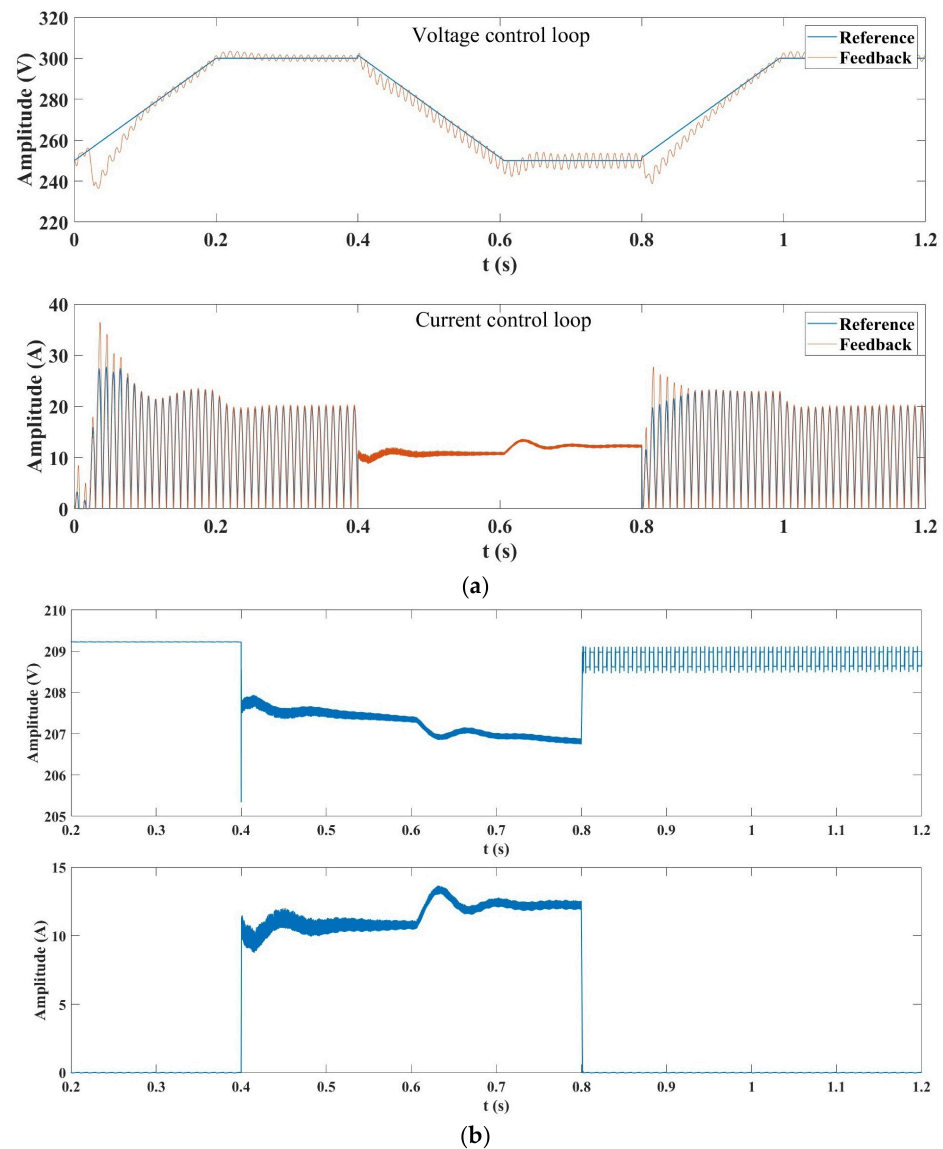


Figure 8. Dynamic responses during the transition between PFC and DC-side inversion modes. (a) Dynamic tracking waveforms of the control loops. (b) Transient responses of the DC input voltage and current.

4.3. Transient Performance Under Load Variations

To further validate the robustness of the dual-loop control strategy, load step variations were simulated under the double-frequency suppression mode.

As depicted in Figure 9, the system initially operates under a no-load condition. Step loads of 1 kW are abruptly applied at 0.6 s and 0.8 s, respectively. The sudden increase in power demand causes a momentary dip in the bus voltage and a corresponding surge in the inductor current. However, the control loops exhibit rapid dynamic response, achieving a new steady state within approximately 0.1 s for each transient event. Even under full-load conditions, the controller successfully confines the ripple components, demonstrating excellent stability and dynamic stiffness. The settling time of the bus voltage after each 1 kW load step is approximately 0.1 s, and the DC input current ripple remains very small, indicating the good dynamic stiffness of the proposed control.

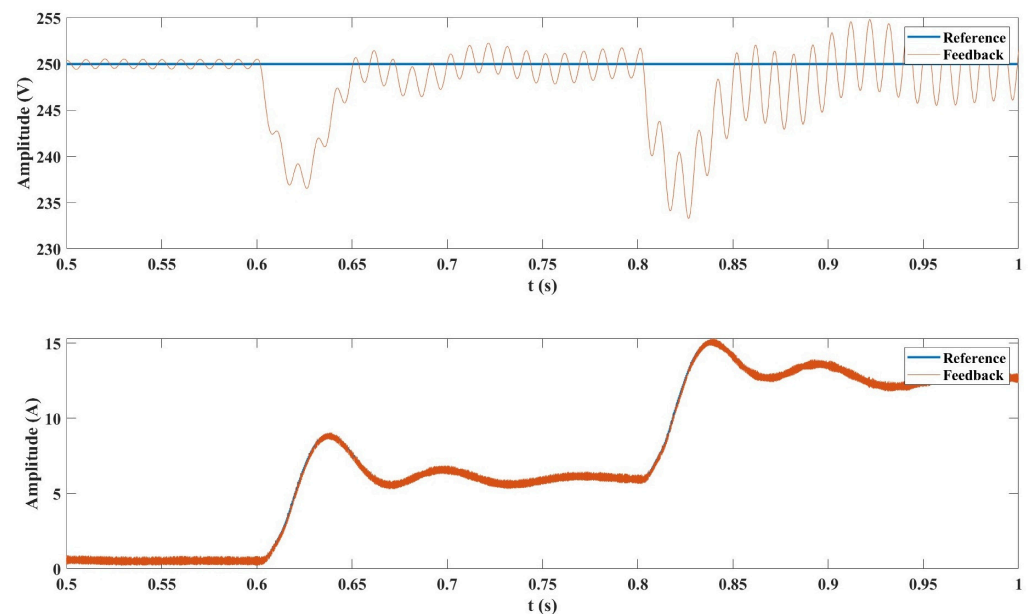


Figure 9. Voltage and current control loop dynamic waveforms under step load changes in boost mode.

5. Experimental Verification

To verify the accuracy and effectiveness of the proposed double-line frequency ripple suppression method in substation UPS applications, a 3 kVA power UPS prototype was developed. The system adopts a dual-DSP control scheme using DSP F28035 chips, with one DSP controlling the rectifier stage and the other managing the inverter stage. The DSPs of the rectifier and inverter operate at switching and control sampling frequencies of 20 kHz and 10 kHz, respectively. The on-chip 12-bit ADC is used to sample the DC input voltage and current, DC bus voltage, AC input voltage, and inductor current. The control algorithm is executed within one switching cycle, so the total sampling and calculation delay is less than one control period, which has been taken into account in the controller design. The AC input isolation transformer has a turns ratio of 220:190, and the rated DC input voltage is 220 Vdc. The overall system's structure is illustrated in Figure 10. All experiments were conducted at room temperature under steady-state conditions. The voltages and currents were measured using a digital oscilloscope with isolated voltage probes and Hall-effect current sensors at the DC input, DC bus, and inverter output. The efficiency was obtained from the ratio of measured output power to the sum of DC input power and AC input power depending on the operating mode.

In Figure 10b, the PFC module integrates both power factor correction and second-harmonic ripple suppression functions. To demonstrate the advantages of the proposed scheme, four 1.5 mH inductors (as a comparative experiment of DC input series inductors, totaling approximately 6 mH) are incorporated, as shown in Figure 10b. In the experiments, the inverter outputs a 220 V/50 Hz voltage and supplies a rated load of 2.4 kW/3 kVA with a power factor of 0.8. The tests were conducted in three configurations: direct connection of the DC input to the bus, connection via a series inductor, and connection via a boost circuit. The PFC power circuit and control parameters are presented in Table 1.

To ensure proper operation of the PFC under rated conditions, the bus voltage is set at 300 V, which not only helps the inverter meet the RCD requirements under load but also provides sufficient time for reliable detection during AC input loss, thereby maintaining continuous load power. Furthermore, in the DC input inversion mode, maintaining a low duty cycle is advantageous for suppressing ripple currents and ensuring efficiency.

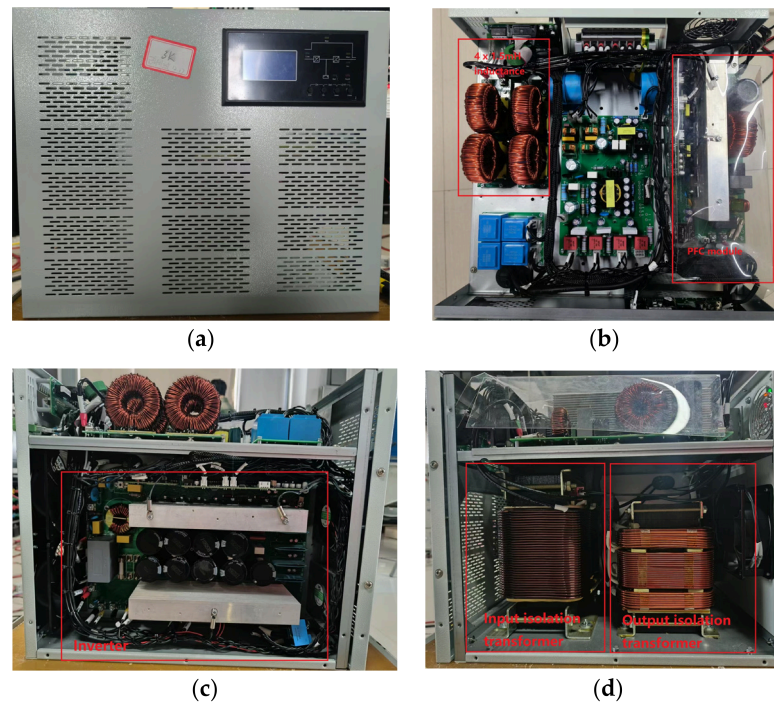


Figure 10. Prototype of a 3 kVA power UPS system. (a) The machine's casing, (b) the PFC and boost converter, (c) the inverter, and (d) the isolation transformers.

Table 1. Parameters of the PFC module system.

Parameters	Value
Rated AC input voltage (V)	220
Rated DC input voltage(V)	220
Inductance L (uH)	550
Bus capacitance (uF)	3540
Bus voltage of AC-DC (V)	300
Bus voltage of DC-DC (V)	250
Switching frequency (kHz)	20

5.1. DC Input Bus Connection Experiment

When the DC input is directly connected to the bus, the second-harmonic component of the inverter's instantaneous output power is directly transferred to the DC input side, as shown in the experimental waveforms in Figure 11.

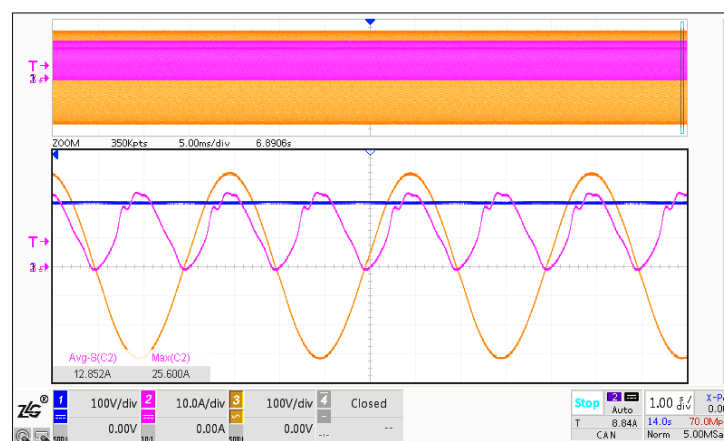


Figure 11. Input voltage and current of the DC bus.

In these waveforms, Channel 1 represents the bus voltage, Channel 2 shows the DC input current, and Channel 3 displays the inverter voltage. The ripple frequency of the DC input current is twice that of the inverter voltage, with a peak current of 25.6 A and an average current of 12.85 A, resulting in a ratio of 1.99, which aligns with Equation (8). This indicates that the direct bus connection scheme cannot meet the inrush current requirements of the DC input for the substation UPS. Additionally, the effective (RMS) value of the DC input ripple voltage is 0.819 V, while the average voltage is 218.8 V, yielding a DC back-feed ripple coefficient of 0.374%, which satisfies the specification.

5.2. DC Input Experiment with Inductor

When a series inductor is connected between the DC input and the bus, the inductor limits rapid current changes, thereby reducing the second-harmonic ripple transferred from the inverter's instantaneous output power to the DC input side. The measurement results are given in Figure 12.

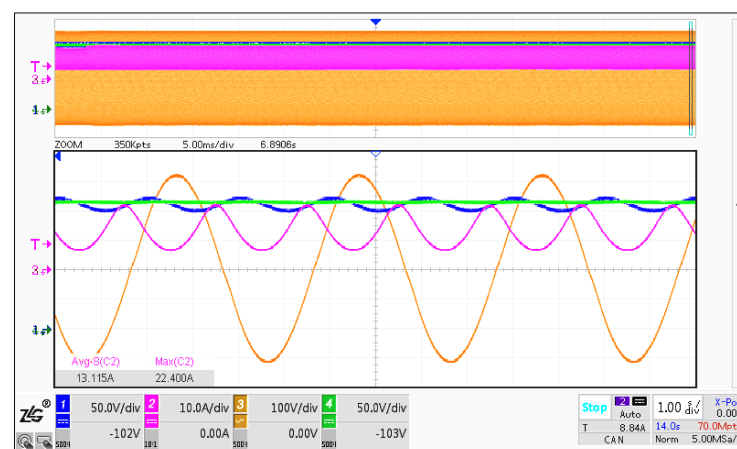


Figure 12. Input voltage and current of DC input with an inductor.

In the observed waveforms, Channel 1 represents the bus voltage, Channel 2 represents the DC input current, Channel 3 represents the inverter voltage, and Channel 4 represents the DC input voltage. Compared with the direct bus connection, the inductor suppresses current fluctuations so that the minimum current remains above zero. The maximum current is 22.4 A, and the average current is 13.115 A, yielding a ratio of 1.708. Although this value still does not satisfy the inrush current requirements for substation UPS, increasing the inductance could further meet the criteria, albeit at a higher cost. Additionally, the effective (RMS) value of the DC input ripple voltage is 0.521 V, with an average voltage of 218.7 V, resulting in a DC back-feed ripple coefficient of 0.238%, which is an improvement over the direct bus connection scheme.

5.3. Voltage Boost Experiment of DC Input

The closed-loop control generates a duty cycle component that counteracts the second-harmonic ripple, effectively suppressing the second-harmonic component in the DC input current when the DC input is connected to the bus via a boost converter. The experimental waveforms are shown in Figure 13, where Channel 1 represents the bus voltage, Channel 2 represents the DC input current, Channel 3 represents the inverter voltage, and Channel 4 represents the DC input voltage.

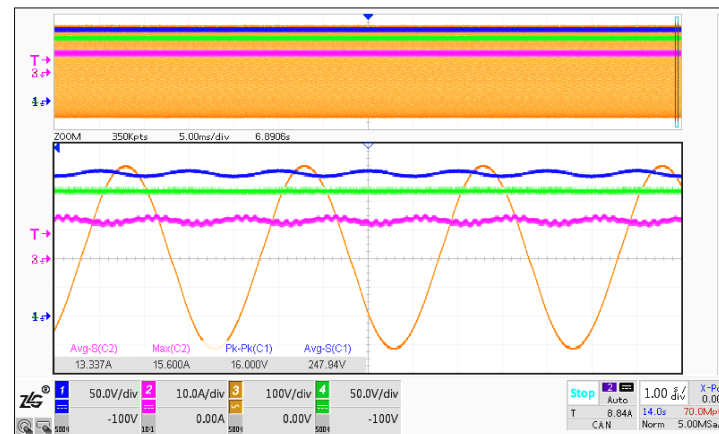


Figure 13. Input voltage and current of DC input under the voltage boost condition.

Compared to the previous two configurations, the inductor current is nearly flat, with a maximum current of 15.6 A and an average current of 13.337 A, resulting in a ratio of 1.1697. This demonstrates excellent suppression of the second-harmonic current, meeting the DC input inrush current requirements for substation UPS systems. Additionally, the RMS value of the DC input ripple voltage is 0.352 V, with an average voltage of 218.8 V, yielding a DC back-feed ripple coefficient of 0.16%, which provides ample margin. Detailed performance comparisons are listed in Table 2.

Table 2. Data comparison of different DC input modes.

Parameters/Experiment		Connect to Bus	With Inductor	Voltage Boost
Reverse ripple voltage	Voltage Ripple (V)	0.819	0.521	0.352
	DC voltage (V)	218.8	218.7	218.8
	Ripple proportion	0.374%	0.238%	0.16%
	Maximum current (A)	25.6	22.4	15.6
Inrush current ratio	Average current (A)	12.85	13.112	13.117
	Inrush ratio (%)	1.99	1.708	1.1697

As summarized in Table 2, the proposed boost connection reduces the DC input inrush current ratio from 1.99 (direct connection) and 1.708 (with inductor) to 1.1697, and it lowers the back-feed ripple coefficient from 0.374% and 0.238% to 0.16%.

Since the boost converter is shared with the PFC circuit, it is crucial to minimize the delay during switching between the DC-side inversion and rectifier-inverter modes to ensure uninterrupted inverter output. Figure 14 shows the waveform for switching from rectifier-inverter mode to DC-side inversion mode, where Channel 1 is the bus voltage, Channel 2 is the DC input current, Channel 3 is the inverter voltage, and Channel 4 is the AC input current. In this transition, the bus voltage is maintained at 300 Vdc during the rectifier-inverter mode; when the AC input is lost, the bus voltage drops to 250 Vdc. During this period—lasting approximately 1.5 AC cycles—the bus capacitor supplies the output energy until the DC-side inverter loads and reaches a steady state, with the inverter voltage remaining stable throughout the process.

Figure 15 shows the waveform for switching from DC-side inversion back to the rectifier-inverter mode. Here, Channel 1 is the bus voltage, Channel 2 is the DC input current, Channel 3 is the inverter voltage, and Channel 4 is the AC input current. Initially, the DC-side inverter operates at a steady state. Once the AC input is restored, a soft-start signal is sent to Q6 and Q7, causing the DC input current to decrease gradually. Combined with AC rectification, this transition allows the inverter to be powered appropriately. After the rectifier soft-start is completed and the bus voltage is boosted back to 300 Vdc, the DC-

side thyristor Q8 is turned off, and the system re-enters rectifier-inverter mode. Throughout the switching process, the inverter voltage remains regulated.

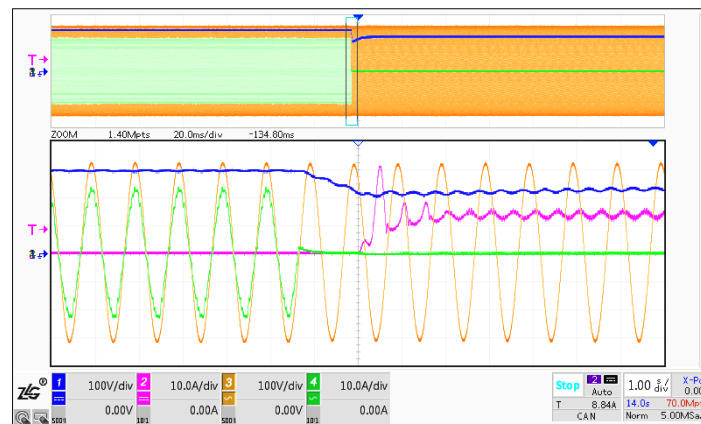


Figure 14. Switching process from rectifier-inverter modes to DC-side inversion.

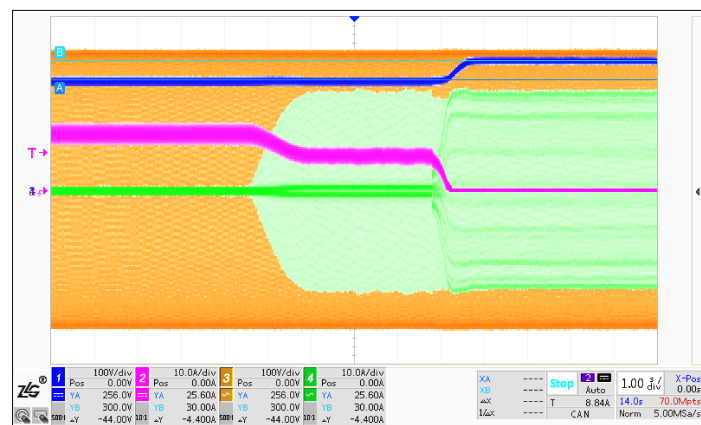


Figure 15. Switching process from DC-side inversion to rectifier-inverter modes.

If the bus voltage remains consistent between the rectifier-inverter and DC-side inverter modes, the design of the isolation transformer for the inverter output is simplified. When the boost converter operates in second-harmonic ripple suppression mode, increasing the average bus voltage reduces the bus voltage ripple coefficient. However, a larger duty cycle may introduce disturbances that increase the DC input ripple coefficient. Table 3 presents the performance data for various bus voltage levels. Although the bus voltage affects the DC input parameters, all values listed meet the requirements for substation UPS systems. Moreover, since the boost power switch employs hard switching, higher bus voltages result in greater losses—yielding an efficiency of 83.0% at 250 Vdc compared to only 81.8% at 300 Vdc. This efficiency reduction at higher bus voltage is mainly attributed to increased conduction and switching losses in the boost switch and diodes, as well as higher core and copper losses in the magnetic components.

Since the proposed method intentionally allows the double-line frequency ripple power to be absorbed by the DC-link capacitor, the low-frequency voltage ripple coefficient of the bus is in the range of 5.37–6.45% (Table 3). The corresponding ripple current is within the rated capability of the selected capacitor, leading to only moderate thermal stress and negligible impacts on inverter performance and capacitor lifetime when proper derating is applied.

Table 3. System performance with different DC input connection schemes.

Parameters/Bus Voltage		250 Vdc	270 Vdc	300 Vdc
Reverse ripple voltage	Voltage ripple (V)	0.352	0.502	0.72
	DC voltage (V)	218.8	218.8	218.8
	Ripple proportion (%)	0.16	0.229	0.329
	Maximum current (A)	15.6	16	16
Inrush current ratio	Average current (A)	13.337	13.369	13.434
	Inrush ratio (%)	1.1697	1.1967	1.1910
	Peak-to-peak (V)	16	16	16
Bus voltage ripple	Average value (V)	247.94	268.13	297.77
	Coefficient (%)	6.45	5.967	5.373
Efficiency (%)		83.0	82.6	81.8

6. Conclusions

This paper proposes a DC-DC converter reuse-based method for suppressing second-harmonic ripples in the DC input by leveraging a power factor correction (PFC) topology. This approach reused a boost converter in both PFC and second-harmonic ripple suppression, thereby reducing hardware costs and increasing power density. Furthermore, a shared controller for both the PFC and second-harmonic ripple suppression is employed, which maintains the input requirement of substation uninterrupted power supply (UPS) systems with reduced computing costs for the processor. The experimental results verify that the proposed method reduces the DC input inrush current ratio from 1.99 (direct connection) and 1.708 (with series inductor) to 1.1697, and it decreases the back-feed ripple coefficient from 0.374% and 0.238% to 0.16% while keeping the DC input current THD around 1.45%. The effectiveness and performance of the proposed method are validated via a 3 kVA power UPS platform, which can be a reliable component for smart cities construction. Future work will focus on further improving the efficiency of the shared boost stage by adopting soft-switching techniques and extending the proposed approach to higher power levels and other types of DC sources.

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