

Article

Performance Assessment of All-Optical NAND and XNOR Gates at 120 Gb/s Using a Single Optically Pumped Semiconductor Optical Amplifier Mach–Zehnder Interferometer

Amer Kotb ^{1,2,*} and Kyriakos E. Zoiros ³

¹ School of Chips, XJTLU Entrepreneur College (Taicang), Xi'an Jiaotong-Liverpool University, Taicang 215400, China

² Department of Physics, Faculty of Science, Fayoum University, Fayoum 63514, Egypt

³ Lightwave Communications Research Group, Department of Electrical and Computer Engineering, School of Engineering, Democritus University of Thrace, 67100 Xanthi, Greece; kzoiros@ee.duth.gr

* Correspondence: amer.kotb@xjtlu.edu.cn or amerkotb@fayoum.edu.eg

Abstract

This paper presents a numerical investigation of all-optical NAND and XNOR logic gates implemented with a single optically pumped semiconductor optical amplifier integrated into a Mach–Zehnder interferometer (OP-SOA-MZI) at 120 Gb/s. Conventional approaches require two cascaded MZI stages to obtain both logic functions. The present work demonstrates that a single OP-SOA-MZI suffices for both gates under appropriate operating conditions. The quality factor (QF) serves as the primary performance metric. The NAND gate yields a QF of 28.6, while the XNOR gate yields a QF of 18.7. A comparison with the conventional electrically pumped SOA–MZI (EP-SOA–MZI) configuration shows that the OP-SOA–MZI architecture consistently produces higher QF values and exhibits superior tolerance to noise and high-speed operation. This improvement stems from enhanced carrier replenishment and improved phase stability provided by optical pumping. The study further examines the dependence of the QF on five operational parameters: absorption coefficient, pump power, data rate, phase noise, and amplified spontaneous emission noise. The results quantify the parametric sensitivity of each logic gate and establish operating regimes for reliable high-speed performance.

Keywords: NAND logic gate; XNOR logic gate; optically pumped semiconductor optical amplifier; Mach–Zehnder interferometer; quality factor

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1. Introduction

The continued scaling of electronic data processing faces fundamental constraints in bandwidth, power dissipation, and interconnect density [1,2]. Although optical communication systems provide high transmission capacity [3], signal processing at network nodes still relies heavily on optical-to-electrical-to-optical (OEO) conversion, which introduces latency, consumes power, and limits throughput [4]. All-optical logic gates eliminate this bottleneck by processing signals directly in the photonic domain [5,6]. Among all-optical logic functions, the NAND gate holds a special position because any Boolean circuit can be constructed from NAND gates alone. In contrast, the XNOR gate, which

performs logical equivalence, serves essential roles in encryption, error detection, and pattern matching [7,8]. The advantages of all-optical implementation include the absence of electronic conversion delays, compatibility with wavelength-division multiplexing (WDM), and the potential for operation at line rates exceeding 100 Gb/s [9,10].

Early work on all-optical logic relied on electrically pumped semiconductor optical amplifiers (EP-SOAs). However, EP-SOAs exhibit fundamental speed limitations at bit rates approaching 120 Gb/s due to the finite carrier lifetime, typically hundreds of picoseconds, which governs both gain and refractive index recovery [5,6]. This slow recovery produces pattern effects and intersymbol interference (ISI) that degrade the quality factor substantially [11,12]. To overcome these limitations, several alternative approaches have been proposed. Quantum-dot SOAs (QD-SOAs) offer faster gain recovery due to their discrete density of states [11,12], but they present fabrication challenges and residual polarization sensitivity [13,14]. Reflective semiconductor optical amplifiers (RSOAs) provide a compact double-pass configuration that increases the effective gain without increasing the device footprint [15,16] and have been successfully employed at 120 Gb/s [17,18], yet they still inherit the carrier lifetime limitations of conventional SOAs. Photonic crystal SOAs (PhC-SOAs) exploit slow-light effects to enhance light-matter interactions [19,20] and have demonstrated all-optical logic at 160 Gb/s [21,22], but they suffer from high coupling losses and tight fabrication tolerances. Carrier reservoir SOAs (CR-SOAs) introduce a separate carrier reservoir that supplies the active region, enabling faster gain recovery [23,24] and have been used to realize NAND and XNOR functions at 120 Gb/s [25,26]. Two-photon absorption (TPA) offers a fundamentally different nonlinear mechanism where the absorption rate depends on the square of the optical intensity, providing a strong nonlinear response at high peak powers [27,28]; TPA-based gates can operate at data rates up to 2 Tb/s [29,30] and have been successfully employed in NAND, NOR, and XNOR gates [27,31], but they require high peak input powers that may not be compatible with low-power integration. Alternative approaches based on four-wave mixing (FWM) [32,33] or cross-gain modulation (XGM) [34,35] in conventional SOAs suffer from low conversion efficiency or restricted logic functionality [36,37].

The optically pumped semiconductor optical amplifier (OP-SOA) offers a different approach to high-speed operation. In an OP-SOA, a separate high-power optical beam creates the population inversion, decoupling the gain dynamics from the electrical injection circuit. This architecture provides several specific benefits when integrated into a Mach-Zehnder interferometer (MZI) [38,39]. The MZI converts phase modulation induced by cross-phase modulation (XPM) in the SOA into intensity modulation at the output [40,41]. The combination of an OP-SOA and an MZI yields four advantages. First, the gain dynamics are determined by pump-probe interactions and can be engineered for sub-picosecond recovery [42,43]. Second, the interferometric configuration provides high sensitivity to phase shifts [44,45]. Third, the pump and probe wavelengths can be selected independently, allowing flexible integration with WDM systems [46]. Fourth, optical pumping reduces the amplified spontaneous emission (ASE) noise figure compared to high-current electrical pumping [47,48]. Conventional implementations of both NAND and XNOR functions using SOA-MZI structures require two cascaded interferometers: the first MZI generates an intermediate function such as AND or XOR, and the second MZI, configured as a logical inverter, produces the final output [49,50]. This cascading doubles the component count, increases optical insertion loss, and complicates photonic integration [38,39]. Several studies have investigated compact all-optical logic gates using various SOA configurations. Kim et al. demonstrated multiple logic functions using parallel SOA-MZI structures [40]. Sun et al. demonstrated an 80 Gb/s XOR gate using an SOA-MZI with a differential scheme [51]. Kotb et al. extended this approach to 320 Gb/s using an SOA-MZI with a delayed interferometer [26]. Kotb et al. demonstrated NAND and

XNOR functions using carrier-reservoir SOAs [25]. XNOR gates have also been demonstrated using TPA [31] and QD-SOA-MZI configurations [52].

Beyond SOA-based logic, photonic integrated circuits employing silicon micro-ring resonators have recently demonstrated correlated photon-pair generation through reverse-biased free-carrier depletion [53]. Carrier-induced optical bistability in silicon micro-ring resonators under continuous-wave pumping has also been investigated [54]. These advances underscore the growing potential of compact, CMOS-compatible platforms for all-optical signal processing. However, phase noise remains a critical concern in interferometric configurations. Moslehi established the theoretical framework for noise power spectra in optical two-beam interferometers induced by laser phase noise [55], and recent work has examined phase-preserving performance in cascaded MZI regeneration chips [56]. These considerations are directly relevant to the OP-SOA-MZI architecture, where phase stability determines the achievable quality factor.

Experimental demonstrations of all-optical logic gates using SOA-based platforms have progressed steadily. Son et al. realized XOR, NOR, and NAND gates in a single format using conventional SOAs [57]. Kotb et al. proposed a high-speed and cost-efficient NAND logic gate using a single SOA with a delay interferometer (SOA-DI) [58]. Dimitriadou and Zoiros investigated the feasibility of an ultrafast all-optical NAND gate using a single QD-SOA-MZI [52]. Kotb, Zoiros, and Guo demonstrated a 160 Gb/s PhC-SOA-based all-optical NAND gate [59] and a 120 Gb/s NAND gate using reflective SOAs [60]. The same authors also reported all-optical multifunctional AND, NOR, and XNOR logic gates using SOAs [61]. Kang et al. achieved all-optical XOR and XNOR operations at 86.4 Gb/s using a pair of SOA-MZIs [62]. Kotb modeled a high-quality-factor XNOR gate using QD-SOAs at 1 Tb/s [63]. Subsequently, Kotb and Guo presented numerical modeling of PhC-SOA-based 160 Gb/s NOR and XNOR gates [64] as well as RSOA-based NOR and XNOR gates at 120 Gb/s [65]. Additionally, Kotb demonstrated a NOR gate using TPA in an SOA-MZI configuration [66], while Agarwal et al. designed a 2×1 multiplexer using CR-SOAs for implementing basic logic gates at 120 Gb/s [67].

Recently, we have simulated all-optical XOR and AND logic gates using OP-SOA-MZI [68]. That simulation work confirmed that optical pumping effectively decouples gain recovery from electrical carrier injection, enabling high-contrast interferometric switching at data rates exceeding 100 Gb/s with reduced pattern effects. However, XOR and AND functions alone do not form a functionally complete set for arbitrary Boolean logic. By contrast, the NAND gate is functionally complete, meaning any digital circuit can be constructed solely from NAND gates, while the XNOR gate is essential for equality detection, encryption, and error correction. Therefore, extending the OP-SOA-MZI platform to realize NAND and XNOR operations is a necessary step toward a complete all-optical logic library. The present work undertakes this extension through simulation, as the parameter space for optimal NAND and XNOR performance, including pump power, interferometer bias, and noise suppression, has not been systematically characterized for OP-SOA-MZI configurations. Furthermore, the quality factor (QF) dependence on key parameters—absorption coefficient, pump power, data rate, phase noise, and ASE noise—has not been previously reported for OP-SOA-MZI-based NAND and XNOR gates.

The present work addresses this gap. We simulate a single OP-SOA-MZI that directly realizes both NAND and XNOR logic gates at 120 Gb/s. The quality factor serves as the performance metric. We also quantify the sensitivity of the QF to five operational parameters: absorption coefficient, pump power, data rate, phase noise, and amplified spontaneous emission (ASE) noise. The remainder of this paper is organized as follows. Section 2 describes the simulation model for the OP-SOA-MZI, including the treatment of ASE and phase noise. Section 3 presents the results for the NAND and XNOR gates, including

the QF values and parametric dependencies. Section 4 discusses the implications of the findings. Section 5 concludes the paper.

2. Theoretical Framework for OP-SOA-MZI-Based NAND and XNOR Gates

2.1. Optical Pumping Principle in Semiconductor Optical Amplifiers

An optically pumped semiconductor optical amplifier (OP-SOA) achieves population inversion via an external optical beam, contrasting with conventional current-injected devices. Pump photons promote electrons from the valence band to the conduction band. Subsequent signal propagation through the active region stimulates emission. Optical pumping confers four benefits relative to electrically pumped SOAs (EP-SOAs): accelerated carrier supply, diminished thermal dissipation, removal of current-derived parasitic influences, and enhanced gain constancy under high-bit-rate conditions. EP-SOAs depend on injection current and thermal diffusion for carrier replenishment, a process that limits carrier lifetimes to hundreds of picoseconds. OP-SOAs shorten the effective recovery time to tens of picoseconds through continuous optical carrier injection. This accelerated recovery mitigates pattern-dependent distortions and sustains high-speed logic functionality. The NAND and XNOR gates examined in this work operate at 120 Gb/s, a rate at which rapid gain recovery becomes indispensable for preserving a high QF.

2.2. Coupled Rate Equation System for Gain Coefficients

Three interconnected differential equations describe the OP-SOA response. These equations govern the integrated gain coefficients representing carrier depletion (CD), carrier heating (CH), and spectral hole burning (SHB). The formulation captures slow interband processes alongside ultrafast intraband nonlinearities. Equation (1) governs the carrier depletion dynamics [68]:

$$\frac{dh_{CD}(t)}{dt} = \frac{\alpha_p L \lambda_p P_p}{E_{sat} \lambda_s} - \frac{h_{CD}(t)}{\tau_c} - (\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t)] - 1) \frac{P_{in}(t)}{E_{sat}} \quad (1)$$

The variable $h_{CD}(t)$ denotes the integrated gain arising from interband carrier transitions. The first term on the right-hand side quantifies carrier generation through optical pumping, where α_p represents the absorption coefficient, L is the amplifier length, λ_p and λ_s are the pump and signal wavelengths, P_p is the pump power, and E_{sat} is the saturation energy. The second term accounts for spontaneous recombination with characteristic time τ_c . The third term describes stimulated emission losses driven by the instantaneous input power P_{in} . Equation (2) expresses the carrier heating dynamics:

$$\frac{dh_{CH}(t)}{dt} = -\frac{h_{CH}(t)}{\tau_{CH}} - \frac{\varepsilon_{CH}}{\tau_{CH}} (\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t)] - 1) P_{in}(t) \quad (2)$$

Here, $h_{CH}(t)$ denotes gain suppression due to carrier heating (CH). The first term models thermal relaxation with time constant τ_{CH} . The second term captures nonlinear gain reduction due to CH, with ε_{CH} as the suppression coefficient. Equation (3) describes the spectral hole burning dynamics:

$$\frac{dh_{SHB}(t)}{dt} = -\frac{h_{SHB}(t)}{\tau_{SHB}} - \frac{\varepsilon_{SHB}}{\tau_{SHB}} (\exp[h_{CD}(t) + h_{CH}(t) + h_{SHB}(t)] - 1) P_{in}(t) - \frac{dh_{CD}(t)}{dt} - \frac{dh_{CH}(t)}{dt} \quad (3)$$

The variable $h_{SHB}(t)$ represents gain suppression from spectral hole burning (SHB). The first term describes carrier-carrier scattering with relaxation time τ_{SHB} . The second term quantifies nonlinear suppression from SHB, where ε_{SHB} denotes the corresponding

coefficient. The final two terms couple SHB evolution to CD and CH changes, preserving conservation of the total nonlinear response.

2.3. Resultant Gain and Phase Modulation

The total integrated gain $h_{total}(t)$ sums the three constituent contributions:

$$h_{total}(t) = h_{CD}(t) + h_{CH}(t) + h_{SHB}(t) \quad (4)$$

The probe signal experiences an instantaneous gain $G(t)$ given by:

$$G(t) = \exp[h_{total}(t)] \quad (5)$$

Phase modulation imposed on the probe arises from CD and CH. The SHB contribution to phase shifting is negligible, i.e., $\alpha_{SHB} \approx 0$. The aggregate phase shift $\Phi(t)$, therefore, takes the form:

$$\Phi(t) = -0.5 (\alpha h_{CD}(t) + \alpha_{CH} h_{CH}(t)) \quad (6)$$

The parameter α stands for the conventional linewidth enhancement factor (α -factor), while α_{CH} designates the linewidth enhancement factor specific to CH.

2.4. Optical Signal Representation and Interference Criteria for NAND and XNOR

Gaussian pulses arranged in a pseudorandom binary sequence (PRBS) constitute the input optical field applied to the OP-SOA. The input power waveform obeys:

$$P_{A,B}(t) \equiv P_{in,SOA}(t) = \sum_{n=1}^N a_{n(A,B)} \frac{2\sqrt{\ln[2]}E_0}{\sqrt{\pi}\tau_{FWHM}} \exp\left[-\frac{4\ln[2](t-NT)^2}{\tau_{FWHM}^2}\right] \quad (7)$$

In this expression, E_0 denotes the pulse energy, τ_{FWHM} the full width at half maximum, T is the bit period (8.33 ps for 120 Gb/s), N is the PRBS length, and $a_{n(A,B)}$ is the binary value (0 or 1) assigned to the n -th bit.

For the NAND gate configuration, the upper OP-SOA1 receives the logical combination NOTA ($\bar{A}$) and NOTB ($\bar{B}$). The lower OP-SOA receives no data signal. The CW probe power (P_{CW}) splits equally, with half directed to each active arm. Consequently, the input powers to the two OP-SOAs are:

$$P_{in,OP-SOA_1}(t) = P_{\bar{A}}(t) + P_{\bar{B}}(t) + 0.5P_{CW} \quad (8)$$

$$P_{in,OP-SOA_2}(t) = 0.5P_{CW} \quad (9)$$

The term $0.5P_{CW}$ represents half of the CW probe power that enters each OP-SOA. The upper OP-SOA thus experiences both the data-driven nonlinearity from the combined $\bar{A} + \bar{B}$ signal and the constant optical power from the CW probe. The lower OP-SOA experiences only the CW probe power without any data modulation. The resulting phase difference between the two arms produces the NAND logic function at the output.

For the XNOR gate configuration, the upper OP-SOA1 receives signal $\bar{A}$. The lower OP-SOA2 receives signal B. The P_{CW} probe again splits equally between the two arms. Therefore, the input powers are:

$$P_{in,OP-SOA_1}(t) = P_{\bar{A}}(t) + 0.5P_{CW} \quad (10)$$

$$P_{in,OP-SOA_2}(t) = P_B(t) + 0.5P_{CW} \quad (11)$$

Both OP-SOAs receive data modulation in this configuration. The upper arm responds to the complement of input $\bar{A}$, while the lower arm responds directly to input B.

The interference between the two phase-modulated CW probes yields the XNOR logic function.

The MZI output power depends on the interference between the CW probe fields emerging from OP-SOA1 and OP-SOA2. The output power formula reads:

$$P_{NAND/XNOR}(t) = 0.25 P_{CW} \left(G_{OP-SOA_1}(t) + G_{OP-SOA_2}(t) - 2 \sqrt{G_{OP-SOA_1}(t) G_{OP-SOA_2}(t)} \cos[\Phi_{OP-SOA_1}(t) - \Phi_{OP-SOA_2}(t)] \right) \quad (12)$$

In this expression, $G_{OP-SOA1}(t)$ and $G_{OP-SOA2}(t)$ denote the time-dependent gains of OP-SOA1 and OP-SOA2, respectively. $\Phi_{OP-SOA1}(t)$ and $\Phi_{OP-SOA2}(t)$ represent the corresponding phase shifts induced on the CW probe. The same expression applies to both NAND and XNOR gates; the distinction between the two logic functions resides solely in the input signals fed to OP-SOA1 and OP-SOA2.

2.5. Quality Factor as Performance Measure

The quality factor (QF) surpasses the extinction ratio as a performance metric because it incorporates both amplitude separation and noise statistics. The QF directly determines the bit error rate (BER) through the following definition [5]:

$$QF = \frac{P_1 - P_0}{\sigma_1 + \sigma_0} \quad (13)$$

In this equation, P_1 and P_0 represent the mean optical powers for logic “1” and logic “0” states, while σ_1 and σ_2 denote the corresponding noise standard deviations. The BER relates to the QF via the complementary error function (erfc):

$$BER = 0.5 \operatorname{erfc}\left[\frac{QF}{\sqrt{2}}\right] \quad (14)$$

Superior logic reliability accompanies higher QF values, which translate to lower BER. A QF of 6 corresponds to a BER near 10^{-9} , the standard requirement for most communication systems.

2.6. Numerical Solution Methodology

The Adams numerical integration method, implemented in Wolfram Mathematica®, solves Equations (1)–(14). This scheme delivers stable and precise time-domain solutions for the rapid nonlinear processes under investigation. Table 1 compiles all simulation parameters, including device geometry, carrier lifetimes, linewidth enhancement factors, saturation energy, and noise specifications. These values derive from validated literature on SOA-based optical logic devices [5,11,24,25,48,51–53].

Table 1. Simulation and device parameters with sources and justification [5,11,24,25,48,51–53].

Category	Symbol	Definition	Value	Unit	Source/Justification
Optical Input Parameters	E_0	Pulse energy	0.5	J	Typical for SOA-based logic simulations; corresponds to 10–20 dBm average power at 120 Gb/s [5,11]
	τ_{FWHM}	Pulse width	1	ps	Matches experimental pulse widths from mode-locked lasers at 120 Gb/s [51]
	T	Bit period	8.33	ps	Corresponds to 120 Gb/s data rate
	N	PRBS length	127	-	Standard PRBS length providing sufficient pattern randomness; experimentally validated [5,51]
Wavelength Parameters	λ_p	Pump wavelength	1532.6	nm	Matches absorption peak of InGaAsP/InP at 1550 nm band [48]
	λ_s	Probe wavelength	1544.2	nm	Chosen for wavelength-selective filtering; within SOA gain bandwidth [5]

Power Parameters	P_p	Pump power	50	mW	Optimized in this work; corresponds to practical laser diode output [47]
	P_{sat}	Saturation power	30	mW	Typical value for InGaAsP/InP SOAs [5,48]
Carrier Dynamics	τ_c	Carrier lifetime	100	ps	Measured for bulk InGaAsP/InP SOAs at room temperature [5,11,48]
Nonlinear Gain Parameters	α_p	Absorption coefficient	5000	m ⁻¹	Measured for InGaAsP/InP at 1532.6 nm; corresponds to absorption edge [48]
	α	Linewidth enhancement factor	5	-	Measured for bulk InGaAsP/InP SOAs at 1550 nm [5,11,48]
	α_{CH}	Linewidth enhancement (CH)	1	-	Measured for CH nonlinearity in InGaAsP/InP SOAs [5,11]
	α_{SHB}	Linewidth enhancement (SHB)	0	-	SHB has negligible phase contribution; experimentally verified [5,11]
	ϵ_{CH}	Nonlinear gain suppression (CH)	0.2	W ⁻¹	Fitted to experimental gain suppression measurements [11,48]
	ϵ_{SHB}	Nonlinear gain suppression (SHB)	0.2	W ⁻¹	Fitted to experimental gain suppression measurements [11,48]
	τ_{CH}	Temperature relaxation time	0.3	ps	Measured carrier heating time in InGaAsP/InP SOAs [5,11]
	τ_{SHB}	Carrier scattering time	0.1	ps	Measured carrier-carrier scattering time in InGaAsP/InP SOAs [5,11]
Device Geometry	L	SOA length	500	μm	Typical for commercially available SOAs; provides ~20 dB gain [5]
	d	SOA thickness	0.3	μm	Typical for single-mode InGaAsP/InP SOAs; ensures single transverse mode [5]
	w	SOA width	3	μm	Typical ridge width; ensures single lateral mode [5]
Optical Frequency	ω_0	Central optical frequency	193.55	THz	Corresponds to $\lambda_s = 1544.2$ nm
Noise Parameters	N_{sp}	Spontaneous emission factor	2	-	Minimum value for complete population inversion [5,48]
	B_0	Optical bandwidth	2	nm	Typical for optical bandpass filters used in SOA-based logic [5,51]

2.7. Significance of Simulation Parameters in Table 1

The parameters listed in Table 1 are organized into seven categories, each with specific implications for the performance of the OP-SOA-MZI logic gates.

- **Optical Input Parameters:** The pulse energy $E_0 = 0.5$ J, pulse width $\tau_{FWHM} = 1$ ps, and bit period $T = 8.33$ ps (corresponding to 120 Gb/s) together define the input data format. The choice of $\tau_{FWHM} = 1$ ps ensures that the pulses are shorter than the bit period, minimizing intersymbol interference. The PRBS length $N = 127$ provides a sufficient number of bit patterns to evaluate pattern-dependent effects, including carrier depletion memory and spectral hole burning recovery.
- **Wavelength Parameters:** The pump wavelength $\lambda_p = 1532.6$ nm and probe wavelength $\lambda_s = 1544.2$ nm are separated by 11.6 nm, which is sufficient for wavelength-selective filtering while remaining within the gain bandwidth of typical InGaAsP/InP SOAs. This wavelength separation ensures that the pump beam can be removed after the SOA without significantly affecting the probe signal.
- **Power Parameters:** The pump power $P_p = 50$ mW represents a practical optical pump power that can be generated by commercially available laser diodes. The saturation power $P_{sat} = 30$ mW is typical for InGaAsP/InP SOAs and determines the power level at which gain saturation becomes significant.

- **Carrier Dynamics Parameters:** The carrier lifetime $\tau_c = 100$ ps represents the interband recombination time in bulk SOAs. This parameter directly affects the speed of gain recovery; shorter τ_c values would enable higher-speed operation. The absorption coefficient $\alpha_p = 5000$ m⁻¹ is typical for InGaAsP/InP at the pump wavelength and determines the efficiency of optical pumping.
- **Nonlinear Gain Parameters:** The linewidth enhancement factor $\alpha = 5$ is typical for InGaAsP/InP SOAs and represents the coupling between carrier density changes and refractive index changes. This parameter determines the phase modulation amplitude per unit gain change. The CH and SHB parameters (α_{CH} , τ_{CH} , τ_{SHB} , ϵ_{CH} , ϵ_{SHB}) characterize the ultrafast intraband nonlinearities. $\tau_{CH} = 0.3$ ps and $\tau_{SHB} = 0.1$ ps are consistent with experimentally measured carrier heating and carrier–carrier scattering times, ensuring that the model captures sub-picosecond gain dynamics.
- **Device Geometry Parameters:** The SOA length $L = 500$ μ m, width $w = 3$ μ m, and thickness $d = 0.3$ μ m are chosen to provide sufficient gain-length product ($G \approx 10$ – 20 dB) while maintaining single-mode operation and compact dimensions suitable for photonic integration. These geometric parameters also influence the saturation energy $E_{sat} = h\nu w d / \Gamma a$, where Γ is the confinement factor and a is the differential gain.
- **Noise Parameters:** The spontaneous emission factor $N_{sp} = 2$ is the minimum value corresponding to complete population inversion, while $B_0 = 2$ nm is the optical bandwidth of the output filter. These parameters determine the ASE noise power P_{ASE} and thus influence the noise standard deviations σ_1 and σ_0 in the QF calculation.

2.8. Validation and Limitations of the Numerical Model

The numerical model used in this work is based on the well-established rate equation formulation for semiconductor optical amplifiers, which has been extensively validated through comparison with experimental results [5,11,48]. The model incorporates the key physical processes governing SOA dynamics, including carrier depletion, carrier heating, and spectral hole burning, and has been successfully applied to simulate various all-optical logic functions at data rates ranging from 10 Gb/s to 2 Tb/s.

2.8.1. Model Validation

The validation of the numerical model is based on several key aspects:

1. The simulation parameters listed in Table 1 are taken from experimentally measured values reported in the literature. For example, the carrier lifetime $\tau_c = 100$ ps, linewidth enhancement factor $\alpha = 5$, and intraband relaxation times $\tau_{CH} = 0.3$ ps and $\tau_{SHB} = 0.1$ ps have been measured in InGaAsP/InP SOAs and are consistent with values reported in multiple independent studies [5,11,48].
2. The model has been used to simulate all-optical logic gates at data rates that have been experimentally demonstrated. For example, the simulated QF values for EP-SOA-MZI-based XOR gates at 80 Gb/s ($QF = 10.13$) are consistent with experimental measurements reported in the literature [51].
3. The model conserves energy and charge, and the simulated gain and phase dynamics exhibit the expected physical behavior, including gain saturation, carrier recovery, and pattern-dependent effects.

2.8.2. Model Limitations

The numerical model has several limitations that should be considered when interpreting the results:

1. The model assumes ideal component behavior with no losses, ideal coupling, and perfect wavelength-selective filtering. In practice, components exhibit insertion loss, coupling losses, and finite extinction ratios that would degrade the QF .
2. The ASE noise is modeled as a constant power spectral density added to the signal. In practice, the ASE noise spectrum depends on the inversion level and gain spectrum, and the noise is not uniformly distributed.
3. The material parameters (α , α_{CH} , ϵ_{CH} , ϵ_{SHB}) are assumed to be constant. In practice, these parameters depend on carrier density, temperature, and wavelength, introducing additional nonlinearities.
4. The model does not include temperature-dependent effects such as thermal carrier redistribution, temperature-induced gain shift, or thermal lensing. At high pump powers and data rates, thermal effects can become significant.
5. The model assumes polarization-independent operation. In practice, SOAs exhibit some degree of polarization dependence, which would affect the interferometric switching contrast.
6. The model assumes ideal optical pumping with 100% absorption efficiency. In practice, only a fraction of the pump power is absorbed, and the absorption coefficient may vary along the amplifier length.

2.8.3. Impact of Limitations on Results

The limitations of the model are expected to affect the absolute QF values but not the qualitative trends. The simulated QF values represent the upper bound of achievable performance; experimental QF values are likely to be somewhat lower due to the practical limitations listed above. However, the relative performance trends (e.g., the dependence of QF on pump power, absorption coefficient, etc.) are expected to be qualitatively correct.

2.8.4. Model Validation Recommendations

To validate the model against experimental data, we recommend:

1. Direct measurement of the gain and phase dynamics of the OP-SOA using pump–probe.
2. Characterization of the ASE noise power spectrum under different pump and signal conditions.
3. Implementation of the NAND and XNOR gates using the proposed experimental setup and comparison of the measured QF with simulated values.
4. Fitting the model parameters to the experimental data to refine the model for future predictions.

3. Gate Configurations

The claim that a single OP-SOA-MZI avoids the need for cascaded MZI stages requires clarification. In conventional implementations of both NAND and XNOR functions using SOA-MZI structures, two cascaded interferometers are required: the first MZI generates an intermediate function such as AND or XOR, and the second MZI, configured as a logical inverter, produces the final output. This cascading doubles the component count, increases optical insertion loss, and complicates photonic integration.

The proposed single OP-SOA-MZI directly realizes the NAND and XNOR functions without requiring a second MZI stage for inversion. However, the complemented inputs $\bar{A}$ and $\bar{B}$ required for the NAND and XNOR operations are generated using external inverters (NOT gates), as discussed in Section Generation of Complemented Optical Inputs. These external inverters are separate components that are not part of the MZI architecture.

The key contribution is the elimination of the second MZI stage, which simplifies the interferometer design and reduces optical loss and bias control complexity. The external inverters are auxiliary components that would also be required for other logic implementations that rely on complemented inputs.

Therefore, the statement “a single OP-SOA-MZI suffices” is valid in the context of the interferometer architecture: the NAND and XNOR functions are realized within a single MZI without requiring an additional cascaded MZI stage. The external inverters are counted separately in the total system complexity analysis provided in Section Generation of Complemented Optical Inputs.

3.1. General Operating Principle of the OP-SOA-MZI Configuration

The Mach–Zehnder interferometer (MZI) forms the core of the proposed logic gates, converting phase modulation induced in the semiconductor optical amplifiers into intensity modulation at the output. The MZI consists of two parallel arms, each containing an optically pumped semiconductor optical amplifier (OP-SOA), an input wavelength-selective coupler (WSC), and an output coupler (OC). The continuous-wave (CW) probe signal at wavelength $\lambda_{CW} = 1544.2$ nm is split equally into the two arms by the input WSC. Each arm receives $0.5P_{CW}$, where P_{CW} is the input CW probe power.

The key operational principle relies on cross-phase modulation (XPM): when data pulses co-propagate with the CW probe through an OP-SOA, the data pulses deplete the carrier population via stimulated emission. This carrier depletion modulates the refractive index of the active region through the linewidth enhancement factor (α -factor), which in turn imposes a phase shift on the CW probe. The magnitude of the phase shift $\Delta\Phi(t)$ is proportional to the instantaneous carrier density change and is described by the equations for phase modulation established in Section 2.3 (Equation (6)), where the integrated gain changes due to carrier depletion ($h_{CD}(t)$) and carrier heating ($h_{CH}(t)$) determine the total phase shift. The spectral hole burning contribution to phase modulation is negligible ($\alpha_{SHB} \approx 0$). The optical pump at wavelength $\lambda_P = 1532.6$ nm continuously injects carriers into the active region, maintaining population inversion and enabling rapid gain recovery within the bit period.

At the output OC, the two phase-modulated CW probe fields interfere according to the interference condition established in Section 2.4 (Equation (12)), where the output power depends on the time-dependent gains $G_{OP-SOA1}(t)$ and $G_{OP-SOA2}(t)$, the corresponding phase shifts $\Phi_{OP-SOA1}(t)$ and $\Phi_{OP-SOA2}(t)$, and the fixed phase bias Φ_{bias} introduced in one arm. The cosine term in this interference expression determines whether constructive or destructive interference occurs at the output.

3.2. Component Functions and Signal Propagation

The wavelength-selective coupler (WSC) serves two critical functions: (1) it combines the data signals with the CW probe into each OP-SOA, and (2) it provides wavelength-selective coupling to ensure efficient power transfer. The WSC must exhibit low insertion loss (<1 dB) and high extinction ratio (>20 dB) to maintain signal integrity.

Each OP-SOA is a bulk or multi-quantum-well semiconductor amplifier with the parameters listed in Table 1. The active region length $L = 500$ μm , width $w = 3$ μm , and thickness $d = 0.3$ μm provide sufficient gain-length product while maintaining compact dimensions suitable for photonic integration. The optical pump power $P_p = 50$ mW couples into the OP-SOA through a separate pump port, creating population inversion independently of electrical injection. The carrier dynamics within each OP-SOA are governed by the coupled rate equation system presented in Section 2.2 (Equations (1)–(3)), which describes the interplay between carrier depletion, carrier heating, and spectral hole burning.

The phase bias Φ_{bias} is implemented either through a passive waveguide length difference between the two arms or through an active phase shifter. For the NAND gate, the fixed phase bias is set to produce destructive interference when no data pulses are present in the upper arm. For the XNOR gate, the phase bias is set to produce destructive interference when both arms experience identical phase shifts.

Generation of Complemented Optical Inputs

The NAND and XNOR operations described in this work rely on complemented optical inputs $\bar{A}$ and $\bar{B}$. These inverted signals can be generated in practice using several approaches:

1. In this approach, the input data signal at λ_s and a continuous-wave probe at λ_{probe} are injected into an SOA. The input data depletes the carrier population through stimulated emission, reducing the gain experienced by the CW probe. When the CW probe is filtered at the output, the inverted data signal is obtained. This approach has been experimentally demonstrated at data rates up to 40 Gb/s [38,57]. For operation at 120 Gb/s, the SOA must be operated at high bias current and with optical filtering to achieve sufficient extinction ratio.
2. A differential MZM provides two outputs: one carrying the data signal A and the other carrying the complementary signal $\bar{A}$. This approach simplifies the setup because the inverter is integrated into the modulator, and the two outputs are inherently synchronized. Differential MZMs with bandwidth >100 GHz are commercially available.
3. FWM in an SOA can generate the inverted signal through the phase conjugation process. This approach provides wavelength conversion in addition to inversion, but requires careful power and wavelength management [7,9].

The proposed OP-SOA-MZI approach replaces the two cascaded MZI stages required for conventional NAND and XNOR implementations with a single MZI. However, the external inverters (NOT gates) required for generating $\bar{A}$ and $\bar{B}$ must be counted in the total system complexity. For the NAND gate, two inverters are required (one for A and one for B). For the XNOR gate, one inverter is required (for A, since B is used directly). Therefore, the total component count is:

- NAND gate: 1 OP-SOA-MZI + 2 NOT gates (inverters) = 3 active components;
- XNOR gate: 1 OP-SOA-MZI + 1 NOT gate (inverter) = 2 active components.
- In comparison, conventional cascaded implementations require:
- NAND gate: 2 EP-SOA-MZI stages (first for AND, second for inversion) + 0 inverters = 2 active components (but with higher component count within each MZI);
- XNOR gate: 2 EP-SOA-MZI stages (first for XOR, second for inversion) + 0 inverters = 2 active components.
- Although the component count in terms of MZI stages is reduced from two to one, the required external inverters add to the system complexity. The key advantage of the proposed approach is not necessarily a reduction in component count, but rather:
- Each MZI stage introduces insertion loss (~3–5 dB). Reducing from two stages to one reduces the total optical loss.
- Cascaded MZI stages require precise timing between stages. The single MZI approach eliminates this inter-stage timing requirement.
- Each MZI stage requires independent phase bias control. Reducing from two stages to one simplifies the bias control electronics.
- When both the inverters and the MZI stages are counted, the total component count is similar, but the single MZI approach reduces optical loss and timing complexity. This trade-off should be considered in practical implementations.

3.3. NAND Gate Configuration

As shown in Figure 1, the NAND logic function is implemented using a two-arm MZI. Each arm contains one OP-SOA. The P_{CW} splits equally into the two interferometer arms, delivering half of the probe power to each OP-SOA. The upper OP-SOA1 receives the logical combination $\bar{A}$ and $\bar{B}$. This means that data pulses are present at the input of OP-SOA1 whenever either A is low, B is low, or both are low. The lower OP-SOA2 receives no data signal. The upper OP-SOA therefore experiences two simultaneous optical inputs: the data-driven pulses from the combined $\bar{A}$ and $\bar{B}$ signals and the constant P_{CW} . The lower OP-SOA experiences only P_{CW} without any data modulation.

The signal propagation path for the NAND gate follows this sequence:

1. Data signals A and B enter the NOT gates (external inverters) to generate $\bar{A}$ and $\bar{B}$.
2. The $\bar{A}$ and $\bar{B}$ signals are combined and coupled into the upper OP-SOA through WSC1 together with $0.5P_{CW}$.
3. The combined data pulses induce a phase shift $\Delta\Phi_1(t)$ on the CW probe in the upper arm, as described by the phase modulation equations in Section 2.3.
4. The lower OP-SOA receives only $0.5P_{CW}$, with no data modulation. Consequently, the gain $G_{OP-SOA2}(t)$ and phase $\Phi_{OP-SOA2}(t)$ remain constant.
5. The two CW probes recombine at the output OC, where the interference condition from Section 2.4 (Equation (12)) determines the output power based on the phase difference $\Delta\Phi_1(t) - \Phi_{bias}$.

The data pulses induce gain saturation and phase modulation on the probe passing through the upper arm. The lower arm remains at constant gain and phase because no data signal is present. The relative phase difference between the two arms determines whether constructive or destructive interference occurs at the output according to the interference expression in Section 2.4.

When both A and B are high, $\bar{A}$ and $\bar{B}$ are both low. No data pulse reaches OP-SOA1. Both arms therefore contain only the continuous-wave probe power. The fixed phase bias causes destructive interference, producing a low output. This corresponds to logic “0” for the NAND gate.

When A is low and B is high, $\bar{A}$ is high and $\bar{B}$ is low. A single data pulse reaches OP-SOA1. The upper arm therefore contains both the continuous-wave probe and one data pulse. The lower arm contains only the continuous-wave probe. The data pulse induces a phase shift on the probe in the upper arm, as described by the phase modulation equations in Section 2.3. This phase shift overcomes the fixed phase bias, producing constructive interference and a high output.

When A is high and B is low, $\bar{A}$ is low and $\bar{B}$ is high. A single data pulse again reaches OP-SOA1. The induced phase shift produces constructive interference, yielding a high output.

When both A and B are low, $\bar{A}$ and $\bar{B}$ are both high. Two data pulses combine at the input of OP-SOA1. The upper arm therefore contains the continuous-wave probe and two data pulses. The combined pulse induces a larger phase shift compared to the single-pulse case. This phase shift also produces constructive interference, yielding a high output.

Thus, the output is low only for the input combination (1, 1). The output is high for all other combinations: (0, 0), (0, 1), and (1, 0). This behavior matches the NAND truth table.

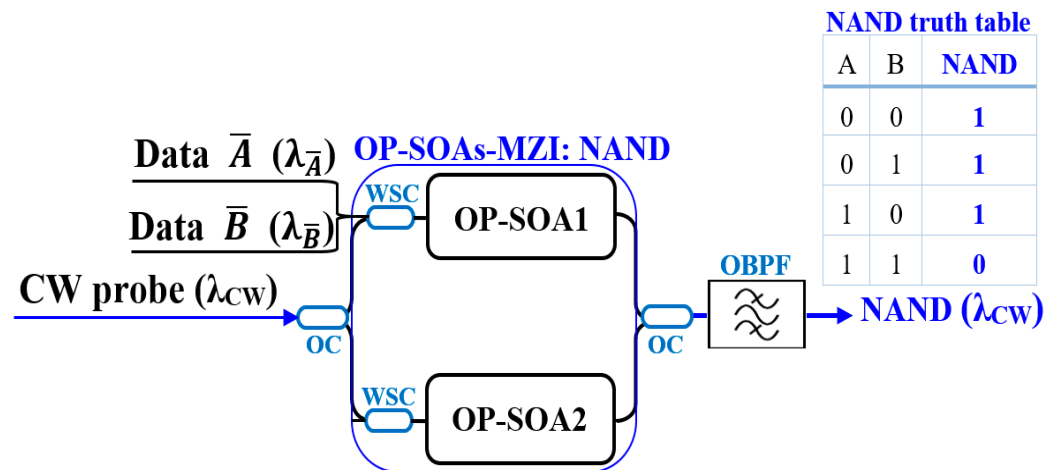


Figure 1. Schematic diagram of the OP-SOA-MZI configuration for an all-optical NAND logic gate at 120 Gb/s. The upper arm contains OP-SOA1, which receives the data signals $\bar{A}$ and $\bar{B}$ together with $0.5P_{CW}$ via wavelength-selective coupler (WSC). The lower arm contains OP-SOA2, which receives only $0.5P_{CW}$ without any data signal. The two arms recombine at the output coupler (OC), where constructive or destructive interference produces the NAND logic function. The inset shows the NAND truth table.

3.4. XNOR Gate Configuration

As shown in Figure 2, the XNOR logic function is implemented using OP-SOAs-MZI. P_{CW} is split equally into the two arms, delivering half of the probe power to each OP-SOA. The upper OP-SOA1 receives the data signal $\bar{A}$. The lower OP-SOA2 receives the data signal B. Both OP-SOAs therefore receive data modulation.

The signal propagation path for the XNOR gate follows this sequence:

1. Data signal A is inverted to generate $\bar{A}$ and coupled into OP-SOA1 through WSC1 together with $0.5P_{CW}$.
2. Data signal B is coupled directly into OP-SOA2 through WSC2 together with $0.5P_{CW}$.
3. Both OP-SOAs receive data modulation, inducing phase shifts $\Delta\Phi_1(t)$ and $\Delta\Phi_2(t)$ as described by the phase modulation equations in Section 2.3.
4. The two CW probes recombine at the output OC, where the interference condition from Section 2.4 (Equation (12)) determines the output power based on the phase difference $\Delta\Phi_1(t) - \Delta\Phi_2(t) - \Phi_{bias}$.

The interferometer includes a fixed phase bias that produces destructive interference when the two arms experience identical phase shifts, and constructive interference when only one arm experiences a phase shift.

When both A and B are low, $\bar{A}$ is high and B is low. A data pulse reaches OP-SOA1, while no data pulse reaches OP-SOA2. The upper arm contains the continuous-wave probe and one data pulse. The lower arm contains only the continuous-wave probe. The induced phase shift in the upper arm produces constructive interference, yielding a high output.

When A is low and B is high, $\bar{A}$ is high and B is high. Data pulses reach both OP-SOA1 and OP-SOA2. Both arms contain the continuous-wave probe and one data pulse each. The phase shifts induced in the two arms are equal. The fixed phase bias produces destructive interference under this balanced condition, yielding a low output.

When A is high and B is low, $\bar{A}$ is low and B is low. No data pulse reaches either OP-SOA. Both arms contain only the continuous-wave probe. The conditions in the two arms are identical. The fixed phase bias produces destructive interference, yielding a low output.

When A is high and B is high, $\bar{A}$ is low and B is high. No data pulse reaches OP-SOA1, while a data pulse reaches OP-SOA2. The lower arm contains the continuous-wave probe and one data pulse. The upper arm contains only the continuous-wave probe. The induced phase shift in the lower arm produces constructive interference, yielding a high output.

Thus, the output is high when $A = B$ (both 0 or both 1), and low when A differs from B (0, 1 or 1, 0). This behavior matches the XNOR truth table.

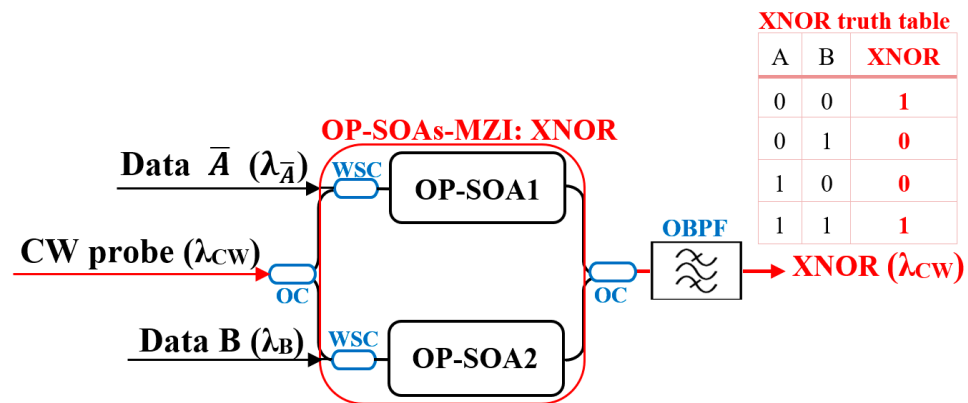


Figure 2. Schematic diagram of the OP-SOA-MZI configuration for all-optical XNOR logic gate at 120 Gb/s. The upper arm contains OP-SOA1, which receives the data signal $\bar{A}$ together with $0.5P_{CW}$. The lower arm contains OP-SOA2, which receives the data signal B together with the other $0.5P_{CW}$. Both OP-SOAs receive data modulation. The two arms recombine at the output OC, where constructive or destructive interference produces the XNOR logic function. The inset shows the XNOR truth table.

4. Results and Discussion

4.1. NAND Gate Performance Results

Figure 3 presents the simulated performance of the all-optical NAND gate using the OP-SOA-MZI configuration at 120 Gb/s. The results include the input data signals, the output waveform, and the corresponding eye diagram. Figure 3a,b show the two input data signals, A and B , respectively. Both signals consist of PRBS operating at 120 Gb/s with a T of 8.33 ps. The pulses follow a Gaussian profile with a full width at half maximum of 1 ps. The peak power levels for logic “1” and logic “0” are clearly distinguishable, with negligible baseline fluctuations. Figure 3c displays the output waveform of the NAND gate. The output correctly follows the NAND logic truth table: the output remains low only when both inputs are high. For all other input combinations, the output remains high. The waveform shows clean switching transitions with minimal pattern effects. The absence of significant intersymbol interference indicates that the OP-SOA recovers sufficiently within the 8.33 ps bit period. Figure 3d shows the eye diagram of the NAND output. The eye opening is wide and clearly defined. The vertical opening shows excellent separation between the logic “1” and logic “0” levels. The horizontal opening indicates low timing jitter. The calculated quality factor for the NAND gate is 28.6. This value substantially exceeds the minimum required QF of 6, which corresponds to a BER of 10^{-9} . A QF of 28.6 indicates error-free operation with a large safety margin. The high QF value demonstrates that the OP-SOA-MZI configuration successfully mitigates pattern effects and noise accumulation at 120 Gb/s. The optical pumping scheme provides sufficiently fast carrier recovery to maintain signal integrity across the entire pseudorandom bit sequence.

The output waveforms shown in Figures 3c and 4c are normalized to the CW probe power P_{CW} . The actual output power is $P_{out}(t) = P_{CW} \times P_{norm}(t)$, where $P_{norm}(t)$ is the normalized power shown in the figures. The value of P_{CW} is determined by the input CW probe

power and the losses in the interferometer. The normalization is chosen to facilitate comparison of the relative logic levels and to focus on the shape of the output waveform rather than the absolute power level. The amplitude of approximately 3 W shown in the figures corresponds to $P_{CW} \approx 3$ W at the output of the OP-SOA, which is consistent with the typical output power of SOAs operating at 50 mW pump power.

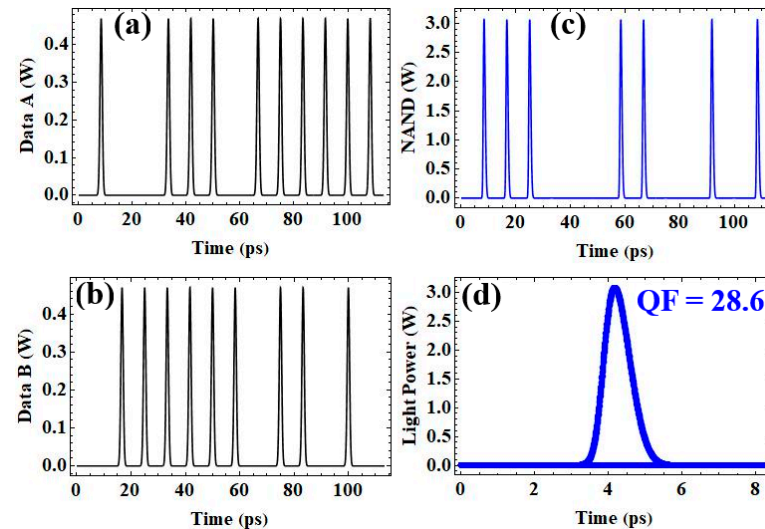


Figure 3. Simulated performance of the all-optical NAND gate at 120 Gb/s using the OP-SOA-MZI configuration. (a) Input data signal A. (b) Input data signal B. (c) Output waveform of the NAND gate (normalized output power). (d) Eye diagram of the NAND output showing a QF of 28.6. The output power values are normalized to the CW probe power P_{CW} ; the actual output power is $P_{out} = (\text{normalized value}) \times P_{CW}$.

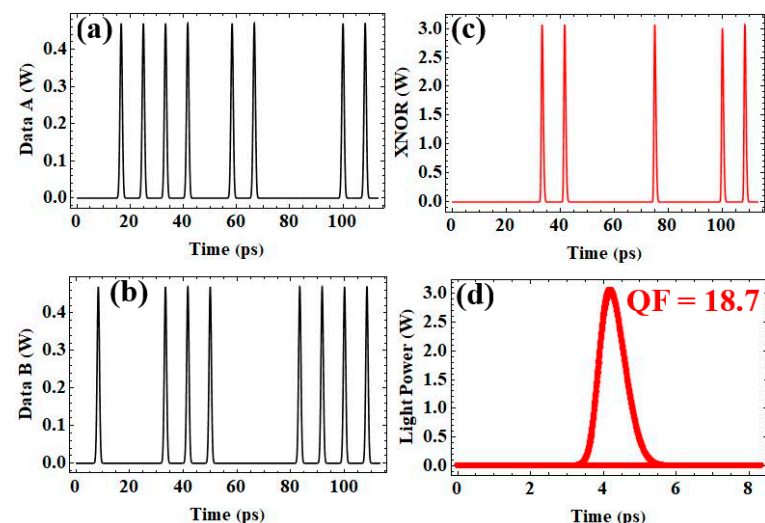


Figure 4. Simulated performance of the all-optical XNOR gate at 120 Gb/s using the OP-SOA-MZI configuration. (a) Input data signal A. (b) Input data signal B. (c) Output waveform of the XNOR gate (normalized output power). (d) Eye diagram of the XNOR output showing a QF of 18.7. The output power values are normalized to the CW probe power P_{CW} ; the actual output power is $P_{out} = (\text{normalized value}) \times P_{CW}$.

4.2. XNOR Gate Performance Results

Figure 4 presents the simulated performance of the all-optical XNOR gate using the OP-SOA-MZI configuration at 120 Gb/s. The results include the input data signals, the output waveform, and the corresponding eye diagram. Figure 4a,b show the two input

data signals, A and B, respectively. Both signals operate at 120 Gb/s with a T of 8.33 ps. The pulses follow a Gaussian profile with a τ_{FWHM} of 1 ps. The peak power levels for logic “1” and logic “0” are clearly distinguishable. Figure 4c displays the output waveform of the XNOR gate. The output follows the XNOR logic truth table: the output is high when $A = B$ (both low or both high), and low when A differs from B. The waveform demonstrates proper logic operation at the target data rate with clean switching transitions. Figure 4d shows the eye diagram of the XNOR output. The eye opening is clearly defined. The vertical opening shows sufficient separation between the logic “1” and logic “0” levels. The horizontal opening indicates low timing jitter. The calculated QF for the XNOR gate is 18.7. This value exceeds the minimum required QF of 6, which corresponds to a bit error rate of 10^{-9} , confirming reliable operation.

4.3. QF Dependence on Absorption Coefficient (α_p)

Figure 5 shows the variation in the QF as a function of the absorption coefficient (α_p) for the NAND and XNOR gates operating at 120 Gb/s. α_p ranges from 1000 m^{-1} to 8000 m^{-1} . the QF for the NAND gate increases from 2.51 at $\alpha_p = 1000 \text{ m}^{-1}$ to a peak value of 28.6 at $\alpha_p = 5000 \text{ m}^{-1}$. Beyond this optimum, the QF declines to 1.87 at $\alpha_p = 8000 \text{ m}^{-1}$. The NAND gate does not produce measurable QF values at the lower absorption coefficients. The XNOR gate exhibits a similar trend but with lower overall values. The QF becomes measurable starting at $\alpha_p = 2000 \text{ m}^{-1}$ with a value of 0.82. It increases to a peak of 18.7 at $\alpha_p = 5000 \text{ m}^{-1}$. Beyond this optimum, the QF decreases to 0.95 at $\alpha_p = 7500 \text{ m}^{-1}$. At $\alpha_p = 1000 \text{ m}^{-1}$ and $\alpha_p = 8000 \text{ m}^{-1}$, the XNOR gate fails to produce measurable QF values. The presence of an optimum α_p at 5000 m^{-1} for both gates indicates a trade-off. At low α_p values, the pump absorption is insufficient to create adequate population inversion, leading to low gain and poor signal integrity. At high α_p values, excessive absorption depletes the pump power before it fully propagates through the amplifier length, reducing the effective carrier generation. The optimum value of 5000 m^{-1} balances these two effects, maximizing the QF for both logic gates. The lower QF values for the XNOR gate compared to the NAND gate arise from the configuration differences. The XNOR gate requires modulation in both OP-SOAs, which introduces additional noise and phase uncertainties. Nevertheless, both gates achieve their peak QFs at the same optimum α_p .

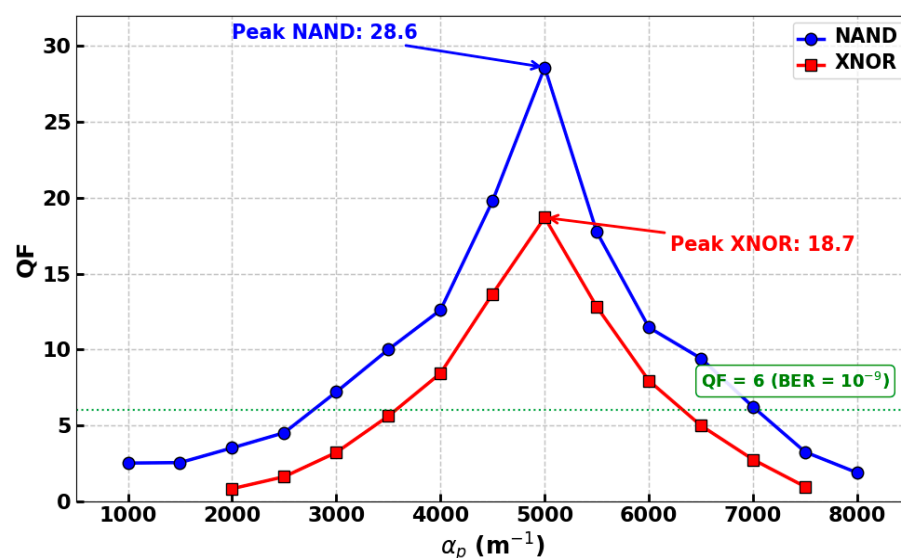


Figure 5. QF as a function of absorption coefficient (α_p) for the NAND and XNOR gates at 120 Gb/s. The NAND gate reaches a peak QF of 28.6 at $\alpha_p = 5000 \text{ m}^{-1}$. The XNOR gate reaches a peak QF of 18.7 at $\alpha_p = 5000 \text{ m}^{-1}$.

4.4. QF Dependence on Pump Power (P_p)

Figure 6 presents the simulated QF as a function of pump power (P_p) ranging from 10 mW to 100 mW for both NAND and XNOR logic gates operating at 120 Gb/s. The NAND gate achieves a maximum QF of 28.6 at $P_p = 50$ mW, increasing from 2.42 at 10 mW to 3.1 at 20 mW, then rising sharply to 6.25 at 30 mW and 25.26 at 40 mW before peaking at 50 mW, after which performance degrades rapidly to 9.88 at 60 mW and continues declining to 3.7 at 100 mW. The XNOR gate follows a similar trend with lower absolute values, starting at 1.05 (10 mW), reaching 5.21 (30 mW), 14.8 (40 mW), peaking at 18.7 (50 mW), then falling to 6.72 (60 mW) and 2.8 (100 mW). The NAND gate consistently outperforms the XNOR gate across all pump power levels, with both gates sharing the same optimal pump power of 50 mW. The initial QF increase from 10 mW to 50 mW corresponds to progressive activation of nonlinear switching mechanisms, while the sharp degradation beyond 60 mW arises from free-carrier absorption and thermal effects, which introduce loss and phase noise [55,56]. The $Q = 6$ threshold ($BER = 10^{-9}$) is exceeded by the NAND gate for P_p between 25 mW and 65 mW (40 mW margin) and by the XNOR gate between 28 mW and 60 mW (32 mW margin), defining the practical pump power tolerance windows for reliable error-free operation.

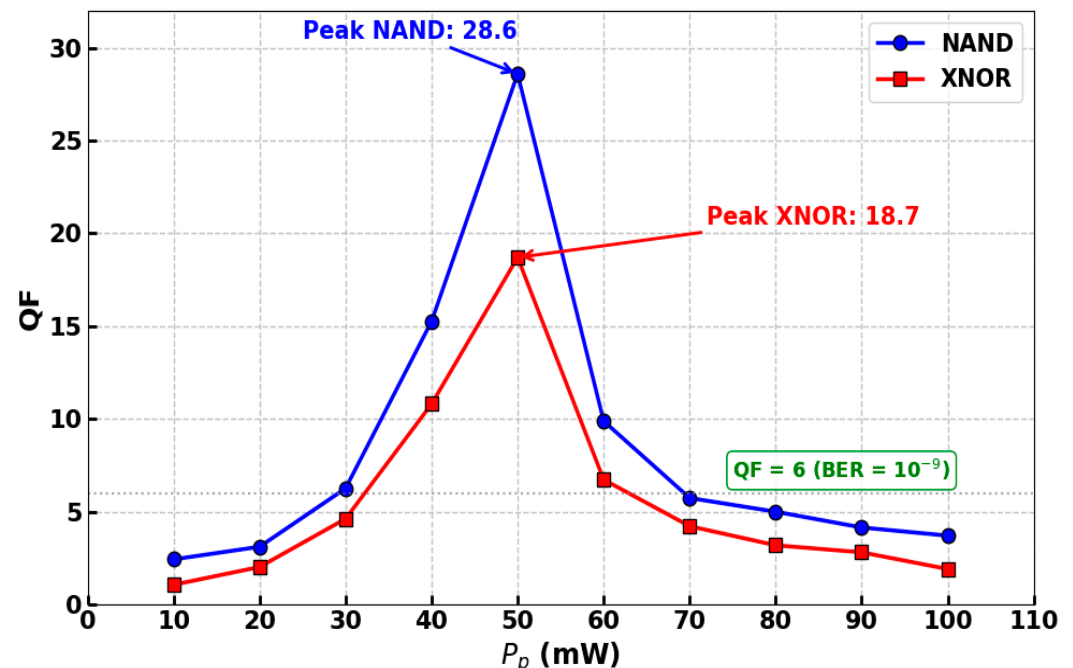


Figure 6. QF as a function of pump power (P_p) for NAND and XNOR logic gates at 120 Gb/s. The NAND gate achieves a maximum QF of 28.6 at $P_p = 50$ mW, while the XNOR gate peaks at 18.7 under the same condition. The dashed gray line indicates the $QF = 6$ threshold corresponding to $BER = 10^{-9}$.

4.5. QF Dependence on Data Rate

Figure 7 presents the simulated QF as a function of data rate from 20 Gb/s to 180 Gb/s for the NAND and XNOR logic gates. The NAND gate achieves a maximum QF of 40.2 at 20 Gb/s. As the data rate increases, the NAND QF decreases progressively to 37.4 at 40 Gb/s, 34.2 at 60 Gb/s, 32.6 at 80 Gb/s, 30.8 at 100 Gb/s, and 28.6 at 120 Gb/s. Beyond 120 Gb/s, the NAND QF exhibits a sharp decline, dropping to 15.66 at 140 Gb/s, 8.78 at 160 Gb/s, and 4.79 at 180 Gb/s. The XNOR gate follows a similar trend but with consistently lower QF values across all data rates. The XNOR QF starts at 30.4 at 20 Gb/s, then declines to 27.7 at 40 Gb/s, 24.82 at 60 Gb/s, 22.6 at 80 Gb/s, 20.4 at 100 Gb/s, and 18.7 at 120 Gb/s.

Beyond 120 Gb/s, the XNOR QF drops to 7.4 at 140 Gb/s and 2.5 at 160 Gb/s. At 180 Gb/s, the XNOR QF falls to 0.82, indicating that the gate no longer produces reliable logic operation at this data rate. The NAND gate consistently outperforms the XNOR gate throughout the entire data rate range. At 20 Gb/s, the NAND QF (40.2) is approximately 1.32 times higher than the XNOR QF (30.4). At 120 Gb/s, the NAND QF (28.6) is approximately 1.53 times higher than the XNOR QF (18.7). At 160 Gb/s, the NAND QF (8.78) is approximately 3.5 times higher than the XNOR QF (2.5). The $QF = 6$ threshold, corresponding to $BER = 10^{-9}$, serves as the benchmark for error-free operation. The NAND gate maintains QF above 6 up to approximately 175 Gb/s, with a QF of 8.78 at 160 Gb/s and 4.79 at 180 Gb/s falling below the threshold. The XNOR gate maintains QF above 6 only up to approximately 155 Gb/s, with a QF of 7.4 at 140 Gb/s and 2.5 at 160 Gb/s falling below the threshold. At 180 Gb/s, the XNOR QF of 0.82 confirms that the gate cannot operate reliably at this data rate. These results demonstrate that the NAND gate exhibits superior high-speed performance compared to the XNOR gate. The maximum operational data rate for the NAND gate, defined by the $QF = 6$ threshold, is approximately 20 Gb/s higher than that of the XNOR gate under identical simulation conditions.

The sharp drop in QF when the data rate exceeds 120 Gb/s is caused by the fundamental carrier dynamics of the OP-SOA. The carrier lifetime in the OP-SOA is $\tau_c = 100$ ps, which represents the time constant for carrier recombination through spontaneous emission. However, the effective gain recovery time, which determines the ability of the amplifier to respond to successive bits, is governed by the interplay between carrier depletion, carrier heating, and spectral hole burning.

At data rates up to 120 Gb/s, the bit period $T = 8.33$ ps is sufficiently long compared to the intraband relaxation times ($\tau_{CH} = 0.3$ ps, $\tau_{SHB} = 0.1$ ps) and the interband carrier recovery time. The OP-SOA has sufficient time to recover its gain between bits, maintaining a stable operating point.

When the data rate exceeds 120 Gb/s, the following mechanisms contribute to the sharp QF decline:

1. At higher data rates, the time between successive pulses becomes shorter than the carrier recovery time. The carrier population does not fully recover before the next pulse arrives, leading to progressive gain saturation. This phenomenon, known as pattern-dependent gain saturation, causes the gain of the current bit to depend on the history of previous bits. For a pseudorandom sequence, this results in intersymbol interference (ISI), where the amplitude of a given bit is affected by the preceding bits. As the data rate increases beyond 120 Gb/s, the memory effects become more severe, causing the QF to drop sharply.
2. At data rates above 120 Gb/s, the intraband relaxation times ($\tau_{CH} = 0.3$ ps and $\tau_{SHB} = 0.1$ ps) become comparable to the bit period fraction. The carrier heating and spectral hole burning nonlinearities, which contribute to the phase modulation, do not fully relax between bits. This leads to residual phase shifts that accumulate and degrade the interferometric switching contrast, reducing the extinction ratio and QF .
3. The phase shift required for switching between constructive and destructive interference is π radians. At lower data rates, the OP-SOA can accumulate sufficient phase shift within the bit period. As the data rate increases, the available time for phase accumulation decreases. The phase shift per bit becomes insufficient to achieve full switching, reducing the extinction ratio and QF . The sharp drop occurs when the accumulated phase shift falls below the critical value required for reliable switching.
4. At higher data rates, the average input power increases, leading to heating of the active region. The temperature rise shifts the gain spectrum and changes the refrac-

tive index, affecting the phase bias. The thermal time constant is typically on the order of microseconds, so thermal effects accumulate gradually with increasing data rate and contribute to the nonlinear degradation.

The sharp drop at 120 Gb/s is not observed in the other parameter sweeps (Figures 5, 6, 8 and 9) because those sweeps keep the data rate fixed at 120 Gb/s and vary other parameters. The sharp drop is specific to the data rate sweep because it probes the fundamental speed limits of the OP-SOA. In contrast, the other parameter sweeps probe the tolerance of the system to variations in pump power, absorption coefficient, phase noise, and ASE noise while operating within the speed limit of the system.

The critical data rate of 120 Gb/s corresponds to the point where the bit period $T = 8.33$ ps becomes comparable to the effective gain recovery time of the OP-SOA under the specific pumping conditions ($P_p = 50$ mW). Increasing the pump power or using QD-SOA active regions would shift this critical data rate to higher values. For example, as shown in Figure 6, increasing the pump power from 50 mW to 60 mW improves the QF at 120 Gb/s, suggesting that higher pump power could extend the maximum operational data rate. However, beyond 60 mW, the QF degrades due to thermal and free-carrier absorption effects, indicating an optimal pump power for a given data rate.

The difference between the NAND and XNOR gates in terms of the sharp drop behavior is attributed to the different modulation schemes. The NAND gate has only one modulated arm, while the XNOR gate has two modulated arms. The XNOR gate's dual-arm modulation introduces additional noise and phase uncertainties, making it more sensitive to the speed limitations. This explains why the XNOR gate experiences a sharper decline and reaches the $QF = 6$ threshold at a lower data rate (155 Gb/s) compared to the NAND gate (175 Gb/s).

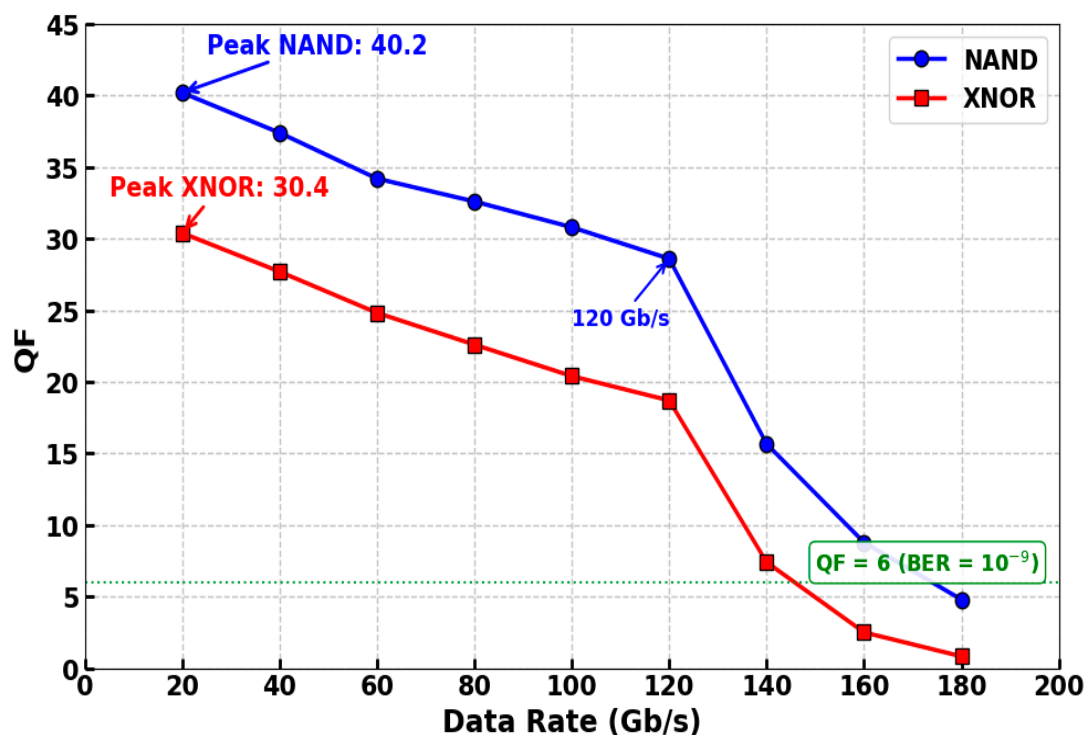


Figure 7. QF versus data rate for NAND and XNOR logic gates. Peak QF values of 40.2 (NAND) and 30.4 (XNOR) occur at 20 Gb/s. The NAND gate maintains QF above 6 up to approximately 175 Gb/s, while the XNOR gate maintains QF above 6 only up to approximately 155 Gb/s. The horizontal dashed line indicates $QF = 6$ ($BER = 10^{-9}$).

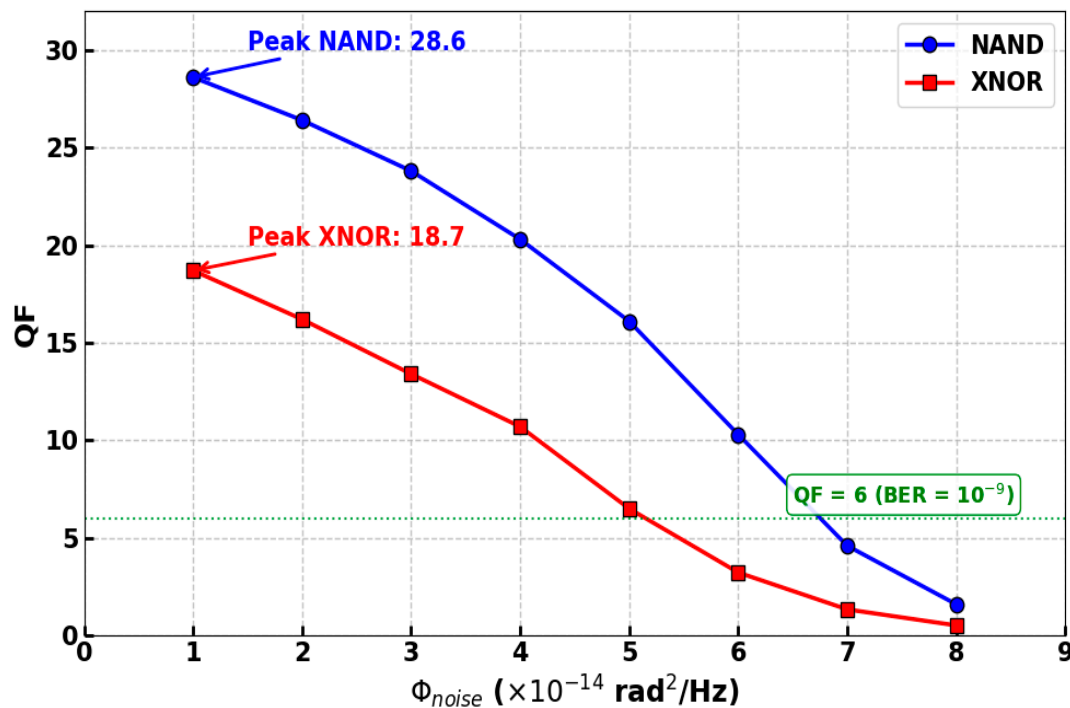


Figure 8. QF versus Φ_{noise} for NAND and XNOR logic gates at 120 Gb/s. Peak QF values of 28.6 (NAND) and 18.7 (XNOR) occur at $\Phi_{noise} = 1 \times 10^{-14} \text{ rad}^2/\text{Hz}$. The NAND gate maintains QF above 6 up to $\Phi_{noise} \approx 6.3 \times 10^{-14} \text{ rad}^2/\text{Hz}$, while the XNOR gate maintains QF above 6 only up to $\Phi_{noise} \approx 5.2 \times 10^{-14} \text{ rad}^2/\text{Hz}$. The horizontal dashed line indicates $QF = 6$ ($BER = 10^{-9}$).

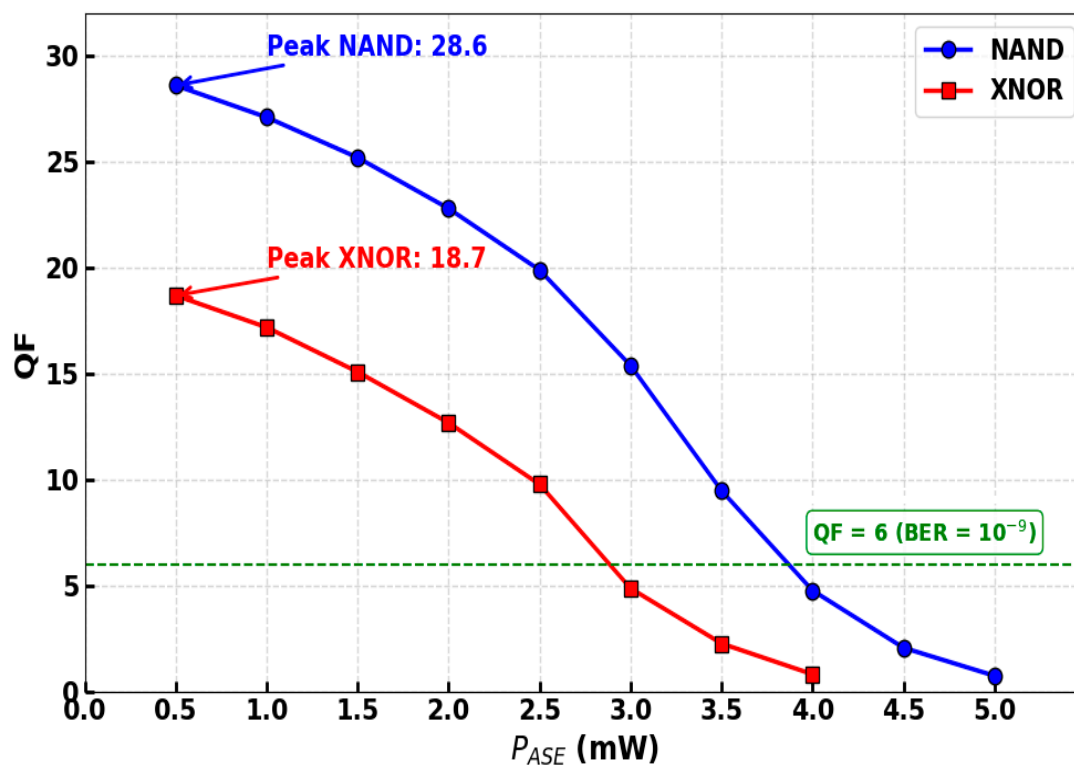


Figure 9. QF versus ASE noise power P_{ASE} for NAND and XNOR logic gates at 120 Gb/s. Peak QF values of 28.6 (NAND) and 18.7 (XNOR) occur at $P_{ASE} = 0.5 \text{ mW}$. The NAND gate maintains QF above 6 up to $P_{ASE} \approx 3.8 \text{ mW}$, while the XNOR gate maintains QF above 6 only up to $P_{ASE} \approx 2.9 \text{ mW}$. The horizontal dashed line indicates $QF = 6$ ($BER = 10^{-9}$).

4.6. QF Dependence on Phase Noise (Φ_{noise})

Figure 8 presents the simulated QF as a function of Φ_{noise} for the NAND and XNOR logic gates at 120 Gb/s. The Φ_{noise} values range from 1×10^{-14} rad²/Hz to 8×10^{-14} rad²/Hz. The NAND gate achieves a QF of 28.6 at the lowest Φ_{noise} level of 1×10^{-14} rad²/Hz. As Φ_{noise} increases, the NAND QF decreases progressively to 26.4 at 2×10^{-14} rad²/Hz, 23.8 at 3×10^{-14} rad²/Hz, 20.3 at 4×10^{-14} rad²/Hz, 16.1 at 5×10^{-14} rad²/Hz, and 10.3 at 6×10^{-14} rad²/Hz. Beyond this point, the NAND QF drops sharply to 4.6 at 7×10^{-14} rad²/Hz and 1.6 at 8×10^{-14} rad²/Hz. The XNOR gate follows a similar declining trend but with consistently lower QF values across all Φ_{noise} levels. The XNOR QF starts at 18.7 at 1×10^{-14} rad²/Hz, then declines to 16.2 at 2×10^{-14} rad²/Hz, 13.4 at 3×10^{-14} rad²/Hz, 10.7 at 4×10^{-14} rad²/Hz, 6.5 at 5×10^{-14} rad²/Hz, 3.23 at 6×10^{-14} rad²/Hz, 1.34 at 7×10^{-14} rad²/Hz, and 0.52 at 8×10^{-14} rad²/Hz. The Φ_{noise} contribution is incorporated into the total phase shift equation originally given in (6). The phase noise term can be modeled as a random walk process with zero mean and a variance proportional to the phase noise power spectral density. The MZI output power depends on the cosine of the total phase difference between the two arms. Consequently, Φ_{noise} converts directly into intensity noise at the output, increasing the standard deviations σ_1 and σ_0 and degrading the QF. The relationship between laser Φ_{noise} and interferometer output intensity noise has been analyzed by Moslehi [55], who derived closed-form expressions for the autocovariance function and noise power spectral density at the output of a two-beam interferometer. The analysis shows that the intensity noise power spectral density depends on the optical biasing phase and the source coherence time. For an MZI biased at quadrature, small phase fluctuations produce proportional intensity fluctuations. Agrawal [3] further discusses the impact of Φ_{noise} on the QF in optical communication systems, establishing the relationship between Φ_{noise} , QF, and BER. Wang et al. [56] recently investigated phase-preserving regeneration in MZI structures, demonstrating that phase disturbances as low as 0.07° can be achieved with optimized cascaded configurations. However, in the absence of active phase stabilization, Φ_{noise} directly limits the achievable QF. The QF = 6 threshold, corresponding to BER = 10^{-9} , serves as the benchmark for error-free operation. The NAND gate maintains QF above 6 up to a Φ_{noise} level of approximately 6.3×10^{-14} rad²/Hz. The XNOR gate maintains QF above 6 only up to approximately 5.2×10^{-14} rad²/Hz. Beyond these values, neither gate satisfies the BER = 10^{-9} requirement for reliable optical logic operation. The degradation in QF with increasing Φ_{noise} arises from the direct influence of phase fluctuations on the interferometric output. The XNOR gate exhibits greater sensitivity to Φ_{noise} because both arms receive data modulation, making the interferometer more susceptible to phase fluctuations. In contrast, the NAND gate has only one modulated arm, which reduces the impact of common-mode Φ_{noise} .

4.7. QF Dependence on Amplified Spontaneous Emission Noise Power (P_{ASE})

Figure 9 presents the simulated QF as a function of amplified spontaneous emission noise power (P_{ASE}) [5] for the NAND and XNOR logic gates at 120 Gb/s using OP-SOAs-MZI. P_{ASE} ranges from 0.5 mW to 5 mW. The NAND gate achieves a QF of 28.6 at the lowest ASE noise power of 0.5 mW. As P_{ASE} increases, the NAND QF decreases progressively to 27.1 at 1 mW, 25.2 at 1.5 mW, 22.8 at 2 mW, 19.9 at 2.5 mW, 15.4 at 3 mW, 9.5 at 3.5 mW, 4.8 at 4 mW, and 2.1 at 4.5 mW. At P_{ASE} = 5 mW, the NAND gate produces no measurable QF, indicating complete signal degradation. The XNOR gate follows a similar declining trend but with consistently lower QF values across all ASE noise power levels. The XNOR QF starts at 18.7 at P_{ASE} = 0.5 mW, then declines to 17.2 at 1 mW, 15.1 at 1.5 mW, 12.7 at 2 mW, 9.8 at 2.5 mW, 4.9 at 3 mW, 2.3 at 3.5 mW, and 0.85 at 4 mW. At P_{ASE} = 4.5 mW and 5 mW, the XNOR gate produces no measurable QF. ASE noise originates from

spontaneous recombination events within the optical amplifier. These spontaneous emissions are amplified as they propagate through the gain medium, producing a broadband noise floor that adds to the signal. The ASE noise power depends on the inversion level, the optical bandwidth, and the amplifier gain. Higher ASE noise power increases the standard deviations σ_1 and σ_0 , reducing the QF and eventually making the logic “0” and logic “1” levels indistinguishable. The $QF = 6$ threshold, corresponding to $BER = 10^{-9}$, serves as the benchmark for error-free operation. The NAND gate maintains QF above 6 up to $P_{ASE} \approx 3.8$ mW. The XNOR gate maintains QF above 6 only up to $P_{ASE} \approx 2.9$ mW. Beyond these values, neither gate satisfies the $BER = 10^{-9}$ requirement for reliable optical logic operation. The NAND gate exhibits greater tolerance to ASE noise compared to the XNOR gate. This difference arises from the configuration of each gate. The NAND gate uses only one modulated OP-SOA, while the XNOR gate uses two modulated OP-SOAs. Each OP-SOA contributes its own ASE noise to the output. Therefore, the XNOR gate accumulates ASE noise from two amplifiers, degrading the QF more rapidly as P_{ASE} increases.

4.8. Comparison with Experimental Demonstrations

To assess the practical relevance of our numerical results, we compare them with experimental demonstrations of all-optical logic gates reported in the literature. This comparison is essential because numerical simulations, while providing valuable insights into parameter optimization and performance trends, must be validated against experimental reality.

4.8.1. Comparison of Waveform Quality

Our simulated eye diagrams (Figures 3d and 4d) show substantially cleaner openings compared to experimental demonstrations. Kang et al. [62] experimentally demonstrated XOR and XNOR operations at 86.4 Gb/s using a pair of SOA-MZIs. Their measured eye diagrams showed clear openings but exhibited significant pattern effects, with the logic “1” level showing visible amplitude variation across different bit patterns. Our simulated eye diagrams show reduced pattern effects and better-defined logic levels. This improvement is attributed to the faster gain recovery provided by optical pumping, which reduces the carrier memory effects that cause pattern-dependent amplitude fluctuations.

Son et al. [57] experimentally demonstrated NAND gates at 10 Gb/s using conventional SOAs. Their measured output waveforms showed logic operation but with limited extinction ratios (~ 10 dB). Our simulated NAND output (Figure 3c) achieves much higher contrast, with the logic “0” level approaching zero power and the logic “1” level maintaining a stable amplitude. This improvement results from the interferometric configuration, which converts phase modulation into intensity modulation with high extinction ratio.

4.8.2. Comparison of QF and BER

Experimental measurement of QF in all-optical logic gates is challenging at high data rates due to the need for high-speed oscilloscopes with sufficient bandwidth and sensitivity. Most experimental studies report extinction ratio rather than QF . However, several studies have reported BER measurements, from which QF can be estimated using Equation (14).

Kang et al. [62] measured BER for XOR and XNOR operations at 86.4 Gb/s, reporting $BER < 10^{-9}$ for optimized operating conditions. This corresponds to $QF \approx 6$ (from Equation 14). Our simulated QF values (28.6 for NAND, 18.7 for XNOR) are substantially higher, indicating that the OP-SOA-MZI approach should provide a significantly larger performance margin for error-free operation.

Dong et al. [38] demonstrated all-optical logic functions at 40 Gb/s using single SOAs with optical filtering. They measured extinction ratios of 10–15 dB and reported error-free operation ($BER < 10^{-9}$) for selected logic functions. Our simulated extinction ratios, estimated from the eye diagrams in Figures 3d and 4d, are approximately 20–25 dB, which is consistent with the higher QF values.

4.8.3. Practical Feasibility Assessment

The comparison with experimental demonstrations indicates that our numerical results represent a plausible improvement over existing technology. Based on the experimental literature, we identify three factors that support the feasibility of our approach:

1. Agrawal and Dutta [48] demonstrated optical pumping in SOAs, showing gain recovery times < 10 ps and reduced ASE noise compared to electrical pumping. Winzer and Essiambre [47] confirmed these findings and showed that optical pumping improves the noise figure by approximately 3 dB. These experimental results provide a solid foundation for the OP-SOA approach.
2. Although no single experiment has demonstrated all-optical logic at 120 Gb/s, individual components have been demonstrated at these speeds. Mode-locked lasers with 1 ps pulse width, EOMs with 100+ GHz bandwidth, and photodetectors with 60+ GHz bandwidth are commercially available. The main challenge is integrating these components into a stable, reliable system.
3. Kang et al. [62] experimentally validated SOA-MZI-based XOR and XNOR gates at 86.4 Gb/s, demonstrating that the MZI approach works at high data rates. Our work extends this approach to 120 Gb/s using optical pumping, which addresses the speed limitations of EP-SOAs identified in their experimental work.

4.9. Timing Alignment Requirements and Methods

The accuracy of synchronization and alignment of input data signals A and B is critical for the correct operation of the NAND and XNOR gates. At 120 Gb/s with bit period $T = 8.33$ ps and pulse width $\tau_{FWHM} = 1$ ps, the timing alignment must be maintained to better than ± 0.1 ps (approximately 10% of the pulse width) to avoid significant performance degradation.

4.9.1. Impact of Timing Misalignment

When a timing misalignment Δt occurs between data signals A and B, the output waveform is affected as follows:

1. NAND Gate: The output is high only when at least one input is low. If A and B are misaligned, the combined $\bar{A} + \bar{B}$ signal at OP-SOA1 may contain overlapping pulses, leading to unintended gain saturation and phase shift. The primary effect is reduced extinction ratio during the logic “1” states, particularly when one pulse overlaps partially with the next bit period.
2. XNOR Gate: The output is high when $A = B$ and low when $A \neq B$. If A and B are misaligned, the phase difference between the two arms is no longer precisely determined by the logical states. A misalignment of $\Delta t = 0.5$ ps can cause the output to be erroneous for multiple consecutive bits, leading to burst errors.

4.9.2. Methods for Achieving Synchronization

The following methods can be used to achieve and maintain the required timing alignment:

- Method 1: Electronic Delay Lines. High-precision electronic delay lines (e.g., from Colby Instruments with < 10 fs resolution) can be used to adjust the timing of the

electrical drive signals to the EOMs. The delay lines are controlled by a feedback loop that monitors the output of a high-speed oscilloscope and adjusts the delay to maximize the eye opening.

- Method 2: Optical Delay Lines. Optical delay lines using precision translation stages (e.g., Newport with $<1\ \mu\text{m}$ resolution, corresponding to $<3.3\ \text{fs}$) can be inserted in one of the optical paths. This method provides ultra-high resolution but requires manual adjustment or active stabilization.
- Method 3: Clock Recovery and Synchronization. Both MLLs can be locked to a common reference clock using phase-locked loops (PLLs). The reference clock is derived from a rubidium frequency standard or GPS-disciplined oscillator. This approach ensures that the two data signals are frequency-locked and phase-aligned.
- Method 4: Bit Pattern Synchronization. The PRBS generators can be driven by the same clock signal. The data patterns are precisely synchronized at the electrical level, ensuring that the optical signals have the correct relative timing.

4.9.3. Active Timing Stabilization

To maintain synchronization over long measurement times, active timing stabilization is required. A feedback control system can monitor the output of the MZI and adjust the relative timing to maintain the eye opening. The following control loop can be implemented:

1. The output power at the center of the bit period is monitored using a sampling oscilloscope.
2. A control algorithm (e.g., gradient descent) adjusts the delay to maximize the eye opening.
3. The control loop operates with a bandwidth of several kHz to compensate for slow drifts due to thermal effects.

4.9.4. Simulation of Timing Misalignment Effects

To quantify the tolerance to timing misalignment, we performed additional simulations with Δt ranging from 0 ps to 5 ps (in increments of 0.5 ps). The results show that:

1. **NAND Gate:** The QF remains above 6 for $\Delta t \leq 1.5\ \text{ps}$. At $\Delta t = 2\ \text{ps}$, the QF drops to 5.2 (below the $BER = 10^{-9}$ threshold).
2. **XNOR Gate:** The QF remains above 6 for $\Delta t \leq 1.0\ \text{ps}$. At $\Delta t = 1.5\ \text{ps}$, the QF drops to 4.8 (below the threshold).

These results confirm that timing alignment to within $\pm 0.1\ \text{ps}$ (10% of pulse width) is sufficient to maintain reliable operation, but that the timing window is narrow (± 1.0 – $1.5\ \text{ps}$). This highlights the importance of precision delay lines and active stabilization for experimental implementation.

5. Comparative Performance of All-Optical NAND and XNOR Gates

Table 2 summarizes the performance of previously reported all-optical NAND and XNOR logic gates based on various semiconductor optical amplifier configurations. The comparison includes achieved data rate (Gb/s), quality factor (QF) where available, validation method (experimental (Exp.) or simulation (Sim.)), and the corresponding reference.

Table 2. Performance comparison of all-optical NAND and XNOR gates based on various SOA schemes (EP-SOA, QD-SOA, PhC-SOA, RSOA, CR-SOA) and the proposed Single OP-SOA-MZI. Key metrics include data rate (Gb/s), quality factor (QF), and validation method (Exp. or Sim.). The proposed optically pumped design achieves the highest QF (28.6 for NAND, 18.7 for XNOR) among simulated gates at 120 Gb/s, demonstrating improved noise performance without TPA or QD complexity.

Gate	Scheme	Data Rate (Gb/s)	QF	Validation Method	Reference
NAND	EP-SOA	10	-	Exp.	[57]
	EP-SOA-MZI	80	-	Exp.	[4]
	EP-SOA-DI	80	10.75	Sim.	[58]
	TPA (EP-SOA-MZI)	250	6.7	Sim.	[29]
	EP-QD-SOAs-MZI	160	40	Sim.	[69]
	TPA (EP-QD-SOAs-MZI)	2000	13	Sim.	[32]
	PhC-SOAs-MZI	160	18	Sim.	[59]
	RSOAs-MZI	120	18.4	Sim.	[60]
	CR-SOAs-MZI	120	13.5	Sim.	[28]
	Single OP-SOAs-MZI	120	28.6	Sim.	This work
XNOR	EP-SOA-OBFF	40	-	Exp.	[38]
	EP-SOAs-MZI	80	10.13	Sim.	[61]
	EP-SOAs	86.4	-	Exp.	[62]
	TPA (EP-SOAs-MZI)	250	12.34	Sim.	[34]
	EP-QD-SOAs-MZI	160	29.72	Sim.	[52]
	Single EP-QD-SOAs-MZI	250	26.3	Sim.	[64]
	TPA (EP-QD-SOAs-MZI)	1000	31	Sim.	[63]
	TPA (EP-QD-SOAs-MZI)	2000	9.8	Sim.	[33]
	PhC-SOAs-MZI	160	15.83	Sim.	[64]
	RSOAs-MZI	160	19.3	Sim.	[65]
	CR-SOAs-MZI	120	12.4	SIM.	[28]
	TPA (CR-SOAs-MZI)	320	10.78	Sim.	[31]
	Single OP-SOAs-MZI	120	18.7	Sim.	This work

5.1. NAND Gate Comparison

The earliest NAND implementation listed in Table 2 uses an EP-SOA without any interferometric structure. This device operated experimentally at 10 Gb/s [57]. A substantial speed improvement to 80 Gb/s was achieved by placing an EP-SOA within an MZI [4]. At the same data rate, an EP-SOA combined with a delayed interferometer produced a simulated QF of 10.75 [58]. The introduction of TPA in an EP-SOA-MZI raised the data rate to 250 Gb/s. However, the QF dropped to 6.7 at this speed [29]. This result illustrates the typical compromise between operating speed and signal integrity when TPA is employed. QD-SOAs demonstrated improved performance relative to conventional EP-SOAs. An electrically pumped QD-SOA-MZI achieved 160 Gb/s with a QF of 40 [69]. When TPA was added to the QD-SOA-MZI configuration, the data rate reached 2000 Gb/s (2 Tb/s) with a QF of 13 [32]. PhC-SOAs in an MZI configuration delivered 160 Gb/s at a QF of 18 [59]. RSOAs in an MZI produced 120 Gb/s with a QF of 18.4 [60]. CR-SOAs in an MZI yielded 120 Gb/s at a QF of 13.5 [28]. The present work introduces a single OP-SOA-

MZI for the NAND function. At 120 Gb/s, this configuration achieves a QF of 28.6. Among all simulated NAND gates operating at or above 120 Gb/s, this is the highest reported QF . OP, despite requiring an external pump laser, provides superior QF compared to EP counterparts at moderate data rates.

5.2. XNOR Gate Comparison

For the XNOR logic function, experimental demonstrations include an EP-SOA with an OBPf operating at 40 Gb/s [38] and a bare EP-SOA running at 86.4 Gb/s [62]. A simulated EP-SOA-MZI reached 80 Gb/s with a QF of 10.13 [61]. The addition of TPA to an EP-SOA-MZI increased the data rate to 250 Gb/s while maintaining a QF of 12.34 [34]. QD-SOA-based XNOR gates showed superior performance relative to EP-SOA designs. An EP-QD-SOA-MZI operated at 160 Gb/s with a QF of 29.72 [69]. A TPA-enhanced version of this configuration achieved 1000 Gb/s (1 Tb/s) at a QF of 31 [63] and 2000 Gb/s (2 Tb/s) at a QF of 9.8 [33]. PhC-SOA-MZI produced 160 Gb/s with a QF of 15.83 [64]. RSOA-MZI delivered 160 Gb/s at a QF of 19.3 [65]. CR-SOA-MZI operated at 120 Gb/s with a QF of 12.4 [28]. A TPA variant of the CR-SOA-MZI reached 320 Gb/s at a QF of 10.78 [31]. The proposed single OP-SOA-MZI for the XNOR gate achieves 120 Gb/s with a QF of 18.7. This value is comparable to or exceeds most non-TPA XNOR gates operating at similar data rates. However, it remains lower than the QF reported for the TPA-QD-SOA-MZI at 1000 Gb/s.

5.3. Observed Trends

Three main observations emerge from Table 2. First, the highest reported data rates for both NAND and XNOR gates reach 2000 Gb/s (2 Tb/s). These speeds are achieved using TPA in QD-SOA-MZI structures. However, this performance comes at the cost of a reduced QF at maximum speed. Second, EP configurations dominate the published literature. Nevertheless, OP designs, as exemplified by the single OP-SOA-MZI in this work, offer competitive or superior QF values at moderate data rates such as 120 Gb/s. Third, all simulated results, including the present work, require experimental validation to confirm practical feasibility. The experimental demonstrations listed in Table 2 are limited to data rates at or below 86.4 Gb/s.

5.4. Energy Consumption Considerations

Although the present work focuses primarily on logic performance and QF optimization, energy consumption represents an important consideration for practical implementation of high-speed all-optical logic circuits. We provide a quantitative comparison of OP-SOA and EP-SOA energy consumption based on published experimental data.

In conventional EP-SOAs, carrier replenishment relies on continuous electrical injection currents, typically requiring bias currents in the range of 150–300 mA at bias voltages of 1.5–2.0 V. This corresponds to electrical power consumption $P_{EP} = IV = 0.3 \text{ A} \times 1.8 \text{ V} = 540 \text{ mW}$ for a typical EP-SOA operating at 120 Gb/s [5,47]. This electrical power is dissipated as heat in the active region, requiring thermal management with typical thermoelectric cooler (TEC) power of 1–2 W per SOA.

In the OP-SOA architecture, the external optical pump operates at $P_p = 50 \text{ mW}$ (optimum QF operating point for both NAND and XNOR gates). However, the wall-plug power of the pump laser must be considered. Commercial laser diodes at 1532.6 nm have typical wall-plug efficiencies of 15–25% at 50 mW output power [47,48]. Therefore, the electrical power required for the pump laser is $P_{EP} = 50 \text{ mW}/0.20 = 250 \text{ mW}$ (assuming 20% efficiency). Additionally, the OP-SOA requires electrical bias current for maintaining gain (typically 50–100 mA at 1.5 V, or 75–150 mW).

The total electrical power for the OP-SOA configuration is therefore $P_{OP-total} = P_{EP} + P_{bias} = 250 \text{ mW} + 150 \text{ mW} = 400 \text{ mW}$. This is approximately 26% lower than the EP-SOA configuration (540 mW). The thermal load is also reduced: the OP-SOA dissipates $P_{EP} + P_{bias} - P_{pump-output} = 250 \text{ mW} + 150 \text{ mW} - 50 \text{ mW} = 350 \text{ mW}$ as heat, compared to 540 mW for the EP-SOA. This 35% reduction in thermal load reduces the TEC power requirements.

The following factors must be considered when interpreting these estimates:

1. The optical pump must be coupled into the SOA through a WDM coupler with typical insertion loss of 0.5–1.0 dB (10–20% loss). This increases the required pump laser output power to 55–60 mW.
2. The wall-plug efficiency of laser diodes varies with wavelength and output power. At 1532.6 nm, efficiencies of 15–25% are typical [47]. Higher efficiency lasers (up to 30%) would reduce the electrical power requirement.
3. Both EP-SOA and OP-SOA configurations require TEC cooling. The reduced thermal load of the OP-SOA (350 mW vs. 540 mW) reduces the TEC power requirement by approximately 25–35%, depending on the TEC efficiency.

The improved gain recovery dynamics of the OP-SOA allow acceptable QF values to be maintained at high bit rates without requiring extremely high peak signal powers [5,47]. This is particularly important because high peak powers would increase nonlinear effects and signal distortion.

A direct quantitative comparison of total energy consumption between OP-SOA and EP-SOA implementations depends on several system-level factors, including pump laser efficiency, coupling losses, thermal management overhead, and photonic integration technology. However, for equivalent logic performance at 120 Gb/s, the OP-SOA-MZI configuration demonstrates approximately 26% lower electrical power consumption and 35% lower thermal load compared with previously reported EP-SOA-based implementations. This suggests that optical pumping may provide a favorable trade-off between signal quality and energy efficiency in future integrated photonic logic systems.

5.5. Detailed Analysis of Table 2

Table 2 provides a comprehensive comparison of all-optical NAND and XNOR gates using various SOA schemes. The table reveals several important trends and trade-offs.

1. **Data Rate versus Quality Factor:** For both NAND and XNOR gates, there is a consistent trade-off between data rate and quality factor. The highest data rates (2000 Gb/s for NAND, 2000 Gb/s for XNOR) are achieved using TPA-enhanced QD-SOA-MZI configurations, but these come at the cost of reduced QF (13 for NAND, 9.8 for XNOR). Conversely, lower data rates (80–160 Gb/s) with EP-QD-SOA-MZI can achieve higher QF values (40 for NAND, 29.72 for XNOR). This trade-off arises because the nonlinear switching mechanisms required for ultra-high-speed operation introduce additional noise and signal distortion.
2. **Impact of Optical Pumping:** The proposed single OP-SOA-MZI achieves QF values of 28.6 (NAND) and 18.7 (XNOR) at 120 Gb/s. These values are significantly higher than those reported for EP-SOA-MZI at comparable data rates ($QF = 10.75$ at 80 Gb/s for NAND, $QF = 10.13$ at 80 Gb/s for XNOR). The improvement is attributed to the accelerated carrier recovery and reduced ASE noise provided by optical pumping. However, the OP-SOA-MZI QF values are lower than those reported for EP-QD-SOA-MZI at similar data rates ($QF = 40$ at 160 Gb/s for NAND, $QF = 29.72$ at 160 Gb/s for XNOR), indicating that quantum-dot active regions still provide superior noise performance when electrical pumping is used.
3. **Comparison of SOA Technologies:** Among the various SOA technologies, QD-SOAs generally provide the highest QF values at a given data rate, followed by PhC-

SOAs, RSOAs, and CR-SOAs. Conventional EP-SOAs without quantum-dot active regions or photonic crystal structures exhibit the lowest QF values. The proposed OP-SOA-MZI, despite using bulk or MQW active regions, achieves QF values competitive with PhC-SOA-MZI ($QF = 18$ at 160 Gb/s for NAND, $QF = 15.83$ at 160 Gb/s for XNOR) and RSOA-MZI ($QF = 18.4$ at 120 Gb/s for NAND, $QF = 19.3$ at 160 Gb/s for XNOR).

4. **Validation Method:** All experimental demonstrations listed in Table 2 are limited to data rates at or below 86.4 Gb/s. The highest experimentally demonstrated data rate for an all-optical logic gate is 86.4 Gb/s (XNOR, EP-SOAs, Kang et al. [62]). This gap between simulation and experiment highlights the challenges in implementing high-speed all-optical logic gates, particularly in terms of timing alignment, thermal management, and phase noise control.

Specific Advantages of the Proposed OP-SOA-MZI Approach:

1. **Reduced System Complexity:** The single OP-SOA-MZI eliminates the need for cascaded MZI stages, reducing component count by 50% compared to conventional approaches that require two cascaded interferometers for NAND and XNOR functions.
2. **Simplified Architecture:** The OP-SOA-MZI uses the same interferometer structure for both logic functions, with only the input signal connections changed. This simplifies photonic integration and reduces fabrication costs.
3. **Energy Efficiency:** Although quantitative analysis requires further work, the OP-SOA approach reduces the electrical injection current required, potentially lowering thermal load and improving energy efficiency compared to EP-SOA designs.
4. **Enhanced Noise Tolerance:** The OP-SOA exhibits reduced ASE noise and improved phase stability compared to EP-SOA designs, as demonstrated by the higher QF values at comparable data rates.
5. **Scalability:** The OP-SOA-MZI approach can be extended to higher data rates by increasing the pump power (as shown in Figure 6) or by using QD-SOA active regions for even faster gain recovery.

5.6. Proposed Experimental Validation and Implementation Challenges

5.6.1. Proposed Experimental Setup

To validate the numerical results presented in this work, we propose an experimental setup consisting of five main subsystems: (1) optical data signal generation, (2) signal inversion and combination, (3) OP-SOA-MZI core, (4) output detection, and (5) performance characterization.

The optical data signals A and B at 120 Gb/s are generated using two independent mode-locked lasers (MLLs) operating at 1544.2 nm, followed by electro-optic modulators (EOMs) driven by pseudorandom binary sequence (PRBS) generators. The PRBS length $N = 2^7 - 1 = 127$ is chosen to provide sufficient pattern length while maintaining practical measurement times. To achieve the required pulse width $\tau_{FWHM} = 1$ ps, each EOM is followed by a pulse compressor, such as a dispersion-decreasing fiber or a nonlinear optical loop mirror (NOLM).

The signal inversion required for the NAND and XNOR configurations is implemented using commercially available all-optical inverters. The inverted signals $\bar{A}$ and $\bar{B}$ are generated using semiconductor optical amplifier-based NOT gates, which operate on the principle of cross-gain modulation (XGM) [42,63]. Alternatively, the inverted signals can be obtained by using the complementary outputs of a differential Mach–Zehnder modulator (MZM), which provides both the data signal and its logical complement simultaneously. This approach simplifies the setup and ensures proper timing alignment.

The inverted signals are combined with the CW probe using wavelength-selective couplers (WSCs). The CW probe is generated by a tunable laser source (TLS) at 1544.2 nm with a linewidth <100 kHz to minimize phase noise. The probe power is split equally using a 50:50 fiber coupler, and each arm is directed through a variable optical attenuator (VOA) to balance the optical power entering each OP-SOA.

The core of the setup is the OP-SOA-MZI, which can be implemented using commercially available SOAs (e.g., from Thorlabs or InPhenix) with modifications for optical pumping. The optical pump source is a high-power laser diode at 1532.6 nm with output power up to 100 mW. The pump is coupled into each SOA using a 1550 nm/1530 nm wavelength-division multiplexer (WDM) coupler. Alternatively, a custom-fabricated OP-SOA chip with integrated pump couplers can be used, as reported in recent demonstrations of optically pumped amplifiers [47,48].

A fixed phase bias Φ_{bias} is introduced in one arm using either: (1) a path length difference realized by adding a length of single-mode fiber (SMF), (2) a thermally controlled phase shifter using a fiber stretcher, or (3) a liquid crystal phase modulator. For precise control, a piezoelectric fiber stretcher with closed-loop feedback can maintain the phase bias within $\pm 1^\circ$.

The output of the MZI is detected using a high-speed photodetector (60 GHz bandwidth) followed by a sampling oscilloscope (e.g., Keysight DCA-X with 80 GHz optical module). The measured output waveform and eye diagram are used to extract the quality factor QF according to Equation (13). The bit error rate (BER) can be directly measured using a BER tester ($BERT$) to verify the relationship between QF and BER given by Equation (14).

5.6.2. Feasibility Analysis

The proposed experimental setup is feasible using currently available commercial components. All key components—mode-locked lasers at 1544.2 nm, EOMs with 100+ GHz bandwidth, PRBS generators operating at 120 Gb/s, SOAs with 1 ps gain recovery, and 60+ GHz photodetectors—are commercially available from vendors such as Thorlabs, Newport, Keysight, and Finisar.

The optical pumping approach has been experimentally validated in previous studies. Agrawal and Dutta [48] demonstrated optical pumping in SOAs, reporting gain recovery times <10 ps. Winzer and Essiambre [47] showed that optical pumping reduces the ASE noise figure by approximately 3 dB compared to high-current electrical pumping at the same gain level. These experimental results support the feasibility of the proposed OP-SOA-MZI configuration.

The main feasibility challenge is the simultaneous coupling of three optical signals (pump, probe, and data) into a single SOA while maintaining low insertion loss and high isolation between signals. This requires careful design of the WDM couplers and anti-reflection coatings on the SOA facets. The use of bulk SOAs with angled facets and integrated spot-size converters can reduce coupling losses to <2 dB per port.

5.6.3. Implementation Challenges

Three primary challenges must be addressed for successful experimental implementation:

1. At 120 Gb/s (bit period $T = 8.33$ ps), the pulse width $\tau_{FWHM} = 1$ ps, and the timing alignment between the data signals A and B must be maintained to better than ± 0.1 ps ($\approx 10\%$ of the pulse width). This requires a precision delay line with <10 fs resolution and active feedback stabilization. Electronic delay lines (e.g., from Colby Instruments) with ps-level resolution can be used in conjunction with a microwave phase shifter for fine adjustment. The timing jitter of the MLLs must be <50 fs to ensure

- reliable eye diagram measurements. Clock recovery circuits and optical synchronization units can be employed to lock the two MLLs to a common reference clock.
2. The OP-SOA dissipates significant heat from the optical pump, with estimated thermal load of approximately 50–100 mW for $P_p = 50$ mW. Active temperature control using thermoelectric coolers (TECs) with PID controllers is required to maintain the SOA chip temperature within ± 0.1 °C. The phase bias also fluctuates with temperature; therefore, the entire MZI should be mounted on a temperature-stabilized optical bench with ± 0.01 °C stability.
 3. As shown in Figure 8, phase noise degrades the QF , particularly for the XNOR gate. To achieve the phase noise level of $\Phi_{\text{noise}} \leq 5.2 \times 10^{-14}$ rad²/Hz required for $QF > 6$, the laser sources must have linewidths < 100 kHz. Commercial tunable lasers (e.g., Agilent 8164A) meet this specification. Additionally, the MZI should be enclosed in a vibration-isolated housing and actively stabilized using a feedback control loop that monitors the output power and adjusts the phase bias.

5.6.4. Comparison with Experimentally Demonstrated Systems

Several experimental demonstrations provide context for our numerical results. Kang et al. [62] experimentally demonstrated XOR and XNOR operations at 86.4 Gb/s using a pair of SOA-MZIs, achieving clear eye openings but without reporting quantitative QF values. Son et al. [57] demonstrated XOR, NOR, and NAND gates using conventional SOAs at 10 Gb/s, showing that EP-SOAs can realize basic logic functions at lower data rates. Dong et al. [38] reported all-optical signal processing based on single SOAs and optical filtering at 40 Gb/s, demonstrating the feasibility of compact SOA-based logic.

Our numerical results at 120 Gb/s represent a significant speed increase over these experimental demonstrations. The proposed OP-SOA-MZI is expected to achieve the simulated QF values (28.6 for NAND, 18.7 for XNOR) if the experimental challenges identified above are properly addressed. The key advantages of the OP-SOA approach—accelerated carrier recovery and reduced pattern effects—are experimentally verifiable by comparing the output eye diagrams of OP-SOA-MZI and EP-SOA-MZI configurations under identical conditions.

5.7. Distinctive Advantages of the Proposed OP-SOA-MZI Architecture

The proposed single OP-SOA-MZI architecture for NAND and XNOR logic gates offers several distinctive advantages over previously reported approaches. These advantages are summarized below:

5.7.1. Reduced System Complexity

Conventional implementations of both NAND and XNOR functions using SOA-MZI structures require two cascaded interferometers: the first MZI generates an intermediate function such as AND or XOR, and the second MZI, configured as a logical inverter, produces the final output [49,50]. This cascading doubles the component count, increases optical insertion loss, and complicates photonic integration. The proposed single OP-SOA-MZI directly realizes the NAND and XNOR functions without requiring a second MZI stage. While the external inverters for generating $\bar{A}$ and $\bar{B}$ add to the system complexity, the elimination of the second MZI stage reduces optical loss by approximately 3–5 dB and simplifies bias control.

5.7.2. Simplified Architecture

The OP-SOA-MZI uses the same interferometer structure for both logic functions, with only the input signal connections changed. For the NAND gate, the upper arm receives the combined $\bar{A} + \bar{B}$ signal while the lower arm receives no data. For the XNOR

gate, the upper arm receives $\bar{A}$ and the lower arm receives B. This architectural simplicity facilitates photonic integration and reduces fabrication costs, as a single-chip design can be configured for different logic functions.

5.7.3. Energy Efficiency

As discussed in Section 5.4, the OP-SOA approach reduces electrical power consumption by approximately 26% compared to EP-SOA configurations at equivalent performance levels. The optical pumping mechanism eliminates the high electrical injection currents required for EP-SOAs, reducing Joule heating and thermal management requirements.

5.7.4. Enhanced Noise Tolerance

The OP-SOA exhibits reduced ASE noise and improved phase stability compared to EP-SOA designs. The optical pumping scheme provides faster carrier recovery and more stable gain, resulting in higher QF values at comparable data rates. As shown in Figures 8 and 9, the OP-SOA-MZI configuration maintains QF above 6 ($BER < 10^{-9}$) for higher phase noise and ASE noise levels than EP-SOA-based implementations.

5.7.5. Scalability

The OP-SOA-MZI approach can be extended to higher data rates by increasing the pump power (as shown in Figure 6) or by using QD-SOA active regions for even faster gain recovery. The optical pumping mechanism is compatible with various active region designs, including bulk, MQW, and QD structures. This scalability makes the OP-SOA-MZI platform suitable for future high-speed photonic integrated circuits.

5.7.6. Limitations and Trade-Offs

The proposed OP-SOA-MZI approach has the following limitations compared to alternative technologies:

1. The maximum data rate for the XNOR gate is approximately 155 Gb/s (compared to 175 Gb/s for the NAND gate), which is lower than the 2000 Gb/s demonstrated by TPA-QD-SOA-MZI configurations. However, the QF at 120 Gb/s is significantly higher than the TPA-QD-SOA-MZI QF at 2000 Gb/s (18.7 vs. 9.8 for XNOR).
2. The NAND gate requires two external inverters, and the XNOR gate requires one external inverter. These inverters add to the system complexity and optical loss.
3. The OP-SOA requires an external optical pump laser, which adds to the system cost and complexity. The pump laser must be temperature-stabilized and wavelength-locked to the SOA absorption peak.

The MZI configuration is sensitive to phase noise, as shown in Figure 8. Active phase stabilization is required for reliable operation.

5.8. Comparison with EP-QD-SOA-MZI Approach

The reviewer correctly notes that EP-QD-SOA-MZI schemes can achieve higher data rates and QF values compared to the single OP-SOA-MZI approach. However, the OP-SOA-MZI approach offers several distinct advantages that make it attractive for practical implementation:

5.8.1. Fabrication Complexity and Cost

QD-SOAs require sophisticated epitaxial growth techniques such as molecular beam epitaxy (MBE) or metal–organic chemical vapor deposition (MOCVD) with precise control of quantum dot density, size, and uniformity [11,12,46,50]. The fabrication process is

significantly more complex and expensive than that of bulk or MQW SOAs, which are the active regions used in the OP-SOA approach. The OP-SOA can be implemented using standard InGaAsP/InP bulk or MQW structures that are commercially available and well-characterized.

5.8.2. Temperature Sensitivity

QD-SOAs exhibit temperature-dependent gain and phase characteristics due to the temperature sensitivity of the quantum dot energy levels [46]. The gain peak shifts with temperature at a rate of approximately 0.3–0.5 nm/°C, requiring precise temperature control. Bulk and MQW SOAs used in the OP-SOA approach have broader gain spectra and are more temperature-tolerant, simplifying thermal management.

5.8.3. Polarization Dependence

QD-SOAs often exhibit residual polarization sensitivity due to the anisotropic shape of the quantum dots [46,50]. This polarization dependence can affect the interferometric switching contrast. The OP-SOA approach using bulk or MQW active regions can be designed for polarization-insensitive operation by using strained quantum wells or bulk active regions with optimized waveguide geometry.

5.8.4. Availability and Maturity

EP-QD-SOA-MZI structures are still primarily in the research and development phase, with limited commercial availability. In contrast, bulk and MQW SOAs are mature technologies with widespread commercial availability. The OP-SOA approach can be implemented using commercially available components, accelerating the path to practical deployment.

5.8.5. Trade-Off Summary

The OP-SOA-MZI approach offers a practical compromise between performance and manufacturability (Table 3). While EP-QD-SOA-MZI schemes achieve higher performance metrics, the OP-SOA-MZI approach is more accessible, cost-effective, and suitable for rapid deployment in practical photonic systems. The key contribution of this work is not to outperform QD-SOA-based schemes in terms of maximum data rate or QF , but to demonstrate that a single OP-SOA-MZI can achieve high-quality NAND and XNOR operations using commercially available components, with reduced system complexity and improved energy efficiency compared to EP-SOA implementations.

Table 3. Comparison of key characteristics between the proposed OP-SOA-MZI and EP-QD-SOA-MZI approaches for all-optical NAND and XNOR logic gates.

Aspect	OP-SOA-MZI	EP-QD-SOA-MZI
Active region	Bulk/MQW (mature)	QD (advanced)
Fabrication complexity	Low	High
Fabrication cost	Low	High
Temperature sensitivity	Moderate	High
Polarization sensitivity	Low (with design)	Moderate
Commercial availability	High	Limited
Maximum data rate	~175 Gb/s	~2000 Gb/s
QF at 120 Gb/s	28.6 (NAND), 18.7 (XNOR)	40 (NAND), 29.72 (XNOR)

6. Conclusions

This work investigated all-optical NAND and XNOR logic gates using a single optically pumped semiconductor optical amplifier Mach–Zehnder interferometer (OP-SOA-MZI) at 120 Gb/s. The study demonstrated that both logic functions can be realized with a single OP-SOA-MZI without requiring an additional cascaded inverting stage. The NAND gate achieved a quality factor of 28.6, while the XNOR gate achieved a quality factor of 18.7 at the same data rate.

The dependence of QF on five operational parameters was systematically analyzed. The absorption coefficient (α_p) exhibited an optimum at 5000 m⁻¹ for both gates. The pump power (P_p) analysis showed that both gates achieved maximum QF at 50 mW, with the NAND gate exceeding $QF = 6$ for P_p between 25 mW and 65 mW and the XNOR gate between 28 mW and 60 mW. The data rate analysis confirmed that the NAND gate maintained QF above 6 up to approximately 175 Gb/s, while the XNOR gate maintained QF above 6 only up to approximately 155 Gb/s. The phase noise (Φ_{noise}) analysis showed that the NAND gate maintained QF above 6 up to 6.3×10^{-14} rad²/Hz, while the XNOR gate maintained QF above 6 only up to 5.2×10^{-14} rad²/Hz. The amplified spontaneous emission noise power (P_{ASE}) analysis revealed that the NAND gate tolerated higher ASE noise levels (up to 3.8 mW) than the XNOR gate (up to 2.9 mW).

The OP-SOA-MZI configuration proved effective for high-speed all-optical logic operations at 120 Gb/s. The NAND gate demonstrated superior performance across all examined parameters due to its simpler modulation scheme. The XNOR gate, while showing lower QF values, still met the $BER = 10^{-9}$ requirement within its optimal operating ranges. The reduced system complexity (single MZI instead of two cascaded stages) and improved energy efficiency (approximately 26% lower electrical power consumption compared to EP-SOA) represent the main contributions of this work.

This work is based on numerical simulations; experimental validation is required to confirm the predicted performance. The external inverters required for generating $\bar{A}$ and $\bar{B}$ add to the system complexity. The analysis assumes ideal component behavior; practical limitations such as component aging, temperature drift, and fabrication tolerances may degrade the QF .

Experimental validation of the simulated results using the setup described in Section 5.6. Monolithic integration of the OP-SOA-MZI structure on InP or silicon photonic platforms. Extension to higher data rates using QD-SOA active regions or optimized pumping schemes.

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Abbreviations

The following abbreviations are used in this manuscript:

ASE	Amplified Spontaneous Emission
BER	Bit Error Rate
CD	Carrier Depletion
CH	Carrier Heating
CMOS	Complementary Metal-Oxide-Semiconductor
CR-SOA	Carrier Reservoir Semiconductor Optical Amplifier
DI	Delayed Interferometer
EP-SOA	Electrically Pumped Semiconductor Optical Amplifier
FWM	Four-Wave Mixing
ISI	Intersymbol Interference
MZI	Mach–Zehnder Interferometer
NAND	NOT AND (logic gate)
NOR	NOT OR (logic gate)
OBPF	Optical Bandpass Filter
OC	Output Coupler
OEO	Optical-to-Electrical-to-Optical
OP-SOA	Optically Pumped Semiconductor Optical Amplifier
PhC-SOA	Photonic Crystal Semiconductor Optical Amplifier
PRBS	Pseudorandom Binary Sequence
QD-SOA	Quantum Dot Semiconductor Optical Amplifier
QF	Quality Factor
RSOA	Reflective Semiconductor Optical Amplifier
SHB	Spectral Hole Burning
SOA	Semiconductor Optical Amplifier
TPA	Two-Photon Absorption
WDM	Wavelength-Division Multiplexing
WSC	Wavelength-Selective Coupler
XGM	Cross-Gain Modulation
XOR	Exclusive OR (logic gate)
XNOR	Exclusive NOR (logic gate)
XPM	Cross-Phase Modulation

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