

Article

A Cascaded Super-Twisting Sliding Mode Control Strategy for Fast Voltage Regulation of SEPICs

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Abstract

In this paper, a cascaded Super Twisting Sliding Mode Control (ST-SMC) is proposed for voltage control of SEPICs. The theoretical analysis shows that the duty cycle affects the output voltage through the internal converter dynamics, including the inductor currents and the coupling capacitor. Therefore, the use of the cascaded control approach is more suitable for voltage regulation of SEPIC converters, consistent with existing studies. In this paper, the input inductor's reference current is generated based on the output voltage error by using the outer-loop ST-SMC. The input inductor current control is achieved by the inner loop ST-SMC method. Thus, both input current and output voltage control are achieved simultaneously. The duty cycle is generated as a result of this cascaded control structure, and the switching signal is generated based on PWM. The main objective of the proposed cascaded ST-SMC method is to improve the dynamic performance of the output voltage control. The effectiveness of the proposed method is investigated by experimental studies under variations in the input voltage, load resistance, and reference voltage. The proposed cascaded ST-SMC method is compared with existing PI-SMC, PI-MPC, and cascaded terminal ST-SMC approaches. Compared to existing methods, a significant improvement is achieved, especially in terms of dynamic response.

Keywords: power electronics; super-twisting sliding mode control; SEPIC; cascaded control; voltage regulation

1. Introduction

The historical development of DC–DC power converters has been closely associated with the increasing demand for efficient and flexible energy conversion systems in industrial electronics, renewable energy applications, electric vehicles, aerospace systems, and portable electronic devices [1,2]. Early studies in power electronics primarily focused on conventional converter topologies such as Buck, Boost, and Buck–Boost converters due to their simple structures and ease of implementation [3,4]. However, these classical converters suffer from several limitations, including inverted output polarity, discontinuous input current, high ripple content, and restricted voltage conversion capability under wide operating conditions [5]. As modern applications began requiring converters capable of both step-up and step-down voltage regulation while maintaining non-inverted output polarity and low input current ripple, more advanced converter structures emerged [6]. Among these topologies, the Single-Ended Primary Inductor Converter (SEPIC) gradually became one of the most attractive solutions because of its capability to

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provide both buck and boost operation while preserving the same polarity between input and output voltages [3,4,7,8]. In addition, SEPICs exhibit continuous input current characteristics, making them highly suitable for renewable energy systems, photovoltaic interfaces, battery-powered applications, LED drivers, and smart-grid systems operating under varying environmental and load conditions. Nevertheless, despite these advantages, SEPICs possess inherently nonlinear fourth-order dynamics and strong coupling among state variables, making their control significantly more challenging than classical converter topologies [6,9].

In addition to their nonlinear fourth-order dynamics, SEPICs present several control challenges that distinguish them from conventional DC–DC converters [8]. The duty ratio affects the output voltage through the internal current and energy-transfer dynamics rather than through a direct single-step relationship. Moreover, the strong coupling between the input current and output voltage, together with transitions between buck and boost operating modes, increases controller-design complexity. Practical implementations are further affected by parameter uncertainties, load disturbances, parasitic components, and measurement noise, all of which may deteriorate transient performance and voltage regulation accuracy. Therefore, advanced nonlinear control strategies with strong robustness and fast dynamic response are highly desirable for SEPIC applications [9–12].

Recent review studies have highlighted that the rapid evolution of DC–DC converter technologies has been accompanied by remarkable advances in control methodologies, ranging from conventional linear regulators to advanced nonlinear, adaptive and observer-based control strategies. These developments aim to improve converter efficiency, robustness, disturbance rejection capability, and dynamic performance under increasingly demanding operating conditions [2,13].

Initially, conventional linear controllers such as Proportional–Integral (PI) and PID regulators were widely employed for SEPICs because of their simple implementation and low computational requirements [14]. However, linear control methods generally provide satisfactory performance only around nominal operating conditions and often exhibit poor robustness against parameter uncertainties, load variations, and external disturbances in nonlinear converter systems. In practical applications, these limitations frequently result in overshoot, oscillatory behavior, slow transient response, and degraded voltage regulation performance [14]. To overcome these limitations, advanced nonlinear and optimization-based control methods were introduced into DC–DC converter applications [13]. Model Predictive Control (MPC) emerged as an attractive solution due to its capability to optimize converter behavior while considering dynamic constraints and multi-variable interactions [15–17]. Although MPC can provide fast transient response and accurate regulation performance, its dependence on accurate system models and high computational complexity limit its practical applicability in fast-switching power electronic systems [13,15,18]. Non-cascaded voltage control structures can provide satisfactory performance for lower-order converters such as buck converters. In [19], the voltage tracking error and the inductor-current dynamics are combined in a unified second-order state-space model, and the duty ratio is generated directly. This structure does not require a separate outer voltage loop and inner current loop. In the SEPIC, the energy transfer from input to output occurs through the inductors and the coupling capacitor. Although non-cascaded control can also regulate the output voltage of a SEPIC, a cascaded structure can help mitigate oscillatory transients associated with the coupled input–output dynamics.

As an alternative, Sliding Mode Control (SMC) became widely recognized as one of the most robust nonlinear control approaches for power electronic converters because of its strong immunity against disturbances, parameter uncertainties, and modeling inaccuracies.

racies [11,17,20]. Conventional first-order SMC forces the system states toward a predefined sliding surface, providing fast transient response and improved robustness. However, the discontinuous nature of classical SMC introduces the well-known chattering phenomenon, which increases switching losses, generates electromagnetic interference, and may degrade converter lifetime and efficiency [20]. To reduce chattering while preserving robustness properties, higher-order sliding mode techniques were later developed. In particular, the Super-Twisting Sliding Mode Control (ST-SMC) algorithm generates continuous control action while maintaining finite-time convergence and strong disturbance rejection capability [21–23]. These characteristics significantly improved the practical applicability of sliding mode techniques in high-frequency switching converters. Consequently, ST-SMC rapidly attracted attention in modern DC–DC converter control applications requiring high dynamic performance and reduced oscillatory behavior. Different variants of sliding mode control have been developed to overcome the limitations of classical SMC while preserving its inherent robustness. Integral Sliding Mode Control (ISMC) eliminates the reaching phase and improves steady-state accuracy, whereas Terminal Sliding Mode Control (TSMC) guarantees finite-time convergence through nonlinear sliding surfaces. Fast Terminal Sliding Mode Control (FTSMC) further accelerates convergence but often requires more complex controller design and parameter tuning. Adaptive SMC methods improve robustness against uncertain system parameters by adjusting controller gains online, whereas higher-order approaches such as ST-SMC reduce chattering while maintaining finite-time convergence and continuous control action. Consequently, selecting an appropriate sliding mode strategy involves balancing robustness, implementation complexity, dynamic performance, and chattering reduction according to application requirements [11,23,24].

In parallel with the evolution of control algorithms, researchers also recognized that the structural organization of the controller substantially influences converter performance. Due to the indirect relationship between the duty cycle and output voltage in SEPICs, cascaded control architectures became increasingly popular [11]. In such configurations, an outer voltage loop generates the reference signal for an inner current loop, enabling improved decoupling between voltage and current dynamics, enhanced transient response, and disturbance rejection capability. Cascaded structures also simplify the regulation of nonlinear converter dynamics by separating slow voltage dynamics from fast current dynamics [25]. Cascaded converter systems have also been investigated at the hardware-topology level. In [26], a distributed multimode control strategy is proposed for series-connected DC–DC converter submodules in a medium-voltage grid-connected PV system. Recent studies have further extended nonlinear control methods by integrating adaptive and observer-based mechanisms into SEPIC systems. Adaptive Sliding Mode Control (ASMC) techniques dynamically adjust controller gains according to operating conditions, thereby reducing dependence on conservative uncertainty bounds while improving disturbance rejection and reducing chattering [24]. Recent observer-based adaptive SMC frameworks further enhance control performance by integrating adaptive gain tuning with disturbance estimation mechanisms, resulting in improved robustness and dynamic response under uncertain operating conditions [24,27]. Similarly, Cascaded Terminal Super-Twisting Sliding Mode Control (CST-SMC) approaches have demonstrated fast dynamic response, finite-time convergence, and enhanced robustness for SEPICs operating under severe parameter uncertainties and load transients [11]. The outer voltage loop generates the input inductor current reference, while the inner current loop generates the duty ratio. However, ref. [11] employs a nonlinear terminal sliding surface containing the current error derivative and a fractional-power term in the inner loop. Consequently, its implementation requires four ST-SMC gains and two additional terminal-surface parameters.

Recently, disturbance-observer-based composite sliding-mode control strategies have been investigated to improve voltage regulation under time-varying disturbances. In [28], a finite-time disturbance observer is combined with a second-order sliding-mode controller for a DC–DC buck converter. The observer estimates lumped disturbances arising from load variations, input-voltage fluctuations, and parameter uncertainties, and the estimated disturbance is incorporated into the control law as a compensation term. This approach can reduce the switching gain required to handle large disturbances and improve disturbance rejection. However, it also introduces additional observer dynamics and observer-gain selection. In contrast, the cascaded ST-SMC proposed in this study is a pure feedback strategy for a fourth-order SEPIC and does not employ explicit disturbance estimation or compensation.

Moreover, discrete-time sliding mode control methods have been proposed to overcome the variable switching frequency limitation associated with analog SMC implementations. The model-based Discrete-Time Sliding Mode Control (DSMC) method in [29] enables fixed switching frequency operation for SEPIC and Ćuk converters supplying HBLEDs and evaluates their power factor and total harmonic distortion performance. A simulation-based comparative study in [30] also shows that an SMC-based SEPIC controller can provide improved voltage regulation and recovery time compared with a conventional PID controller under input voltage, reference voltage and load variations.

Recently, composite control strategies combining sliding mode control with disturbance estimation and feedforward compensation have emerged as an effective solution for enhancing disturbance rejection capability in power electronic converters. By estimating lumped disturbances through disturbance observers (DOs), extended state observers (ESOs), or similar observer-based techniques, these approaches compensate for external disturbances and model uncertainties before they propagate through the feedback loop, thereby improving transient response and steady-state accuracy. Although these composite control frameworks generally introduce additional observer design and parameter tuning requirements, they have demonstrated disturbance rejection capability and enhanced dynamic performance for converter systems operating under severe parameter uncertainties and rapidly varying operating conditions [31,32].

In addition to second-order and discrete-time SMC structures, several studies have investigated reduced-order and hybrid sliding mode approaches to simplify implementation complexity while maintaining robust converter performance. Combined PI-SMC and reduced-order SMC techniques have shown improved steady-state regulation, reduced computational burden, and enhanced adaptability to changing operating conditions [33,34]. Furthermore, PWM-based Integral Sliding Mode Control (ISMC) strategies have demonstrated excellent transient response and stability characteristics in high-frequency SEPIC applications by integrating integral action into the sliding surface design and employing state-space averaging techniques for accurate equivalent control derivation [35].

Despite these advances, the existing SMC-based control methods for SEPICs do not employ standard non-terminal ST-SMC in both the outer voltage and inner current loops. Conventional ST-SMC has previously been applied using a single-loop voltage-control structure, whereas the cascaded method in [11] employs a nonlinear terminal sliding surface in the inner current loop. This terminal formulation requires four ST-SMC gains together with two additional terminal-surface parameters. Therefore, to the best of the authors' knowledge, a cascaded SEPIC control structure employing simple error-based sliding surfaces and standard non-terminal ST-SMC in both loops has not yet been experimentally investigated. Developing such a structure with fewer tuning parameters while retaining fast voltage regulation and cascaded voltage–current control constitutes the main research motivation of this study.

Motivated by this research gap, this paper proposes a cascaded Super-Twisting Sliding Mode Control (ST-SMC) strategy for voltage control of SEPICs. The outer-loop ST-SMC generates the input-inductor-current reference from the output voltage error, whereas the inner loop ST-SMC generates the duty ratio from the input current error. Unlike [11], the proposed method employs simple error-based sliding surfaces in both loops and does not require a nonlinear terminal sliding surface. This reduces the number of controller coefficients from six to four and results in different closed loop current error dynamics. The experimental results demonstrate shorter transient times than those reported in [11] under load and reference voltage variations. The proposed method is also experimentally evaluated under input voltage variations, buck and boost load conditions, a boost to buck transition, reference voltage changes, and start-up operation.

The main contributions of this study can be summarized as follows:

- (i) Development of, to the best of the authors' knowledge, the first cascaded standard non-terminal ST-SMC implementation for voltage regulation of a SEPIC, using simple error-based sliding surfaces in both the outer voltage and inner current loops.
- (ii) Reduction of the controller coefficients from six in the cascaded terminal ST-SMC method in [11] to four by eliminating the additional terminal surface parameters while retaining cascaded voltage–current regulation.
- (iii) Quantitative comparison with PI-SMC, PI-MPC, and cascaded terminal ST-SMC in terms of tuning requirements, sensor requirements, settling time, and voltage deviation.
- (iv) Experimental validation under load changes in buck and boost modes, input voltage variations, a boost to buck transition, reference voltage changes, and start-up operation.

2. Modeling of SEPIC

The circuit diagram of the SEPIC is depicted in Figure 1. The input side inductor current (i_{L1}), capacitor voltage (V_{C1}), output side inductor current (i_{L2}), and capacitor voltage (V_{C2}) are the state variables of this fourth-order system. The charge and discharge states of these inductors and capacitors depend on the switch (S) position. It is worth noting that the output capacitor voltage equals the output voltage (V_O) in both switch positions (ON or OFF).

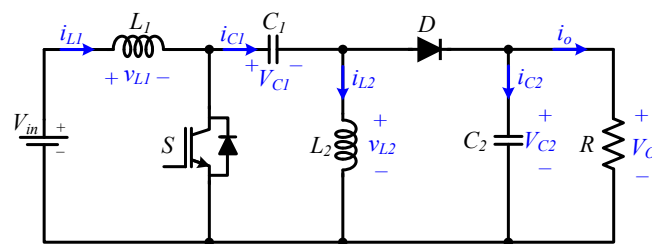


Figure 1. Circuit diagram of the SEPIC.

The system variables for the ON position of S can be defined as follows:

$$v_{L1} = V_{in} \quad (1)$$

$$v_{L2} = -V_{C1} \quad (2)$$

$$i_{C1} = i_{L2} \quad (3)$$

$$i_{C2} = -i_o \quad (4)$$

where v_{L1} and v_{L2} denote the voltage of L_1 and L_2 inductances, respectively. i_{C1} and i_{C2} represent the current of C_1 and C_2 , respectively.

The system variable equations for the OFF position are as follows:

$$v_{L1} = V_{in} - V_{C1} - V_o \quad (5)$$

$$v_{L2} = V_o \quad (6)$$

$$i_{C1} = i_{L1} \quad (7)$$

$$i_{C2} = i_{L1} - i_{L2} - i_o \quad (8)$$

Under ideal CCM steady-state operating conditions, $V_{C1} \approx V_{in}$. Hence, inductor voltage in (5) can be simplified as $v_{L1} = -V_o$. Now, the generalized derivative equations based on the switching state (S) can be obtained by combining the above equations as

$$\frac{di_{L1}}{dt} = \frac{1}{L_1} [S V_{in} - V_o(1 - S)] \quad (9)$$

$$\frac{di_{L2}}{dt} = \frac{1}{L_2} [V_o(1 - S) - S V_{C1}] \quad (10)$$

$$\frac{dV_{C1}}{dt} = \frac{1}{C_1} [S i_{L2} + (1 - S)i_{L1}] \quad (11)$$

$$\frac{dV_{C2}}{dt} = \frac{1}{C_2} [(1 - S)(i_{L1} - i_{L2}) - i_o] \quad (12)$$

Also, the averaged model can be derived as a function of the duty cycle ($d \in [d_{min}, d_{max}]$). The voltage gain of the SEPIC can be obtained according to the average voltage across L_1 being zero for periodic operation as follows:

$$\frac{V_o}{V_{in}} = \frac{d}{(1-d)} \quad (13)$$

It can be concluded that the voltage gain depends on the duty cycle. However, the switching state in (12) is multiplied only by the inductor currents. Therefore, the duty cycle affects the output voltage through the internal current and energy dynamics of the SEPIC. Since the energy transfer from the input side to the output side involves the inductors and the coupling capacitor (C_1), the voltage and current dynamics are coupled. Therefore, controlling the output voltage by a cascaded control structure is more effective for mitigating undesired oscillations during transients.

3. Design of Cascaded Super Twisting Sliding Mode Control Method

The main control objective in this paper is to regulate the SEPIC's output voltage. According to (13), the output voltage control can be achieved directly from an averaged (steady-state) perspective. However, as discussed in the previous section, the control input affects V_o through the inductor current dynamics. Therefore, nonlinear cascaded control structures provide more effective voltage regulation for SEPICs. Considering the inherent coupling between input and output power flow in the converter, the input inductor current (i_{L1}) and output voltage (V_o) are selected as the control variables of the inner and outer loops, respectively.

3.1. Design of Outer Control Loop

The objective for the outer control loop is to regulate the output voltage. The sliding surface function (σ_v) can be written as the difference between the measured and reference (V_o^*) output voltages as follows:

$$\sigma_v = V_o - V_o^* \quad (14)$$

Design of the sliding control method based only on this surface function leads to undesired high-frequency ripples at the controller output, which is known as chattering. Chattering minimization or less-chattering-based SMC techniques exist in the literature. Among these techniques, each approach has its own unique advantages and disadvantages as discussed in the introduction. The super twisting approach effectively reduces the chattering. Super twisting SMC function that generates the input inductor current reference can be written as follows:

$$i_{L1}^* = -\alpha_v |\sigma_v|^{0.5} \text{sign}(\sigma_v) - \beta_v \int \text{sign}(\sigma_v) dt \quad (15)$$

where α_v and β_v denote the controller coefficients. The tuning of these coefficients is discussed in the next subsection.

3.2. Design of Inner Control Loop

The inner loop control aim is to regulate the input inductor current whose reference is generated by the outer loop. Similar to the voltage control loop, the sliding surface function for current control can be defined by

$$\sigma_i = i_{L1} - i_{L1}^* \quad (16)$$

The control action is obtained at the output of the inner loop control. The duty cycle can be obtained by the super-twisting SMC technique as follows:

$$d = -\alpha_i |\sigma_i|^{0.5} \text{sign}(\sigma_i) - \beta_i \int \text{sign}(\sigma_i) dt \quad (17)$$

where α_i and β_i denote the controller coefficients of the inner loop. In the ST-SMC method, β is effective in reducing the steady-state error while α affects the dynamic response of the controller [36]. By considering these facts, the controller gains were tuned under two operating conditions: steady state and a step change in the load resistance, which is the most common transition scenario in practice. α_i and α_v values are selected to be small and the β_v and β_i are increased step by step, observing the steady-state error. The values (β_v and β_i) that converge to the steady-state error of approximately zero are selected as the appropriate coefficient values. The same procedure is repeated for determining α_i and α_v values under a repeating load step scenario. It is worth noting that the value of α_i is relatively small because it is effective in reducing chattering.

The block diagram of the proposed ST-SMC method is depicted in Figure 2. The output voltage error is applied to the outer-loop ST-SMC method, which generates the input inductor current reference (i_{L1}^*). The inner loop ST-SMC method is composed to control the input inductor current. The duty cycle (d) signal is generated by the inner loop controller and applied to PWM. Thus, a cascaded control structure is composed, and both voltage and current controls are achieved simultaneously.

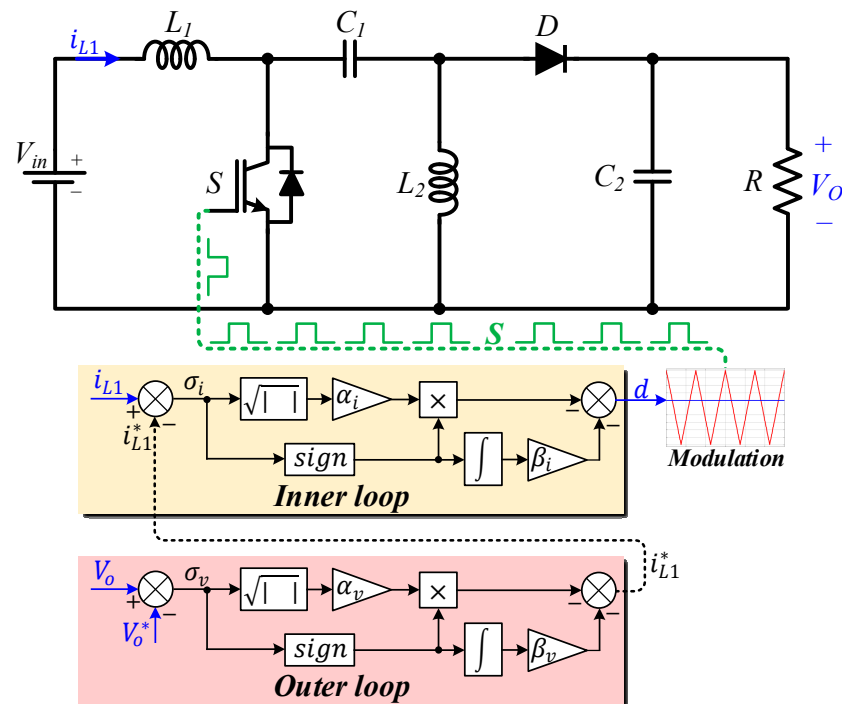


Figure 2. Block diagram of the proposed ST-SMC method.

3.3. Stability Analysis

The stability of the SMC can be analyzed by the Lyapunov function. Since both the outer and inner loops are designed using the same technique, the stability proof of the ST-SMC method is presented. In a general form, the stability is proved if the following three conditions are satisfied [37]:

$$V > 0 \text{ for } (\sigma_j \neq 0)$$

$$V \rightarrow \infty \text{ for } (|\sigma_j| \rightarrow \infty) \quad (18)$$

$$\dot{V} < 0 \text{ for all } (\sigma_j \neq 0)$$

where V represents the Lyapunov function and $\sigma_j, j \in \{v, i\}$. The function can be defined as follows:

$$V = 2\beta_j |\sigma_j| + \frac{1}{2} (\beta_j \int \text{sign}(\sigma_j) dt)^2 + \frac{1}{2} [\alpha_j |\sigma_j|^{0.5} \text{sign}(\sigma_j) + \beta_j \int \text{sign}(\sigma_j) dt]^2 \quad (19)$$

The auxiliary terms can be defined by (20) and (21) to obtain the Lyapunov function in quadratic form.

$$\xi_{1j} = |\sigma_j|^{0.5} \text{sign}(\sigma_j), \quad \xi_{1j}^2 = |\sigma_j| \quad (20)$$

$$\xi_{2j} = -\beta_j \int \text{sign}(\sigma_j) dt, \quad -\xi_{2j} = \beta_j \int \text{sign}(\sigma_j) dt \quad (21)$$

Substituting the definitions in (20) and (21) into (19) gives

$$V = 2\beta_j \xi_{1j}^2 + \frac{1}{2} \xi_{2j}^2 + \frac{1}{2} [\alpha_j \xi_{1j} - \xi_{2j}]^2 = \xi_{1j}^2 \left(2\beta_j + \frac{1}{2} \alpha_j^2 \right) - \alpha_j \xi_{1j} \xi_{2j} + \xi_{2j}^2 \quad (22)$$

Hence, the Lyapunov function in (19) can be written in quadratic form as follows [37]:

$$V = \xi_j^T P \xi_j \quad (23)$$

where

$$P = \begin{bmatrix} 2\beta_j + 0.5\alpha_j^2 & -0.5\alpha_j \\ -0.5\alpha_j & 1 \end{bmatrix}, \quad \xi_j = \begin{bmatrix} |\sigma_j|^{0.5} \text{sign}(\sigma_j) \\ -\beta_j \int \text{sign}(\sigma_j) dt \end{bmatrix} \quad (24)$$

Since P is positive definite for $\alpha_j > 0$ and $\beta_j > 0$, the Lyapunov function is also positive definite. Also, V is radially unbounded. Hence, the first two conditions in (18) are satisfied.

The derivative of the quadratic function can be written as follows:

$$\dot{V} = -\frac{1}{|\sigma_j|^{0.5}} \xi_j^T Q_j \xi_j \quad (25)$$

where

$$Q_j = \begin{bmatrix} \alpha_j \beta_j + 0.5 \alpha_j^3 & -0.5 \alpha_j^2 \\ -0.5 \alpha_j^2 & 0.5 \alpha_j \end{bmatrix} \quad (26)$$

It is evident that the positive definition of α_j and β_j will result in $Q_j > 0$. Hence, the Lyapunov derivative in (25) is negative definite ($\dot{V} < 0$) for all $\sigma_j \neq 0$ and the third condition in (18) is also satisfied.

4. Experimental Results

The effectiveness of the proposed control strategy is investigated through experimental studies performed on a SEPIC prototype. The experimental setup is shown in Figure 3. The control method is implemented on a rapid prototyping system (dSPACE MicroLabBox). HAS 50-S and LV 25-P sensors from LEM are used as current and voltage transducers, respectively. Experimental setup and controller parameters are given in Table 1.

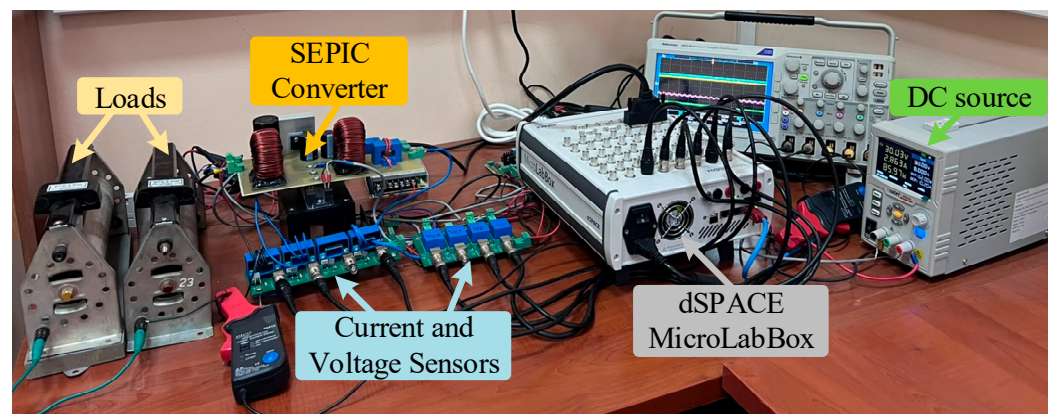


Figure 3. Experimental setup.

Table 1. Experimental setup and control parameters.

Parameters	Symbol	Value
Input voltage	V_{in}	20 V–60 V
Reference voltage	V_o^*	30 V–50 V
Load resistance	R	10 Ω and 20 Ω
Inductances	L_1 and L_2	0.8 mH and 0.8 mH
Capacitances	C_1 and C_2	150 μ F and 300 μ F
Outer ST-SMC coefficients	α_v and β_v	0.7, 500
ST-SMC coefficients	α_i and β_i	0.16, 50
Switching frequency	f_{sw}	20 kHz
Sampling time	T_s	20 μ s

Figure 4 shows the steady-state responses of the output voltage, input voltage, input inductor current and output current in buck and boost modes. The output voltage reference is 40 V and the load resistance is 10 Ω during both buck and boost modes. As shown

in Figure 4a, the input voltage is 60 V for buck operation and the output voltage is regulated to its reference. Also, the output current is 4 A, and the average of the input current is approximately 3 A. The input voltage is 30 V, while the output voltage reference remains the same in the boost mode, as shown in Figure 4b. The output voltage is regulated to its reference in the boost mode. The average input current is approximately 6 A, while the output current is the same as in buck mode. The steady-state results demonstrate that the proposed cascaded ST-SMC method successfully regulates the output voltage in buck and boost operating modes.

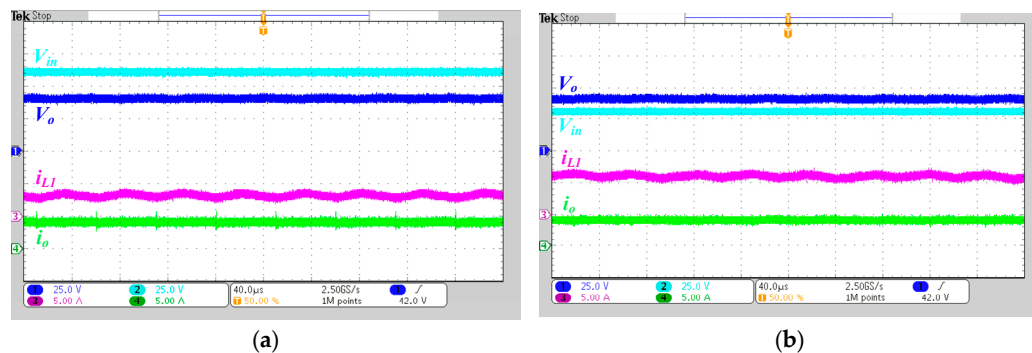


Figure 4. Steady-state responses of converter variables. (a) Buck mode. (b) Boost mode.

The dynamic response capability of the proposed controller is investigated under a step change in the load resistance under both operating conditions. The load resistance is changed from 20 Ω to 10 Ω and returns to 20 Ω . Figure 5a shows the responses of the output voltage, input voltage, input inductor current and output current in buck mode. The input voltage is 60 V and the output voltage reference is 40 V in this test. When the load resistance is abruptly changed from 20 Ω to 10 Ω , the output current increases to 4 A. An undershoot occurs in the output voltage and it is regulated again to 40 V after a 4 ms transition time. Similar responses can be observed for load resistance variation from 10 Ω to 20 Ω , as shown in Figure 5a. The step change responses for boost operation are shown in Figure 5b. The output current is doubled after the step change in the load resistance from 20 Ω to 10 Ω . An undershoot occurs when the load resistance is changed, and the output voltage is regulated to its reference after 7 ms transition time. The output current doubles after the step change, and the input current almost doubles. Undesired ripples exist in the input current under 10 Ω load condition. Nevertheless, the output voltage is not affected by these ripples, as shown in the figure. Similar responses are shown for the step change in the load resistance from 10 Ω to 20 Ω . These results indicate that the proposed cascaded ST-SMC method provides robust voltage regulation under abrupt load variations.

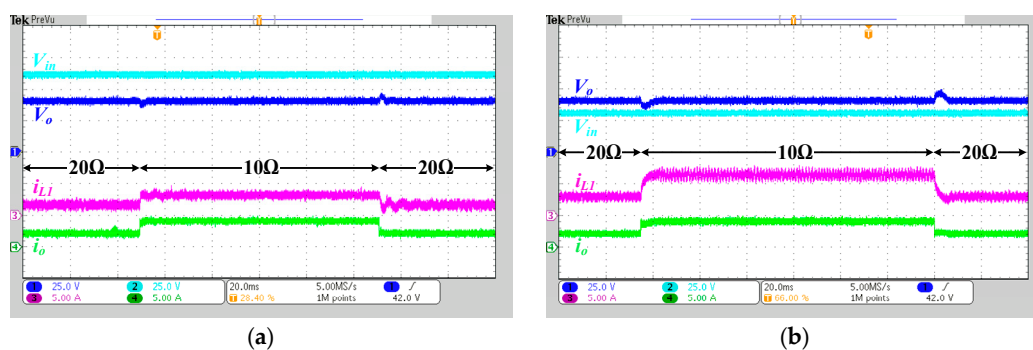


Figure 5. Dynamic responses of converter variables under step change in load resistance from 20 Ω to 10 Ω and 10 Ω to 20 Ω . (a) Buck mode. (b) Boost mode.

The dynamic response of the proposed cascaded ST-SMC method is further investigated under a step change in the input voltage from 20 V to 60 V while the output voltage reference is 40 V. It is worth noting that the operating condition of the converter changed from boost to buck mode during this test. Therefore, both mode transition and input voltage variation are tested together by this test. The converter operates in boost mode before the step change and the output voltage is regulated to 40 V as shown in Figure 6a. The input voltage is increased from 20 V to 60 V and it is observed that the output voltage remains stable during the transition period. In addition, the start-up response of the proposed cascaded ST-SMC method is investigated for a step change in the input voltage from 0 V to 30 V while the reference voltage is 40 V. The output voltage is increased in parallel with the input voltage and regulated to its reference within approximately 30 ms, as shown in Figure 6b. These results verify that the proposed controller successfully regulates the output voltage to its reference during mode transitions, voltage variations and start-up conditions.

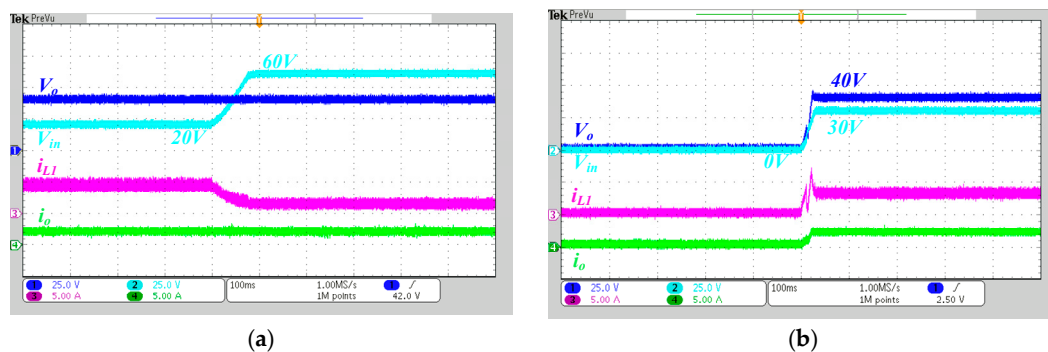


Figure 6. Dynamic responses of converter variables. (a) Under a step change in V_{in} . (b) Start-up test.

The effectiveness of the proposed controller for operation mode change is investigated by changing the reference voltage. The reference voltage is abruptly increased from 30 V to 50 V while the input voltage is 40 V, as shown in Figure 7. This change also changes the operation mode from buck to boost. The regulation of the output voltage to its new reference is achieved in 5 ms without overshoot, as shown in the magnified view of the related part in Figure 7. The output and input currents are also increased after changing the reference. The reference voltage is reduced from 50 V to 30 V. Similar performance with the increment test is observed, as shown in the figure. These results verify that the proposed method is capable of controlling the output voltage to various reference values and mode transitions from buck to boost and vice versa.

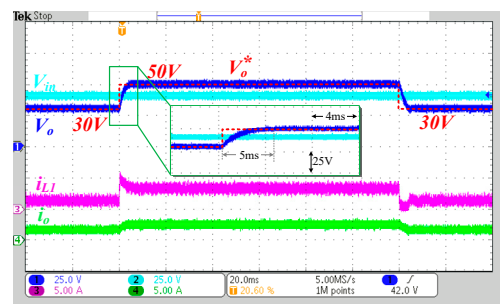


Figure 7. Dynamic responses of converter variables under a step change in V_o^* .

The performance of the proposed cascaded ST-SMC method is compared with existing PI-SMC, PI-MPC and Cascaded Terminal ST-SMC methods for the SEPIC. The com-

parison is based on the number of controller coefficients, robustness to parameter variations, required sensor number, and dynamic response metrics, as shown in Table 2. It is worth noting that the experimental studies in this paper, [16] and [11], are obtained using the same experimental setup. The PI-MPC method presented in [16] proposes an auto-tuning coefficient (weighting factor). Therefore, it does not require a coefficient that needs to be tuned. Although this achievement is significant, the method is not robust to parameter variation and requires more sensors than other methods. The PI-SMC method in [34] is robust against parameter variations. Also, the method requires fewer coefficients (2) to tune, compared to [11] and the proposed method. However, the method exhibits the worst dynamic performance in terms of settling time. The cascaded terminal ST-SMC method exhibits better dynamic performance than that of the PI-SMC method. In addition, no measurable deviation is observed for Cascaded Terminal ST-SMC and the proposed cascaded ST-SMC methods during the step-change input voltage test. However, the method requires six coefficients that need to be tuned, which increases the design complexity. Among these methods, the proposed cascaded ST-SMC method exhibits significantly improved dynamic performance with a maximum 7 ms transition time. Also, the proposed method requires the same number of sensors as the other SMC methods.

Table 2. Comparison of cascaded control methods for SEPIC setup and control parameters.

Description			[34]	[16]	[11]	Proposed
Control approach			PI-SMC	PI-MPC	Cascaded Terminal ST-SMC	Cascaded ST-SMC
Number of controller coefficients			2	Auto-tuned	6	4
Robustness to parameter variations			Robust	Model-dependent	Robust	Robust
Required sensor number			2	4	2	2
Dynamic responses (time, deviation)	R step	Buck	40 ms, ~4 V	32 ms, ~6 V	32 ms, ~4 V	4 ms, ~3 V
		Boost	70 ms, ~6 V	32 ms, ~5 V	65 ms, ~5 V	7 ms, ~5 V
	V_{in} step		60 ms, 6 V	32 ms, ~10 V	No deviation	No deviation
	V_o^* step		Not reported	44 ms	23 ms	5 ms

5. Conclusions

In this study, a cascaded Super-Twisting Sliding Mode Control (ST-SMC) strategy has been proposed to address the voltage regulation problem of SEPICs, which inherently exhibit nonlinear dynamics and an indirect control path between the duty cycle and output voltage. Unlike conventional control approaches, the proposed method explicitly accounts for the cascaded nature of the converter dynamics by employing an outer voltage loop and an inner current loop, both designed using the Super-Twisting Sliding Mode Control technique. The experimental results demonstrate that the proposed controller significantly improves the dynamic performance of the SEPIC. In particular, the transition times under load variations are reduced to 4 ms in buck mode and 7 ms in boost mode, which represents a substantial improvement compared to conventional PI-SMC, PI-MPC, and cascaded terminal ST-SMC approaches. As summarized in Table 2, the response times of existing methods range between 23 ms and 70 ms under similar conditions, whereas the proposed method achieves significantly faster transient behavior. Moreover, the proposed controller maintains stable output voltage without observable deviation during abrupt input voltage changes, including operating mode transitions between boost and buck regions.

Future work may focus on adaptive or self-tuning versions of the proposed cascaded ST-SMC strategy to further improve robustness under parameter uncertainty. In addition, composite control frameworks combining disturbance-estimation techniques, such as disturbance observers or extended-state observers, with feedforward compensation can improve disturbance rejection and transient performance. Although the proposed controller is designed as a pure feedback strategy, integrating disturbance estimation and feedforward compensation into the cascaded ST-SMC framework represents a potential direction for future research. Extending the proposed approach to digitally controlled systems with lower sampling rates and investigating its performance under non-ideal conditions, including parasitic components and sensor noise, may also provide useful insights into practical implementation.

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Abbreviations

The following abbreviations are used in this manuscript:

AC	Alternating Current
ASMC	Adaptive Sliding Mode Control
CCM	Continuous Conduction Mode
CST-SMC	Cascaded Terminal Super-Twisting Sliding Mode Control
DC	Direct Current
DSMC	Discrete-Time Sliding Mode Control
ISMC	Integral Sliding Mode Control
MPC	Model Predictive Control
PI	Proportional–Integral
PWM	Pulse Width Modulation
SEPIC	Single-Ended Primary Inductor Converter
SMC	Sliding Mode Control
STA	Super-Twisting Algorithm
ST-SMC	Super-Twisting Sliding Mode Control
THD	Total Harmonic Distortion

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