

Article

A 128-Stage High-Precision Analog Accumulator Utilized for TDI-CMOS Image Sensors

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Abstract

A 128-stage high-precision analog accumulator is proposed for TDI-CMOS image sensors, incorporating a decoupling capacitor multiplication technique and a noise sampling compensation circuit. The proposed decoupling capacitor multiplication technique enlarges the effective decoupling capacitance while reducing the required layout area, thereby suppressing parasitic effects during high-stage accumulation. A noise sampling compensation circuit is further employed to reduce accumulated circuit noise and improve the signal-to-noise ratio (SNR). The proposed accumulator is designed and verified using a 55 nm standard CMOS process. Post-layout simulation results indicate that the proposed design achieves a 20.945 dB SNR improvement under 128-stage accumulation, with the effective accumulation stage count approaching the ideal value. The total layout area is 4.711 mm × 88.43 mm. The proposed design demonstrates a potential approach for implementing compact, low-noise, and high-stage analog accumulators for TDI-CMOS image sensors.

Keywords: TDI; CMOS image sensor; capacitance multiplication; noise suppression

1. Introduction

TDI (Time Delay Integration) image sensors are specialized line-scan image sensors that capture image information using a two-dimensional pixel array [1,2]. In low-light environments and high-speed scanning applications, TDI technology enhances the SNR (Signal-to-Noise Ratio) by achieving n times exposure and accumulation of the same pixel signal through the relative motion between the scene and the sensor, resulting in an improvement of $\sqrt{n}$ in SNR and thus enhancing image quality [3,4]. This makes TDI image sensors suitable for applications requiring high resolution, high-speed readout, and low noise [5]. The unique advantages of CMOS technology have positioned TDI CMOS image sensors as a current research focus [6]. The TDI analog accumulation method has become the mainstream accumulation technique due to its lower implementation difficulty and better overall performance [7,8]. However, achieving a higher SNR necessitates a greater number of analog accumulation stages, which introduces parasitic effects that reduce the effective accumulation stages of the circuit [9,10].

Reference [11] proposes an improved 128-stage analog accumulator that combines decoupling capacitors to offset parasitic effects, thereby enhancing the measurement sensitivity and SNR of the sensor. However, the use of decoupling capacitors increases the chip area, and their effectiveness diminishes with higher accumulation stages, ultimately achieving only 64 stages of accumulation. Reference [12] presents a two-step analog accumulator architecture for TDI CIS with 64 stages, introducing a novel accumulation method to reduce



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the number of integrators. The study demonstrates that this two-step structure can achieve 54 effective accumulation stages, effectively mitigating the impact of parasitic effects in high-stage analog accumulators. However, the timing design of the two-step accumulator is complex and requires a significant chip area for timing circuits, making its contribution to SNR improvement negligible for high-stage analog accumulators (such as those with 100 stages or more). Reference [13] optimizes the parasitic coupling of circuits by adopting decoupling switches and positive feedback capacitors. For a compact 128-stage analog accumulator architecture, this method improves the signal-to-noise ratio (SNR) by 21.068 dB, pushing the circuit performance close to the ideal theoretical limit. However, this scheme is sensitive to capacitor matching accuracy and susceptible to process variations, thereby requiring auxiliary calibration for performance enhancement. On this basis, Reference [14] proposes an improved strategy, which replaces the fixed positive feedback capacitor with a top-plate sampling charge injection structure, together with the optimization of on-chip calibration circuits, switch timing and device dimensions. The proposed method can effectively suppress process, voltage, and temperature (PVT) fluctuations and realize high-linearity parasitic compensation over the full output swing. The optimized 128-stage accumulator achieves an SNR improvement of 21.067 dB, which greatly enhances the circuit robustness and provides a feasible technical reference for the design of high-precision and high-order analog accumulators.

To achieve high SNR with a larger number of accumulation stages within a smaller area, this study presents the analysis and design of a high-stage TDI CIS readout accumulation circuit, implementing a 128-stage analog accumulation based on a 55 nm standard CMOS process. Compared with previous analog accumulators, this work focuses on improving the practicality of high-stage analog accumulation by optimizing the bias decoupling and noise suppression circuits. The proposed accumulator incorporates a decoupling capacitor multiplication technique to minimize the size of the decoupling capacitors, making the decoupling scheme more suitable for high-stage analog accumulators. Additionally, a noise sampling compensation technique is proposed for the analog accumulation circuit to sample and suppress the noise introduced by the subsequent analog readout path, thereby reducing its influence on the accumulated signal.

2. Readout Circuit Architecture for TDI CIS

The overall circuit architecture of the proposed design and its placement within the image sensor chip module are illustrated in Figure 1. An image signal is captured by a 128×1024 pixel array. This signal is then accumulated by a 128-stage analog-domain accumulator. After the image signal undergoes 128 rounds of accumulation, it is quantified by an ADC (Analog-to-Digital Converter).

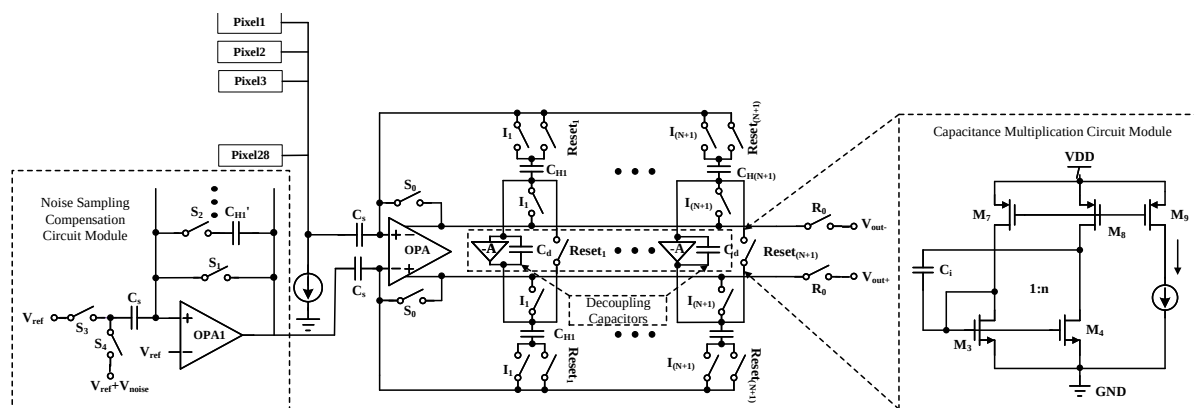


Figure 1. Overall circuit architecture diagram.

2.1. Area-Optimized Design of Decoupling Capacitors

As illustrated in Figure 1, adding decoupling capacitors is an effective technique for suppressing parasitic effects in the accumulator. This method significantly enhances performance without introducing additional switches or timing controls, while preserving the inherent operating characteristics of the accumulator. To effectively reduce parasitic effects, a decoupling capacitor is integrated at each stage of the analog accumulator. The equivalent parasitic capacitance introduced by these decoupling capacitors can be calculated based on the circuit topology as follows:

$$C_{pi} \approx \frac{C_{pti}C_{pbi}}{C_{pti} + C_{pbi} + 2C_d} \quad (1)$$

After integrating the decoupling capacitor C_d into the analog accumulator, the equivalent parasitic capacitance decreases as C_d increases. This reduction alleviates the coupling degradation effect of parasitic components on accumulation performance. However, it also increases the total circuit area. Therefore, to balance area constraints and accumulation efficiency, the capacitance multiplication circuit used in this study aims to minimize reliance on large-area capacitors.

However, the capacitance multiplication circuit can only multiply capacitors used for coupling voltage or filtering functions, making it unsuitable for charge storage capacitors. Simulation results indicate that applying capacitance multiplication to charge storage capacitors may degrade the accumulation performance. Although the area occupied by the 258 storage capacitors and 2 sampling capacitors in the 128-stage analog accumulator cannot be reduced, the capacitance multiplication circuit can be employed to implement the decoupling capacitor C_d . This approach allows for a higher number of effective accumulation stages while maintaining a smaller circuit area.

The capacitance multiplication circuit is primarily categorized into voltage mode and current mode types. Compared with voltage mode circuits, current mode designs provide easier and more precise adjustment for capacitance scaling ratios and can operate at higher frequencies. Therefore, this study employs a current mode capacitance multiplier to amplify the effective value of the decoupling capacitor C_d . The capacitance multiplication circuit module is illustrated on the right side of Figure 1. When implemented in current mode, the capacitance multiplier achieves capacitance scaling by adjusting the current amplification factor of the current mirror. Once the input voltage is fixed, the equivalent input impedance is inversely proportional to the input current. Thus, if the input current is amplified by a factor of n under the same input voltage, the equivalent input impedance decreases to $1/n$ of its original value, resulting in a proportional increase in effective capacitance. By analyzing the relationship between the input current i_{in} and input voltage v_{in} , and neglecting the parasitic capacitances at the top and bottom plates of the multiplied capacitor C_i , we derive

$$\frac{i_{in}}{v_{in}} \approx sC_i(n+1) \quad (2)$$

From Equation (2), it is evident that this circuit amplifies the bias current by a factor of n through the current mirror, yielding an equivalent capacitance of $(n+1)C_i$. In order to ensure the stability of the mirror current coefficient of the current mirror, special attention needs to be paid to the current matching of the current mirror in the capacitor multiplication circuit module, and the transistor size and layout matching are designed.

It should be noted that the proposed active capacitance multiplier is employed only to enlarge the effective decoupling capacitance at the bias node rather than participating in the signal accumulation process. Unlike gain-setting capacitors in switched-capacitor circuits, the multiplication accuracy of the proposed circuit is not the primary factor affecting

the accumulation accuracy. According to Equation (1), suppression of parasitic coupling only requires the decoupling capacitance C_d to be sufficiently larger than the parasitic capacitance. Therefore, moderate variations in the multiplication factor have negligible influence on the accumulation performance, provided that the equivalent capacitance remains sufficiently larger than the parasitic capacitance.

Since the active capacitance multiplier is connected only to the bias decoupling node instead of the signal transfer path, current mirror mismatch mainly changes the equivalent capacitance rather than introducing signal transfer errors. Consequently, moderate mismatch only affects the decoupling capability of the bias node without noticeably degrading the accumulation accuracy. Similarly, the bandwidth requirement of the capacitance multiplier is considerably lower than that of the signal path because it is not involved in high-speed signal sampling or charge transfer. Therefore, the achievable line rate of the proposed accumulator is mainly determined by the signal transfer path rather than the capacitance multiplier itself.

Moreover, the thermal and flicker noise generated by the current mirrors are largely filtered by the enlarged equivalent decoupling capacitance and are not directly coupled into the signal accumulation path. As a result, the additional noise introduced by the capacitance multiplier has a negligible influence on the accumulated output signal. Although the active capacitance multiplier introduces additional bias current, it consists only of a simple current mirror for bias stabilization. Therefore, the additional power consumption is expected to be small compared with the overall column power and represents a reasonable trade-off for achieving a substantial reduction in the required on-chip decoupling capacitance.

2.2. Noise Sampling Compensation Circuit Design

The noise sampling compensation circuit designed in this study is implemented using a programmable gain amplifier architecture. This circuit employs correlated double sampling to suppress the output-referred noise in the 128-stage analog accumulator, specifically compensating for the adverse effects of thermal noise from preceding circuit stages on the accumulator's output. The improved decoupling capacitor multiplication technique is integrated with this noise compensation method to form the analog accumulation circuit architecture shown in Figure 1. Input signals are received through the switching circuit of transistors S_3 and S_4 .

The timing diagram of the 128-stage analog accumulator is shown in Figure 2. In the noise sampling compensation circuit, S_1 serves as the sampling switch, while the switch in series with the hold capacitor C_{HN}' functions as the hold switch. The operation principle of the circuit is explained using hold switch S_2 as an example. When switches S_1 and S_3 are closed and switches S_2 and S_4 are open, the circuit is in the sampling state. During this state, the negative input of the accumulator circuit is connected to V_{ref} . When switches S_2 and S_3 are closed and switches S_1 and S_4 are open, the circuit enters the hold state. In this state, the hold capacitor C_{H1}' is connected to the circuit, preparing to process the input signal. When switch S_3 opens and switch S_4 closes, the input noise signal is processed by the noise sampling compensation circuit to compensate for its effect on the analog accumulator. After processing by the noise sampling compensation circuit, the generated compensation signal is applied to the analog accumulator to reduce the influence of circuit noise on the accumulation result. Although the influence of thermal noise is not as significant as that of parasitic noise, it should not be overlooked in high-precision accumulation applications. This compensation method effectively suppresses the overall circuit's thermal noise while occupying a smaller chip area.

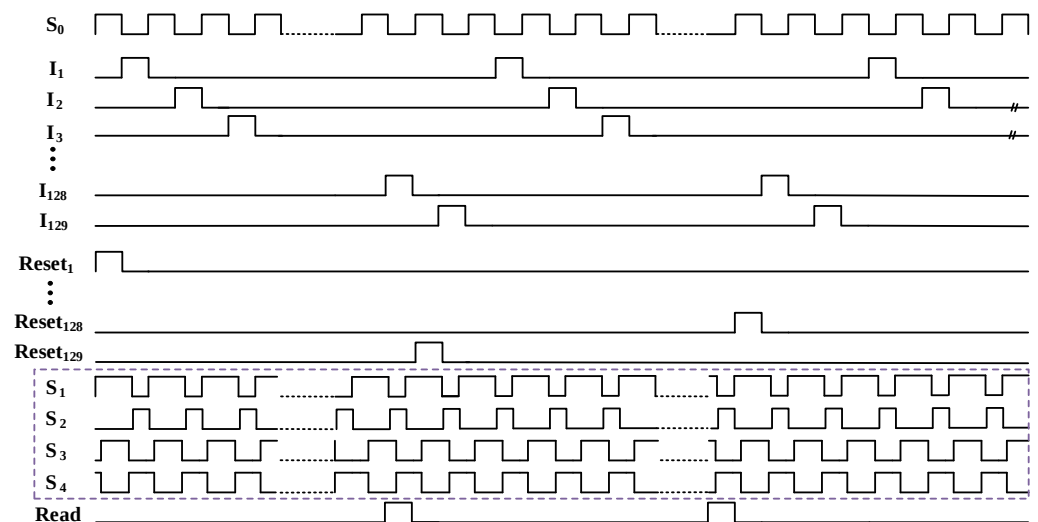


Figure 2. Sequence diagram of the whole circuit of analog accumulator.

The basic principle of the proposed noise suppression technique is to sample the switching thermal noise generated during the operation of the accumulator and store the sampled noise voltage in the noise compensation circuit connected to the negative input terminal of the accumulator operational amplifier. The stored noise voltage is then used to compensate for the noise contribution during signal accumulation. The specific process of its theoretical derivation is as follows.

The noise sampling compensation circuit completes the acquisition of noise V_{noise} such as switching thermal noise in the circuit during the sampling process of the accumulator. The noise sampling compensation circuit inputs the signal V_{ref} in the sampling state and the input signal $V_{ref} + V_{noise}$ in the holding state, so the output voltage of the module is

$$V_{out} = [V_{ref} - (V_{ref} + V_{noise})] \cdot \frac{C_S'}{C_H'} + V_{ref} \quad (3)$$

The above formula can be simplified to

$$V_{out} = V_{ref} - V_{noise} \cdot \frac{C_S'}{C_H'} \quad (4)$$

During the first accumulation process of the accumulator, the signals of the positive and negative phase input terminals of the sampling state are V_{rst1} and V_{ref} , and the signals of the positive and negative phase input terminals of the holding state are V_{sig} and $V_{ref} + V_{noise1}$, so after accumulating once, the output expression of the accumulator is

$$V_{out1-} - V_{out1+} = \left(V_{rst1} - V_{sig1} - V_{noise1} \cdot \frac{C_S'}{C_H'} \right) \cdot \frac{C_S}{C_H} + V_{noise1}' \quad (5)$$

where V_{noise1}' is the switching thermal noise and other noise generated by the accumulator after completing a single accumulation. Simplify the above formula to obtain

$$V_{out1-} - V_{out1+} = (V_{rst1} - V_{sig1}) \cdot \frac{C_S}{C_H} + V_{noise1}' - V_{noise1} \cdot \frac{C_S'}{C_H} \cdot \frac{C_S}{C_H} \quad (6)$$

After the accumulator completes N accumulations, its output expression is

$$V_{outN^-} - V_{outN^+} = \sum_{i=1}^N \left[(V_{rsti} - V_{sigi}) \cdot \frac{C_S}{C_H} \right] + \sum_{j=1}^N \left(V_{noiseN'} - V_{noiseN} \cdot \frac{C_{S'}}{C_{H'}} \cdot \frac{C_S}{C_H} \right) \quad (7)$$

Therefore, only the $C_S'/C_{H'}$ ratio needs to be designed to reduce the noise during the operation of the accumulator, thereby improving the signal-to-noise ratio of the circuit.

The noise sampling compensation circuit significantly reduces the impact of noise on the final accumulation result by implementing noise compensation at each accumulation step, as indicated by Equation (7). Theoretical analysis shows that this circuit achieves noise suppression. In the noise sampling compensation circuit, different holding capacitors can be selectively connected to the circuit through switches such as S_2 and S_2' , allowing for the selection of noise compensation multipliers tailored to different noise levels. When the overall noise has a more severe impact on the final accumulation result, the sampled portion of the noise is amplified by a larger factor to provide compensation. Therefore, regardless of whether the overall noise interference in the accumulator is significant or minimal, this circuit effectively suppresses the total noise. The proposed noise compensation circuit samples the circuit noise before signal accumulation and injects a scaled compensation signal into the subsequent accumulation stage. The capacitor ratio $C_S'/C_{H'}$ determines the compensation coefficient rather than the signal gain. Therefore, its value is selected according to the gain of the subsequent accumulation stage. Since the subsequent accumulation stage exhibits approximately unity gain, a 1:1 capacitor ratio is adopted to provide appropriate noise compensation while preserving the useful accumulated signal.

In practical implementation, PVT variations may affect the compensation accuracy through variations in device parameters, switch characteristics, operational amplifier offset voltage, and capacitor values. Temperature variations mainly influence transistor mobility, threshold voltage, and transconductance, which may further affect the switch on-resistance and amplifier offset characteristics. Process and voltage variations may also introduce deviations in transistor operating points and capacitor values. However, the influence of these variations on the final compensation accuracy is limited due to the characteristics of the switched-capacitor structure. The compensation factor is mainly determined by the ratio between the sampling and feedback capacitors rather than the absolute device parameters. Since both capacitors in the switched-capacitor network are implemented using the same capacitor type, the influence of process- and temperature-induced capacitance variations is reduced, and the compensation accuracy is mainly determined by the relative capacitor matching. In practical implementation, bottom-plate sampling together with CMOS transmission switches is employed to suppress charge injection and clock feedthrough. An input-offset storage (IOS) technique is further adopted to reduce the influence of operational amplifier offset voltage on the compensation accuracy. Therefore, although PVT variations may introduce deviations in individual circuit parameters, their impact on the final noise compensation accuracy is limited.

3. Physical Verification

In the TDI CIS with column-parallel readout, the 1024-column circuit is evenly divided into two sections to process the exposure output signals for the odd and even pixel columns. These two sections are placed above and below the pixel module, respectively. Since the layout design of these two sections is identical, only one section's layout design—namely, that for 512 columns—will be described here.

The overall layout of the analog accumulator in a 128×512 TDI CIS is shown in Figure 3. Following the layout plan described in the previous section, the layout was drawn. Under a single TDI column width of $9.2 \mu\text{m}$, the 128×512 layout dimensions are 4.711 mm wide and 44.215 mm high. the 128×1024 layout dimensions are 4.711 mm wide and 88.43 mm high.

Mismatch issues in the MOS transistors within the layout have a significant impact on circuit accuracy. Therefore, this paper ensured symmetric placement of MOS transistors during layout, employing a common-centroid layout methodology. All matched transistors maintain the same layout orientation, such as consistent gate direction, to avoid mismatch caused by process variations. The capacitance in the analog accumulator adopts MOM capacitance, and a variety of matching methods are used to keep the accuracy error of the circuit at one thousandth.

The input/output signal paths of the accumulator were minimized to reduce the effects of parasitics. Wiring directions for metal traces on the same layer are kept uniform.

Beneath the holding capacitors lie the decoupling capacitors and the capacitance multiplication circuit. The noise compensation circuit is located in the bottom region of the entire layout.

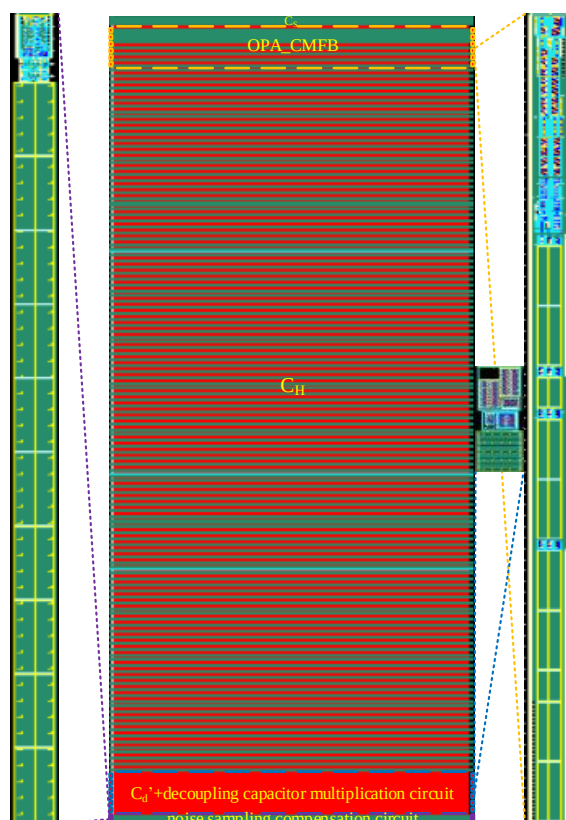


Figure 3. The 128×512 overall layout.

As shown in Figure 3, the layout area of the decoupling capacitor multiplication circuit is slightly larger than that of the multiplied capacitor itself. When the multiplied capacitor area corresponds to 40 fF , the combined circuit (including the multiplier) occupies an area equivalent to approximately 100 fF of capacitance. This implies that with a multiplication factor of 5, a capacitor area saving of 100 fF per column is achieved for the decoupling capacitor. Furthermore, if a 100 fF capacitor is multiplied by a factor of 5, a capacitor area saving of 340 fF per column is realized for the decoupling capacitor.

For a fixed multiplication factor, larger multiplied capacitances yield greater circuit area savings.

The capacitor multiplication concept proposed in this paper can also be applied to techniques such as positive feedback capacitor compensation and adaptive compensation capacitor techniques. This enables a reduction in the actual capacitor area introduced by these techniques without compromising their effectiveness in enhancing accumulation performance.

TDI image sensors suffer from various non-ideal effects during operation, which creates a deviation between the achieved SNR improvement and the theoretical value. The accumulation stage number corresponding to the SNR improvement after accounting for all non-ideal factors is defined as the effective accumulation stage count of the TDI image sensor. The derivation of the effective accumulation stage count is presented as follows.

The SNR improvement obtained by subtracting the SNR of single accumulation from the SNR of N -time accumulation in the TDI image sensor is expressed as

$$\Delta \text{SNR}_{\text{eff}N} = \text{SNR}_{\text{eff}N} - \text{SNR}_{\text{eff}1} = 10 \cdot \log(N_{\text{eff}}) \quad (8)$$

where $\text{SNR}_{\text{eff}N}$ denotes the signal-to-noise ratio of the accumulator after N accumulation cycles with non-ideal factors considered; $\text{SNR}_{\text{eff}1}$ represents the signal-to-noise ratio after a single accumulation cycle under non-ideal conditions.

The effective accumulation stage count N_{eff} of the TDI image sensor can thus be derived as

$$N_{\text{eff}} = 10^{\frac{\Delta \text{SNR}_{\text{eff}N}}{10}} \quad (9)$$

Post-layout simulation results verifying the effective accumulation stages of the analog accumulator in the 128-stage analog-domain TDI circuit are shown in Figure 4a.

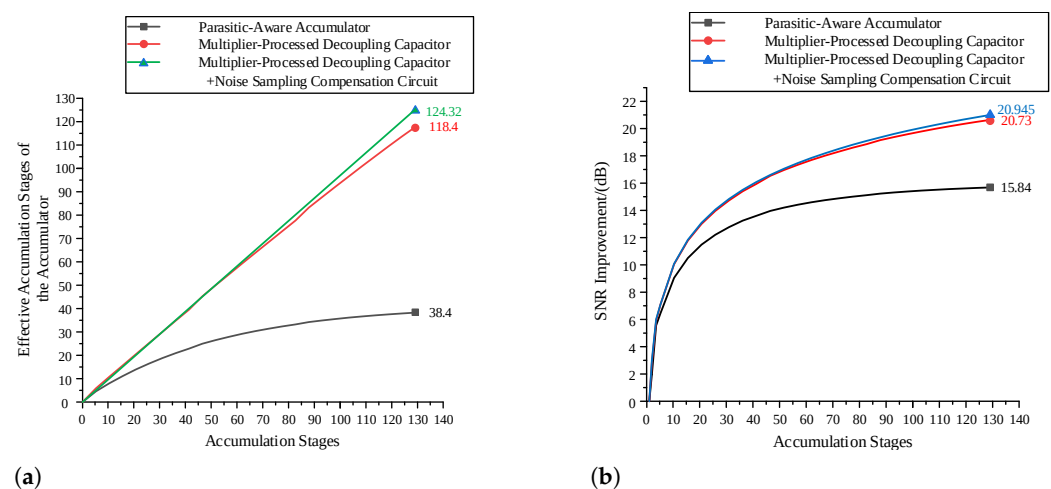


Figure 4. Post-layout Simulation Comparisons of Accumulation Stages and SNR Improvement. (a) Post-layout simulation comparison of effective accumulation stages; (b) Comparison diagram of SNR improvement effect of post-layout simulation.

With the multiplied decoupling capacitor, the effective accumulation stages reach 118.4 stages while achieving an area reduction of approximately 12.9 pF (capacitance equivalent) compared to traditional decoupling capacitors. Furthermore, after incorporating the noise compensation circuit for additional noise suppression, the post-layout simulation shows that the accumulator achieves 124.32 effective stages. Although this represents a decrease of 3.104 stages compared to pre-layout simulation results, it still significantly enhances the effective accumulation stages impacted by parasitics.

Figure 4b shows the post-layout simulation SNR comparison for the analog accumulator in the 128-stage analog-domain TDI circuit. Post-layout simulation results reveal that

integrating optimized decoupling capacitors and noise compensation circuits delivers a 20.945 dB SNR gain compared with the scheme without the analog accumulator.

Although this represents a decrease of 0.105 dB compared to the pre-layout simulation SNR, the overall design demonstrates a significant noise suppression effect on the high-stage analog accumulator. The noise suppression techniques designed in this paper demonstrate the theoretical feasibility of the approach.

The noise simulation bandwidth is determined by the closed-loop characteristics of the accumulator, including the operational amplifier and feedback capacitor network. The simulated noise therefore represents the integrated RMS noise within the effective operating bandwidth of the circuit. After post-layout noise simulation, the operational amplifier noise and switching kTC noise are obtained as 535 μ Vrms and 220 μ Vrms, respectively. Since these noise sources are statistically independent, the total noise is calculated using the root-sum-square method, resulting in a total RMS noise of approximately 578.5 μ Vrms.

The PVT simulation results of the proposed accumulator are shown in Figure 5. The simulation corners are arranged from left to right in the order of ss, tt, and ff process corners. Within each process corner, the supply voltage is swept from 2.97 V, 3.30 V, to 3.63 V, and for each voltage condition, the temperature is further swept from -40°C , 27°C , to 125°C . As shown in Figure 5, the proposed circuit exhibits stable performance under all PVT corners. The best case occurs at the ss/3.63 V/ 27°C corner, where the SNR improvement reaches 20.978 dB, whereas the worst case occurs at the ff/3.63 V/ 125°C corner with an SNR improvement of 20.883 dB. The maximum variation is only 0.095 dB, demonstrating that the proposed accumulator maintains excellent robustness against process, voltage, and temperature variations.

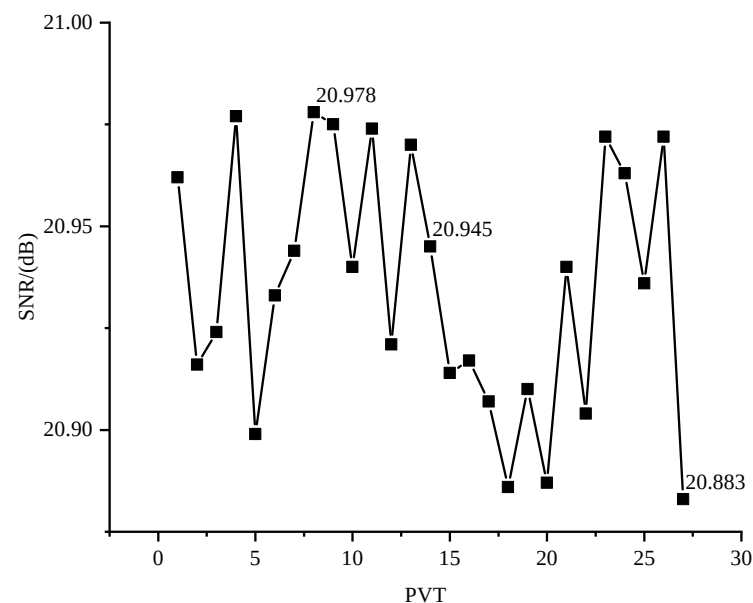


Figure 5. The signal-to-noise ratio of the accumulator is affected by PVT.

The process mismatch model provided by the foundry was adopted to perform 200 Monte Carlo simulations of the proposed accumulator circuit. The simulation results are shown in Figure 6. As observed from Figure 6, the SNR improvement exhibits limited variation under different process mismatch conditions, indicating that the proposed accumulator is relatively insensitive to process variations.

The ideal SNR improvement of a 128-stage accumulator is 21.07 dB under ideal accumulation conditions. The slight deviation observed in the Monte Carlo results is mainly attributed to statistical variations in circuit noise and device mismatch. Although a small

number of samples exceed the theoretical value due to random noise fluctuations, the average SNR improvement reaches 20.947 dB, which is very close to the theoretical limit. This demonstrates that the proposed accumulator achieves near-ideal accumulation performance under post-layout simulation conditions while effectively mitigating practical circuit non-idealities.

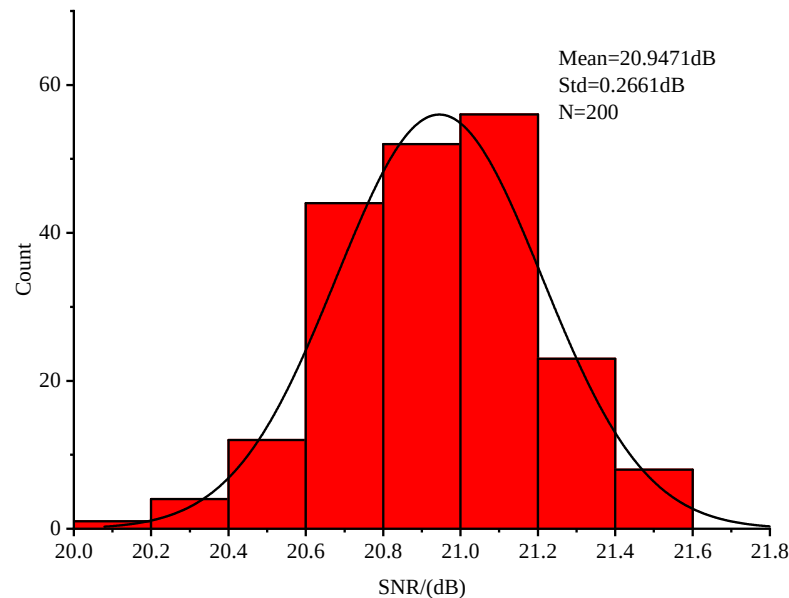


Figure 6. Monte Carlo simulation results of signal-to-noise ratio of accumulator.

A synthetical evaluation target (SET) is proposed to evaluate the performance of TDI, where Δ SNR is the SNR improvement of the TDI-CIS, R_{Line} is the line rate; power represents the power consumption of one column pixels.

$$SET = \frac{\Delta SNR \cdot R_{Line}}{power} \quad (10)$$

Table 1 compares the post-layout simulation results of the proposed design with representative TDI CMOS image sensor readout circuits reported in the literature. Compared with the analog accumulators in Refs. [11,12], the proposed design achieves a significantly higher effective accumulation stage count and substantially improves the line rate while maintaining competitive power efficiency. In particular, Ref. [12] adopts a two-step accumulation architecture to alleviate accumulation errors, whereas the proposed design employs a simpler accumulation structure with more straightforward timing implementation.

Compared with the digital-domain accumulation scheme in Ref. [15], the proposed analog accumulator achieves considerably higher SNR improvement and line rate at the expense of moderately increased power consumption. Ref. [16] adopts a hybrid charge-domain/digital-domain accumulation architecture and achieves higher line rate and SNR improvement than the proposed design; however, this is accompanied by significantly higher power consumption and a reduced column count, leading to increased circuit complexity and implementation cost. Under comparable process technology, accumulation stage count, accumulation domain, and array scale, the proposed design outperforms the analog accumulator in Ref. [17] in both line rate and SNR improvement, demonstrating the effectiveness of the proposed capacitance multiplication and noise compensation techniques.

Table 1. Literature Comparison.

	Technology (nm)	Accumulator	Column	Maximum Stage	Line Rate (Hz)	Δ SNR (dB)	Power/Column (μ W)	SET * [(dBHz)/ μ W]	Performance Data
[11]	180	Analog	1024	128	3.875 k	16.6	488.3	131.73	Measurement
[12]	180	Analog	512	64	4 k	18.034	/	/	Simulation
[15]	110	Digital	512	32	9.302 k	14.82	153.2	899.84	Measurement
[16]	110	Hybrid	400	256	100 k	24.15	10,413.97	231.9	Simulation
[17]	55	Analog	1024	128	7.75 k	20.9	290	558.53	Simulation
[18]	180	Hybrid	1010	86	0.45 k	17.1	/	/	Measurement
[19]	110	Analog	120	45	100 k	16.31	530	3077.4	Measurement
This work	55	Analog	1024	128	24.22 k	20.945	332.85	1524.32	Simulation

* SET is a comprehensive evaluation index. The larger the value, the better the performance of the TDI image sensor.

Compared with the TDI image sensor reported in Ref. [19], which mainly improves system performance through pseudomultisampling and ADC optimization, the proposed analog accumulation circuit provides higher SNR improvement, lower power consumption, and a simpler analog accumulation architecture. In addition, the proposed design achieves a higher SET value than Refs. [11,15–17], indicating a superior overall trade-off among line rate, power consumption, and SNR improvement.

It should be noted that several of the compared works report measured silicon results, whereas all performance metrics presented in this work are obtained from post-layout simulations. Nevertheless, even when compared with previous simulation-based analog accumulator designs, the proposed circuit demonstrates competitive performance in terms of effective accumulation capability, line rate, and SNR improvement.

Although the proposed analog accumulator is primarily developed for TDI CMOS image sensors, similar low-noise analog front-end circuits are also required in CMOS-integrated intelligent sensing systems, where weak sensor signals must be accurately acquired and processed before analog-to-digital conversion. Examples include CMOS-integrated gas sensing systems and other intelligent sensor interfaces with optimized signal-to-noise ratio, which similarly rely on low-noise readout circuits to improve sensing performance [20]. The proposed capacitance multiplication technique increases the effective decoupling capacitance at the feedback bias node, thereby mitigating charge loss caused by parasitic capacitance during repeated analog accumulation without requiring a large on-chip capacitor. Furthermore, the noise sampling compensation circuit suppresses accumulated readout noise and improves the accumulation accuracy of weak input signals. Therefore, the proposed circuit techniques may provide a useful reference for the design of low-noise analog front-end circuits in future intelligent sensing systems requiring repeated weak-signal integration.

4. Conclusions

In this work, a high-stage analog accumulation circuit for TDI-CMOS image sensors is analyzed and designed based on a 55 nm standard CMOS process. A capacitance multiplication technique is proposed to enhance the effective decoupling capacitance while reducing the required capacitor area, thereby mitigating parasitic coupling effects during high-stage accumulation. Meanwhile, a noise sampling compensation circuit is integrated to suppress circuit noise and improve accumulation accuracy. Post-layout simulation results demonstrate that the proposed accumulator achieves a 20.945 dB SNR improvement under 128-stage accumulation compared with the original scheme without the analog accumulator, with a total layout area of 4.711 mm $\times$ 88.43 mm. These results demonstrate

the effectiveness of the proposed techniques for implementing compact and high-precision multi-stage analog accumulators in TDI-CMOS image sensor readout circuits.

Author Contributions: Conceptualization, Z.G.; methodology, Z.G.; software, F.G.; validation, Y.W.; formal analysis, X.H.; investigation, X.H.; resources, Y.W.; data curation, F.G.; writing—original draft preparation, Z.G. and X.H.; writing—review and editing, Z.G. and Y.W.; visualization, F.G.; supervision, Y.W.; project administration, Z.G.; funding acquisition, Z.G. All authors have read and agreed to the published version of the manuscript.

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References

1. Liu, K.-L.; Hsieh, C.-C.; Lai, S.-Y.; Chiu, C.-F. A time delay multiple integration linear CMOS image sensor for multispectral satellite telemetry. In Proceedings of the 2016 IEEE Asian Solid-State Circuits Conference (A-SSCC), Toyama, Japan, 7–9 November 2016; pp. 37–40.
2. Ekin, M.B.; Acar, Y.; Ekin, M. Attitude Guidance Effects on Image Quality for Spaceborne Electro-Optic Imagers with TDI. In Proceedings of the 2023 10th International Conference on Recent Advances in Air and Space Technologies (RAST), Istanbul, Turkey, 7–9 June 2023; pp. 1–6.
3. Cheng, K.-W.; Yin, C.; Hsieh, C.-C.; Chang, W.-H.; Tsai, H.-H.; Chiu, C.-F. Time-delay integration readout with adjacent pixel signal transfer for CMOS image sensor. In Proceedings of the Technical Program of 2012 VLSI Design, Automation and Test, Hsinchu, Taiwan, 23–25 April 2012; pp. 1–4.
4. Li, Y.H.; Wan, X.D. Compressive imaging beyond the sensors physical resolution via coded exposure combined with time-delay integration. *Opt. Lasers Eng.* **2023**, *164*, 107491. [\[CrossRef\]](#)
5. Gao, T.; Zheng, L.; Wu, X.; Ji, H.; Yang, B.; Xu, W. Research on Modeling the Nonlinear Response Function of TDI CMOS Imaging System. *IEEE J. Sel. Top. Appl. Earth Obs. Remote Sens.* **2024**, *17*, 3768–3779. [\[CrossRef\]](#)
6. Xu, R.; Guo, Z.; Liu, S.; Yu, N. Global Ramp Uniformity Correction Method for Super-Large Array CMOS Image Sensors. *Chin. J. Electron.* **2024**, *33*, 415–422. [\[CrossRef\]](#)
7. Lepage, G.; Bogaerts, J.; Meynants, G. Time-Delay-Integration Architectures in CMOS Image Sensors. *IEEE Trans. Electron Devices* **2009**, *56*, 2524–2533. [\[CrossRef\]](#)
8. Nie, K.; Yao, S.; Xu, J.; Gao, J. Thirty Two-Stage CMOS TDI Image Sensor with On-Chip Analog Accumulator. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2014**, *22*, 951–956. [\[CrossRef\]](#)
9. Gao, C.; Yao, S.; Xu, J.; Gao, J.; Nie, K. Analysis of noise of current accumulator in Time-Delay-Integration CMOS image sensor. In Proceedings of the 2011 IEEE International Conference of Electron Devices and Solid-State Circuits, Tianjin, China, 17–18 November 2011; pp. 1–2.
10. De Moor, P.; Robbelein, J.; Haspeslagh, L.; Boulenc, P.; Ercan, A.; Minoglou, K. Enhanced time delay integration imaging using embedded CCD in CMOS technology. In Proceedings of the 2014 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 15–17 December 2014; pp. 4.6.1–4.6.4.
11. Nie, K.; Yao, S.; Xu, J.; Gao, J.; Xia, Y. A 128-Stage Analog Accumulator for CMOS TDI Image Sensor. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2014**, *61*, 1952–1961. [\[CrossRef\]](#)
12. Xia, Y.; Nie, K.; Xu, J.; Yao, S. A Two-Step Analog Accumulator for CMOS TDI Image Sensor with Temporal Undersampling Exposure Method. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2016**, *24*, 1104–1117. [\[CrossRef\]](#)
13. Huang, F.J.; Xu, J.T.; Nie, K.M. Research on analog accumulator suitable for high-stage TDI CMOS image sensors. *Acta Sci. Nat. Univ. Nankaiensis* **2016**, *49*, 71–75+80.
14. Li, J.; Huang, F.; Zong, Y.; Gao, J. High-stage analog accumulator for TDI CMOS image sensors. *J. Semicond.* **2016**, *37*, 025001. [\[CrossRef\]](#)
15. Yin, C.; Liao, T.; Liu, K.L.; Kao, C.-C.; Chiu, C.-F.; Hsieh, C.-C. A 32-Stage 15-b digital time-delay integration linear CMOS image sensor with data prediction switching technique. *IEEE Trans. Electron Devices* **2017**, *64*, 1167–1173. [\[CrossRef\]](#)

16. Gao, J.; Zhang, B.; Nie, K.; Xu, J. Research on a pulse-based high-line-rate TDI CMOS image sensor. *Microelectron. J.* **2021**, *111*, 105021. [[CrossRef](#)]
17. Guo, Z.; Li, C.; Xu, R.; Cheng, X.; Su, C.; Wu, L. A High SNR Improvement CMOS Analog Accumulator with Charge Compensation Technique. *Sensors* **2022**, *22*, 7050. [[CrossRef](#)] [[PubMed](#)]
18. Jo, Y.R.; Hong, S.K.; Kwon, O.K. A Tileable CMOS X-Ray Line Detector Using Time-Delay-Integration with Pseudomultisampling for Large-Sized Dental X-Ray Imaging Systems. *IEEE Trans. Electron Devices* **2017**, *64*, 211–216. [[CrossRef](#)]
19. Xu, J.; Shi, X.; Nie, K.; Gao, Z. A global shutter high speed TDI CMOS image sensor with pipelined charge transfer pixel. *IEEE Sens. J.* **2018**, *18*, 2729–2736. [[CrossRef](#)]
20. Tian, X.-H.; Zhou, T.-Y.; Meng, Y.; Zhao, Y.-M.; Shi, C.; Hou, P.-X.; Zhang, L.-L.; Liu, C.; Cheng, H.-M. A Flexible NO₂ Gas Sensor Based on Single-Wall Carbon Nanotube Films Doped with a High Level of Nitrogen. *Molecules* **2022**, *27*, 6523. [[CrossRef](#)] [[PubMed](#)]

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