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A Frequency-Reconfigurable Dual-Band Variable-Gain Phase Shifter for 5G mm-Wave Beamforming

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Abstract

This paper presents a frequency-reconfigurable dual-band phase shifter operating in the n257 (26.5–29.5 GHz) and n260 (37–40 GHz) bands for fifth-generation (5G) communication. The proposed phase shifter is based on an active vector-summing architecture and provides simultaneous gain and phase control for beamforming applications. To support dual-band operation with a large frequency separation, a reconfigurable RC–RL polyphase filter (PPF) is employed for in-phase/quadrature (I/Q) signal generation. The proposed PPF reconfigures its inductance and capacitance according to the operating band, reducing insertion loss and minimizing I/Q phase error in both frequency bands. Gain and phase are controlled by digital-to-analog converter (DAC)-assisted vector summation with 4-bit gain and 6-bit phase control resolution, while a reconfigurable output matching network provides optimized impedance matching in each operating mode. The phase shifter is implemented in a 28 nm fully depleted silicon-on-insulator (FDSOI) process with a core area of 0.26 mm². The measured RMS phase errors are <1.18° and <1.5°, and the RMS gain errors are <0.26 dB and <0.35 dB in the n257 and n260 bands, respectively. The measured DC power consumption is 11 mW and 15.4 mW in the n257 and n260 bands, respectively.

Keywords: phase shifter; beamforming; millimeter wave; RFIC; dual band; frequency reconfigurable; variable gain; polyphase filter



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1. Introduction

Fifth-generation (5G) new radio (NR) communication operating in frequency range 2 (FR2) utilizes multiple millimeter-wave (mm-wave) frequency bands to support high-data-rate wireless communication [1]. Among the FR2 bands, n257 (26.5–29.5 GHz) and n260 (37–40 GHz) are widely adopted for 5G communication. Because different countries allocate different FR2 bands, dual-band RF front-end circuits supporting both the n257 and n260 bands are required for global 5G terminals.

In mm-wave communication systems, phased-array beamforming is widely adopted to compensate for the high free-space path loss at high frequencies [2,3]. In such systems, phase shifters control the beam direction by adjusting the relative phase of each channel. Therefore, accurate phase control with low insertion loss is essential, particularly for dual-band operation over multiple frequency bands.

There have been previous studies on frequency-reconfigurable phase shifters for 5G communication. A passive-type frequency-reconfigurable phase shifter was presented in [4]. By reconfiguring the inductors and capacitors in the passive phase-shifting network, optimized performance can be achieved in both the n257 and n260 bands. However, since it is a passive phase shifter, gain control is not possible and the insertion loss is relatively large. In addition, achieving very high phase resolution is difficult because the phase-shifting resolution depends on the number of control bits. An active-type frequency-reconfigurable phase shifter was presented in [5], where in-phase/quadrature (I/Q) generation is performed using a tunable RC–CR network and phase shifting is achieved by vector summation. However, gain control is not possible because the vector-summing core does not include gain-control functionality. Therefore, a frequency-reconfigurable active phase shifter with simultaneous gain and phase control is a suitable solution for dual-band beamforming systems.

To address this challenge, this article presents a frequency-reconfigurable dual-band phase shifter operating in the n257 and n260 bands for 5G communication. The phase-shifter topology was previously employed as a building block in the 28/37 GHz frequency-reconfigurable dual-band beamforming front-end integrated circuit (IC) reported in [6]. Whereas [6] focused on the implementation and system-level performance of the complete front-end IC, the present work provides a dedicated phase-shifter-level analysis and independent characterization of a separately fabricated standalone phase-shifter IC. The complete front-end IC in [6] demonstrated system-level performance including transmitter linearity, receiver noise performance, and modulated-signal measurements. In beamforming systems, high phase and gain resolutions together with low control errors are important for reducing phase-quantization effects and facilitating channel mismatch calibration, thereby improving beamforming accuracy [7]. Accordingly, accurate phase and gain control is an essential requirement for high-performance phased-array transceivers. In particular, the design trade-offs of the reconfigurable RC–RL polyphase filter (PPF) and vector-summing core are discussed in greater detail, and standalone gain/phase-control performance, RMS errors, power consumption, and chip area are newly presented. The proposed phase shifter is based on an active vector-summing architecture and provides simultaneous gain and phase control for beamforming applications. To support dual-band operation, a reconfigurable RC–RL PPF is employed for I/Q signal generation, reducing insertion loss and I/Q phase error in both operating bands. The phase shifter is implemented in a 28 nm fully depleted silicon-on-insulator (FDSOI) process and demonstrates accurate gain and phase control with low DC power consumption.

2. Architecture of the Proposed Frequency-Reconfigurable Dual-Band Active Phase Shifter

Figure 1 shows the overall architecture of the proposed frequency-reconfigurable dual-band active phase shifter, which consists of an input balun, an I/Q generator, a vector-summing core, control digital-to-analog converters (DACs), and an output-matching network. The input balun converts the single-ended RF input signal into differential signals for the subsequent differential signal processing blocks. The I/Q generator generates quadrature basis vectors with 90° phase difference for phase shifting. The vector-summing core combines the I and Q vectors with programmable weighting factors to realize the desired phase and gain states, while the gain and phase control DACs generate bias currents according to the selected digital control codes. The output-matching network transforms the output impedance of the vector-summing core to $50\ \Omega$. As shown in Figure 1, the circuit blocks can be classified into slightly frequency-sensitive, frequency-sensitive, and frequency-insensitive blocks. For dual-band operation, frequency reconfiguration is applied

only to the frequency-sensitive blocks, while the frequency-insensitive blocks are shared by both operating bands. The input balun is implemented using a wideband structure because its performance is less sensitive to impedance variation than the I/Q generator and output-matching network.

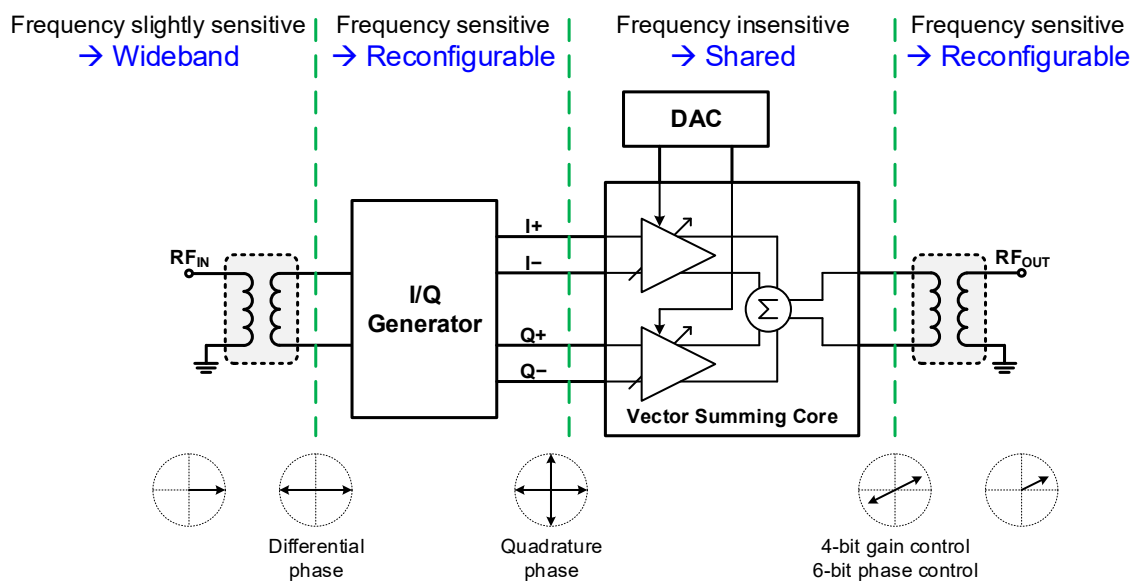


Figure 1. Overall architecture of the proposed frequency-reconfigurable dual-band active phase shifter.

3. Reconfigurable RC–RL PPF for Dual-Band I/Q Generation

3.1. Comparison of I/Q Generator Topologies

Several I/Q generator topologies have been reported for mm-wave phase shifters, including hybrid couplers, quadrature all-pass filters, and PPFs. Hybrid couplers can achieve low insertion loss and good quadrature accuracy, but they require a large chip area because of their distributed transmission-line structures. Quadrature all-pass filters are more compact but are sensitive to loading effects from subsequent stages [8,9]. Among these topologies, PPF-based I/Q generators are suitable for highly integrated CMOS phase shifters because of their compact implementation and their reduced sensitivity to the loading effect. Therefore, a PPF-based I/Q generator is adopted in this work.

When a PPF is used to support the widely separated n257 and n260 bands, a fixed broadband implementation and a frequency-reconfigurable implementation can be considered. Two-stage RC–RC and RC–RL PPFs provide relatively wide low-phase-error bandwidths around their respective design frequencies. However, a single fixed PPF does not maintain sufficiently low I/Q phase error over the entire frequency range from 26.5 to 40 GHz. The proposed PPF therefore reconfigures its capacitance and inductance to optimize the quadrature response separately for the n257 and n260 bands.

Another possible approach is to employ two independently optimized PPF paths, one for each frequency band. Although this approach can provide accurate I/Q generation in both bands, it duplicates the passive networks and routing and requires an RF path-selection interface, resulting in increased chip area, insertion loss, and parasitic loading. In contrast, the proposed reconfigurable PPF uses one shared signal path and changes only the frequency-dependent passive components. Because the PPF is passive, this reconfiguration does not require an additional active I/Q-generation core or static DC power. Therefore, the frequency-reconfigurable PPF provides a suitable trade-off among phase accuracy, insertion loss, chip area, and power consumption for the two widely separated bands.

3.2. RC–RC and RC–RL PPFs

To support dual-band operation, the capacitors and inductors in the PPF must be reconfigured according to the selected operating band. Figure 2 shows the schematics of reconfigurable RC–RC and RC–RL PPFs. As shown in Figure 2a, the RC–RC PPF suffers from impedance mismatch at two interfaces. The first mismatch occurs between the first and second stages, where the capacitive output impedance of the first stage drives the capacitive input impedance of the second stage. The second mismatch occurs between the second stage and the input of the vector-summing core, where the capacitive output impedance of the second stage drives a capacitive load. These two mismatches result in large insertion loss. In contrast, the RC–RL PPF shown in Figure 2b alleviates impedance mismatch at both interfaces. The first RC stage is connected to the second RL stage, which provides impedance compensation between the two stages. In addition, the inductive output impedance of the second RL stage compensates for the capacitive input impedance of the vector-summing core, thereby reducing insertion loss.

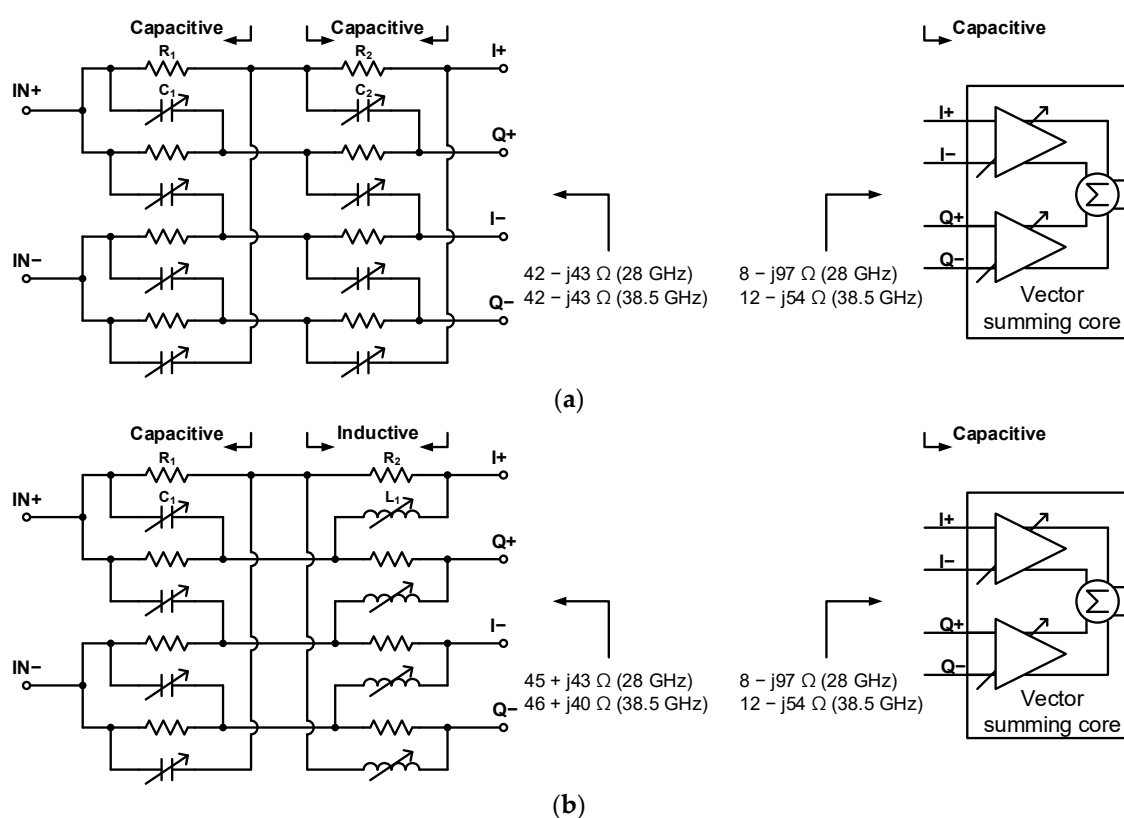


Figure 2. Reconfigurable PPF schematics: (a) RC–RC PPF; (b) RC–RL PPF.

Figure 3 compares the simulated I/Q amplitude imbalance, I/Q phase error, and insertion loss of 1-stage RC, 2-stage RC–RC, and 2-stage RC–RL PPFs at 28 GHz and 38.5 GHz. The insertion-loss comparison was performed using ideal R, C, and L components, and all PPF topologies were evaluated under the same loading condition by connecting the vector-summing core. In both frequency bands, the 1-stage RC PPF exhibits a very narrow bandwidth over which the I/Q phase error remains low, making it unsuitable for dual-band I/Q generation. In contrast, both 2-stage RC–RC and RC–RL PPFs exhibit wideband I/Q phase-error characteristics and nearly identical I/Q amplitude imbalance and phase-error performance. However, the RC–RL PPF achieves 9 dB lower insertion loss than the RC–RC PPF because the RL second stage alleviates the impedance mismatch, both between the two PPF stages and at the interface to the vector-summing core, thereby

reducing the insertion loss while maintaining nearly identical I/Q amplitude imbalance and phase-error characteristics. Therefore, the reconfigurable RC–RL PPF is selected as the I/Q generator for the proposed dual-band phase shifter.

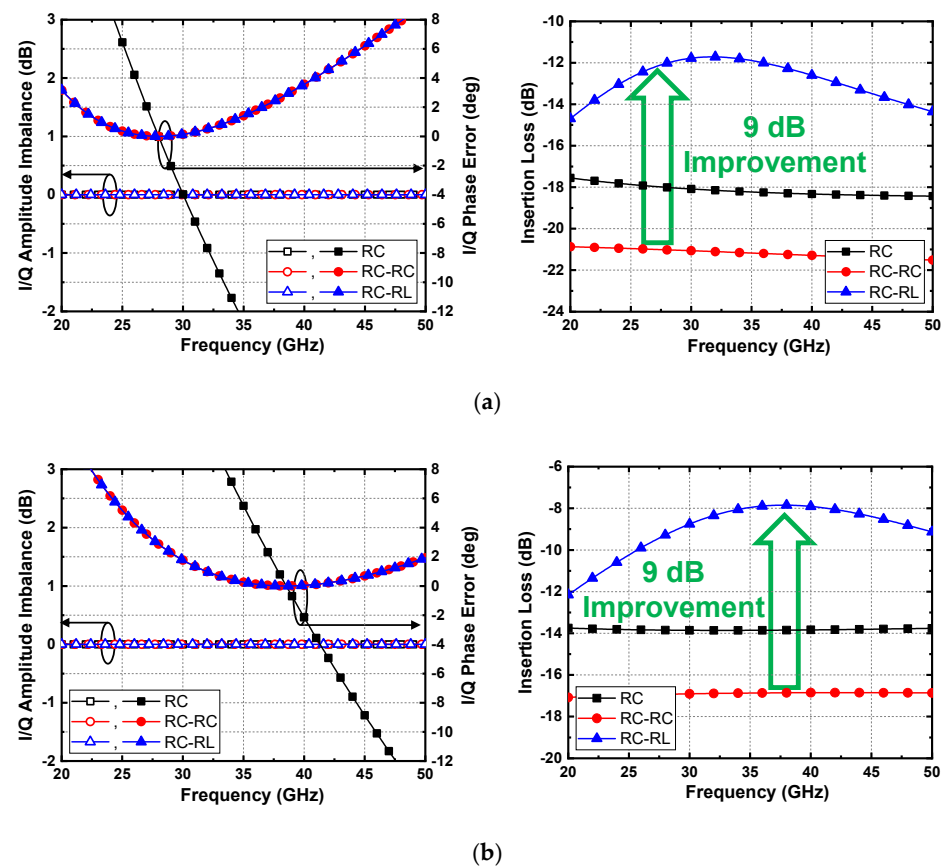


Figure 3. Simulated I/Q amplitude imbalance, I/Q phase error, and insertion loss of 1-stage RC PPF, 2-stage RC–RC PPF, and 2-stage RC–RL PPF: (a) n257 mode and (b) n260 mode.

3.3. Proposed Reconfigurable RC–RL PPF

The quadrature center frequencies of the RC and RL stages are determined by Equations (1) and (2), respectively.

$$f_0 = \frac{1}{2\pi RC} \quad (1)$$

$$f_0 = \frac{R}{2\pi L} \quad (2)$$

For the n257 mode centered at 28 GHz, the equivalent capacitance and inductance are 67 fF and 483 pH, respectively. For the n260 mode centered at 38.5 GHz, they are changed to 49 fF and 351 pH, respectively. These equivalent values are selected to minimize the I/Q phase error around each operating frequency. The switched capacitor and reconfigurable inductor change these equivalent values according to the selected operating mode, thereby shifting the quadrature center frequency to the desired frequency band.

Based on the analysis in Sections 3.1 and 3.2 and the above design procedure, the proposed RC–RL PPF is implemented to support dual-band operation with a compact layout. The center frequency of the PPF is tuned by reconfiguring the capacitors and inductors according to the selected operating band.

Figure 4a shows the schematic of the proposed reconfigurable RC–RL PPF. The first stage is implemented as an RC PPF using switched capacitors, while the second stage is

implemented as an RL PPF using reconfigurable inductors. The reconfigurable inductor is implemented by selectively bypassing a portion of the inductor through a switch, thereby providing two effective inductance values for the n257 and n260 operating modes. By changing the effective capacitance and inductance, the center frequency is shifted to support both n257 and n260 modes. The switch settings for each operating mode are summarized in Table 1. Figure 4b shows the layout of the proposed PPF. To reduce layout area and routing complexity, the first-stage RC PPF is placed inside the second-stage RL PPF. This integrated layout reduces layout area and enables closely matched routing lengths, allowing accurate quadrature signal generation.

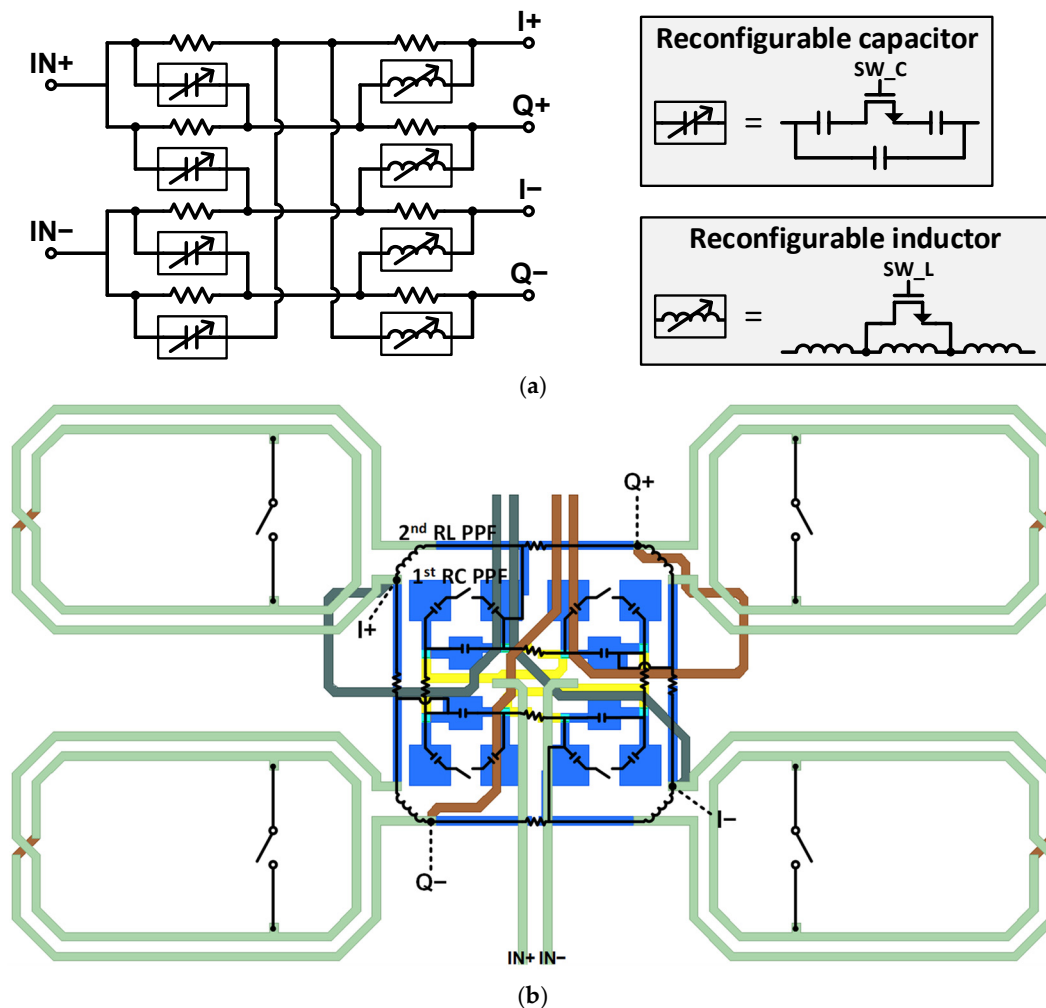


Figure 4. Proposed reconfigurable RC-RL PPF: (a) circuit schematic and (b) layout.

Table 1. Switch control for n257 and n260 mode selections in the proposed reconfigurable RC-RL PPF.

Operating Mode	SW_C	SW_L
n257	ON	OFF
n260	OFF	ON

4. Variable-Gain Vector-Summing Core

After quadrature signals are generated by the reconfigurable PPF, the proposed vector-summing core performs phase shifting and gain control through vector summation. The core consists of a vector-summing amplifier, quadrant selection double-pole double-throw (DPDT) switches, and gain and phase control DACs, as shown in Figure 5.

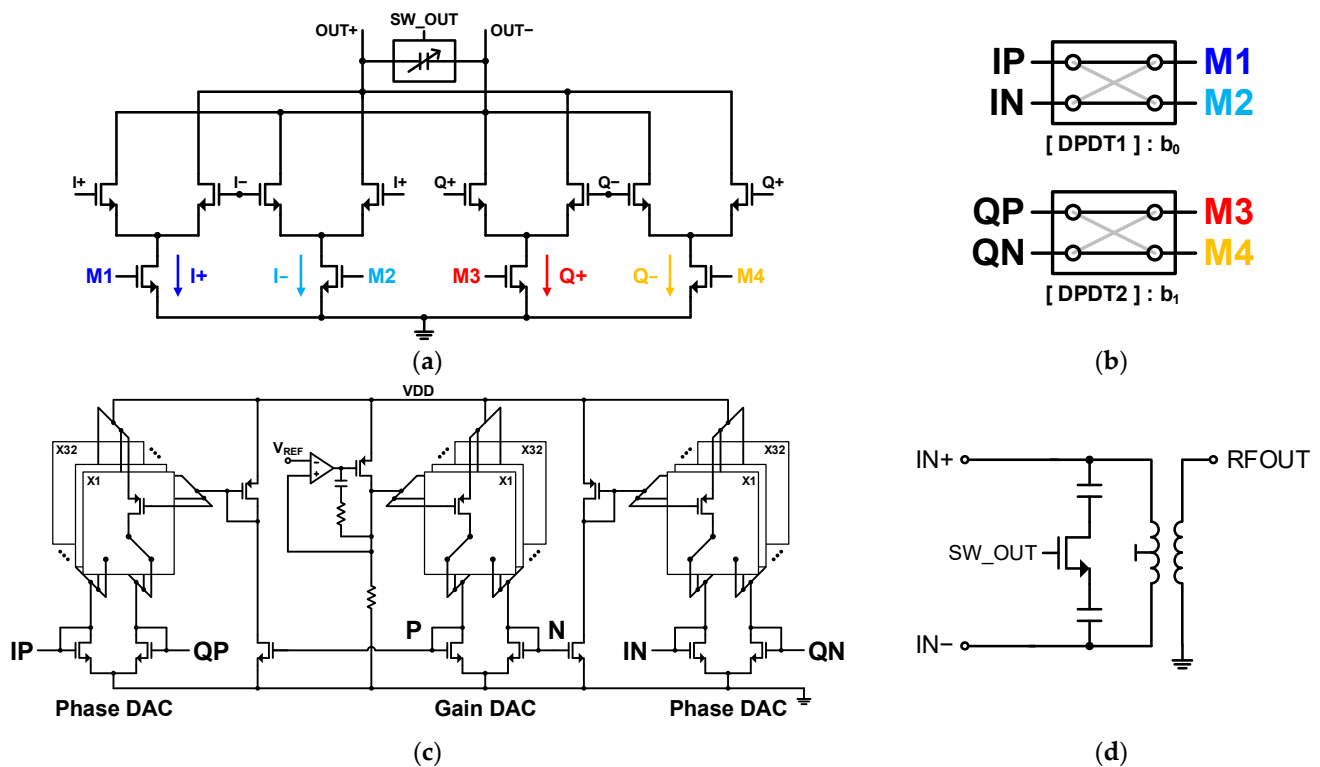


Figure 5. Proposed variable-gain vector-summing core: (a) vector-summing amplifier with switched output capacitor; (b) quadrant selection DPDT switches; (c) gain- and phase-control DACs; and (d) reconfigurable output network consisting of a switched capacitor controlled by SW_OUT and an output transformer.

Figure 5c shows the gain- and phase-control DACs. The gain of the vector-summing core is determined by the current ratio between P and N controlled by the gain DAC. The output phase is determined by the current ratio between the I and Q signals controlled by the phase DACs. By steering the weighted currents, discrete gain and phase states can be generated. Figure 5a shows the vector-summing amplifier. The weighted I/Q currents are summed to generate the output signal with the desired gain and phase. To support dual-band operation, Figure 5d shows the proposed reconfigurable output network. A switched capacitor controlled by SW_OUT is placed at the differential output of the vector-summing amplifier and operates together with the output transformer. By changing the effective output capacitance according to the selected operating mode, the output impedance response is reconfigured for the n257 and n260 bands. Figure 5b shows the quadrant selection DPDT switches, which control the polarity of the I and Q signals to enable full 360° phase coverage.

5. Measurement Results

The proposed frequency-reconfigurable dual-band phase shifter was fabricated in a 28 nm FDSOI process. Figure 6 shows the chip photograph of the fabricated phase shifter. The core area is 0.26 mm². The fabricated chip was mounted on an FR-4 PCB and characterized using ground-signal-ground RF probes. A standard short-open-load-through calibration was performed up to the probe tips before measurement, and no additional de-embedding was applied. All measurements were conducted with a 1.1 V supply voltage and a vector-summing core bias voltage of 1.1 V. S-parameters were measured using an Anritsu 37397D vector network analyzer. All measurements were performed at room temperature. The proposed chip integrates a DAC and serial peripheral interface (SPI) to control the phase and gain states. During the measurement, all phase and gain states

were sequentially configured by programming the on-chip DAC through the SPI interface, thereby validating the full 360° phase coverage and the 16 dB gain-tuning range.

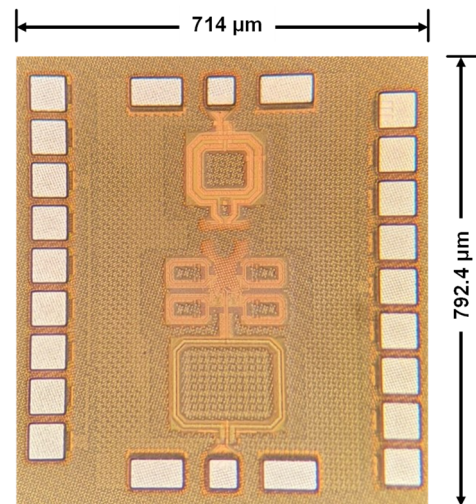


Figure 6. Chip photograph of the fabricated frequency-reconfigurable dual-band phase shifter.

Figure 7 shows the measured S-parameters and phase- and gain-control performances of the proposed phase shifter in the n257 and n260 modes. In the n257 mode, input and output matching are achieved in the low-frequency band, while in the n260 mode, input and output matching are achieved in the high-frequency band. The measured maximum gain is -4.3 dB in the n257 mode and -6.4 dB in the n260 mode. The measured vector constellations show that all phase states cover the full 360° range in both operating modes. The proposed phase shifter achieves 6-bit phase control with a phase resolution of 5.625° and 4-bit gain control with a 16 dB gain-control range.

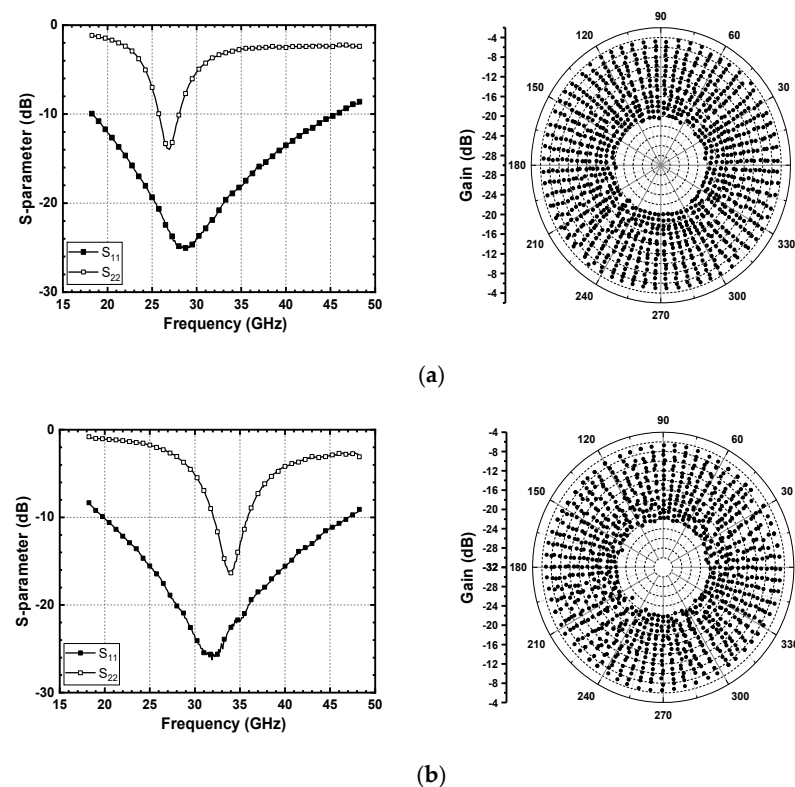


Figure 7. Measured S-parameters and phase- and gain-control performances: (a) n257 mode and (b) n260 mode.

Figure 8 shows the measured RMS phase and gain errors over frequency. At each frequency, the RMS phase and gain errors were calculated using all combinations of the 64 phase states and the 16 calibrated gain settings. The measured gain settings exhibit monotonic 1 dB gain steps over a 16 dB gain-control range. In the n257 mode, the RMS phase error is below 1.18° , and the RMS gain error is below 0.26 dB. In the n260 mode, the RMS phase error is below 1.5° , and the RMS gain error is below 0.35 dB, demonstrating accurate gain and phase control in both operating bands.

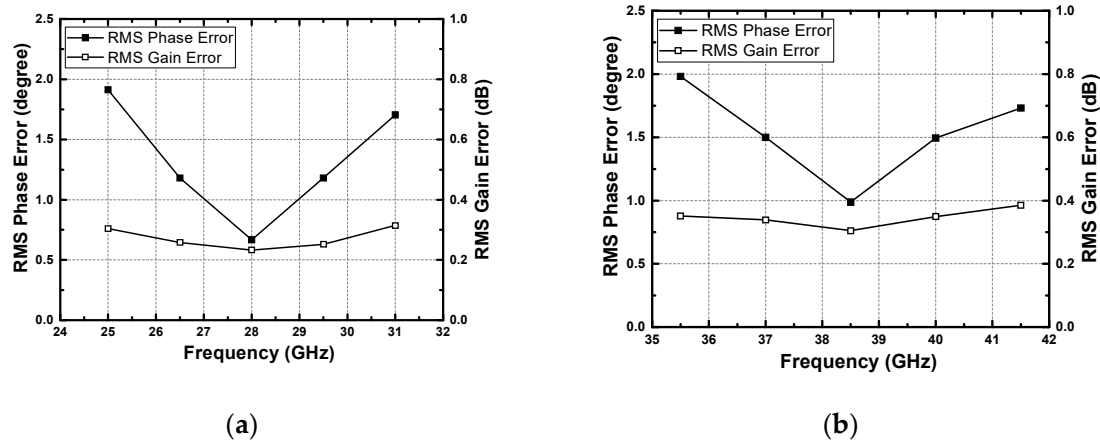


Figure 8. Measured RMS phase and gain errors in (a) n257 mode and (b) n260 mode.

Table 2 summarizes the performance of the proposed phase shifter and compares it with previously reported multi-band mm-wave phase shifters. The proposed phase shifter is the only design in the comparison table that supports gain control. It achieves the lowest phase and gain errors with the highest phase- and gain-control resolution. It also has the lowest power consumption among the compared works.

Table 2. Performance comparison with previously reported multi-band mm-wave phase shifters.

Parameter	This Work		[10]	[11]	[5]		[12]
Process	28 nm FDSOI		65 nm CMOS	45 nm SOI	90 nm CMOS		0.18 μ m BiCMOS
Frequency (GHz)	26.5–29.5	37–40	15–38	22–44	24–30	35–41	15–35
Phase-Control Resolution (bit/ $^\circ$)	6/5.625		6/5.625	5/11.25	Cont. ³		4/22.5 ³
Gain-Control Resolution (bit)	4		-	-	-		-
Max Gain/Gain-Control Range (dB)	-4.3/16	-6.4/16	-1.7/-	-7.5 ² /-	-4.5/-	-5.9/-	5/-
RMS Phase Error ($^\circ$)	<1.18	<1.5	2–3.5 ¹	<3 ¹	2–4 ¹	3.7–5.1 ¹	4.2–13 ¹
RMS Gain Error (dB)	<0.26	<0.35	0.7–1 ¹	<1.6 ¹	0.1–0.6 ¹	0.1–0.35 ¹	1–2.2 ¹
Power Dissipation (mW)	11	15.4	19.2	62	17.6 ⁴		25.2 ⁴
Core Area (mm ²)	0.26		0.16	0.7 ²	0.34		0.19

¹ Error by only phase control. ² Graphical analysis. ³ External DAC control. ⁴ Core power.

6. Conclusions

A frequency-reconfigurable dual-band variable-gain phase shifter implemented in a 28 nm FDSOI process is presented. A reconfigurable RC–RL PPF is proposed to generate I/Q signals with low phase and gain errors in both n257 and n260 bands for dual-band operation. A variable-gain vector-summing core is also implemented to simultaneously achieve phase and gain control.

The proposed phase shifter shows an RMS phase error below 1.18° and an RMS gain error below 0.26 dB over the 26.5–29.5 GHz frequency range. It shows an RMS phase error

below 1.5° and an RMS gain error below 0.35 dB over the 37–40 GHz frequency range. It achieves 6-bit phase control with a phase resolution of 5.625° and 4-bit gain control with a 16 dB gain-control range in both n257 and n260 bands.

The proposed frequency-reconfigurable architecture introduces additional passive switching elements to support dual-band operation, resulting in increased circuit complexity compared with a single-band implementation. Nevertheless, the measured results demonstrate that accurate gain and phase control can be maintained in both operating bands with low RMS phase and gain errors. The proposed architecture is expected to be applicable to future highly integrated beamforming transceivers.

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Conflicts of Interest: The authors declare no conflicts of interest.

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