

Article

A Voltage Spike Suppression Strategy for Arm Multiplexing Alternate Arm Converter

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Abstract

The arm multiplexing alternate arm converter (AM-AAC) can reduce the number of sub-module capacitors, but transient voltage spikes may appear at commutation instants when phase-shifted carrier pulse-width modulation (PSC-PWM) is used with a low submodule count. This paper analyzes the spike-generation mechanism from the discrete sampling behavior of symmetric regular sampling. The analysis shows that interleaved carrier phases produce nonuniform response delays among submodules, so the arm voltage follows a staircase transition rather than an ideal step change. After mirror folding by the commutation switches, this transition is coupled to the ac side as a voltage spike. Analytical expressions are derived for the spike duration and amplitude, revealing their dependence on the submodule number and phase-shift conduction angle. A suppression strategy is then proposed by shifting the carrier phase of the commutation switches so that commutation occurs near the midpoint of the spike duration. MATLAB R2024b simulations and RTDS hardware-in-the-loop experiments verify that the proposed method substantially reduces the spike amplitude without additional hardware, while PSC-PWM maintains lower output-current THD than nearest-level modulation in low-submodule AM-AAC applications.

Keywords: arm multiplexing alternate arm converter (AM-AAC); voltage spike; phase-shifted carrier; symmetric regular sampling; suppression method

1. Introduction

The modular multilevel converter (MMC) is a key enabling apparatus for large-scale renewable-energy grid integration and efficient power consumption. Owing to its modular design, high scalability, superior harmonic performance, and flexible power-flow and voltage-control capability, the MMC plays an indispensable role in connecting intermittent renewable energy sources, such as wind and photovoltaic generation, to power grids and in realizing high-capacity long-distance flexible transmission [1–3]. Existing studies show that, in an MMC system, capacitors can account for more than 50% of the total submodule volume and approximately 80% of the total submodule weight [4,5]. As the demand for higher power density and lightweight design continues to increase in applications such as offshore wind power, reducing the number and volume of submodule capacitors while maintaining converter performance has become a major research focus [6–8].



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Existing studies mainly optimize the original MMC topology to form new modular multilevel topologies, with the objective of reducing the number of submodule capacitors and related components.

- (1) References [9–11] adopt arm multiplexing technology. A multiplexing structure and the corresponding commutation switches are introduced into the topology, and the commutation switches are switched as required so that the multiplexing structure is inserted into either the upper arm or the lower arm. In this way, the submodule utilization is improved, and the required numbers of submodules and capacitors are reduced. Reference [9] mainly introduces a high-voltage dc capacitor as the multiplexing structure. When the upper or lower arm must output a relatively high voltage, the high-voltage dc capacitor is connected in series with the corresponding arm to support the voltage. During the remaining intervals, the required output voltage is lower, and the number of submodule capacitors can therefore be reduced. References [10,11] replace the flying capacitor with submodules, so that the output voltage can be adjusted to a rectified sinusoidal waveform. However, these topologies are constrained by energy balance and can operate only at a fixed modulation index.
- (2) The topologies reported in [12–15] consist of a multilevel voltage source converter (VSC) connected in series with cascaded submodules, which further improves submodule utilization. References [12,13] combine a two-level voltage source converter with cascaded submodules. The VSC operates at the fundamental frequency and generates $\pm 0.5 V_{dc}$ at the arm midpoint, which is combined with the output voltage of the cascaded submodules to synthesize the phase voltage; however, the topology can operate only at a fixed modulation index. References [14,15] replace the two-level converter with a three-level converter connected in series with cascaded submodules. Compared with the former topology, an additional zero level is introduced, and the operating range of the topology can be extended by adjusting the duration of this zero level.
- (3) References [16–18] propose an alternate arm converter (AAC) topology. Compared with the conventional MMC topology, the cascaded submodules no longer support the dc-side voltage. Instead, a high-voltage dc support capacitor is configured to maintain the dc-side voltage. The upper- and lower-arm cascaded submodules are not inserted simultaneously; rather, with the aid of commutation switches, they alternate between inserted and blocked states to generate the output voltage. This operation reduces the required arm output voltage and the number of submodule capacitors. Owing to energy-balance constraints, the AAC can operate only at the sweet spot [17]. To address this issue, [19–21] propose several solutions. Reference [19] proposes a short-overlap control method, in which MMC operation is emulated during the overlap interval to charge and discharge the submodules and achieve energy balance. Reference [20] shows that the conduction angle of the arm conduction switch can be coordinated with the power-factor angle to jointly regulate the energy balance of the submodule capacitors. Reference [21] proposes a third-harmonic injection method to extend the AAC modulation range.

Reference [22] proposes a new modular multilevel topology named the arm multiplexing alternate arm converter (AM-AAC). This topology combines the methods in the preceding categories (1) and (3), namely applying arm multiplexing technology to the AAC. As a result, submodule utilization is further improved, the capacitor requirement is reduced, and energy balance is achieved by introducing a phase-shifted conduction angle, so that the topology is not restricted to a fixed modulation index. The topology also provides ac fault ride-through capability and dc fault-current blocking capability. However, studies have shown that, in medium- and low-voltage distribution applications where

the number of cascaded submodules in the arm is small, nearest level modulation (NLM) is unable to suppress low-order harmonics effectively, causing severe current distortion and deteriorating power quality. Phase-shifted carrier PWM (PSC-PWM) can solve the problems associated with NLM. Nevertheless, experiments revealed a voltage spike in the AM-AAC at the commutation-switch transition instant that is not observed in simulation. This voltage spike not only degrades the system power quality but also produces an unexpected voltage difference with respect to the grid-side voltage, increases the voltage stress of power devices, and threatens the safe operation of the converter.

This converter-level safe operation issue also reflects the broader research emphasis on uncertainty awareness, security, and resilience in modern power-electronic-dominated systems. For example, ref. [23] investigated a system-level and macroscopic resilience-enhancement problem against uncertain cyber-physical coordinated attacks by considering power-communication network interdependence. Compared with this macroscopic power-system operation problem, the present paper focuses on a specific AM-AAC internal issue, namely, the voltage spike caused by the interaction between digital sampling and commutation. Therefore, the two studies address security and reliability at different levels, while both contribute to the safe operation of modern power systems.

A review of the relevant literature indicates that most voltage spikes are caused by rapidly varying inductor currents. Reference [24] describes a voltage spike caused by leakage inductance in a nonideal coupled inductor and proposes a topology that suppresses the spike by reducing the dc current. References [25,26] introduce passive snubber circuits and suppress voltage spikes by recovering leakage-inductance energy; however, these methods add many passive components and increase the system cost and volume. Reference [27] optimizes the switching control strategy to eliminate the voltage spike in the corresponding topology. The voltage spikes discussed in [28,29] are related to the high dv/dt and parasitic components during fast MOSFET switching transients. Reference [28] suppresses voltage spikes by improving the MOSFET gate-drive circuit, whereas [29] proposes reducing the switching frequency and output-side parasitic inductance to suppress output voltage spikes at the source.

The voltage spike investigated in this paper is fundamentally different from those reported above. A detailed analysis shows that the spike is not caused by an abrupt change in inductor current; instead, it is closely related to the discrete nature of the digital control system. Regular sampling, which is commonly used in engineering practice, cannot accurately track a discontinuity in the modulation wave. The sampled modulation signal decreases gradually in the form of a staircase waveform. Based on this mechanism, this paper establishes a mathematical model under symmetric regular sampling, accurately calculates the delay-time differences among different submodules, and proposes a voltage spike suppression strategy accordingly. The proposed strategy introduces specific carrier phase-shift control for the commutation switches and drives them to switch at the midpoint of the spike duration, thereby effectively reducing the spike level. The control strategy is simple and does not require any additional hardware structure that would increase the system cost and volume.

The novelty of this work is further clarified as follows. Existing PSC-PWM carrier-phase studies, such as the carrier phase displacement-angle optimization for modular multilevel converters in [30], mainly optimize the relative phase relationship among submodule carriers to improve steady-state modulation performance. In contrast, the voltage spike addressed in this paper is specific to the AM-AAC commutation process and is caused by the combined effect of symmetric regular-sampling delay, interleaved submodule carrier responses, and voltage folding by the commutation switches. Therefore, the proposed strategy does not re-optimize the submodule PSC-PWM carrier set; instead, it adjusts

the carrier phase used for commutation-switch signal generation so that the arm-mode transition occurs near the midpoint of the predicted spike interval.

The remainder of this paper is organized as follows. Section 2 introduces the topology and operating mechanism of the AM-AAC. Section 3 analyzes the mechanism and influencing factors of the AM-AAC voltage spike. Section 4 proposes a voltage spike suppression method and presents simulation and experimental results to verify its effectiveness. Section 5 compares the AM-AAC under NLM and PSC-PWM. Finally, Section 6 concludes this paper.

2. AM-AAC Topology and Operating Principle

2.1. Topological Structure

The topology of the AM-AAC is shown in Figure 1. Compared with the conventional AAC, the AM-AAC has only one arm in each phase. Each arm consists of cascaded half-bridge submodules (HBSM) and four groups of commutation switches. DS_{jp} and SS_{jp} ($j = a, b, c$) denote the positive-arm direction switch and the positive-arm selection switch, respectively, and they are mainly turned on simultaneously during the first half of the fundamental period. DS_{jn} and SS_{jn} denote the negative-arm direction switch and the negative-arm selection switch, respectively, and they are mainly turned on simultaneously during the second half of the fundamental period. The cascaded HBSMs are also referred to as the multiplexing shaping circuit (MSC). DS_{jp} , SS_{jp} , DS_{jn} , and SS_{jn} are collectively called commutation switches. u_s is the ac-side voltage, V_{dc} is the dc-side voltage, and v_{ssj} and i_{ssj} are the voltage and current of the MSC in phase j , respectively.

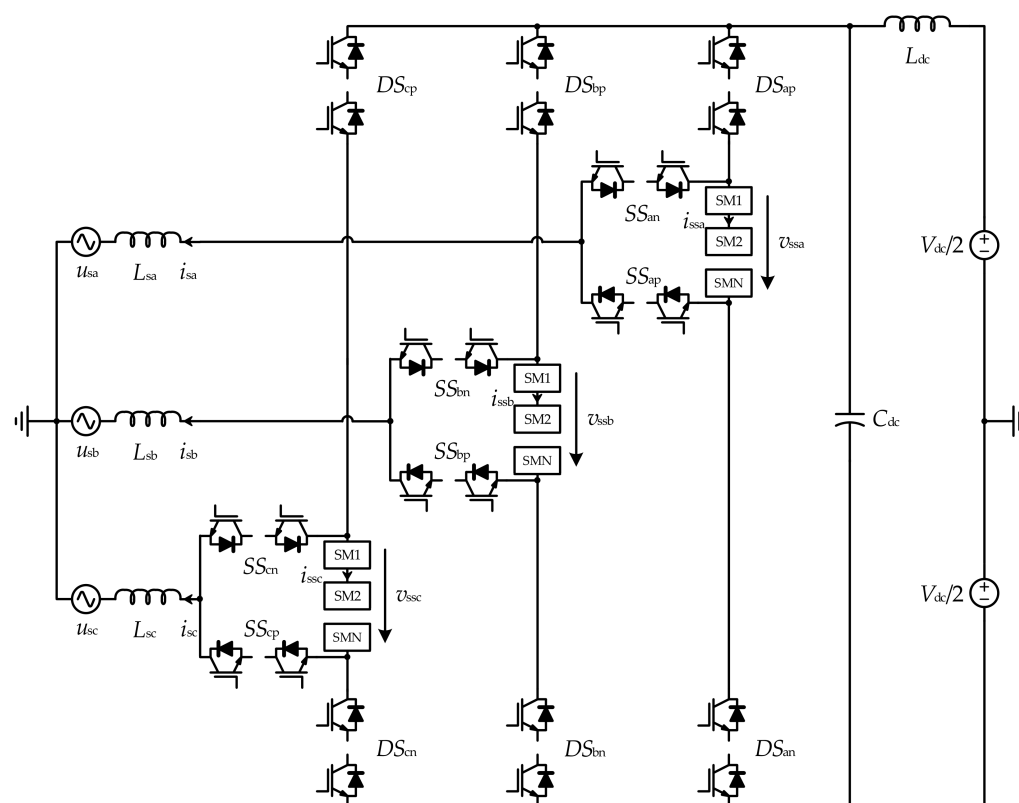


Figure 1. AM-AAC topology.

The grid-side voltage and current of the AM-AAC are expressed as follows:

$$\begin{cases} u_{sj} = V_m \sin(\omega t + \varphi_{0j}) \\ i_{sj} = I_m \sin(\omega t + \varphi_{0j} + \varphi) \end{cases} \quad (j = a, b, c) \quad (1)$$

2.2. Operating Principle

Because each phase of the AM-AAC has only one arm, the arm must operate in a multiplexed manner to achieve the operating effect of an AAC, alternating between the positive-arm and negative-arm modes. This function can be realized by properly controlling the commutation switches. Taking phase a as an example, Figure 2 shows the conduction states of the commutation switches and the current flow paths in the positive-arm multiplexing mode and negative-arm multiplexing mode, respectively, while Table 1 lists the conduction states of different switches under different operating modes.

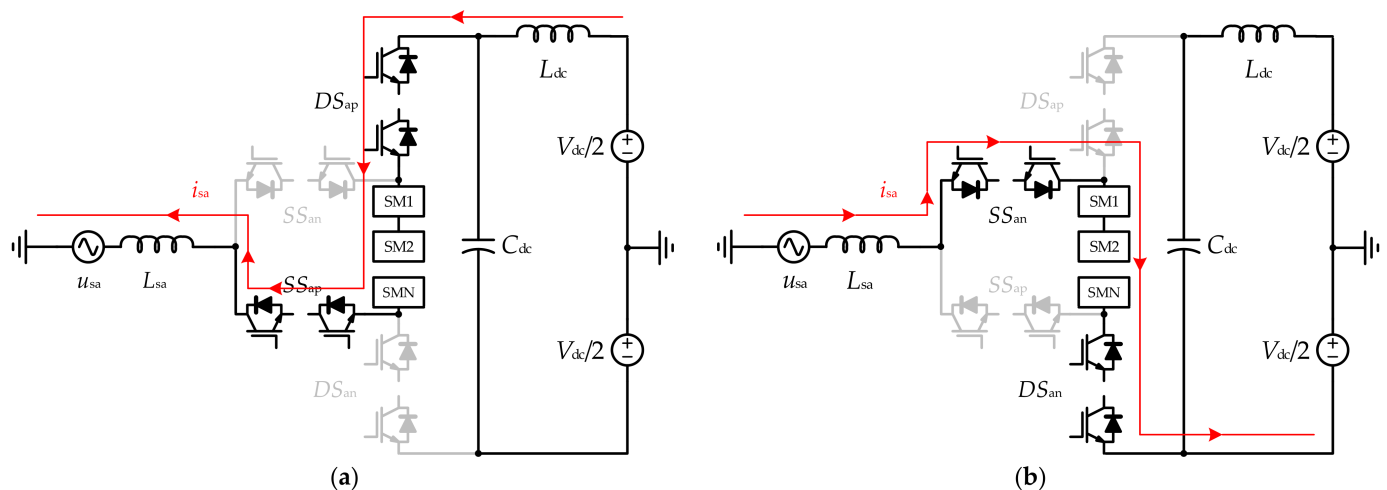


Figure 2. Current flow paths under different multiplexing modes: (a) $i_{sa} > 0$, P-AMM. (b) $i_{sa} < 0$, N-AMM.

Table 1. Operating modes of the AM-AAC.

Operating Mode	Switch State (1: on, 0: off)			
	SS _{ap}	SS _{an}	DS _{ap}	DS _{an}
P-AMM	1	0	1	0
N-AMM	0	1	0	1

Based on these two operating modes of the AM-AAC and Kirchhoff's law, the voltage equations of the MSC under different operating modes can be written as follows:

$$v_{ssa} = \begin{cases} \frac{V_{dc}}{2} - V_m \sin(\omega t), & \omega t \in [0, \pi] \\ \frac{V_{dc}}{2} + V_m \sin(\omega t), & \omega t \in [\pi, 2\pi] \end{cases} \quad (2)$$

2.3. Energy-Balance Analysis of the AM-AAC

The conventional AAC has an energy-balance problem and can operate only in the sweet-spot mode with a fixed modulation index M :

$$M = \pi/4 \quad (3)$$

The AM-AAC has the same problem. The current equation of the MSC is given by:

$$i_{ssa} = \begin{cases} I_m \sin(\omega t + \varphi), & \omega t \in [0, \pi] \\ -I_m \sin(\omega t + \varphi), & \omega t \in [\pi, 2\pi] \end{cases} \quad (4)$$

Combining (2) and (4), the energy inside the MSC over one period is calculated as follows:

$$\Delta E_{ap} = \int_0^T v_{ssa} \cdot i_{ssa} dt = \frac{2I_m \cos \varphi}{\omega} \left(V_{dc} - \frac{\pi V_m}{2} \right) \quad (5)$$

To balance the energy of the submodules inside the MSC, the energy inside the MSC over one period is set to zero:

$$\Delta E_{ap} = 0 \quad (6)$$

Thus,

$$V_m = \frac{2}{\pi} V_{dc} \quad (7)$$

Therefore, without any additional control method, the AM-AAC can also operate only in the sweet-spot mode with a fixed modulation index M , as shown in (7). To overcome this limitation, phase-shifted conduction is introduced, and the switching instant between the P-AMM and N-AMM modes of the MSC is delayed by a phase angle α , thereby extending the operating range of the AM-AAC.

The corresponding MSC voltage and current are then rewritten as follows:

$$v_{ssa} = \begin{cases} \frac{V_{dc}}{2} - V_m \sin(\omega t), & \omega t \in [\alpha, \pi + \alpha] \\ \frac{V_{dc}}{2} + V_m \sin(\omega t), & \omega t \in [\pi + \alpha, 2\pi + \alpha] \end{cases} \quad (8)$$

$$i_{ssa} = \begin{cases} I_m \sin(\omega t + \varphi), & \omega t \in [\alpha, \pi + \alpha] \\ -I_m \sin(\omega t + \varphi), & \omega t \in [\pi + \alpha, 2\pi + \alpha] \end{cases} \quad (9)$$

The voltage waveform and phase-shifted conduction diagram are shown in Figure 3.

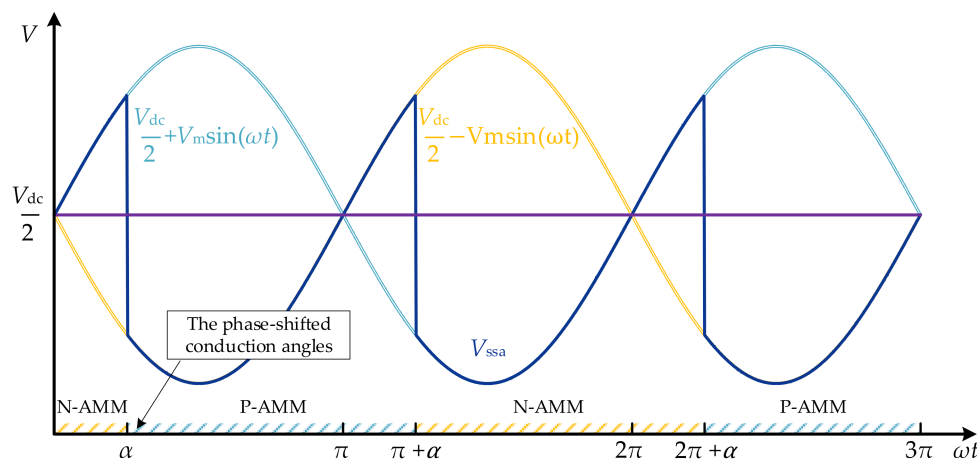


Figure 3. Schematic diagram of phase-shifted conduction.

The energy inside the MSC over one period is calculated as follows:

$$\Delta E_{ap} = \int_0^T v_{ssa} \cdot i_{ssa} dt = 2V_{dc} I_m \cos(\alpha + \varphi) - \pi V_m I_m \cos(\varphi) \quad (10)$$

To balance the energy of the submodules inside the MSC, the energy inside the MSC over one period is set to zero:

$$\Delta E_{ap} = 0 \quad (11)$$

Thus,

$$\alpha = \arccos\left(\frac{\pi}{4} M \cos \varphi\right) - \varphi \quad (12)$$

where M is the system modulation index, which is expressed as:

$$M = V_m / (V_{dc}/2) \quad (13)$$

It can be seen that the introduction of the phase-shifted conduction angle α achieves energy balance inside the MSC and extends its operating range, so that it is no longer restricted to the sweet spot. In addition, each phase has an independent phase-shifted conduction angle α , which enables the AM-AAC to operate under asymmetric grid faults.

3. Mechanism and Influencing Factors of AM-AAC Voltage Spikes

3.1. Mechanism of Voltage Spike Generation

Pulse-width modulation techniques are mainly divided into natural sampling (NS) and regular sampling (RS), among which symmetric regular sampling (SRS) is widely used in digital-control engineering applications. In NS, the continuous time-varying modulation wave is compared with the triangular carrier in real time, and the turn-on and turn-off instants of the switches are directly determined by the intersections of the two waveforms. Thus, sampling and comparison are fully synchronized in the time domain. However, a digital controller is limited by its discrete control clock and cannot track a continuous signal in real time. Taking SRS as an example, the controller samples the modulation wave only at the peak or valley of the triangular carrier and holds this sampled value constant within the current switching period. Consequently, the continuous modulation wave is represented inside the controller as a staircase waveform composed of piecewise constant values, which is then compared with the carrier to generate gate pulses. This discretization causes a time-domain deviation between the pulse edges of SRS and those of ideal NS, as shown in Figure 4. Table 2 shows the differences among various sampling methods.

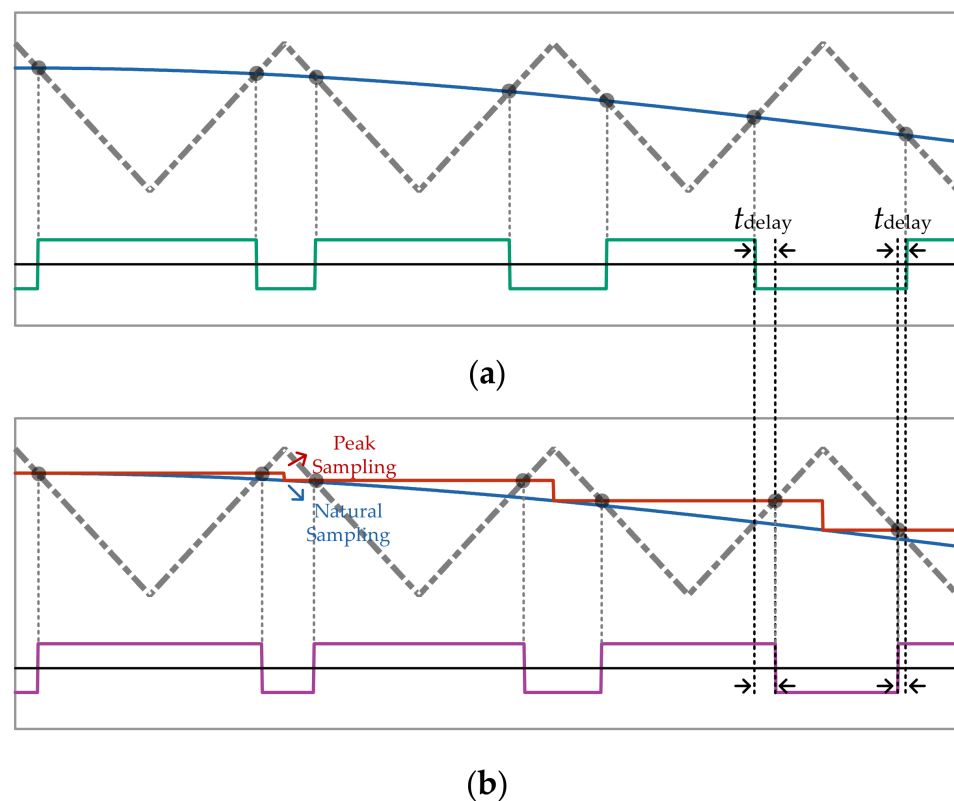


Figure 4. Natural sampling and regular sampling: (a) Natural sampling. (b) Regular sampling.

Table 2. Sampling method comparison.

Sampling Method	Sampling Procedure	Sampling Delay
Natural Sampling	Direct comparison with the carrier signal.	No
Regular Sampling	Sample-and-hold before comparison with the carrier signal.	Yes
Practical digital implementation	Regular sampling is typically adopted due to hardware constraints.	Typically yes

Evidently, because RS replaces the continuous modulation wave with a staircase waveform, the calculated switching action instant t_{RS} advances or lags the ideal NS action instant t_{NS} in the time domain. The magnitude of this time difference is positively correlated with the instantaneous dynamic rate of change dv/dt of the modulation wave. The time deviation introduced by sampling is defined as:

$$\Delta t_{\text{delay}} = t_{RS} - t_{NS} \quad (14)$$

The sign indicates whether the switching action is delayed or advanced. In a PSC-PWM scheme, the phases of multiple triangular carriers are uniformly shifted according to the number of submodules. Therefore, the sampling instants of the carriers associated with different submodules are interleaved in the time domain, causing the action deviation Δt_{delay} of different submodules to exhibit spatial discreteness and nonuniformity.

For the AM-AAC topology using PSC-PWM, when the modulation wave in the control system undergoes a step change near the alternate-commutation point, the actual switching instants of the submodule switches exhibit different degrees of time-domain delay or advance. Because the delay times of the power devices differ, the total cascaded arm output voltage v_{ssj} cannot accurately follow the transient step of the modulation wave. Instead, it exhibits the staircase transition behavior shown in Figure 5a. At the discontinuity of the modulation wave, the commutation switches perform the commutation action. Under ideal NS, when the upper and lower arms are alternately inserted, for example, from forward insertion to reverse insertion, the output voltage waveform is mirror-folded with respect to half of the dc-side voltage $V_{dc}/2$, allowing the converter ac side to output a smooth sinusoidal voltage waveform, as shown in Figure 5b. However, owing to the discrete nature of digital sampling, the tracking delay of PSC-PWM at the discontinuity breaks the dynamic balance of arm-voltage switching and excites a transient voltage spike at the converter ac-side output during commutation, as shown in Figure 5c. This voltage spike not only produces a transient voltage difference with the grid-side electromotive force and induces abrupt inrush current, but also significantly deteriorates the spectral quality of the output voltage and current and imposes severe dv/dt voltage-stress shocks on the arm components.

3.2. Influencing Factors of Voltage Spikes

The characteristics of the ac-side transient voltage spike can be quantitatively described mainly by two dimensions: spike duration and spike waveform amplitude. Accordingly, f_c is defined as the switching frequency, T_c as the switching period, and α as the phase-shifted conduction angle. In addition, f_w , T_w , and ω_w denote the fundamental frequency, fundamental period, and fundamental angular frequency, respectively; $t_{\text{delay}i}$ denotes the gate-response delay time of the i -th submodule, where $i = 1, 2, \dots, N$; and t_{delay} denotes the spike duration.

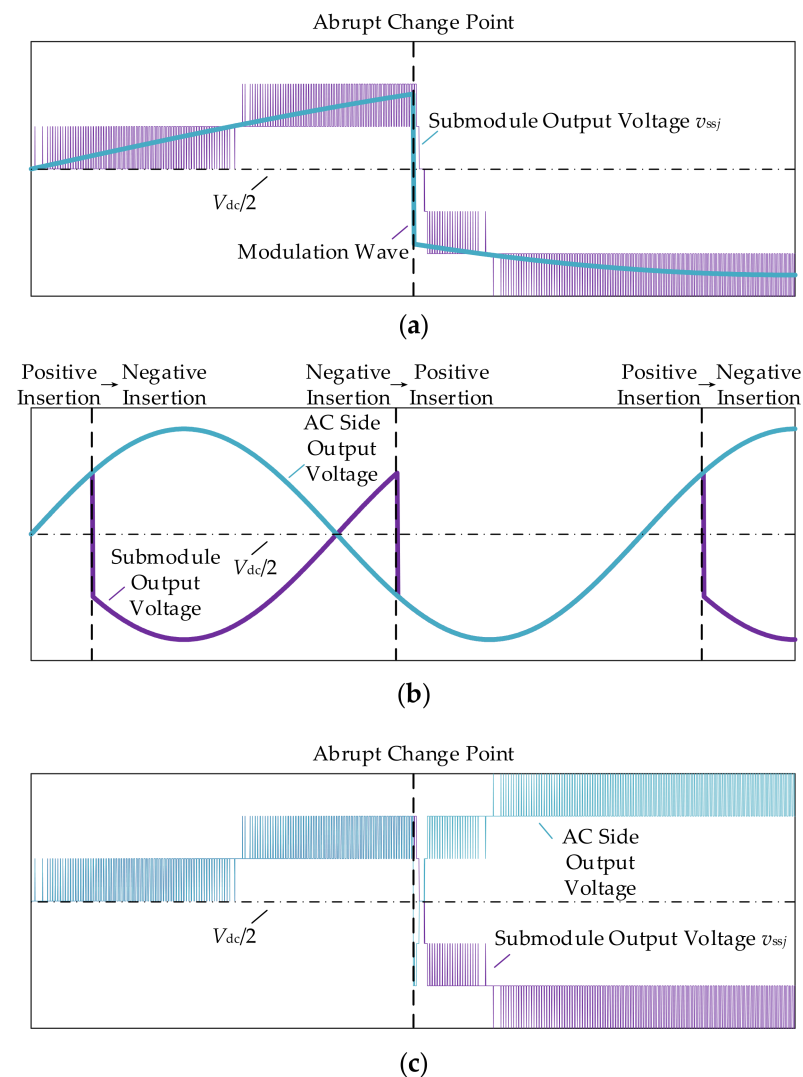


Figure 5. Voltage spike generation process: (a) Modulation wave and submodule output voltage. (b) Submodule and ac-side output voltages under ideal conditions. (c) Submodule and AC side output voltages under actual conditions.

3.2.1. Spike Waveform Amplitude

The spike waveform amplitude is analyzed next. As shown in Figure 5c, the spike magnitude is three levels. The spike is formed because the waveform generated by the PWM switching signals of the submodules cannot accurately track the modulation wave at its discontinuity. Therefore, the step signal at the discontinuity changes slowly as a staircase waveform. The waveform is folded with respect to $V_{dc}/2$ at the discontinuity, and thus the spike waveform amplitude is equal to two times the number of levels between the ac-voltage amplitude at the discontinuity and $V_{dc}/2$ minus one. The voltage spike amplitude is:

$$v_{\text{spike}} = \left[\text{ceil} \left(\frac{V_m |\sin \alpha|}{V_{CN}} \right) \times 2 - 1 \right] V_{CN} \quad (15)$$

where ceil denotes the ceiling function, and V_{CN} is the rated submodule capacitor voltage.

Figure 6 shows the relationship among the spike waveform amplitude v_{spike} , the number of submodules N , and the phase-shifted conduction angle α . The spike waveform amplitude v_{spike} exhibits an envelope similar to the absolute value of a sine function as α varies. As the number of submodules N increases, the relative proportion of the voltage spike to the dc bus voltage V_{dc} , namely its per-unit value, generally decreases

monotonically. It is worth noting that when the phase-shifted conduction angle α is 0 or $\pm\pi$, the spike waveform amplitude v_{spike} is zero.

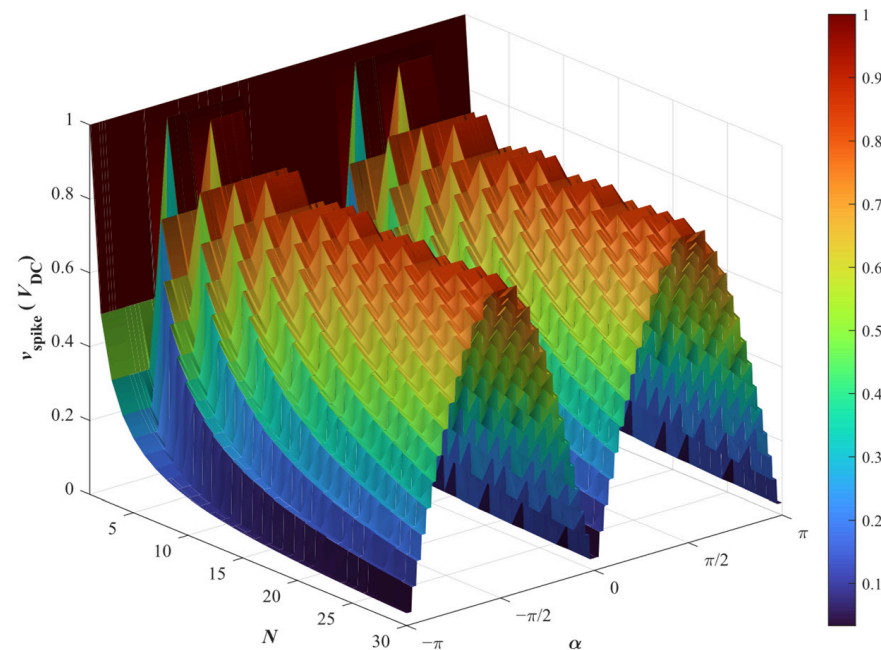


Figure 6. Theoretical variation of voltage spike amplitude.

3.2.2. Spike Duration

The time-domain duration of the voltage spike is mainly determined by the tracking-delay effect of the modulation strategy on the voltage step signal. In the AM-AAC topology, because of the inherent discrete-sampling characteristic of PSC-PWM, the controller cannot track the discontinuity of the modulation wave in real time. During the commutation transient, the control responses of different submodules exhibit different time-domain delays. Under the coordinated action of multiple submodules, the cascaded arm output voltage v_{ssj} can only decrease step by step as a staircase waveform. When this behavior is combined with the commutation actions of the arm direction switch and arm selection switch, a transient voltage spike is coupled to the ac side.

For a single submodule, taking peak sampling as an example, the delay time can be analyzed as follows.

During the conduction interval, the modulation signal of the cascaded submodules is:

$$v_{\text{ssa}} = \begin{cases} \frac{V_{\text{dc}}}{2} - V_{\text{m}} \sin(\omega t), & \omega t \in [\alpha, \pi + \alpha] \\ \frac{V_{\text{dc}}}{2} + V_{\text{m}} \sin(\omega t), & \omega t \in [\pi + \alpha, 2\pi + \alpha] \end{cases} \quad (16)$$

According to (16), the voltage discontinuity occurs at:

$$t_{\text{mut}} = \frac{k\pi + \alpha}{100\pi}, \quad k = 0, 1, \dots \quad (17)$$

The carrier peak instant corresponding to the i -th submodule is:

$$t_{\text{p}} = (0.5 - \frac{i-1}{N} + k)t_{\text{c}}, \quad k = 0, 1, \dots \quad (18)$$

Then $t_{\text{delay}i}$ is calculated as:

$$t_{\text{delay}i} = \left[1 - \text{mod} \left(\frac{\pi + \alpha}{100\pi T_c} - \frac{N - 2i + 2}{2N} \right) \right] T_c \quad (19)$$

The analysis shows that the submodule delay time lies within the following range:

$$t_{\text{delay}i} \in, (0, T_c] \quad (20)$$

According to the relative position between the triangular-carrier peak and the modulation-wave discontinuity, $t_{\text{delay}i}$ varies linearly from 0 to T_c .

The spike duration t_{delay} is the maximum of the delay times of these submodules:

$$t_{\text{delay}} = \max(t_{\text{delay}i}), i = 1, 2, \dots, N \quad (21)$$

It is worth noting that when the phase-shifted conduction angle α is 0 or $\pm\pi$, the spike waveform amplitude v_{spike} is zero. Therefore, (19), (20), and (21) are applicable only within the following range:

$$-\pi < \alpha < 0, 0 < \alpha < \pi \quad (22)$$

Figure 7 shows the relationship among the spike duration t_{delay} , the number of submodules N , and the phase-shifted conduction angle α within the range defined by (22). For a fixed α , t_{delay} increases with the number of submodules N and exhibits a rising trend similar to a logarithmic function. For a fixed N , the submodule delay time varies periodically with the phase-shifted conduction angle α . When the number of submodules N exceeds 10, t_{delay} remains above $0.9T_c$ regardless of the value of α .

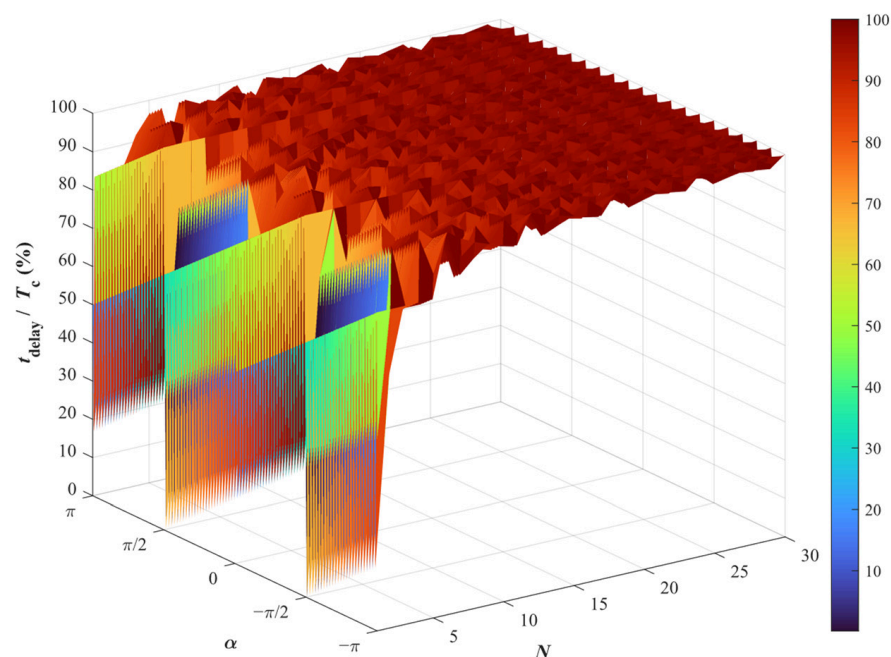


Figure 7. Theoretical variation of voltage spike duration.

It is worth noting that the delay analysis above is derived by taking the triangular carrier and symmetric regular sampling as an example, which is consistent with the digital PWM implementation used in the subsequent MATLAB simulation and RTDS platform. For other sampling schemes, such as asymmetric regular sampling, or for other carrier configurations, such as sawtooth or inverse-sawtooth carriers, similar delay phenomena can still occur when the sampling instants do not coincide with the modulation-wave

discontinuity. In such cases, similar analysis can also be conducted, but the delay expression should be recalculated according to the actual sampling instant distribution.

4. Voltage Spike Suppression Method for the AM-AAC

4.1. Suppression Method

Because carrier phase shifting cannot accurately track the step signal, the arm submodule output voltage waveform v_{ssj} is as shown in Figure 5c. When the commutation switches change from positive to negative at the discontinuity, the waveform is folded with respect to $V_{dc}/2$, and the spike magnitude is three levels. If the commutation switches change from positive to negative at the midpoint of the spike duration t_{delay} , the spike magnitude is suppressed to one level. The following subsection investigates how to control the commutation switches to switch at the midpoint of t_{delay} .

Compared with existing voltage-spike mitigation approaches based on passive snubbers, clamping circuits, or power-circuit modification, the proposed method requires no additional hardware and does not change the AM-AAC topology. Compared with conventional modulation optimization, the submodule PSC-PWM carrier arrangement is retained, while only the carrier phase of the commutation-switch signal is shifted according to the analytically derived spike duration. This makes the suppression strategy a timing correction targeted at the AM-AAC switching transition rather than a general harmonic-optimization method.

From the loss perspective, the proposed strategy does not alter the carrier frequency, duty ratio, or number of switching events of the cascaded submodules. It only shifts the existing commutation-switch transitions in time, while the total conduction duration over one fundamental period remains essentially unchanged. Therefore, no additional switching events are introduced, and the strategy is not expected to cause significant additional switching losses or thermal stress, although the switching energy may vary slightly because the shifted transitions occur at slightly different instantaneous voltage and current values.

4.2. Modulation Strategy

Section 3 derived the expression of the spike duration t_{delay} as follows:

$$t_{delay} = \max(t_{delayi}), i = 1, 2, \dots, N \quad (23)$$

When the commutation-switch delay time t_{delays} satisfies (24), the voltage spike can be effectively suppressed.

$$t_{delays} = 0.5t_{delay} \quad (24)$$

The switching signal of the commutation switches is also generated through carrier phase shifting. By changing the carrier phase-shift angle to control the delay time, the commutation switches can be made to switch at half of the spike delay time. Let the carrier phase-shift angle β of the commutation switches be:

$$\beta = \frac{2\pi}{N}m \quad (25)$$

Similarly, the commutation-switch delay time t_{delays} is obtained as:

$$t_{delays} = \left[1 - \text{mod} \left(\frac{\pi + \alpha}{100\pi T_c} - \frac{N - 2m + 2}{2N} \right) \right] T_c \quad (26)$$

Solving (24) gives m , from which the corresponding carrier phase-shift angle of the commutation switches is obtained. The commutation-switch signal is generated by comparing the switching reference with a triangular carrier having this phase-shift angle, thereby driving the commutation switches with PWM signals and suppressing the voltage spike.

The specific implementation process is shown in Figure 8. It is worth noting that the proposed method does not require online optimization, iterative calculation, additional closed-loop controllers, extra sensors, or modifications to the main circuit. Under a fixed operating condition, the carrier phase-shift angle of the commutation switches remains constant and therefore does not need to be updated in real time. When the operating parameters change, for example, when a change in the modulation index M leads to an updated phase-shifted conduction angle α , the spike duration and the corresponding commutation-switch carrier phase β can be updated through direct algebraic calculation or a pre-calculated lookup table. Therefore, the additional computational burden is negligible.

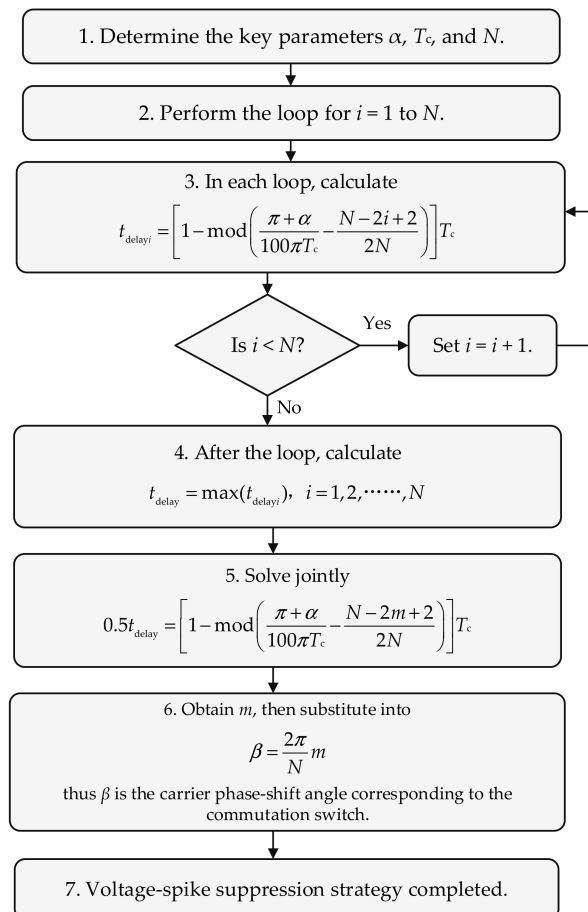


Figure 8. Flowchart of voltage spike suppression strategy.

For asymmetric operating conditions, the modulation reference, phase-shifted conduction angle, and commutation-switch timing of each phase can be determined independently. Accordingly, the carrier phase-shift angles β_a , β_b , and β_c can also be calculated and updated separately according to the operating condition of each phase. This phase-wise implementation allows the proposed strategy to be extended to asymmetric network conditions without introducing additional coupling among the three phase-control channels. Immediately after an abrupt parameter change, the previously calculated carrier phase may temporarily deviate from the new optimal value until the updated parameters are applied. Therefore, the transient suppression performance is related to the parameter-update and control-execution delay. Because the proposed method requires only direct calculation or table lookup, this additional update delay can be kept small in a digital implementation.

It should be emphasized that the expressions used to determine the commutation-switch carrier phase are obtained under the same triangular-carrier and symmetric-regular-sampling conditions as the preceding delay analysis. If a different sampling method or

carrier waveform is adopted, the proposed timing adjustment idea can still be used, but the corresponding delay expression and carrier-phase calculation should be re-derived according to the actual sampling sequence.

4.3. Simulation Verification

To verify the correctness of the theoretical analysis of the AM-AAC voltage spike generation mechanism and the effectiveness of the voltage spike suppression method, a discrete-time numerical simulation model of a single-phase open-loop AM-AAC was built in MATLAB. The model used the PSC-PWM strategy. The main electrical and control parameters of the system are listed in the following table.

Considering the discrete nature of the control execution in an actual digital microprocessor, symmetric regular sampling was adopted in the control logic of this simulation, and the modulation wave was processed using zero-order hold. The value of the modulation reference signal u_{ref} at the sampling instant t_k , namely the triangular-carrier peak, was held until the next sampling period, namely:

$$u_{\text{ref}}^*(t) = u_{\text{ref}}(t_k), t \in [t_k, t_{k+1}) \quad (27)$$

4.3.1. Verification of the Voltage Spike Phenomenon

Under the baseline simulation condition, the eight cascaded submodules of the single-phase arm correspond to eight triangular carriers with a fixed $\pi/4$ phase displacement on the time axis. Figure 9 shows the actual output voltage waveforms of the arm submodules. It can be clearly observed that, owing to the discrete characteristic of digital regular sampling, the submodules do not complete level switching at the same instant during the commutation interval where the modulation wave undergoes a step change. Instead, they respond sequentially according to their respective carrier peak sampling instants. According to the theoretical analysis above, the delay time t_{delay} of each submodule is determined by (19) and is distributed within the range from 0 to T_c . Consequently, the step decrease in the total cascaded arm voltage v_{ssa} at the modulation-wave discontinuity is decomposed into a series of staircase transitions with different delays. Together with the positive–negative switching action of the commutation switches at the discontinuity of the modulation wave, the v_{ssa} waveform is mirror-folded with respect to $V_{\text{dc}}/2$. The staircase descending waveform is coupled to the ac side after folding, forming the voltage spike shown in Figure 10, which agrees with the preceding theoretical derivation.

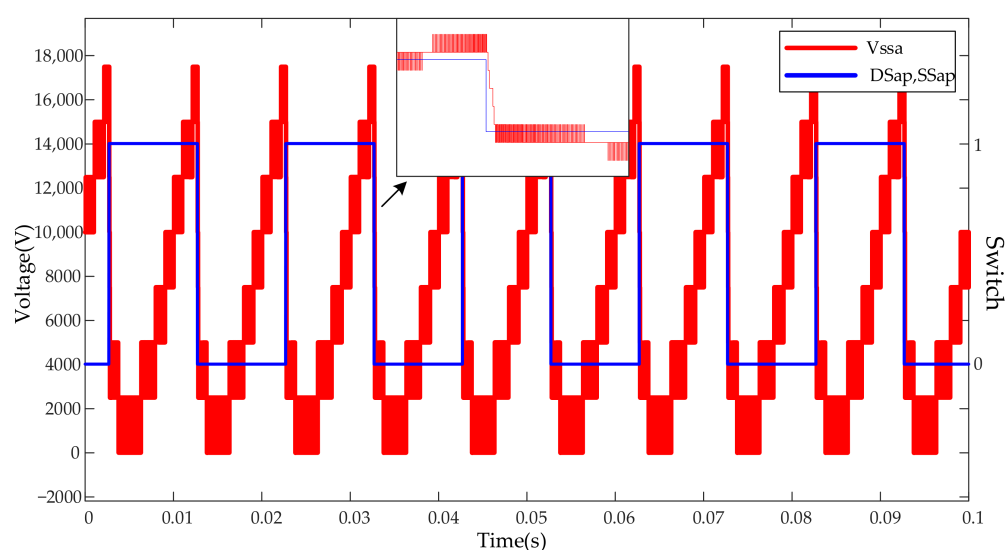


Figure 9. Arm submodule output voltage waveforms.

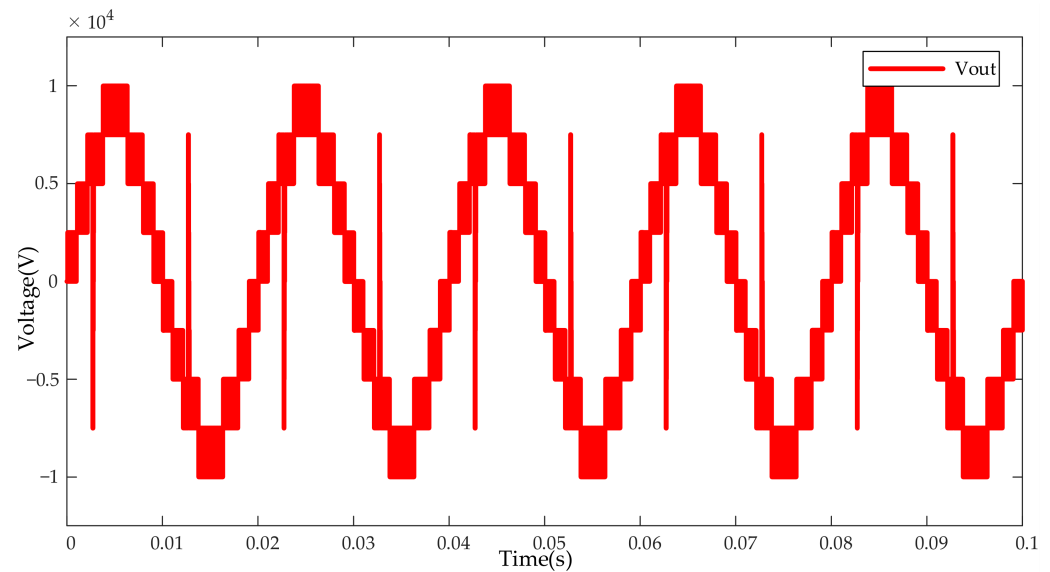


Figure 10. Converter output waveforms.

4.3.2. Experimental Verification of Factors Influencing Voltage Spikes

To verify the correctness of the theoretical analysis in Section 3.2 regarding the influencing factors of voltage spike duration and amplitude, this subsection uses the baseline simulation parameters in Table 3, keeps the dc-side voltage V_{dc} , modulation index M , power-factor angle φ , number of submodules N , and switching frequency f_c unchanged, and scans the phase-shifted conduction angle α over the range $[-\pi, \pi]$ with an interval of $\pi/6$. The spike duration t_{delay} and spike amplitude v_{spike} are measured, and the simulation results are compared with the theoretical calculations.

Table 3. Simulation parameters.

Parameter	Value
Dc-side voltage V_{dc}/V	20,000
Modulation index M	0.8165
System power-factor angle φ/rad	0
Number of submodules N	8
Rated submodule voltage V_{CN}/V	2500
Fundamental frequency f_w/Hz	50
Simulation time step T_s/s	1×10^{-6}
Switching frequency f_c/Hz	1×10^{-4}

First, the spike amplitude is verified. Figure 11 shows the comparison between the simulated measured value and theoretical calculated value of the voltage spike amplitude v_{spike} under different phase-shifted conduction angles α . In the simulation, v_{spike} is measured as the maximum absolute deviation of the ac-side output voltage from the ideal sinusoidal envelope within the spike interval. The theoretical value is calculated from (15). The comparison shows that the simulated measurements are basically consistent with the theoretical calculations, verifying the correctness of the theoretical analysis of the spike amplitude in Section 3.2.1.

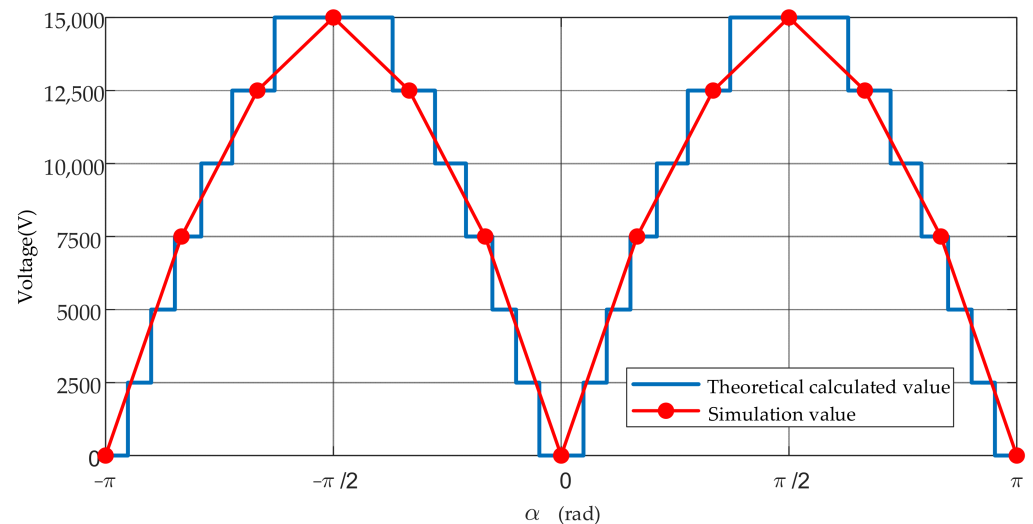


Figure 11. Verification of spike amplitude.

Second, the spike duration is verified. Figure 12 compares the simulated measured value and theoretical calculated value of the spike duration t_{delay} under different phase-shifted conduction angles α . In the simulation, t_{delay} is measured by taking the discontinuity instant of the modulation wave as the starting point and the instant when the ac-side output voltage returns to the normal sinusoidal envelope as the ending point; the time difference between the two instants is taken as the measured t_{delay} . The theoretical value is calculated by jointly solving (19) and (21). The comparison shows that the simulated measurements agree well with the theoretical calculations, verifying the correctness of the theoretical analysis of spike duration in Section 3.2.2. When $N = 8$, t_{delay} varies periodically with α and ranges from $0.875T_c$ to T_c . The physical reason for this fluctuation is that changing α shifts the position of the modulation-wave discontinuity on the time axis. Consequently, the relative distances between the carrier sampling instants of the submodules and the discontinuity vary, and the maximum delay time t_{delay} exhibits an α -dependent periodic variation.

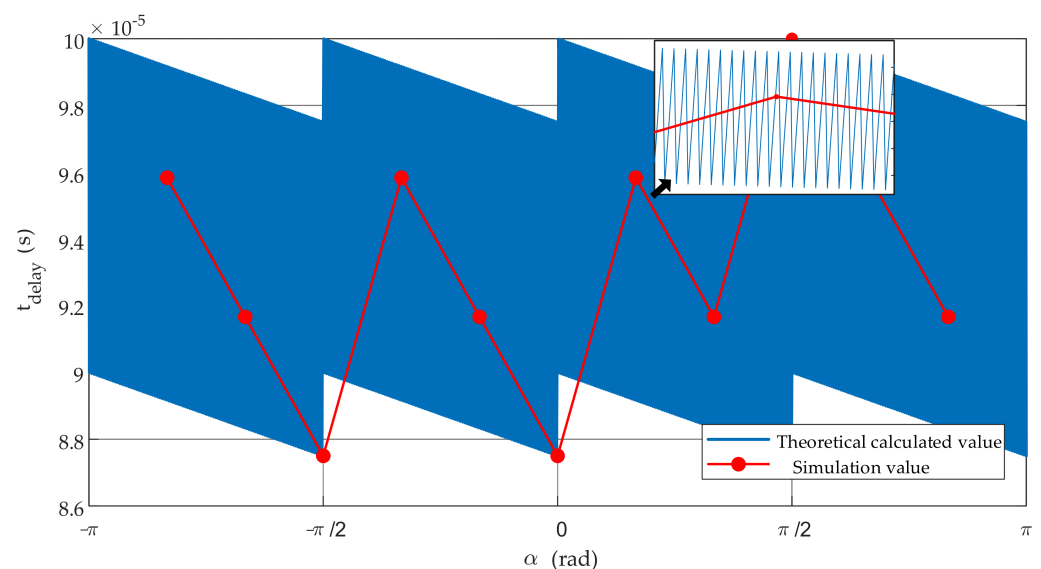


Figure 12. Verification of spike duration.

A small discrepancy between the theoretical and simulated spike durations can be observed in the enlarged view of Figure 12. This discrepancy mainly results from the simplification adopted in the analytical delay model. In the theoretical derivation, the submodule

delay is approximated by the interval between the modulation-wave discontinuity and the subsequent sampling and reference-update instant. In the actual symmetric-regular-sampling PWM process, however, the gate signal changes only when the held sampled reference intersects the triangular carrier. Consequently, the actual PWM response delay also includes a small carrier-comparison timing offset that is not included in the simplified analytical expression. In addition, the spike duration measured in the simulation is quantized by the fixed simulation time step of 1 μs . The simulation model used for this comparison employs ideal switches without dead time; therefore, dead-time effects do not contribute to the observed difference. Since the resulting deviation is small relative to the switching period, it does not materially affect the subsequent midpoint-based voltage spike suppression strategy.

Overall, for a fixed number of submodules N , the simulated measured spike duration and amplitude under different phase-shifted conduction angles α agree well with the theoretical analysis in Section 3.2. The numerical simulations fully verify the correctness of the theoretical derivation of the voltage spike influencing factors and provide reliable parameter support for the design of the subsequent voltage spike suppression strategy.

4.3.3. Voltage Spike Suppression

To ensure the energy balance of the AM-AAC topology, α is a fixed value in practice. As shown in Table 3, the simulated α was calculated as 0.8513 rad. Under this condition, the voltage spike amplitude v_{spike} and voltage spike duration t_{delay} were 12,500 V, or five levels, and 8.9×10^{-5} s, respectively. Combining (24) gives the commutation-switch delay time t_{delays} as 4.45×10^{-5} s. Jointly solving (26) gives $m = 0.658$. Therefore, the corresponding carrier phase-shift angle of the commutation switches was 0.5168 rad, namely 29.625° . After applying this angle in the simulation, the final converter ac-side output voltage waveform is shown in Figure 13. It can be seen that the voltage spike was suppressed from 12,500 V to 5000 V, indicating a significant suppression effect.

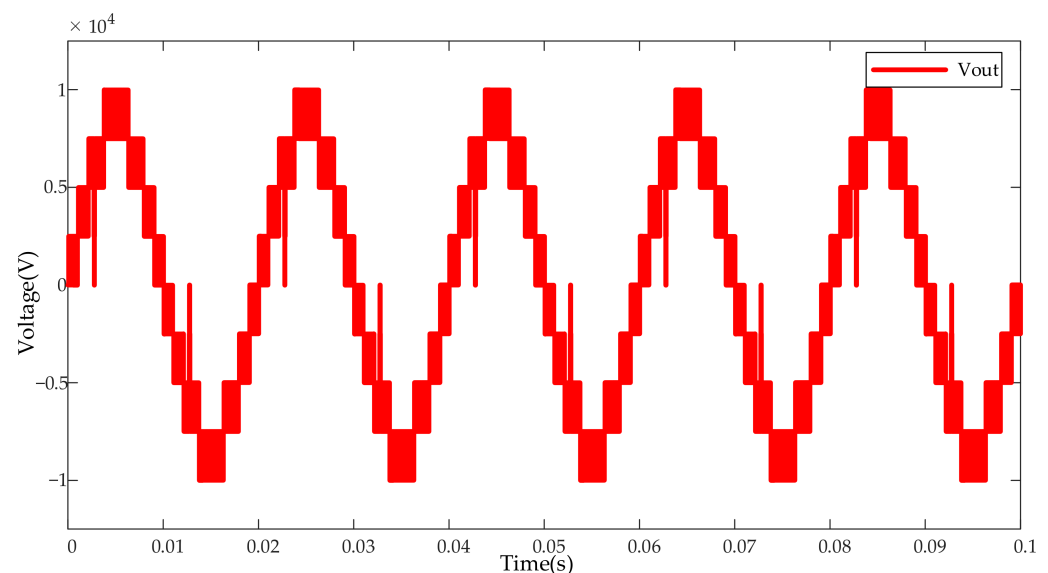


Figure 13. Simulink verification of voltage spike suppression.

4.3.4. Sensitivity Analysis

To further evaluate the robustness and practical applicability of the proposed suppression strategy, additional sensitivity simulations were performed on multiple key parameters including the number of submodules N , the phase-shifted conduction angle α , and the switching frequency f_c .

First, the phase-shifted conduction angle α and the other operating parameters were kept unchanged, while only the number of submodules N was varied. Figure 14a shows the voltage-spike amplitudes before and after the suppression. Next, N and the other operating parameters were kept unchanged, while only α was varied. The corresponding results are shown in Figure 14b.

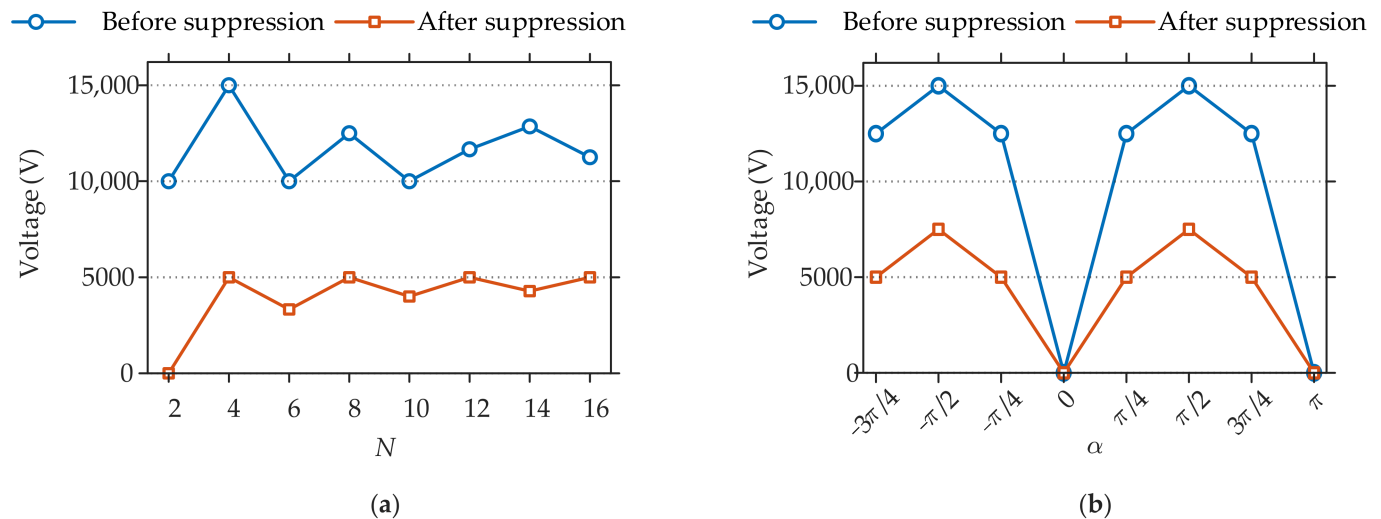


Figure 14. Sensitivity analysis of voltage-spike amplitude: (a) different numbers of submodules N with α fixed; (b) different phase-shifted conduction angles α with N fixed.

As shown in Figure 14a, although the spike amplitude changes with N , the proposed strategy consistently reduces it, confirming that the suppression method remains effective for different converter scales. Figure 14b shows that changing α also changes the spike amplitude because the relative timing between arm commutation and the carrier sampling instants is altered. Nevertheless, the spike amplitude is substantially reduced after suppression for all tested values of α , demonstrating the robustness of the proposed strategy against variations in the phase-shifted conduction angle.

Because the switching frequency does not directly affect the instantaneous voltage-spike amplitude, the ac-side output-current THD was selected as the performance index under different switching frequencies. For comparison, the THD obtained using NLM under the same operating conditions was also evaluated, as shown in Figure 15.

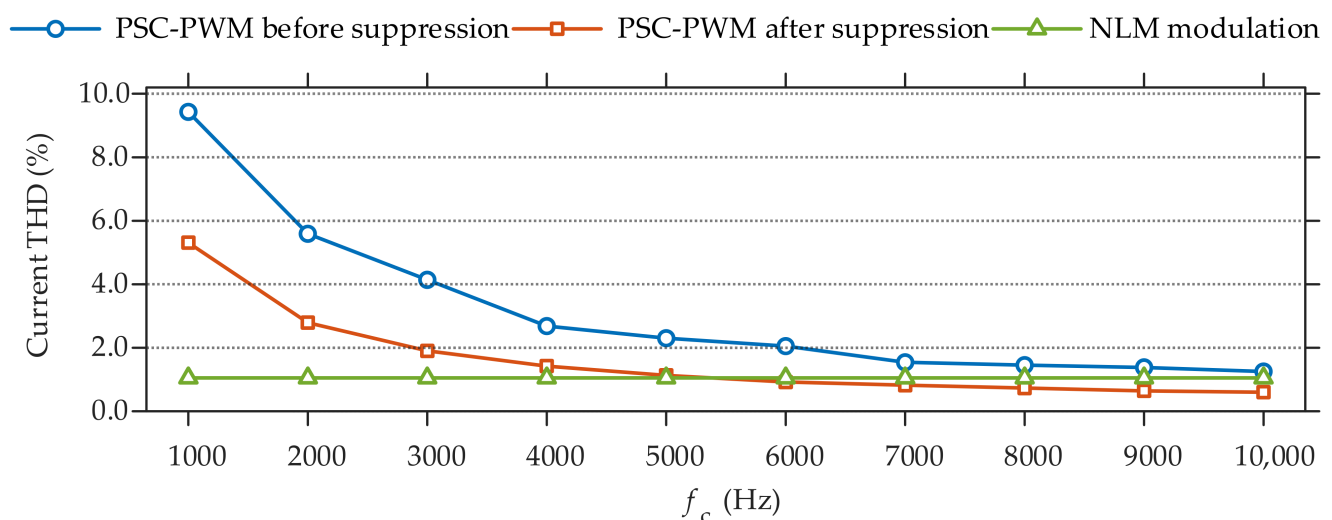


Figure 15. Output-current THD comparison under different switching frequencies.

At relatively low switching frequencies, the current THD of PSC-PWM is higher than that of NLM due to the voltage spike, regardless of whether the suppression strategy is applied. As f_c increases, the THD decreases. With the proposed suppression strategy, the PSC-PWM current THD becomes lower than that of NLM at higher switching frequencies. These results verify that the proposed strategy remains effective under different switching-frequency settings and can improve the output-current quality when PSC-PWM operates at a sufficiently high carrier frequency.

Finally, the sensitivity of the commutation-switch carrier phase-shift angle β to variations in the switching frequency f_c and sudden fluctuations in the DC-bus voltage V_{dc} was evaluated, and the corresponding results are presented in Tables 4 and 5.

Table 4. Sensitivity analysis of switching frequency variation.

f_c (kHz)	t_{delay} (μs)	β ($^\circ$)
8	0.9072	122.20
9	0.8595	104.84
10	0.8165	90.95
11	0.7776	79.59
12	0.7423	80.54

Table 5. Sensitivity analysis of dc voltage variation.

V_{dc} (kV)	M	β ($^\circ$)
18	0.9072	134.12
19	0.8595	263.14
20	0.8165	118.72
21	0.7776	29.31
22	0.7423	348.54

The sensitivity results show that the optimal commutation-switch carrier phase β varies relatively moderately with the switching frequency, whereas changes in the DC-bus voltage have a more pronounced influence because they alter the modulation index M and subsequently the phase-shifted conduction angle α . Nevertheless, the proposed strategy requires only direct algebraic calculation or a pre-calculated lookup table and does not require additional sensors or modifications to the existing control loop. Therefore, when small parameter variations occur, β can be updated with negligible computational burden. Moreover, since the voltage spike occupies only a very small fraction of each fundamental period, the probability that an occasional parameter fluctuation occurs exactly within the spike interval is relatively low.

4.4. Experimental Verification

On the basis of the Simulink simulation, a real-time digital simulation system (RTDS) was used for real-time digital emulation, as shown in Figure 16. The RTDS was controlled by an RTU-BOX205 real-time digital controller to conduct hardware-in-the-loop verification. The RTDS power circuit model operates with a fixed simulation substep of 5×10^{-6} s. The RTU-BOX205 only serves as a standalone digital controller. RTDS transmits the simulated voltage and current signals of the power circuit via its analog output (AO) board, which are sampled by the analog-to-digital converter (ADC) on RTU-BOX205. After control calculations, RTU-BOX205 generates PWM pulses and sends them back to RTDS through its digital input (DI) board to drive the circuit model inside RTDS. All waveform data for spike analysis are recorded at the 5×10^{-6} s resolution of RTDS, so aliasing artifacts are eliminated during peak evaluation.



Figure 16. Experimental platform.

The experimental parameters were scaled down by a factor of 1000 from the preceding simulation parameters. When voltage spike suppression was not applied, the output voltage waveform is shown in Figure 17. The voltage spike was five levels, with an amplitude of 12.5 V.

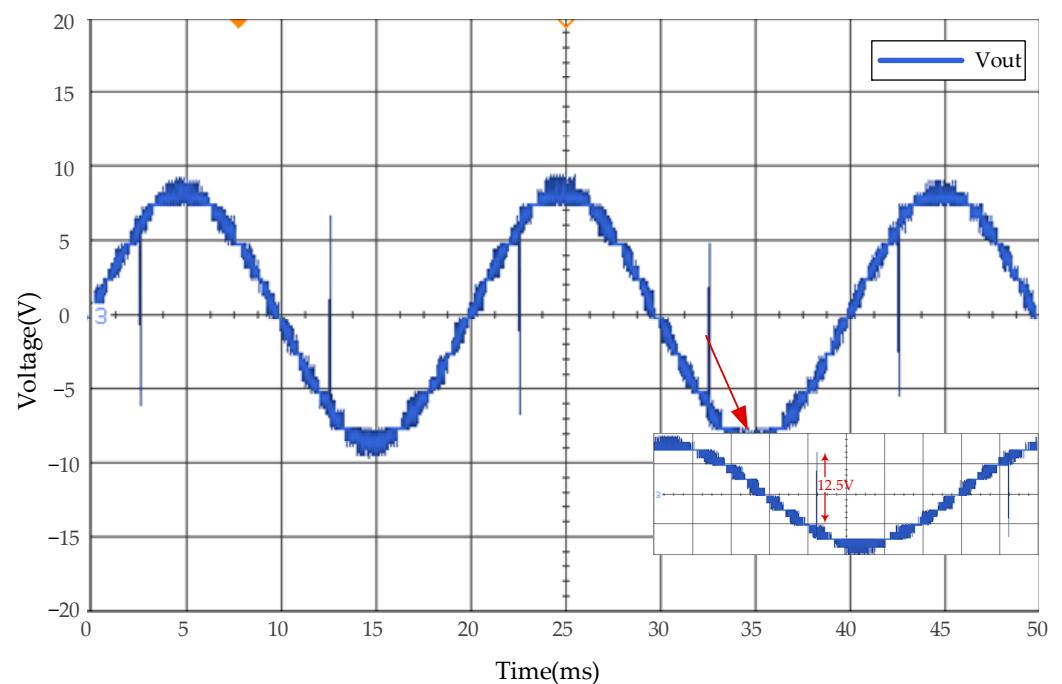


Figure 17. Experimental voltage waveform.

After applying the voltage spike suppression method, the output voltage waveform was as shown in Figure 18. The voltage spike was suppressed to two levels, with an amplitude of only 5 V, showing a significant suppression effect.

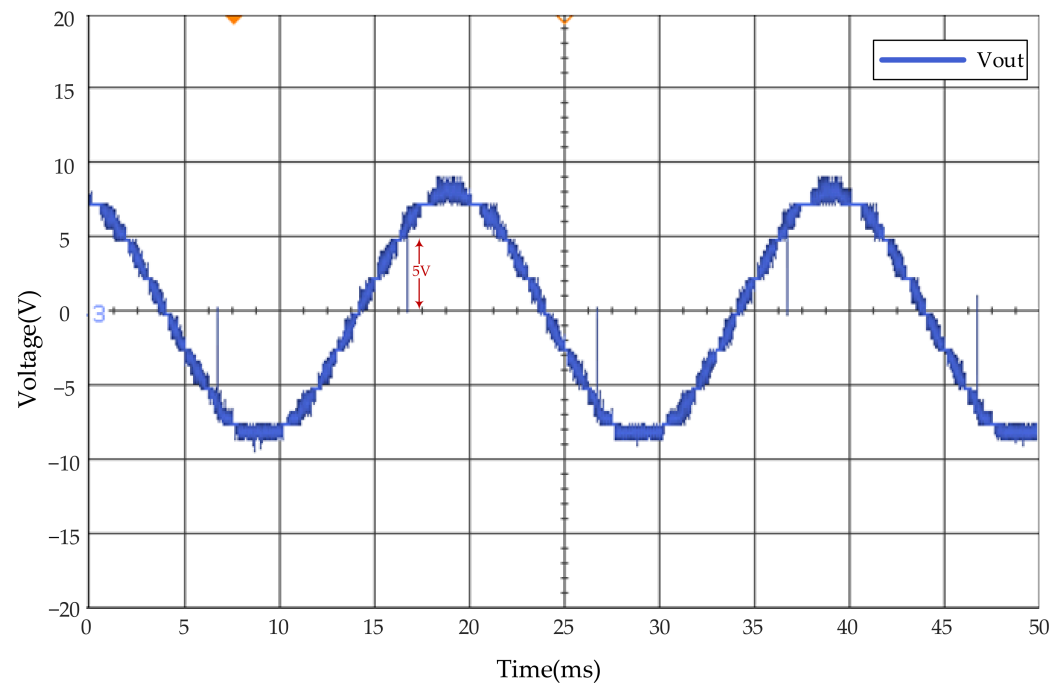


Figure 18. Experimental Voltage spike suppression.

The experimental results demonstrate that voltage spikes indeed occur in the AM-AAC in practice and can be suppressed by the method proposed in this paper. The results are highly consistent with the theoretical analysis and simulation results, thereby confirming the correctness of the proposed theory.

5. Comparison of Modulation Methods

The duration and amplitude of the above spike are both related to the discrete-sampling characteristic of PSC-PWM. The following compares PSC-PWM and NLM under medium- and low-voltage conditions to show that NLM is not a feasible alternative in low-submodule applications for medium- and low-voltage distribution networks.

From the viewpoint of the modulation mechanism, conventional NLM approximates the sinusoidal reference signal with a staircase waveform. Its approximation error fundamentally arises from quantizing the continuous modulation wave into $N + 1$ discrete levels through integer rounding. Fourier-series decomposition of the NLM output staircase voltage waveform shows that its harmonic energy is mainly concentrated in the low-frequency range. When the number of submodules N is small, the geometric envelope error between the staircase waveform and the target sinusoidal waveform increases significantly. As a result, the amplitudes of the resulting low-order characteristic harmonics are large and cannot be sufficiently attenuated by the low-pass filtering characteristic of the arm inductor, directly causing severe distortion of the grid-side current. In contrast, PSC-PWM shifts the phases of N triangular carriers successively by $2\pi/N$, so that the switching pulses of different submodules are interleaved in the time domain. In the spectrum of the cascaded arm output voltage, the switching sideband harmonics of the individual submodules undergo destructive interference during cascaded superposition because of the carrier phase differences. Therefore, the equivalent switching frequency of the arm is increased to the order of $N \cdot f_c$, and the harmonic energy is shifted as a whole to sideband groups around $N \cdot f_c$ and its integer multiples. This frequency-domain shifting effect enables PSC-PWM to suppress low-frequency harmonic energy to a very low level even with a small number of submodules. The essence of this mechanism is that it achieves a significant improve-

ment in the ac-side low-frequency harmonic characteristics at the cost of increased system switching loss.

To quantitatively evaluate the output-current quality difference between the two modulation strategies in the AM-AAC topology, Figure 19 presents the family of comparison curves showing the grid-side current THD versus the number of submodules N under different switching frequencies. The examined range of N covers $N = 1$ to $N = 30$ to represent medium- and low-voltage distribution-network applications.

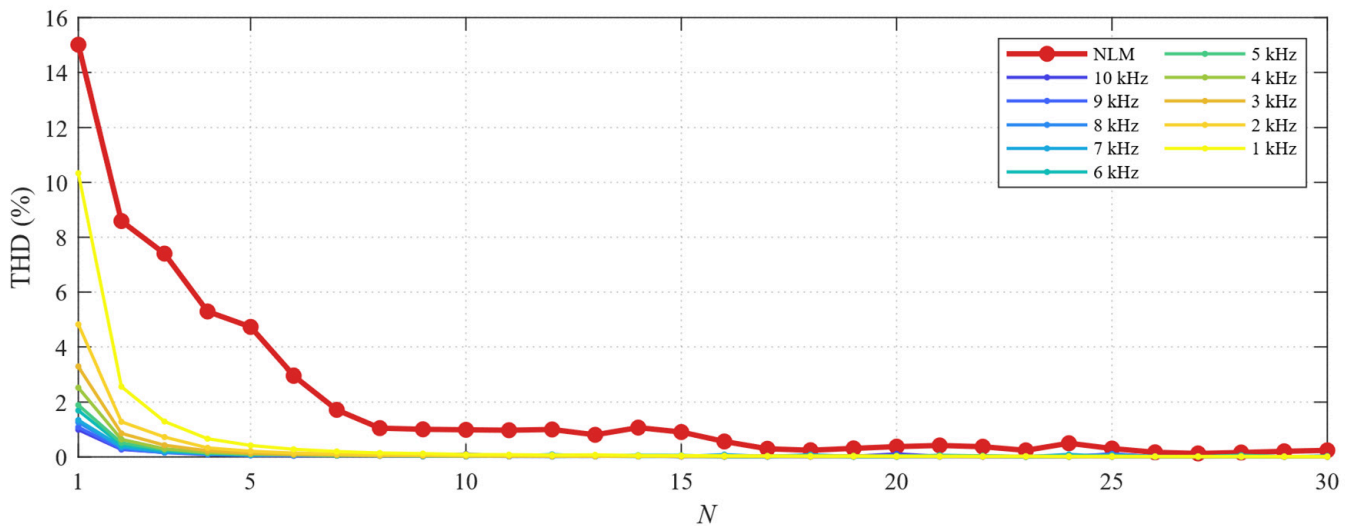


Figure 19. Comparison of the two modulation methods.

Because the output harmonic characteristic of NLM is essentially independent of the switching frequency f_c , it is represented by only one curve. The other ten curves show the variation in THD of PSC-PWM with the number of submodules N under different switching frequencies.

Taking $N = 5$ as an example, the THD of NLM remains 4.73%. For PSC-PWM, THD is 0.115% at $f_c = 10$ kHz and 0.419% at $f_c = 1$ kHz, corresponding to improvement factors of 41 and 11, respectively. When N increases to 10, the THD of NLM is 0.99%, whereas the THD of PSC-PWM is distributed between 0.017% and 0.107%, with a minimum improvement factor of 10.9. When $N = 30$, the THD of NLM is 0.24%, while the maximum THD of PSC-PWM is 0.035% at $f_c = 4$ kHz, corresponding to an improvement factor of 6.86.

The results show that, in medium- and low-voltage applications with a small number of submodules ($N \leq 30$), PSC-PWM achieves lower THD than NLM for the same number of submodules N , and it is significantly superior to NLM when $N \leq 15$. As the number of submodules N increases, the current THD under NLM gradually approaches that under PSC-PWM, and the THD improvement ratio of PSC-PWM over NLM gradually decreases.

From the viewpoint of solution scalability, there is no strict theoretical upper limit on N for implementing PSC-PWM with individual carrier phase shifting, because the method remains technically feasible as long as the digital controller and PWM hardware can provide sufficient channels and synchronization accuracy. However, the results in Figure 19 show that the incremental power-quality benefit of PSC-PWM gradually decreases as N increases. In the investigated AM-AAC, when N is below approximately 15, PSC-PWM provides a clear THD advantage over NLM, and the proposed voltage spike suppression strategy makes this modulation method more attractive in practice. By contrast, when N exceeds approximately 15, the THD difference between PSC-PWM and NLM becomes relatively small, while PSC-PWM still requires individual carrier phase shifting and commutation-switch timing adjustment. Therefore, from a practical engineering perspective, $N \approx 15$ can

be regarded as a crossover point in this study: for low-submodule applications ($N < 15$), PSC-PWM with the proposed suppression method is recommended; for larger- N cases, the simpler NLM can be a more cost-effective choice unless stricter harmonic-performance requirements are imposed.

Although voltage spikes occur when PSC-PWM is used in the AM-AAC, the proposed suppression method effectively mitigates their influence and preserves the harmonic-performance advantage of PSC-PWM in low-submodule applications. In particular, when N is below approximately 15, PSC-PWM with spike suppression provides a more favorable tradeoff between output-current quality and implementation complexity than NLM. As N increases further, the THD advantage of PSC-PWM becomes less pronounced, and the simpler NLM may become a more suitable engineering choice for AM-AAC systems with a larger number of submodules.

6. Conclusions

This paper investigated the voltage spike problem that occurs when PSC-PWM is applied to the AM-AAC in medium- and low-voltage scenarios with a small number of submodules. First, the topology, operating principle, and energy-balance conditions of the AM-AAC were analyzed, and it was shown that PSC-PWM provides better output-current quality than NLM when the number of submodules is small. Then, starting from the discrete-hold characteristic of regular sampling in a digital control system, the intrinsic mechanism by which sampling delay at the modulation-wave discontinuity and commutation-switch waveform folding jointly form the spike level was revealed. The relationships between the spike amplitude and duration and parameters such as carrier frequency and submodule number were also established.

On this basis, this paper proposed a suppression method that adjusts the carrier phase of the commutation switches so that they switch at the midpoint of the spike duration. Simulation and experimental results show that the proposed method requires no additional hardware and can reduce the number of voltage spike levels by half or more, thereby effectively reducing device voltage stress and improving output-voltage quality. Meanwhile, the modulation-method comparison shows that the practical advantage of PSC-PWM with spike suppression is most evident in low-submodule AM-AAC applications. In particular, when N is below approximately 15, PSC-PWM with the proposed suppression method provides a clear current-THD advantage over NLM. As N increases, this advantage gradually diminishes, and the simpler NLM may become a more attractive engineering option for larger- N systems. This observation further clarifies the applicable range and engineering value of the proposed method.

Finally, this study has several limitations, which suggest directions for future work. The present analysis is mainly developed for PSC-PWM with triangular carriers and symmetric regular sampling, and the validation is conducted through MATLAB/Simulink simulations and RTDS hardware-in-the-loop tests over the investigated range of parameters. For other regular-sampling schemes or carrier configurations, such as asymmetric regular sampling and sawtooth or inverse-sawtooth carriers, the same suppression principle can be extended, but the delay relationship and the commutation-switch carrier phase need to be re-derived according to the actual sampling-instant distribution. Future work will focus on generalized delay models for these modulation implementations, adaptive carrier-phase adjustment under wider operating and transient conditions, and further validation on a physical AM-AAC prototype.

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