

Article

Reduced Reverse Leakage in Ti/PtSe₂/n-GaN Schottky Diodes Enabled by an Ultrathin PtSe₂ Interlayer

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Abstract

Gallium nitride (GaN) Schottky barrier diodes (SBDs) are promising for power electronics, but their reverse-bias leakage remains strongly influenced by the rectifying interface's microscopic nature. We fabricated PtSe₂/n-GaN diodes with a transferred ultrathin PtSe₂ interlayer (~1.56 nm, trilayer) to weaken direct interfacial chemical bonding. The Ti/PtSe₂/n-GaN devices exhibit a suppressed reverse leakage current density of 1.3×10^{-7} A/cm² at -1 V, a 7.5×10^4 rectification ratio at ± 1 V, a 0.8 V turn-on voltage, and a 144 V breakdown voltage. Same-wafer Ti/n-GaN control devices display much higher leakage (6.23×10^{-5} A/cm² at -1 V) and a lower rectification ratio (1.144×10^3). Furthermore, Pt/PtSe₂/n-GaN devices reduce leakage to 1.19×10^{-8} A/cm² and increase the rectification ratio to 1.09×10^5 . These results demonstrate the ultrathin interlayer effectively suppresses reverse leakage while preserving the rectifying interface's sensitivity to anode metal selection.

Keywords: Gallium nitride Schottky barrier diodes; platinum diselenide ultrathin interlayer; reverse leakage current suppression

1. Introduction

Gallium nitride (GaN) Schottky barrier diodes (SBDs) are important components for next-generation power electronics because of the wide bandgap, high electron mobility, and high critical electric field of GaN [1]. In practical devices, however, the reverse-bias characteristics of GaN SBDs are strongly affected not only by device-level field-management strategies but also by the microscopic nature of the rectifying interface. In direct metal/n-GaN contacts, interfacial states and metal-induced gap states (MIGS) can reduce the dependence of the effective Schottky barrier on metal selection, thereby limiting interface-level approaches to barrier engineering [2–4].

To suppress the reverse leakage current of GaN SBDs, incorporating an ultrathin interfacial layer between the metal and semiconductor has become an important junction-engineering strategy [5,6]. Conventional thick insulating dielectric layers (such as Al₂O₃ or SiO₂) typically rely on passive physical isolation to block leakage, which inevitably introduces a significant barrier and substantially increases the forward series resistance. In contrast, ultrathin two-dimensional (2D) van der Waals (vdW) materials, such as transition metal dichalcogenides like PtSe₂, offer a distinct mechanism for modulating the Schottky interface. Among various 2D materials, PtSe₂ is particularly attractive for device integration due to its exceptional air stability, high chemical inertness, and unique layer-dependent electronic structure. Unlike conventional thick insulators that completely block carrier transport, the extreme thinness of few-layer PtSe₂ permits a significant probability



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for carrier tunneling under forward bias. Simultaneously, it provides sufficient physical separation to effectively disrupt the strong orbital overlap between the heavy metal and the GaN surface. This delicate balance between tunneling transparency and orbital isolation positions PtSe₂ as an ideal candidate for interfacial engineering, overcoming the traditional trade-off between reverse blocking capability and forward resistance. Benefiting from the intrinsic vdW gap, the ultrathin 2D layer can effectively weaken the direct strong chemical bonding and atomic orbital hybridization between the metal and the semiconductor, thereby suppressing MIGS at an atomic scale. This interfacial-decoupling effect allows forward transport via carrier tunneling while providing pronounced suppression of reverse leakage. Although, similar to common constraints in 2D material-based electronics, the ultrathin vdW layer still introduces a certain resistance trade-off under forward bias due to inherent physical limitations in sheet and contact resistance, its unique capability for interface modulation at atomic thicknesses makes it an efficient materials-level strategy to balance reverse leakage suppression and forward transport characteristics [7,8].

In this work, we use transferred trilayer PtSe₂ as an ultrathin interlayer between the anode metal and n-GaN to construct PtSe₂/GaN-based Schottky diodes. The primary objective of the present study is not to extract a quantitative pinning factor, but to examine whether such an ultrathin PtSe₂ interlayer is associated with reduced reverse leakage and improved rectification in a proof-of-concept device structure. We first demonstrate Ti/PtSe₂/n-GaN SBDs and compare them with same-wafer Ti/n-GaN control devices to clarify the role of the PtSe₂ interlayer. Furthermore, Pt/PtSe₂/n-GaN devices were fabricated to examine the tuning sensitivity of the rectifying behavior to anode selection via a direct comparison with the Ti/PtSe₂/n-GaN SBDs.

2. Experimental Methods

Prior to the wet-transfer process, the commercial GaN-on-sapphire substrates were rigorously cleaned using a standard multi-step solvent sequence. This sequence included successive ultrasonic baths in acetone, ethanol, and deionized water for 10 min each, followed by drying with high-purity nitrogen gas. This rigorous surface preparation is essential to remove organic contaminants and native adsorbates, ensuring that the subsequently transferred PtSe₂ film forms a high-quality, continuous van der Waals interface largely free of trapped macroscopic particulates.

Figure 1 shows the wet-transfer process used to prepare the PtSe₂/GaN heterostructure. First, the PtSe₂/Cu sample coated with polymethyl methacrylate (PMMA) on the front side was floated on a 0.025 g/mL ammonium persulfate solution for 12 h to remove the Cu substrate. The released PMMA/PtSe₂ film was then transferred into deionized water and brought into contact with the submerged GaN/sapphire substrate. During the wet-transfer process, to prevent the formation of interfacial bubbles or voids and ensure an intimate van der Waals contact between the 2D layer and the GaN surface, residual water trapped at the interface was continuously removed with a syringe until the PtSe₂ film was firmly attached. During the subsequent drying process, the evaporation of interfacial water generated strong capillary forces, pulling the ultrathin film into intimate van der Waals contact with the GaN surface without forming covalent bonds. Due to localized surface tension during the wet-transfer, the resulting flakes occasionally exhibit irregular shapes. To address this, as described below, high-precision optical alignment was employed to specifically target the continuous central regions. The sample was then dried at 100 °C for 8 h, followed by PMMA removal in acetone.

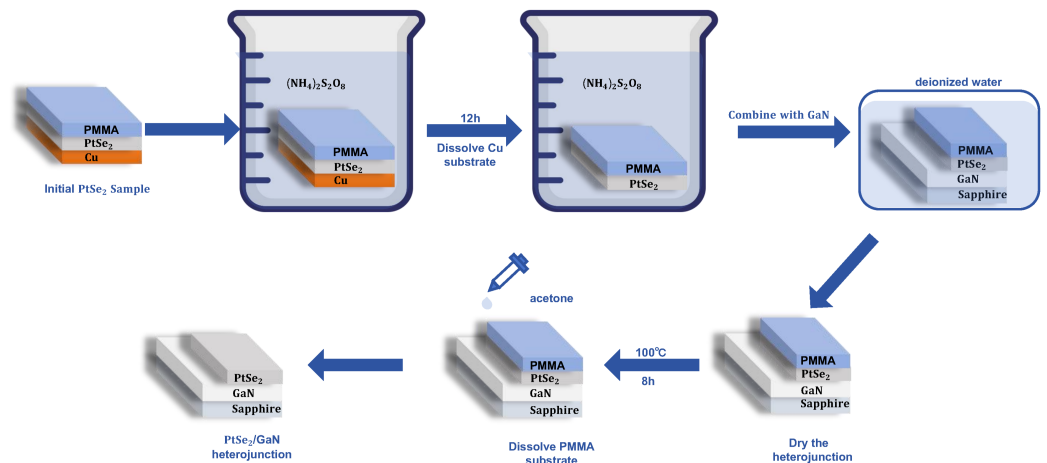


Figure 1. Diagram of the PtSe₂/GaN heterojunction preparation process.

For the interlayer-engineered devices, Schottky electrodes were fabricated on the PtSe₂ flakes by photolithography and magnetron sputtering. Two anode metals were used, namely Ti and Pt, yielding Ti/PtSe₂/n-GaN and Pt/PtSe₂/n-GaN Schottky devices, respectively. Through microscope-assisted optical alignment, each Schottky electrode was selectively patterned onto a single, continuous PtSe₂ flake to eliminate edge-induced leakage. Ohmic electrodes were formed on the exposed GaN region without PtSe₂ coverage using the same Al/Ti metallization. To prevent thermal degradation of the pre-transferred ultrathin van der Waals PtSe₂ layer, the Al/Ti ohmic contacts were intentionally kept in an as-deposited state without post-metallization annealing. In addition, same-wafer Ti/n-GaN control devices without PtSe₂ insertion were fabricated using identical processing conditions. The schematic cross-section and optical microscopy image of the fabricated PtSe₂/GaN SBD are shown in Figure 2a and Figure 2b, respectively. The distance between the Schottky and ohmic electrodes was 60 µm in all device groups. To strictly decouple the interference of edge electric-field crowding effects on the leakage current, it must be emphasized that all tested devices (both the control and the interlayer-engineered devices) possess completely identical macroscopic contact areas and perimeters, and none employ edge termination techniques such as field plates or guard rings.

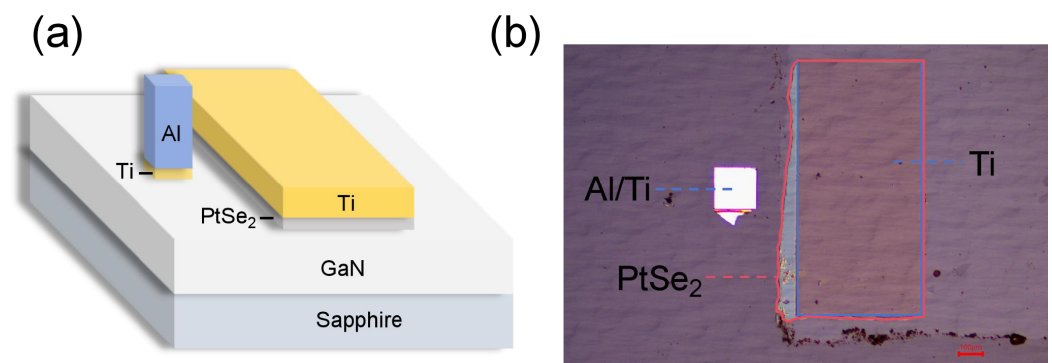


Figure 2. (a) Schematic cross-section of the PtSe₂/GaN SBD. (b) Optical microscopy image of the fabricated PtSe₂/GaN SBD device.

3. Results & Discussion

Figure 3a shows the Raman spectra acquired from the transferred PtSe₂/GaN heterostructure. Two characteristic PtSe₂ vibrational modes near 181 cm^{−1} and 209 cm^{−1} (assigned to the in-plane E_g and out-of-plane A_{1g} modes) are observed, consistent with re-

ported Raman signatures of few-layer PtSe₂ [9,10]. The GaN phonon features near 569 cm⁻¹ and the A₁(LO) mode near 734 cm⁻¹ are also observed [11], indicating spectral coexistence of the transferred PtSe₂ and the underlying GaN. Figure 3b shows the AFM height image of a representative PtSe₂ flake. The thickness ($t = 1.56$ nm) is extracted from the line profile measured across the flake edge onto the adjacent GaN surface. The minor nanoscale fluctuations observed in the AFM profile are typical for wet-transferred 2D materials, primarily originating from inevitable PMMA polymer residues and strain-induced wrinkles rather than inherent lattice non-uniformity. This thickness is consistent with an approximately trilayer PtSe₂ flake when compared with the reported interlayer spacing of 1T-PtSe₂ [10].

Few-layer PtSe₂ exhibits thickness- and defect-sensitive electronic properties, and depending on layer number, strain, defects, and transfer-induced residues, it can evolve from a semiconducting state toward a narrow-gap or semimetallic regime [12,13]. The Raman and AFM results confirm the successful transfer of few-layer PtSe₂ onto GaN and support an approximately trilayer thickness, although they do not by themselves fully determine the electronic phase of PtSe₂ in the final device environment. Accordingly, the following discussion focuses on experimentally observed device characteristics rather than on a uniquely established phase-specific transport model.

The relatively low forward current density in PtSe₂-interlayered devices can be limited by the sheet resistance of the ultrathin PtSe₂ layer and by the top-metal/PtSe₂ contact resistance R_c , both of which are recognized bottlenecks in 2D-material-based electronic structures [14–17].

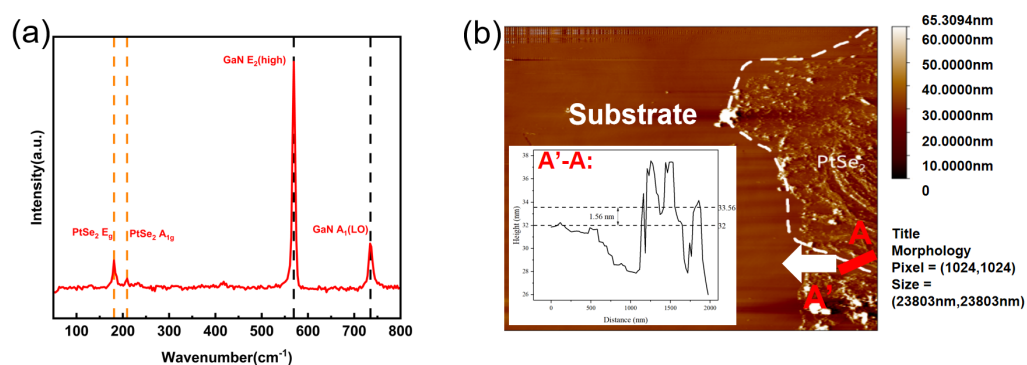


Figure 3. (a) Raman spectra of PtSe₂ and GaN. (b) Atomic Force Microscope (AFM) height image of a representative PtSe₂ flake. The thickness (1.56 nm) is extracted from a line profile measured across the flake edge onto the adjacent GaN surface.

Figure 4a,b present the reverse breakdown and forward turn-on characteristics of the Ti/PtSe₂/n-GaN SBD. Using a breakdown criterion of $J = 0.1$ A/cm², a breakdown voltage of 144 V is obtained. Such a blocking capability is comparable to that of reported low-voltage GaN Schottky rectifiers in the 100–200 V range [18]. The forward turn-on voltage is 0.8 V at $J = 1.0 \times 10^{-3}$ A/cm². To clarify the physical impact of the vdW PtSe₂ interlayer and exclude geometric artifacts, a Ti/n-GaN control device was fabricated on the same wafer. It must be emphasized that all tested devices (with and without the interlayer) possess identical macroscopic geometric dimensions and electrode spacing, and none employ edge termination structures such as field plates. As shown in Figure 4c, under the condition of identical edge electric field distribution, the Ti/n-GaN control exhibits a high reverse leakage current density of 6.23×10^{-5} A/cm² at -1 V, with a rectification ratio of only 1.144×10^3 . In contrast, with the insertion of the PtSe₂ layer, the reverse leakage current density of the Ti/PtSe₂/n-GaN device is substantially suppressed to 1.3×10^{-7} A/cm² at -1 V, and the rectification ratio jumps to 7.5×10^4 . This nearly three-order-of-magnitude reduction in reverse leakage, observed under strictly controlled variables (identical dimen-

sions and substrate), strongly demonstrates that the performance improvement originates from the inherent material properties of the PtSe₂/GaN interface rather than edge leakage or geometric area effects [19]. Furthermore, similar to widely recognized bottlenecks in 2D material-based electronics [14–17], the relatively low forward current density is primarily limited by the sheet resistance of the ultrathin PtSe₂ layer and the top-metal/PtSe₂ contact resistance. Therefore, this forward-bias resistance limitation should be clearly distinguished from the ultralow reverse leakage phenomenon governed by the rectifying junction.

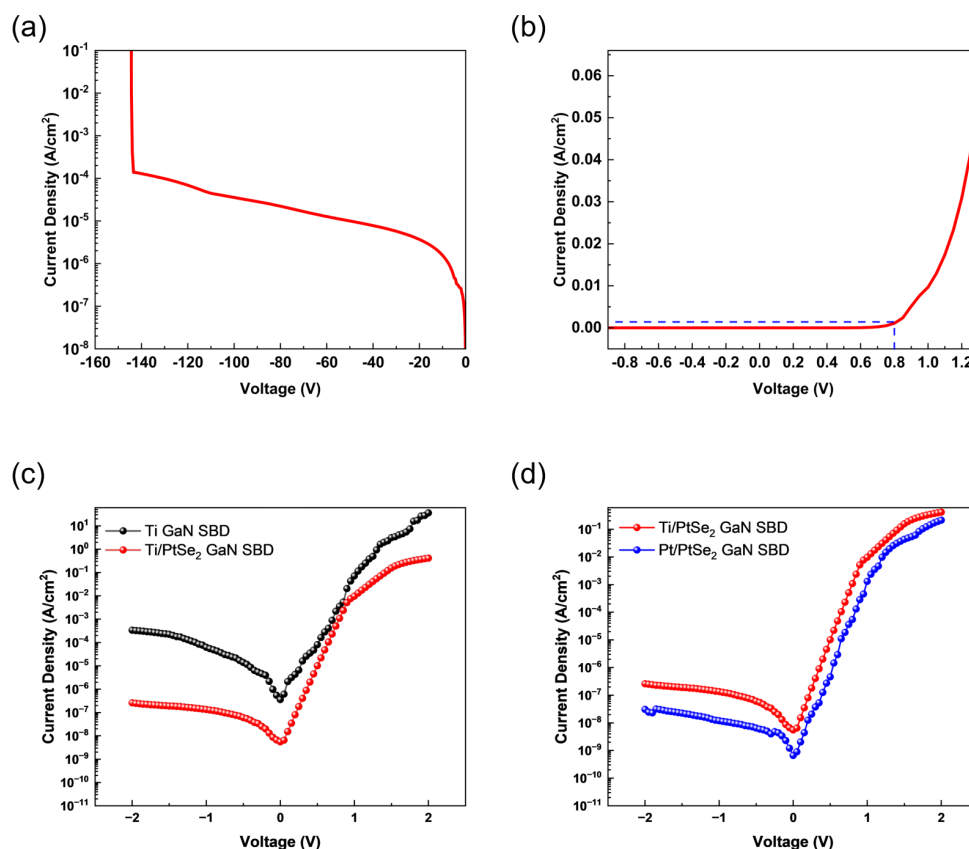


Figure 4. Electrical characterization of the PtSe₂/GaN Schottky barrier diode (SBD). (a) Reverse current density–voltage (J – V) characteristics; the breakdown voltage is 144 V at $J = 0.1$ A/cm². (b) Forward turn-on behavior, showing a turn-on voltage $V_{on} = 0.8$ V at $J = 1.0 \times 10^{-3}$ A/cm². (c) J – V characteristics comparing the Ti/GaN and Ti/PtSe₂/GaN SBDs with identical geometric dimensions. (d) J – V characteristics of the Ti/PtSe₂/GaN and Pt/PtSe₂/GaN SBDs with different anode metals.

To further elucidate the modulation effect of the anode work function on the PtSe₂/GaN rectifying interface, a Pt/PtSe₂/n-GaN SBD was fabricated and directly compared with the Ti/PtSe₂/n-GaN device. As shown in Figure 4d, under identical fabrication processing and electrical measurement conditions, the two device groups display distinctly different rectifying characteristics. Specifically, the SBD with a high-work-function Pt anode exhibits a further suppressed reverse leakage current density of 1.19×10^{-8} A/cm² at -1 V, accompanied by an enhanced rectification ratio of 1.09×10^5 at ± 1 V. This prominent evolution in electrical behavior resulting solely from the alteration of the anode metal demonstrates that the effective rectifying interface retains a pronounced sensitivity to the work function of the selected metal [20–22].

A qualitative interpretation of the observed characteristics is illustrated schematically in Figure 5. In this physical picture, the transferred PtSe₂ layer relies on its van der Waals gap to weaken direct interfacial chemical bonding and effectively suppress metal-induced

gap states (MIGS) relative to a direct Ti/GaN contact. Therefore, the PtSe₂ interlayer is qualitatively interpreted here as an ultrathin interfacial barrier that modifies the effective rectifying interface by weakening direct metal/GaN coupling while permitting carrier tunneling. The observed Ti/Pt anode dependence further confirms that the PtSe₂/GaN contact retains sensitivity to anode selection [7,8,23–25].

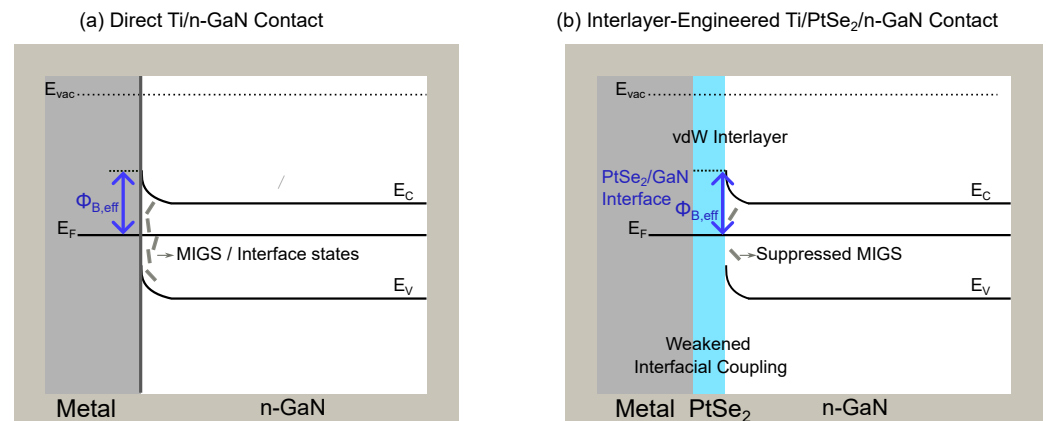


Figure 5. Schematic energy-band diagrams of Ti/n-GaN Schottky contacts (a) without and (b) with an ultrathin PtSe₂ interlayer. In the direct metal/semiconductor contact, interfacial coupling and metal-induced gap states (MIGS) are illustrated near the interface, leading to a rectifying barrier at the metal/GaN junction. With the insertion of the PtSe₂ layer, the rectifying interface is effectively shifted to the PtSe₂/GaN junction, accompanied by reduced interfacial coupling and a suppressed density of MIGS. The diagrams are qualitative and are intended to illustrate possible interface-modification effects rather than quantitatively extracted barrier parameters.

The forward-bias characteristics were analyzed using a thermionic-emission-like framework,

$$J = J_0 \left[\exp \left(\frac{qV}{nk_B T} \right) - 1 \right], \quad (1)$$

$$J_0 = A^* T^2 \exp \left(-\frac{q\Phi_B}{k_B T} \right), \quad (2)$$

where J_0 is the reverse saturation current density, A^* is the effective Richardson constant, n is the ideality factor, and Φ_B is treated as the effective Schottky barrier height of the rectifying interface [3]. By linearly fitting the forward $\ln(J)$ – V curves in the voltage range of 0.3 V to 0.8 V at 300 K, the extracted ideality factors for the Ti/n-GaN control, Ti/PtSe₂/n-GaN, and Pt/PtSe₂/n-GaN devices are determined to be 3.87, 2.42, and 2.63, respectively. Due to the incorporation of the ultrathin van der Waals interlayer, non-ideal factors such as barrier inhomogeneity, series resistance, and interfacial tunneling components are inevitably involved [9,26,27], causing the ideality factors to deviate from unity. Specifically, the relatively large ideality factors suggest that current transport involves non-ideal mechanisms, such as trap-assisted tunneling across the ultrathin vdW interface and lateral barrier inhomogeneities. Instead of relying on a precise effective Richardson constant (A^*) to extract the absolute Schottky barrier height, this relative analysis serves as a compact phenomenological description of forward transport, and the extracted barrier height should be interpreted as an effective parameter incorporating interface transport characteristics rather than an ideal, uniform Schottky barrier height [28,29].

While the reduction in reverse leakage upon PtSe₂ insertion is substantial, the current is not completely eliminated. Given the suppression of intrinsic MIGS, the residual reverse leakage current in the interlayer-engineered devices is hypothesized to be predominantly governed by trap-assisted tunneling (TAT). These transport traps likely originate from

minor transfer-induced imperfections, such as nanoscale PMMA polymer residues or strain-induced wrinkles at the delicate vdW interface, as evidenced by the earlier AFM morphological analysis. Furthermore, considering the rigorous operating environments typically required for power diodes, the intrinsic thermal and chemical stability of the PtSe₂ material system provides a reliable theoretical foundation for the endurance of the vdW interface against severe thermal degradation, which is a critical advantage over highly reactive direct-metal contacts.

Notably, in 2D van der Waals heterostructures, the effective Richardson constant A^* can deviate significantly from the theoretical bulk values due to varying tunneling probabilities across the van der Waals gap. A relative barrier analysis approach is implemented here. Since the Ti/PtSe₂/n-GaN and Pt/PtSe₂/n-GaN SBDs are co-fabricated on the same wafer substrate with an identical interlayer thickness, it is reasonable to assume that their interfacial tunneling probabilities and the corresponding effective Richardson constants are approximately equal [28–30]. Consequently, the ratio of their room-temperature saturation current densities $J_{0,Ti}$ and $J_{0,Pt}$ eliminates the unknown parameter A^* :

$$\frac{J_{0,Ti}}{J_{0,Pt}} = \exp \left[\frac{q(\Phi_{B,Pt} - \Phi_{B,Ti})}{k_B T} \right] \quad (3)$$

This allows the relative Schottky barrier height shift (Φ_B) induced by the alteration of the anode metal to be directly and quantitatively extracted via logarithmic transformation:

$$\Delta\Phi_B = \Phi_{B,Pt} - \Phi_{B,Ti} = \frac{k_B T}{q} \ln \left(\frac{J_{0,Ti}}{J_{0,Pt}} \right) \quad (4)$$

This methodology uses experimentally extrapolated saturation current densities to directly determine $\Delta\Phi_B$, confirming that the ultrathin interlayer attenuates interfacial chemical pinning and preserves work-function sensitivity [31].

4. Conclusions

In summary, we have demonstrated PtSe₂/n-GaN Schottky diodes incorporating a transferred ultrathin PtSe₂ interlayer with an approximately trilayer thickness. The Ti/PtSe₂/n-GaN device exhibits a reverse leakage current density of 1.3×10^{-7} A/cm² at -1 V, a rectification ratio of 7.5×10^4 at ± 1 V, a turn-on voltage of 0.8 V, and a breakdown voltage of 144 V. Same-wafer Ti/n-GaN control devices with identical macroscopic geometric dimensions indicate that, under comparable testing conditions, the introduction of the PtSe₂ interlayer leads to a substantial reduction in reverse leakage by nearly three orders of magnitude. Furthermore, based on a comparative analysis of devices with different anode metals, we discussed and verified the anode-dependent barrier behavior at the PtSe₂/GaN rectifying interface. These results are consistent with the physical picture of weakened interfacial chemical pinning. While the macroscopic electrical data support the proof-of-concept barrier modulation, further studies are worth considering to comprehensively explore the deep-level kinetics and the microscopic continuity of the delicate van der Waals interface. Such investigations could include thickness-dependent phase engineering, variable-temperature I - V transport analysis, and non-destructive atomic-level profiling. The present study therefore establishes a 2D interlayer-engineered route toward lower-leakage GaN Schottky contacts and provides a practical basis for further optimization through expanded metal selection and device-level engineering.

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