

Article

Constraint-Aware Predictive Energy Coordination of Multiple Energy-Storage Converters for DC Bus Stabilization

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Abstract

Direct current (DC) bus voltage stability in grid-connected microgrids with multiple energy-storage converter branches is governed by the coupled dynamics of photovoltaic generation, heterogeneous battery storage, and the grid-connected inverter. Conventional independent and droop control methods allocate branch power mainly from local voltage or state-of-charge information, and therefore cannot fully account for converter limits, battery condition, or inverter current admissibility. This paper proposes a constraint-aware predictive energy coordination (CAPEC) method for DC bus stabilization. A DC bus energy model with variable losses is combined with one-step disturbance prediction and a safety governor that allocates storage power according to state of charge (SOC), state of health (SOH), power reserve, thermal margin, current capability, and ramp limits. The grid-connected inverter is treated as a constrained energy regulation path with active power saturation and antiwindup correction. Small-signal and energy function analyses show that CAPEC increases equivalent DC bus damping and yields bounded voltage recovery for feasible references and bounded prediction errors. MATLAB R2023b studies for combined photovoltaic and load variation, grid interface disturbance, and heterogeneous storage conditions show that CAPEC limits the maximum voltage deviation to 2.86 to 6.35 V. A reduced power laboratory experiment further verifies the Case B breaker disturbance and confirms stable DC bus behavior during unplanned grid interface switching.

Keywords: DC bus voltage stability; energy storage converter; constrained power allocation; predictive coordination; grid connected microgrid

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1. Introduction

The increasing penetration of photovoltaic generation, battery energy-storage systems, and power electronic loads is changing medium- and low-voltage distribution networks from passive radial feeders into converter-dominated microgrids [1,2]. In a grid-connected microgrid, several direct current (DC) sources are commonly connected to a shared DC bus through DC/DC converters, and the bus is connected to the alternating current (AC) feeder through a voltage-source inverter [3,4]. This structure reduces conversion stages and allows energy-storage modules with different voltage levels to participate in the same power-exchange process. It also makes the DC bus capacitor the

instantaneous energy buffer for source-side and grid-side power variations [5]. A disturbance in any branch may therefore appear as a voltage excursion of the common DC bus and then propagate to the inverter current loop and the point of common coupling.

Existing DC microgrid control schemes can be grouped into several representative categories. Independent current or voltage control provides a direct local regulation structure [6], but it does not impose a physically meaningful sharing rule among parallel storage branches [7,8]. Fixed droop control improves autonomous sharing by modifying the voltage reference according to branch current or power; however, its sharing ratio is determined by preset droop coefficients [8]. Adaptive droop control updates the droop coefficient according to loading state or state of charge (SOC) [9,10]. Consensus secondary control improves current sharing and voltage restoration through adjacent information, whereas model predictive control can explicitly handle constraints and predicted disturbances [11,12]. Data-based power management and modified droop strategies further improve hybrid storage utilization, but they generally emphasize either source-side sharing or bus voltage restoration [13,14]. The interaction between multiple storage converters and the grid-connected inverter is still frequently reduced to a single power-balance relation.

Such a simplification is inadequate for the studied grid-connected microgrid. The inverter is not only an AC-side power-tracking interface [15], but also a controllable energy release path for the DC bus capacitor [16,17]. If the inverter maintains a scheduled active power command during a rapid photovoltaic power reduction, a large load step, or a temporary grid interface disturbance, the storage converters must compensate the resulting mismatch through branch current variations. Conversely, an excessively fast inverter active power correction may cause the d-axis current command to exceed its current limit, excite the LCL filter, or induce integral windup [18,19]. Therefore, DC bus stability should be formulated as a coordinated energy regulation problem involving source-side allocation, inverter power correction, and converter constraints.

The limitations of fixed droop control can be further interpreted from the DC bus energy balance without introducing additional equations in the Introduction. In a fixed droop scheme, the contribution of each branch is governed primarily by its preset droop gain rather than by its real-time electrochemical and thermal capability [8,10]. When a module has a low state of charge, aged cells, higher internal resistance, or reduced current capability, fixed droop may still require a strong response to the same bus voltage deviation. Dynamic coupling further increases this risk because the branch with the weakest margin may experience the largest relative stress when the DC bus requires strong support. Recent modified droop-and-passivity-based controls improve current sharing, but they generally still rely on local voltage to power mapping and do not fully coordinate the inverter energy-release path [14,15].

Although advanced methods introduce additional communication or optimization layers, practical implementation details are often insufficiently specified. Comparative reviews of DC microgrid power management show that source-side coordination, inverter regulation, and converter constraints are frequently handled in separate layers [20,21]. Recent distributed and cooperative secondary controls improve voltage restoration and sharing accuracy, but their interaction with the grid-connected inverter is usually not the main design object [22,23]. Distributed model predictive control and cooperative secondary control can handle constraints, yet their computational burden and parameter tuning become nontrivial when storage modules are heterogeneous [12,24]. Operating constraints related to battery state, aging, and DC link fluctuation are also important for practical hybrid storage systems [25,26]. These gaps motivate constraint-aware predictive energy coordination (CAPEC) as a constraint-aware predictive energy coordination

framework in which DC bus energy, branch safety, and inverter admissibility are integrated within a physically interpretable control structure.

The main contributions of this paper are as follows: First, a DC bus energy coupling model with variable loss terms is established for a grid-connected microgrid containing photovoltaic generation, heterogeneous energy-storage modules, bidirectional DC/DC converters, and a grid-connected inverter. Second, CAPEC is proposed as a constraint-aware predictive energy coordination method. Short-horizon disturbance prediction is combined with a safety governor so that storage branch power references are allocated within SOC, state of health (SOH), power, ramp rate, current, and thermal limits. Third, the grid-connected inverter is formulated as a constrained DC bus energy actuator with energy feedback, feedforward disturbance compensation, saturation, and antiwindup correction. Fourth, small-signal and energy function analyses clarify the damping mechanism and provide practical tuning conditions. Fifth, the simulation design and the supplementary laboratory experiment verify the proposed method under renewable power variation, grid interface disturbance, and heterogeneous storage operating conditions relevant to modern grid-connected PV systems [27,28].

The remainder of this paper is organized as follows: Section 2 describes the microgrid topology and establishes the DC bus energy coupling model. Section 3 formulates the stability control problem under converter constraints and positions the proposed method against representative control schemes. Section 4 develops the proposed CAPEC method. Section 5 presents stability analysis and parameter design. Section 6 describes the simulation platform, physical experimental verification, benchmark methods, and performance evaluation. Section 7 concludes this paper.

The principal abbreviations and symbols used throughout this paper are listed as Table 1.

Table 1. The principal abbreviations and symbols. A superscript * is a reference value, and Δ is a perturbation or deviation.

Abbreviation or Symbol	Definition
CAPEC	Constraint-aware predictive energy coordination
ICM; FDC	Independent control method; fixed droop control
ESS; PCC; PV	Energy-storage system; point of common coupling; photovoltaic source
SOC; SOH	State of charge; state of health
N	Number of energy-storage branches
V_{dc} , V_{dc}^*	Measured and rated DC bus voltages
C_{dc} , E_{dc}	Equivalent DC bus capacitance and capacitor energy
P_i , P_i^*	Actual and reference power of storage branch i
P_{pv} , P_{inv} , P_{loss}	PV power, inverter DC-side power, and equivalent loss
$P_{load,dc}$, P_{g0}	DC-side equivalent load demand and scheduled grid active power
P_{gu} , P_g^* , P_{glim}	Unsaturated, final, and current limited inverter active power references
Q_g^*	Reactive power reference of the grid-connected inverter
P_d , P_{dp}	Observed and predicted power disturbance

$i_d, i_q, I_{\max}$	dq axis inverter currents and current limit
$V_{b,i}, i_i, L_i$	Storage terminal voltage, branch current, and branch inductance
r_i, d_i, η_i, τ_i	Equivalent resistance, duty ratio, efficiency, and power-tracking time constant
$P_{ich,\max}, P_{idis,\max}$	Maximum charging and discharging powers of branch i
$R_i, \Delta t$	Branch ramp limit and coordination sampling period
$S_{ich}, S_{idis}, \rho_i$	Charge capability score, discharge capability score, and preliminary allocation factor
Ω_i, q_i, h_i	Feasible power interval, priority factor, and ramp penalty coefficient
a_1 to a_3, μ_d	Capability score weights and disturbance prediction coefficient
$K_E, K_I, K_G, K_{GI}, K_F, k_{aw}$	Energy feedback, integral, inverter, feedforward, and antiwindup gains
z_E, ξ_E, e_E	Storage integral state, inverter integral state, and DC bus energy error
$\Delta V_{\max}, t_{\text{rec}}, e_{\text{share}}, e_g$	Maximum voltage deviation, recovery time, sharing error, and grid active power-tracking error

2. System Description and DC Bus Energy Coupling Model

Figure 1 presents the studied grid-connected microgrid. A photovoltaic source and N energy-storage modules are connected to the common DC bus through individual bidirectional DC/DC converters. The DC bus is connected to the AC feeder through a grid-connected inverter and an LCL filter. The AC feeder contains local loads, distribution transformers, and the point of common coupling to the utility grid. The energy-storage modules may be homogeneous or heterogeneous in rated power, capacity, internal resistance, SOC, SOH, and allowable ramp rate.

For terminology consistency, an energy-storage module is the battery pack, an energy-storage converter is the bidirectional DC/DC converter interfacing the module with the DC bus, and an energy-storage branch is the combined module and converter. The term grid-connected inverter is the DC/AC converter between the common DC bus and the AC feeder. These terms are used consistently in the following sections, tables, and figure captions.

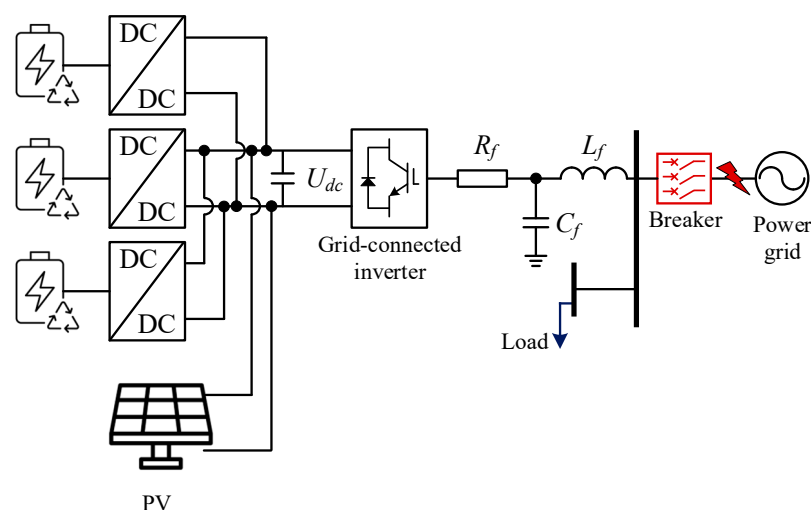


Figure 1. Topology of the grid-connected microgrid with multiple energy-storage converter branches.

The energy stored in the DC bus capacitor is written as follows:

$$E_{dc} = \frac{1}{2} C_{dc} V_{dc}^2 \quad (1)$$

where E_{dc} is the capacitor energy, C_{dc} is the equivalent DC bus capacitance, and V_{dc} is the measured DC bus voltage. Differentiating (1) yields the energy balance of the common DC bus:

$$\frac{dE_{dc}}{dt} = \sum_{i=1}^N P_i + P_{pv} - P_{inv} - P_{loss} \quad (2)$$

where P_i is the power injected from storage branch i to the DC bus, P_{pv} is the photovoltaic power injected into the DC bus, P_{inv} is the active power absorbed by the grid-connected inverter from the DC bus and delivered to the AC side, and P_{loss} is the total converter and line loss referred to the DC side. Positive P_i is discharging from the corresponding storage module to the DC bus, and negative P_i is charging from the DC bus to the module. This energy balance is consistent with the power flow convention adopted in the simulation and experimental validation.

Unlike the simplified constant loss model, the loss term is represented as a voltage- and current-dependent expression:

$$P_{loss} = P_0 + r_{inv} \frac{P_{inv}^2}{V_{dc}^2} + \sum_{i=1}^N r_i i_i^2 \quad (3)$$

where P_0 is the no load equivalent loss, r_{inv} is the equivalent conduction resistance of the inverter path, r_i is the equivalent resistance of DC/DC branch i , and i_i is the branch current. In severe transients, (3) captures the fact that losses increase with current and therefore slightly reduce the effective damping available for DC bus voltage recovery. If detailed semiconductor loss data are unavailable, P_0 , r_{inv} , and r_i can be identified from steady-state operating points or set from manufacturer efficiency curves.

From (1) and (2), the voltage dynamic equation is:

$$C_{dc} V_{dc} \frac{dV_{dc}}{dt} = \sum_{i=1}^N P_i + P_{pv} - P_{inv} - P_{loss} \quad (4)$$

Equation (4) indicates that V_{dc} is not a local variable of a single converter. It is the common energy state of the DC subsystem. Variations in P_i , P_{pv} , P_{inv} , or P_{loss} directly alter the capacitor charging power and subsequently affect all controllers that use the DC bus voltage as feedback. This coupling explains why DC bus voltage stability, branch-level power sharing, and inverter active power correction should be treated within one coordinated energy framework [7,23].

2.1. Energy-Storage Converter Model

Each energy-storage module is interfaced by a non-isolated bidirectional buck boost DC/DC converter. This topology is widely used when the storage terminal voltage may be lower or higher than the DC bus voltage and galvanic isolation is not required [4,5]. For systems requiring isolation, a dual active bridge can be used, and the outer power coordination layer proposed in this paper remains applicable after replacing the inner plant model. Under continuous conduction mode, the averaged branch dynamics are:

$$L_i \frac{di_i}{dt} = V_{b,i} - (1-d_i)V_{dc} - r_{L,i} i_i \quad (5)$$

where L_i is the inductor of branch i ; $V_{b,i}$ is the storage terminal voltage; d_i is the duty ratio; and $r_{L,i}$ is the inductor and switch-equivalent resistance. The average DC bus power of the branch is:

$$P_i = \eta_i V_{bi} i_i \quad (6)$$

where η_i is the conversion efficiency of branch i . In the simulation and controller design, the inner current loop is much faster than the outer energy coordination loop. Therefore, the current-tracking dynamics can be approximated by:

$$\tau_i \frac{dP_i}{dt} + P_i = P_i^* \quad (7)$$

where P_i^* is the branch power reference produced by the coordination layer and τ_i is the equivalent power-tracking time constant of branch i . The value of τ_i is determined by the current loop bandwidth, digital sampling delay, and converter filter parameters.

2.2. Grid-Connected Inverter Model

The grid-connected inverter is modeled in the synchronous dq reference frame aligned with the PCC voltage vector. This representation follows common DC link voltage and grid-connected inverter control practice [16,17]. Its current dynamics are:

$$L_f \frac{di_d}{dt} = u_d - v_d - R_f i_d + \omega L_f i_q \quad (8)$$

$$L_f \frac{di_q}{dt} = u_q - v_q - R_f i_q - \omega L_f i_d \quad (9)$$

where L_f and R_f are the filter inductance and resistance; i_d and i_q are the dq axis currents; u_d and u_q are the inverter output voltages; v_d and v_q are the PCC voltages; ω is the synchronous angular frequency. When the dq frame is aligned with the PCC voltage, $v_q = 0$, and the active and reactive powers are:

$$P_{inv} = \frac{3}{2} v_d i_d \quad (10)$$

$$Q_{inv} = -\frac{3}{2} v_d i_q \quad (11)$$

Equations (10) and (11) indicate that inverter active power is mainly regulated through i_d , whereas reactive power is mainly regulated through i_q . However, both current components share the same current capacity. Therefore, the DC bus voltage correction loop must respect the inverter current constraint, especially when LCL filter dynamics and power quality limits are considered [18,19].

$$i_d^2 + i_q^2 \leq I_{\max}^2 \quad (12)$$

where $I_{\max}$ is the maximum admissible inverter current. This constraint is essential during deep photovoltaic drops or grid interface disturbances because an unconstrained DC voltage PI controller can otherwise request an infeasible active current command.

3. Control Problem Formulation

The control objective is to maintain DC bus voltage stability while respecting the physical limits of each DC/DC converter and the grid-connected inverter. The DC bus energy error is defined as follows:

$$e_E = E_{dc} - E_{dc}^* = \frac{1}{2} C_{dc} \left(V_{dc}^2 - (V_{dc}^*)^2 \right) \quad (13)$$

where E_{dc}^* is the reference capacitor energy and V_{dc}^* is the DC bus voltage reference. Near the rated voltage, energy feedback and voltage feedback are locally equivalent; however, energy feedback provides a clearer physical interpretation under large voltage deviations.

The instantaneous power imbalance to be compensated by the storage system and the inverter correction is:

$$\Delta P = P_{pv} - P_{load,dc} - P_{g0} - P_{loss} \quad (14)$$

where $P_{load,dc}$ is the DC-side equivalent of the internal load demand seen by the common DC bus, and P_{g0} is the scheduled active power delivered by the grid-connected inverter. In practical implementation, $P_{load,dc}$ does not need to be measured directly. It can be obtained from measured inverter power, a local load estimator, or a recursive power imbalance observer based on (4).

Each storage branch has a time-varying feasible power interval:

$$-P_i^{ch,max}(SOC_i) \leq P_i^* \leq P_i^{dis,max}(SOC_i) \quad (15)$$

where $P_i^{ch,max}$ and $P_i^{dis,max}$ are the maximum charge and discharge powers of branch i . They depend on the state of charge, SOC_i , of the module. The following ramp rate limit is also imposed:

$$|P_i^*(k) - P_i^*(k-1)| \leq R_i \Delta t \quad (16)$$

where R_i is the power ramp rate limit and Δt is the outer coordination sampling period. Equations (15) and (16) restrict excessive current steps that may increase semiconductor thermal cycling or battery current stress.

The coordination objective is therefore to minimize the bus energy error, deviation from the scheduled grid power, branch stress, and SOC imbalance subject to the constraints (12), (15), and (16). The proposed method differs from conventional MPC because it does not solve a repeated full-order receding horizon optimization at the converter switching frequency. Instead, it uses one-step disturbance prediction and a low-dimensional projection on the storage branch feasible set. It also differs from adaptive droop control, which modifies local voltage to power slopes but does not explicitly coordinate inverter active power saturation. Consensus secondary control relies on graph-based information exchange and convergence, whereas CAPEC uses common DC bus energy measurements and branch capability information in a supervisory allocation layer. Table 2 summarizes these distinctions.

Table 2. Technical comparison of representative control strategies for the studied grid-connected microgrid.

Method	Main Mechanism	Limitation in the Studied System	Technical Distinction of CAPEC
Independent control method (ICM)	Each converter follows a local current or voltage reference.	No branch-level energy coordination is imposed. The inverter follows its scheduled power and cannot relieve DC bus energy imbalance.	CAPEC uses a common DC bus energy observer and allocates storage references according to branch feasibility.
Fixed droop control (FDC)	Preset voltage-to-power droop coefficients determine branch response.	Power sharing is governed by fixed gains rather than real-time SOC, SOH, thermal, power, and ramp margins.	CAPEC replaces fixed slopes with safety-constrained allocation and feasible projection.
Adaptive droop control	Droop gains are updated according to SOC, loading state, or bus voltage condition.	Local slope adaptation improves sharing but does not solve inverter saturation or multi-constraint branch feasibility.	CAPEC couples branch capability scores with bounded inverter active power correction.

Consensus secondary control	Neighbor information is exchanged to restore voltage and improve current sharing.	Performance depends on communication graph convergence and branch references are not explicitly projected onto electrothermal limits.	CAPEC uses supervisory energy coordination based on common measurements and local constraints; graph consensus is not required in the core allocation.
Conventional model predictive control (MPC)	A receding horizon optimization predicts states and computes constrained inputs.	Full model optimization can be sensitive to model size, solver time, and tuning when storage branches are heterogeneous.	CAPEC uses one-step disturbance prediction and low-dimensional projection, retaining explicit constraints with lower real-time burden.
Data-based or reinforcement learning control	A control policy is obtained from historical data or online interaction.	Safety near operating points not covered by data is difficult to guarantee without an additional feasibility layer.	CAPEC retains a physical energy model and hard feasibility bounds.
Proposed CAPEC	Energy observer, disturbance prediction, safety governor, feasible projection, and inverter saturation with antiwindup.	Reliable branch measurements and bounded communication delay are required.	Storage converters and the grid-connected inverter are coordinated under SOC, SOH, thermal, current, power, and ramp constraints.

4. Constraint-Aware Predictive Energy Coordination

Figure 2 presents the information flow of the proposed CAPEC method. The measured DC bus voltage, branch currents, storage terminal voltages, SOC, SOH, and inverter current are first sent to the energy observer and disturbance predictor. The predicted imbalance and the DC bus energy error are then converted into a total storage support demand and processed by the safety governor.

The safety governor constructs branch capability scores and sends preliminary power shares to the projection block, which enforces SOC, power, current, thermal, and ramp constraints before the local current controllers receive their references. In parallel, the inverter correction path computes an active power reference from the same energy error and predicted disturbance. This reference is saturated by the inverter current limit, and the antiwindup feedback returns the saturated error to the integral state. The architecture therefore links prediction, constrained allocation, inverter saturation, and antiwindup correction through a single DC bus energy variable.

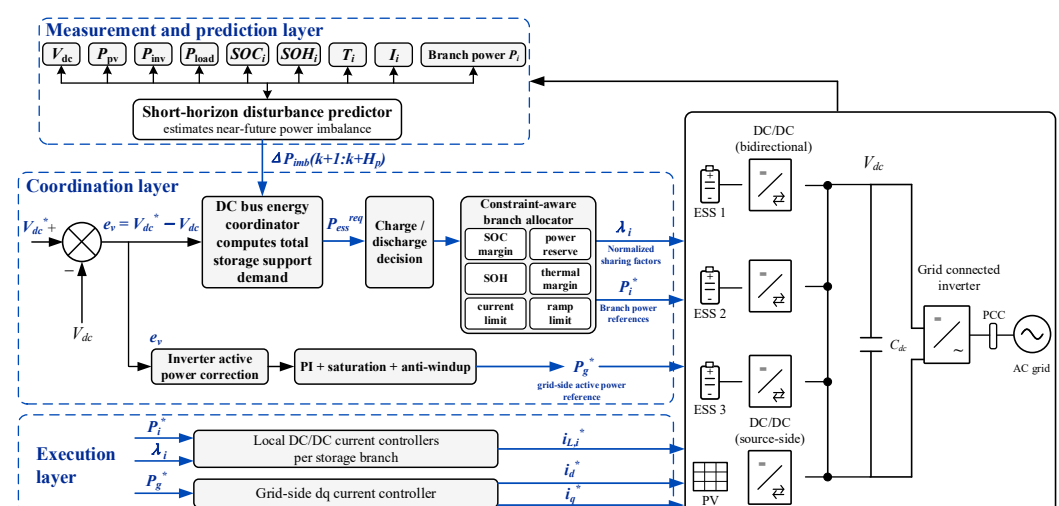


Figure 2. Control architecture and information flow of the proposed CAPEC method.

4.1. Power Imbalance Observer and Short-Horizon Prediction

The measured DC bus voltage and converter powers are used to estimate the unmeasured disturbance acting on the DC bus. From (4), the observed disturbance is defined as follows:

$$P_d = C_{dc} V_{dc} \frac{dV_{dc}}{dt} - \sum_{i=1}^N P_i - P_{pv} + P_{inv} + P_{loss} \quad (17)$$

where P_d represents the residual power caused by load variation, measurement error, unmodeled converter loss, and grid interface disturbance. A first-order prediction is adopted:

$$P_d^p(k+1) = P_d(k) + \mu_d [P_d(k) - P_d(k-1)] \quad (18)$$

where $P_d^p(k+1)$ is the predicted disturbance for the next coordination step and μ_d is the prediction coefficient. A smaller μ_d provides conservative filtering, whereas a larger μ_d improves anticipatory response under rapid photovoltaic or load variations. To avoid noise amplification, μ_d is limited within $0 \leq \mu_d \leq 1$, and the derivative of V_{dc} in (17) is obtained through a low-pass differentiator.

The total storage support demand is then generated from energy feedback and predicted disturbance compensation:

$$P_{ess}^* = \text{sat}_{R_E} \left[-K_E e_E - K_I z_E - P_d^p \right] \quad (19)$$

where P_{ess}^* is the total power required from all storage branches; K_E is the proportional energy feedback gain; K_I is the integral energy feedback gain; z_E is the integral state of the energy error; and $\text{sat}(\cdot)$ is saturation by the total available charge and discharge capability of all storage branches. Positive P_{ess}^* corresponds to discharging support.

4.2. Safety Governor for Heterogeneous Storage Modules

For each module, a capability score is constructed from energy availability, power reserve, state of health, and thermal margin. In the discharge mode, the score is:

$$s_i^{\text{dis}} = a_1 \frac{SOC_i - SOC_{\min}}{SOC_{\max} - SOC_{\min}} + a_2 \frac{P_i^{\text{dis}, \max} - P_i}{P_i^{\text{rated}}} + a_3 SOH_i \quad (20)$$

where s_i^{dis} is the discharge capability score; $SOC_{\min}$ and $SOC_{\max}$ are the allowable SOC limits; P_i^{rated} is the rated power; SOH_i is the state of health; and a_1 to a_3 are non-negative normalized weights satisfying $a_1 + a_2 + a_3 = 1$. The four terms, respectively, quantify the SOC-associated discharge margin, unused branch discharge capability, degradation-related support reduction, and converter thermal derating requirement.

In the charging mode, the score is:

$$s_i^{\text{ch}} = a_1 \frac{SOC_{\max} - SOC_i}{SOC_{\max} - SOC_{\min}} + a_2 \frac{P_i^{\text{ch}, \max} + P_i}{P_i^{\text{rated}}} + a_3 SOH_i \quad (21)$$

where s_i^{ch} is the charge capability score. This definition reduces the charging allocation assigned to modules with high SOC. To prevent division by zero, each score is lower-bounded by a positive constant $s_{\min}$.

The normalized allocation factor is:

$$\rho_i = \frac{s_i}{\sum_{j=1}^N s_j} \quad (22)$$

where s_i is selected as s_i^{dis} when $P_{ess}^* \geq 0$ and as s_i^{ch} when $P_{ess}^* < 0$. The preliminary branch reference is denoted by ρ_i and is then projected onto the feasible set defined by (15) and (16).

4.3. Constrained Allocation by Projection

The final branch power reference is obtained by the following quadratic projection:

$$\min_{P_1^*, \dots, P_N^*} \sum_{i=1}^N \left[\frac{(P_i^* - \rho_i P_{\text{ess}}^*)^2}{q_i} + h_i (P_i^* - P_i(k-1))^2 \right] \quad (23)$$

$$\text{subject to } \sum_{i=1}^N P_i^* = P_{\text{ess}}^*, \quad P_i^* \in \Omega_i \quad (24)$$

where q_i is a positive priority factor, h_i is a ramp penalty coefficient, and Ω_i is the feasible interval of branch i given by (15) and (16). If the equality constraint cannot be satisfied because the total demand exceeds the available capability, the equality is relaxed to the nearest feasible total power, and the residual is passed to the inverter correction and grid exchange supervision layer. For $N = 3$ to 6 storage branches, the projection can be implemented by analytical saturation and redistribution. For a larger storage cluster, a low-dimensional quadratic programming solver may be executed at the slower coordination sampling rate.

Compared with a pure SOC-based allocation, (23) and (24) explicitly include converter power limits, ramp limits, thermal limits, and heterogeneous ratings. Compared with full model predictive control, the prediction horizon is short and the optimization dimension is low, which reduces real-time computational burden while preserving the feasibility protection required by the storage branches [12].

4.4. Constrained Inverter Active Power Correction

The grid-connected inverter is controlled as a constrained actuator for DC bus energy release. Its unsaturated active power reference is:

$$P_g^u = P_{g0} + K_G e_E + K_{Gi} \xi_E + K_F P_d^p \quad (25)$$

where P_g^u is the unsaturated inverter active power reference, P_{g0} is the scheduled grid exchange power, K_G is the inverter energy feedback gain, K_{Gi} is the integral gain, ξ_E is the inverter energy integral state, and K_F is the disturbance feedforward gain. When the DC bus energy exceeds the reference, the inverter increases active power export within its current capability. When the DC bus energy is below the reference, the inverter reduces active power export to mitigate capacitor discharge stress.

The admissible active power range is determined from the inverter current limit and the reactive power demand:

$$|P_g^*| \leq P_g^{\text{lim}} = 1.5 v_d \sqrt{I_{\text{max}}^2 - (i_q^*)^2} \quad (26)$$

where P_g^* is the final saturated active power reference; P_g^{lim} is the active power limit under the required reactive current i_q^* , and v_d is the PCC d axis voltage. The saturated reference is:

$$P_g^* = \text{sat}_{P_g^{\text{lim}}} (P_g^u) \quad (27)$$

To avoid integral windup during large disturbances, the integral state is updated by:

$$\frac{d\xi_E}{dt} = e_E + k_{aw} (P_g^* - P_g^u) \quad (28)$$

where k_{aw} is the antiwindup gain. When the inverter reference is not saturated, $P_g^* = P_g^u$, and (28) reduces to standard integral control. When saturation occurs, the correction term drives the integrator toward a feasible value.

The inverter current references are:

$$i_d^* = \frac{2P_g^*}{3v_d} \quad (29)$$

$$i_q^* = -\frac{2Q_g^*}{3v_d} \quad (30)$$

where Q_g^* is the reactive power reference. If the current magnitude obtained from (29) and (30) exceeds $I_{\max}$, active power correction is limited after satisfying the selected priority. In this paper, DC bus protection is assigned higher priority than reactive power support only when V_{dc} violates the emergency band; otherwise, reactive power support at the PCC is maintained according to the grid code requirement.

4.5. Local Converter Current Control

The branch current reference is computed from the power reference as follows:

$$i_i^* = \frac{P_i^*}{\eta_i V_{b,i}} \quad (31)$$

where i_i^* is the current reference of branch i . A first-order filter is used to avoid abrupt reference changes:

$$\tau_f \frac{di_i^r}{dt} + i_i^r = i_i^* \quad (32)$$

where i_i^r is the filtered current reference and τ_f is the reference filter time constant. The averaged duty ratio command is generated by:

$$d_i = \text{sat}_{[d_{\min}, d_{\max}]} \left[d_i^0 + k_{pi} (i_i^r - i_i) + k_{ii} \int (i_i^r - i_i) dt \right] \quad (33)$$

where d_i^0 is the feedforward duty ratio; k_{pi} and k_{ii} are the current PI gains; and $d_{\min}$ and $d_{\max}$ are the duty ratio limits. The saturation in (33) is consistent with the branch feasible set in the coordination layer.

5. Stability Analysis and Parameter Design

Figure 3 illustrates the coordinated damping mechanism of CAPEC. The storage path supplies synthetic damping through the feasible branch references P_i^* , whereas the inverter path supplies an additional damping path through P_g^* . These two paths act on the same DC bus energy state but are constrained by different physical limits.

The storage path receives the predicted imbalance, passes it through the safety governor, and projects the branch references onto the admissible set. The inverter path receives the same energy error, applies current-based saturation, and returns the saturation mismatch to the antiwindup loop. Their stable interaction is supported by time scale separation, positive energy feedback gains, and feasible reference projection. The resulting structure clarifies why CAPEC remains robust to bounded prediction error. It also tolerates moderate parameter uncertainty while avoiding infeasible converter commands.

5.1. Small-Signal Model

Linearizing (4) around an operating point $V_{dc} = V_{dc}^*$, $P_i = P_{i0}$, and $P_{inv} = P_{inv0}$ yields:

$$C_{dc} V_{dc}^* \frac{d\Delta V}{dt} = \sum_{i=1}^N \Delta P_i + \Delta P_{pv} - \Delta P_{inv} - \Delta P_{loss} \quad (34)$$

where ΔV is the small-signal DC bus voltage deviation. The aggregated response of the storage allocation loop is approximated as follows:

$$\sum_{i=1}^N \Delta P_i = -D_s \Delta V + G_s \Delta P_d \quad (35)$$

where D_s is the equivalent source-side damping produced by storage power feedback, and G_s is the disturbance feedforward gain assigned to the storage side. The inverter correction is expressed as follows:

$$\Delta P_{inv} = D_g \Delta V + G_g \Delta P_d \quad (36)$$

where D_g is the equivalent inverter-side damping and G_g is the inverter disturbance feed-forward gain. The loss perturbation is approximated by $\Delta P_{\text{loss}} = G_{\text{loss}} \Delta V$, where G_{loss} is the equivalent voltage sensitivity of losses. Substituting (35) and (36) into (34) yields:

$$C_{\text{dc}} V_{\text{dc}}^* \frac{d\Delta V}{dt} = -(D_s + D_g + G_{\text{loss}}) \Delta V + (G_g - G_g + 1) \Delta P_d \quad (37)$$

The dominant DC bus voltage pole is therefore:

$$\lambda_v = -\frac{D_s + D_g + G_{\text{loss}}}{C_{\text{dc}} V_{\text{dc}}^*} \quad (38)$$

Equation (38) demonstrates the damping effect of the proposed method. Fixed droop control increases only D_s and maintains D_g close to zero because the inverter active power command is not coordinated with DC bus energy [8,10]. CAPEC increases both D_s and D_g while constraining their commands within the feasible converter set. The voltage mode is locally asymptotically stable when $D_s + D_g + G_{\text{loss}} > 0$.

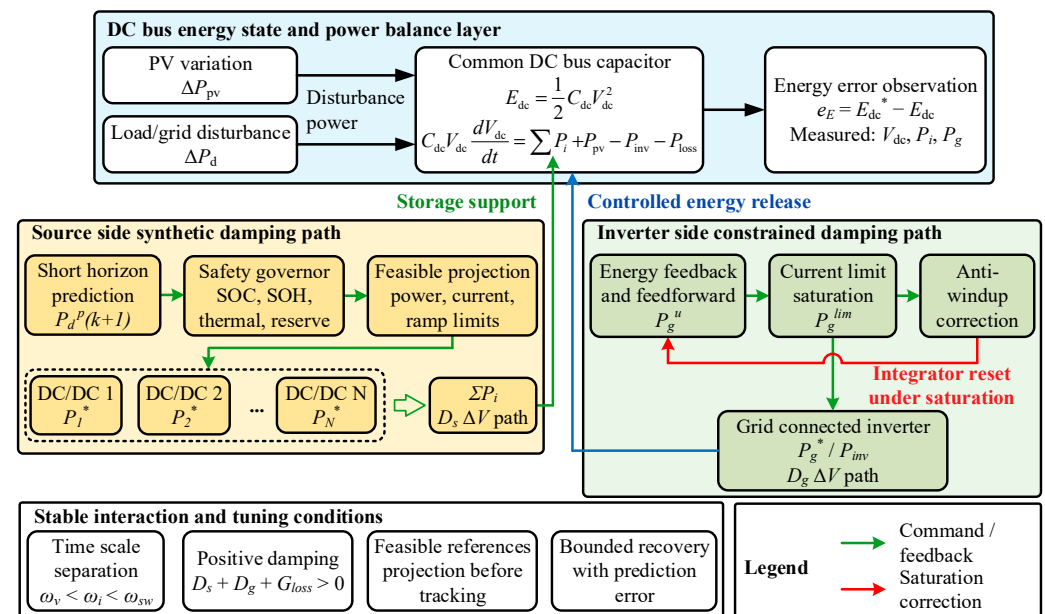


Figure 3. Coordinated damping paths and stability conditions of CAPEC.

5.2. Energy Function Analysis

To analyze large disturbance behavior before saturation is reached, the following candidate energy function is selected:

$$W = \frac{1}{2} e_E^2 + \frac{1}{2} c_z z_E^2 + \frac{1}{2} c_\xi \xi_E^2 \quad (39)$$

where W is the storage function; c_z and c_ξ are positive constants; and z_E and ξ_E are the integral states of the storage and inverter correction loops. If the allocation projection is feasible and the current loops have higher bandwidth than the energy coordination loop, substituting (19) and (25) into the energy dynamics yields:

$$\frac{dW}{dt} \leq -\alpha_E e_E^2 - \alpha_z z_E^2 - \alpha_\xi \xi_E^2 + \beta_d \|e_E\| |P_d - P_d^p| \quad (40)$$

where α_E , α_z , α_ξ , and β_d are positive constants determined by controller gains and converter-tracking bandwidth. Equation (40) indicates input-to-state stability with respect to prediction error. If the disturbance prediction error is bounded, the DC bus energy error is also bounded. If the prediction error converges to zero and the references remain feasible, e_E converges to a neighborhood of zero determined by measurement noise and loss modeling error.

5.3. Tuning Principles

The weighting coefficients in (20) and (21) are not empirical fitting parameters. They are selected according to the physical stress component to be prioritized. For lithium battery modules with similar age, a_1 and a_2 are assigned larger values because SOC and the power reserve determine the immediate support capability. When modules have different ages or cooling conditions, a_3 and a_3 are increased to prevent aged or thermally stressed modules from being overused. The recommended initial setting is $a_1 = 0.35$, $a_2 = 0.35$ and $a_3 = 0.15$, followed by sensitivity verification under the maximum credible PV drop and load step.

The gains K_E and K_G are selected so that the desired voltage pole in (38) is slower than the inner current loop but faster than the dominant disturbance time scale. A practical condition is:

$$5\omega_v \leq \omega_i, \quad 0 < \omega_v \leq 0.2\omega_{sw} \quad (41)$$

where ω_v is the desired outer voltage energy bandwidth; ω_i is the inner current loop bandwidth; and ω_{sw} is the switching angular frequency. The integral gains K_I and K_{GI} are increased only after the transient response is sufficiently damped because excessive integral action may conflict with current limits during severe disturbances. Table 3 summarizes the physical meanings and recommended design rules of the key CAPEC parameters, including capability weighting factors, energy damping gains, prediction coefficient, branch ramp limit, and antiwindup gain.

Table 3. Parameter design guidance for CAPEC.

Parameter	Physical Meaning	Recommended Design Rule
a_1	SOC participation weight	Increase when energy balance among modules is the priority
a_2	Power reserve weight	Increase when transient voltage support is the priority
a_3	State of health weight	Increase for aged or heterogeneous battery modules
K_E, K_G	Energy damping gains	Select from the target pole in (38) and keep the outer loop slower than current loops
K_I, K_{GI}	Integral recovery gains	Use small values and enable antiwindup correction under saturation
μ_d	Prediction coefficient	Set close to zero for noisy measurements and close to one for fast repetitive disturbances
R_i	Branch ramp limit	Determine from battery current limit and semiconductor thermal rating
k_{aw}	Antiwindup gain	Choose to discharge the integrator within one to three outer loop time constants

6. Case Study

6.1. Simulation System Configuration

For the executable simulation, three benchmark methods are retained to directly examine the incremental effect of the proposed controller. Method A is independent control (ICM), in which each energy-storage branch tracks a local reference and the grid-connected inverter follows the scheduled active power command without DC bus energy coordination. Method B is fixed droop control (FDC), in which the branch power references are generated from the DC bus voltage deviation by constant droop gains. Method C is the proposed CAPEC, in which short-horizon disturbance prediction, safety-constrained branch allocation, and bounded inverter active power correction are simultaneously activated. The same converter ratings, current limits, DC bus capacitance, and disturbance profiles are used for all methods. Table 4 lists the main simulation parameters, initial operating conditions, and case definitions to improve reproducibility.

Table 4. Main simulation parameters, initial operating conditions, and case definitions.

Item	Parameter or Event	Value or Description
Simulation platform	Software and solver	MATLAB R2023b fixed step EMT model; simulation time 0 to 8 s; integration step 50 μ s.
AC system	Feeder and transformer	13.8 kV distribution feeder; 0.48 kV inverter side; 60 Hz nominal frequency.
DC bus	Rated voltage and capacitance	$V_{dc}^* = 800$ V; $C_{dc} = 20$ F.
PV source	Initial operating power	3.0 MW before the disturbance sequence.
Storage branch 1	Battery and converter rating	Bidirectional DC/DC converter module; 1.0 MW, 2.0 MWh, initial SOC 80%, SOH 98%.
Storage branch 2	Battery and converter rating	Bidirectional DC/DC converter module; 0.8 MW, 1.6 MWh, initial SOC 65%, SOH 92%.
Storage branch 3	Battery and converter rating	Bidirectional DC/DC converter module; 0.7 MW, 1.4 MWh, initial SOC 50%, SOH 86%.
Storage limits	Operating bounds	SOC range 20% to 90%; ramp limits 1.0, 0.8, and 0.6 MW/s for branches 1 to 3.
Grid-connected inverter	Rating and current limit	3.0 MVA. The d axis active current is limited by I_{max} , and active current priority is used only when the DC bus enters the emergency band.
CAPEC controller	Sampling and principal parameters	Coordination period $\Delta t = 10$ ms; $\mu_d = 0.6$; $a_1 = 0.35$, $a_2 = 0.35$, $a_3 = 0.15$; $K_E = 3.0$, $K_I = 6.0$, $K_G = 1.2$, $K_{GI} = 2.0$, $K_F = 0.35$, and $k_{aw} = 8.0$ in the per unit implementation.
Case A	PV and load disturbance	PV power changes from 3.0 MW to 1.8 MW and then to 2.6 MW; a representative feeder load increases by 30% and later returns to its initial value.
Case B	Grid interface disturbance	The scheduled grid exchange is changed over a short interval to emulate breaker operation or an abrupt external grid power request.
Case C	Heterogeneous storage condition	Rated power, initial SOC, SOH, and ramp limits differ among the three storage branches.

6.2. Evaluation Indices

The maximum DC bus voltage deviation is defined as follows:

$$\Delta V_{\max} = \max_t |V_{dc}(t) - V_{dc}^*| \quad (42)$$

where $\Delta V_{\max}$ measures the worst transient voltage excursion. The recovery time is:

$$t_{\text{rec}} = \inf \{t : |V_{dc}(\tau) - V_{dc}^*| \leq \varepsilon V_{dc}^*, \forall \tau \geq t\} \quad (43)$$

where ε is the allowable voltage recovery band. The power sharing error is:

$$e_{\text{share}} = \sqrt{\frac{1}{N} \sum_{i=1}^N \left(\frac{P_i}{P_i^{\text{rated}}} - \frac{P_{\Sigma}}{P_{\Sigma}^{\text{rated}}} \right)^2} \quad (44)$$

where P_{Σ} is the total storage power and $P_{\Sigma}^{\text{rated}}$ is the total storage rated power. This normalized definition is suitable for heterogeneous storage modules. The grid active power-tracking error is:

$$e_g = \sqrt{\frac{1}{T} \int_0^T (P_g(t) - P_{g0}(t))^2 dt} \quad (45)$$

where T is the evaluation window. In Table 5, e_g is normalized by the rated inverter active power and reported in percent. A lower e_g is desirable, but CAPEC does not treat grid power-tracking as the sole objective. During DC bus emergencies, the inverter may temporarily deviate from P_{g0} within its current limit to protect the DC bus energy state. Consequently, a nonzero grid active power-tracking error under CAPEC does not indicate inferior performance; it reflects the intended priority assigned to DC bus energy protection when inverter current constraints are active.

Table 5. Quantitative performance indices for the three simulation cases.

Case	Method	$\Delta V_{\max}$ (V)	$V_{\min}$ (V)	$V_{\max}$ (V)	t_{rec} (s)	e_{share} (%)	e_g (%)
A	ICM	88.06	711.94	800.00	6.002	30.84	0.000
	FDC	73.68	726.32	800.00	6.002	2.95	0.000
	CAPEC	6.35	793.65	806.12	2.772	1.05	3.818
B	ICM	16.72	783.28	800.00	3.476	28.13	9.068
	FDC	16.23	783.77	801.68	3.198	2.27	9.068
	CAPEC	2.86	797.70	802.86	0.000	2.11	8.612
C	ICM	60.16	739.84	800.00	6.002	23.06	0.000
	FDC	50.48	749.52	800.00	6.002	10.24	0.000
	CAPEC	4.94	795.06	804.93	2.092	2.87	2.664

6.3. Simulation Results and Discussion

Case A combines photovoltaic fluctuation and load step disturbance. The photovoltaic output decreases from 3.0 MW to 1.8 MW and then recovers to 2.6 MW, while a representative feeder load increases by 30% and subsequently returns to its initial value. This case verifies whether the storage allocation layer and inverter correction layer can jointly suppress the power deficit caused by simultaneous source-side reduction and AC-side demand increase. Figure 4 reports the DC bus voltage, total storage support power, and branch powers under CAPEC.

Case B considers a grid interface power disturbance. The disturbance is imposed by changing the scheduled grid exchange power over a short interval, which emulates breaker operation or an abrupt external grid power request. This case evaluates the effects of inverter current limitation and antiwindup correction. Figure 5 uses the same three waveform groups as Case A, allowing for a consistent comparison of DC bus response, total storage support, and branch-level allocation.

Case C considers heterogeneous storage operation. Three storage modules are assigned different rated powers, initial SOC values, SOH values, and ramp limits. This case verifies whether the proposed safety constrained allocation avoids treating nonidentical modules as equal power sources. Figure 6 highlights the redistribution of support power toward branches with higher admissible capability.

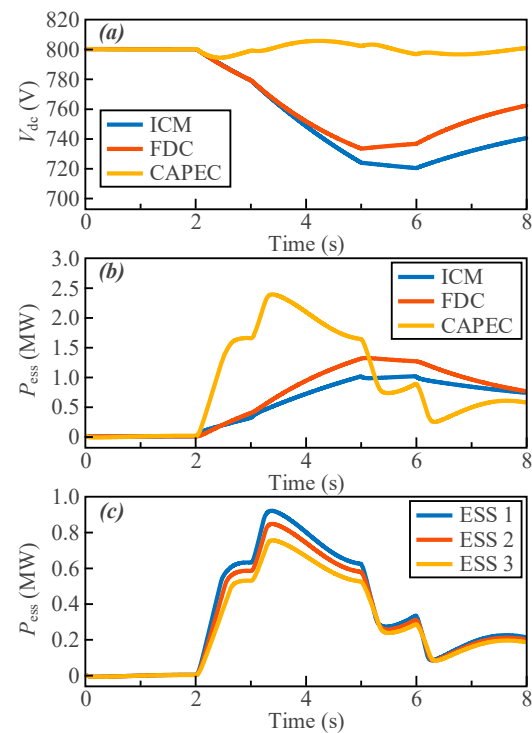


Figure 4. Simulation results of Case A under combined photovoltaic fluctuation and load step. (a) DC bus voltage. (b) Total storage support power. (c) Branch powers under CAPEC.

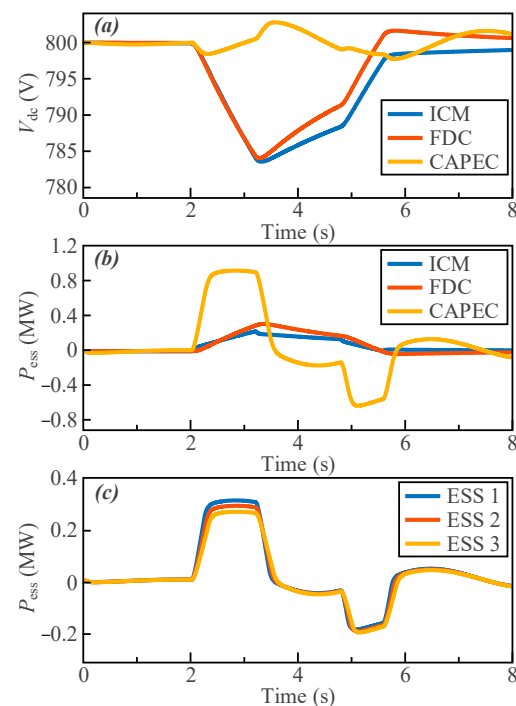


Figure 5. Simulation results of Case B under grid interface power disturbance. (a) DC bus voltage. (b) Total storage support power. (c) Branch powers under CAPEC.

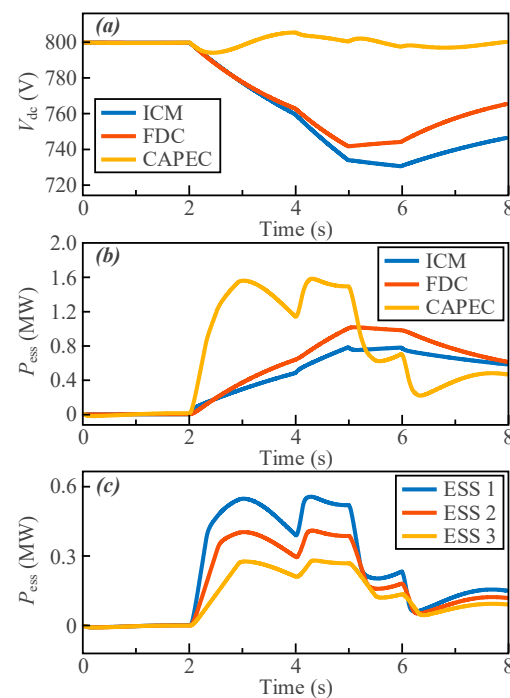


Figure 6. Simulation results of Case C under heterogeneous storage conditions. (a) DC bus voltage. (b) Total storage support power. (c) Branch powers under CAPEC.

The simulation section contains three nonoverlapping cases: combined source and load disturbance, grid interface disturbance, and heterogeneous storage operation. Each case is represented by one figure with three waveform groups, which reduces repeated descriptions while retaining the variables required to evaluate DC bus stability, total support demand, and branch-level allocation.

The simulation results indicate that CAPEC provides the most significant improvement in DC bus voltage deviation, recovery time, and capability-based branch sharing. In Case A, CAPEC limits the maximum DC bus voltage deviation to 6.35 V, compared with 88.06 V for ICM and 73.68 V for FDC. The grid active power-tracking error of 3.818% is introduced because the inverter temporarily deviates from its scheduled power to preserve DC bus energy within its current limit. In Case B, CAPEC reduces the voltage deviation to 2.86 V and keeps eg at 8.612%, slightly below the 9.068% obtained by the benchmark methods. In Case C, CAPEC reduces the voltage deviation to 4.94 V and lowers the sharing error to 2.87%, while the 2.664% grid-tracking error reflects the deliberate use of inverter support during a constrained energy transient. These results show that CAPEC prioritizes DC bus protection and feasible converter operation over exact short-term grid active power tracking.

6.4. Physical Experimental Verification

To address the practical applicability of the proposed method, a reduced power laboratory platform was constructed to reproduce the grid interface disturbance represented by Case B. The experimental setup includes a DC source and photovoltaic emulator, a common DC bus, a grid-connected inverter with an LCL filter, a programmable breaker, and an AC grid interface. The topology and the corresponding laboratory platform are shown in Figures 7 and 8. The experiment focuses on the DC bus response during unplanned breaker operation, which is the physical counterpart of the grid interface power disturbance used in the simulation.

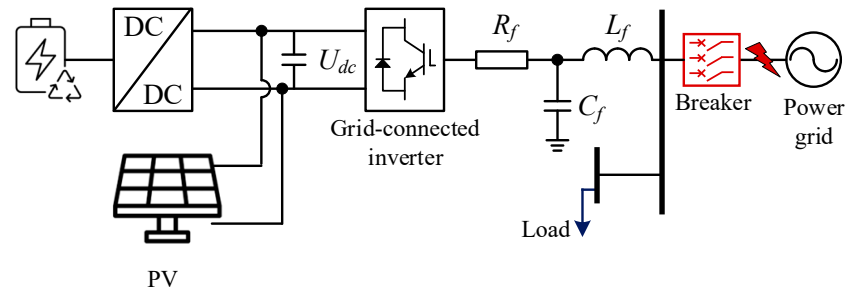


Figure 7. Physical experimental topology for the grid interface disturbance validation.



Figure 8. Physical experimental platform.

The oscilloscope records in Figures 9 and 10 use the same channel definition. The green trace is the DC bus current, the magenta trace is the DC bus voltage, the cyan trace is the inverter-side AB voltage, and the blue trace is the grid-side AB voltage. During unintended breaker opening, the grid exchange path is interrupted and the DC bus current changes rapidly, while the DC bus voltage remains bounded without sustained oscillation. During breaker closing, the inverter-side voltage resynchronizes with the grid-side voltage after the switching transient, and the DC bus voltage remains close to the operating level observed before the event.

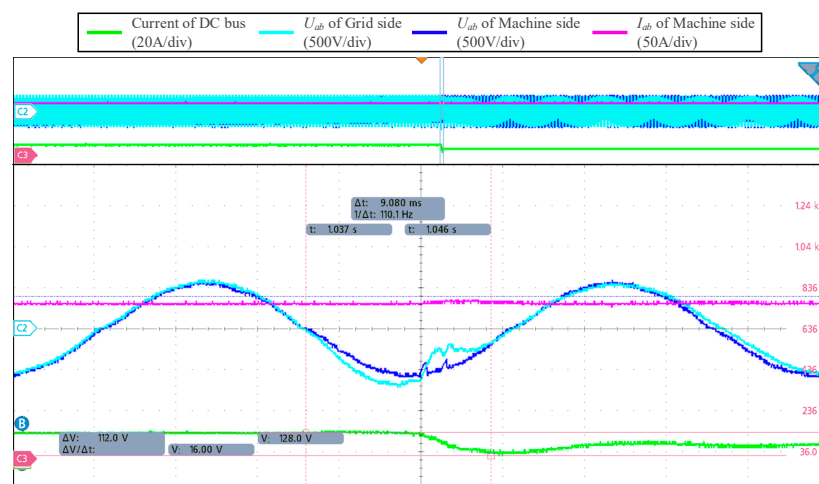


Figure 9. Measured waveforms after unintended breaker opening.

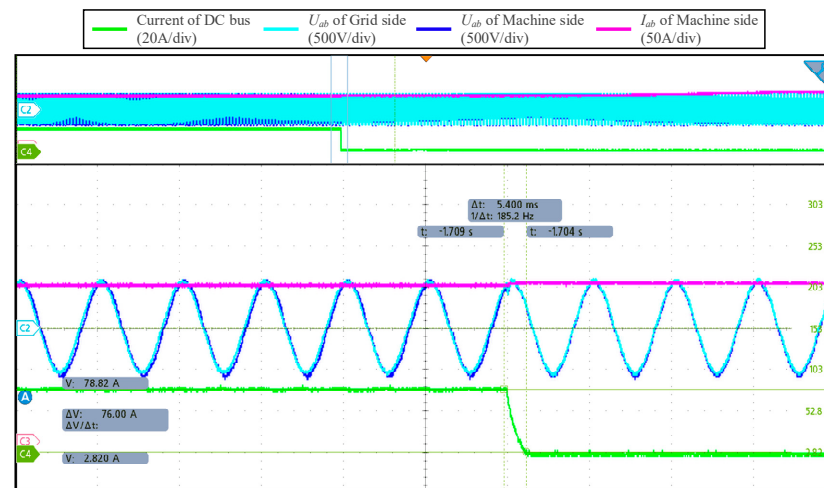


Figure 10. Measured waveforms after breaker closing.

The physical test does not replace the detailed MATLAB R2023b comparison because the laboratory platform is operated at reduced power and is configured for the Case B-type breaker disturbance. It nevertheless demonstrates that the proposed control structure can be implemented on a real converter platform and that the DC bus response remains stable under abrupt grid interface switching. The result therefore complements the simulation study by confirming the practical feasibility of the disturbance prediction, inverter saturation, and DC bus energy regulation concepts.

The robustness of CAPEC follows from the separation between performance objectives and hard feasibility constraints. Disturbance prediction improves transient response, but the projection layer prevents a prediction error from producing branch references outside the admissible power, current, thermal, SOC, or ramp rate limits. Parameter uncertainties in C_{dc} , converter loss, and branch resistance enter the disturbance observer as residual power and are therefore re-estimated at each coordination step. Conservative margins in the capability scores can further absorb errors in SOC and SOH.

The proposed controller requires measurements of V_{dc} , branch current, storage terminal voltage, SOC, and inverter current. These signals are typically available in battery energy-storage stations. High bandwidth communication among all branches is not required for the basic implementation because the capability scores are calculated in the supervisory controller using local measurements collected at the energy management layer. If communication delay exists, μ_d can be reduced and R_i can be tightened so that the outer coordination loop remains slower than the inner current loops. Long delays may reduce sharing accuracy and should be handled by hierarchical grouping or local fallback droop control.

7. Conclusions

This paper reformulates DC bus voltage stabilization in a grid-connected microgrid with multiple energy-storage converter branches as a constrained energy coordination problem. The proposed CAPEC method integrates short-horizon disturbance prediction, safety-constrained storage allocation, and inverter active power correction with saturation and antiwindup protection. By considering SOC, power reserve, SOH, thermal margin, current limit, and ramp rate within a unified feasible capability set, CAPEC enables storage branches to provide support according to their actual operating capability. Small-signal analysis shows that CAPEC enhances the equivalent DC bus damping through both source-side allocation and inverter-side correction. The energy function analysis further indicates bounded voltage recovery under bounded prediction error and feasible

converter references. Three simulation cases verify the effectiveness of CAPEC under combined PV and load disturbance, grid interface disturbance, and heterogeneous storage operation, while a reduced power physical experiment verifies the Case B breaker disturbance on a laboratory converter platform. The results demonstrate reduced DC bus voltage excursions, improved capability-based power allocation, and bounded grid-side active power correction. The present verification remains limited to a reduced power experiment and simulation cases with bounded communication delay and selected battery aging states. Future work will include hardware-in-the-loop tests, broader battery-aging conditions, larger storage clusters, and more complex communication-delay and packet-loss cases.

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