

Article

Submodule Cyclic Control and Its Auxiliary Methods for MMC Capacitor Voltage Balancing

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Abstract

Submodule capacitor voltage balancing in modular multilevel converters (MMCs) is a key issue for ensuring stable converter operation and reducing device voltage stress. To address the high computational burden and high switching frequency of the conventional sorting-based voltage balancing method under nearest-level modulation (NLM), this paper analyzes the mechanism of capacitor voltage imbalance from the perspective of periodic submodule energy distribution. The effects of submodule insertion time, arm-current integration, and the phase difference of the AC current on capacitor voltage imbalance are investigated. On this basis, a submodule cyclic control method for MMC capacitor voltage balancing is proposed. By periodically circulating the control signals of submodules, each submodule sequentially experiences different insertion patterns within one cyclic control period, thereby achieving balanced energy distribution among submodule capacitors. Furthermore, to address the prolonged cyclic control period caused by an increased number of submodules, a grouping-based auxiliary control method is designed to shorten the cyclic control period while maintaining the capacitor voltage fluctuation within the required range. To provide direct correction of out-of-margin capacitor voltage deviations during the post-fault balancing process, an over-margin auxiliary control method is further proposed. Finally, a three-phase nine-level MMC simulation model is established in PSCAD/EMTDC to verify the proposed method under steady-state and transient operating conditions. The simulation results show that the proposed method can effectively achieve submodule capacitor voltage balancing, shorten the cyclic control period, enhance post-fault voltage-balancing capability, and reduce both the switching frequency and the computational burden of real-time sorting while maintaining satisfactory voltage balancing performance.

Keywords: modular multilevel converter; capacitor voltage balancing; capacitor voltage energy analysis; submodule cyclic control



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1. Introduction

With the increasing penetration of renewable energy, long distance transmission of offshore wind power, development of voltage-source-converter-based high-voltage DC (VSC-HVDC) transmission, and medium- and high-voltage DC distribution systems, power electronic converter equipment is developing toward higher voltage, larger capacity, higher efficiency, and higher reliability [1,2]. Owing to its modular structure, low harmonic content

of output voltage, low equivalent switching frequency, strong scalability, and suitability for high-voltage and high-power conversion scenarios, MMC has become an important converter topology in VSC-HVDC transmission, offshore wind power integration, medium-voltage DC distribution, and hybrid AC/DC systems [3].

An MMC is composed of numerous cascaded submodules, whose capacitors in these submodules not only serve as energy buffers but also provide the basis for generating multilevel output voltages. When the submodule capacitor voltages are unevenly distributed, some devices can be subjected to increased voltage stress, thereby potentially causing output voltage distortion, arm-energy fluctuation, increased circulating current, and additional device losses [4]. Therefore, achieving submodule capacitor voltage balancing without significantly increasing the switching frequency and control complexity is a fundamental issue in the valve-level control of MMCs.

Existing MMC capacitor voltage balancing strategies can generally be divided into two groups. One category realizes capacitor voltage balancing through external auxiliary balancing control loops, while the other achieves this objective by optimizing the capacitor voltage balancing algorithm or modulation algorithm [5]. The former usually starts from the perspectives of arm energy, phase-unit energy, or submodule capacitor voltage deviation, and introduces auxiliary control components into the modulation wave, circulating-current control, or arm-energy control loop to regulate the energy distribution among different arms or submodules. For example, an enhanced energy control strategy has been reported to realize DC capacitor voltage balancing in MMCs and enhance the operating stability of hybrid AC/DC microgrids [6]. A major benefit of this type of method is that capacitor voltage can be regulated from the system energy level, with a relatively clear control objective. However, such methods usually require additional voltage and current measurement units as well as closed-loop controllers, resulting in a relatively complex control structure. For high-level and high-power MMCs, they may also increase the difficulty of control parameter tuning and the cost of hardware implementation.

In comparison, optimizing the capacitor-voltage balancing algorithm requires no significant modification of the outer control architecture of the MMC, and is therefore more flexible in engineering applications. The conventional sorting-based voltage balancing method is one of the most widely used approaches. Its basic principle is to collect and sort the capacitor voltages of all submodules in each arm in real time. When the arm current flows in the charging direction, submodules with lower capacitor voltages are selected with priority so that their capacitor voltages increase. When the arm current is in the discharging direction, submodules with higher capacitor voltages are preferentially switched in so that their capacitor voltages decrease, thereby achieving voltage balancing among submodules. To reduce the dependence of the conventional sorting method on arm-current measurement and real-time sorting, a currentless sorting-and-selection method has been proposed in [7], which achieves a balancing performance close to that of the conventional sorting method without using arm-current signals. A current-free voltage balancing strategy for individual submodules was further developed in [8], in which capacitor voltage tracking is realized by regulating the DC component associated with each submodule capacitor current. For voltage balancing under carrier phase-shifted PWM (CPS-PWM), an efficient capacitor voltage balancing strategy adapted to CPS-PWM was proposed in [9], while a robust capacitor voltage balancing method considering wide power-range operation was presented in [10] to improve dynamic performance under low-power conditions. For capacitor voltage sorting under space-vector PWM, an efficient sorting algorithm was proposed in [11] to lower the computational burden in embedded implementation. These studies have achieved satisfactory performance in reducing sensor dependence, improving balancing speed, and enhancing modulation adaptability. However, most of these methods

still require capacitor voltage feedback, sorting, or selection logic. With the increase in the number of submodules per arm, the computational burden of the controller and the submodule switching frequency may still increase significantly.

In recent years, increasing attention has been paid to voltage balancing control with low sensor dependence and low computational burden. A sensorless voltage balancing method was proposed in [12], where submodule capacitor voltage equalization of MMCs is realized via single-carrier PWM, reducing the dependence of conventional methods on voltage and current measurements. In [13], a capacitor voltage self-balancing method relying on switching-state matrix construction was proposed, where the switching-state matrix is constructed offline and switching signals are periodically assigned, thus avoiding extensive sensor requirements and complex real-time computation. In [14], a selection criterion for submodule switching-state vector combinations was further proposed for self-balancing half-bridge MMCs to reduce device switching losses. In [15], neural network prediction was introduced into submodule capacitor voltage balancing control, where the predicted voltage variation trend is used to assist submodule switching decisions. These methods indicate that capacitor voltage balancing control is gradually evolving from pure real-time voltage sorting toward switching-sequence design, state-matrix construction, sensor simplification, and intelligent prediction.

The modulation strategy also affects the submodule capacitor voltage balancing performance. Nearest-level modulation (NLM) has high application value for high-voltage and high-power MMCs because of its simple implementation and low switching frequency. However, during the NLM process, the quantization and rounding of the modulation wave cause the insertion durations of different submodules within one fundamental period to be unequal. In addition, different submodules experience different magnitudes and directions of the arm current, leading to unequal charge and discharge quantities in submodule capacitor units [16]. Regarding the output quality and modulation performance of NLM, a flexible NLM scheme was introduced in [17] to enhance the adaptability of conventional NLM under different operating conditions. In [18], the output voltage quality of MMCs was improved through offset injection, while in [19], the effectiveness of modified nearest-level control in improving the power quality of HVDC-MMC systems was verified on a real-time hardware-in-the-loop platform. In [20], an equivalent NLM model built around the DC voltage control loops of submodules was established to improve the computational efficiency of electromagnetic transient simulations. In [21], the deviation between the modulation and staircase waveforms was corrected, which helps reduce submodule capacitor voltage fluctuation and suppress circulating current to a certain extent. Topology-assisted approaches have also been proposed to reduce capacitor voltage ripple and converter losses. For example, an APF-MMC diverts low-frequency ripple power through an additional active power filter branch [22], whereas a high-ratio-transformer-based soft open point coordinates a dedicated topology with mixed-frequency modulation [23]. These methods operate at a different topology level from the signal reassignment method studied here. In summary, most existing NLM improvement methods mainly focus on modulation wave correction or output voltage quality, while insufficient attention has been paid to the energy distribution characteristics of submodules within and beyond the fundamental period. Therefore, a capacitor voltage balancing strategy needs to be developed suitable for NLM from the perspectives of submodule insertion duration, insertion sequence, and periodic energy exchange, while maintaining low computational burden and low switching frequency.

2. Analysis of MMC Capacitor Voltage Imbalance Based on Energy Balance

Figure 1 shows a basic three-phase topology for the modular multilevel converter. Each phase unit is divided into one upper arm and one lower arm, and every arm consists of

N series-connected submodules connected with a current-limiting reactor. The submodule investigated in this paper adopts a half-bridge topology, which comprises two IGBTs, two antiparallel diodes, and one energy storage capacitor. Under normal operating conditions, the submodule has two operating states: (1) the inserted state, in which the submodule output voltage is U_C and (2) the bypass state, in which the submodule output voltage equals 0. Moreover, this submodule also has a blocked state, which is generally used under fault conditions.

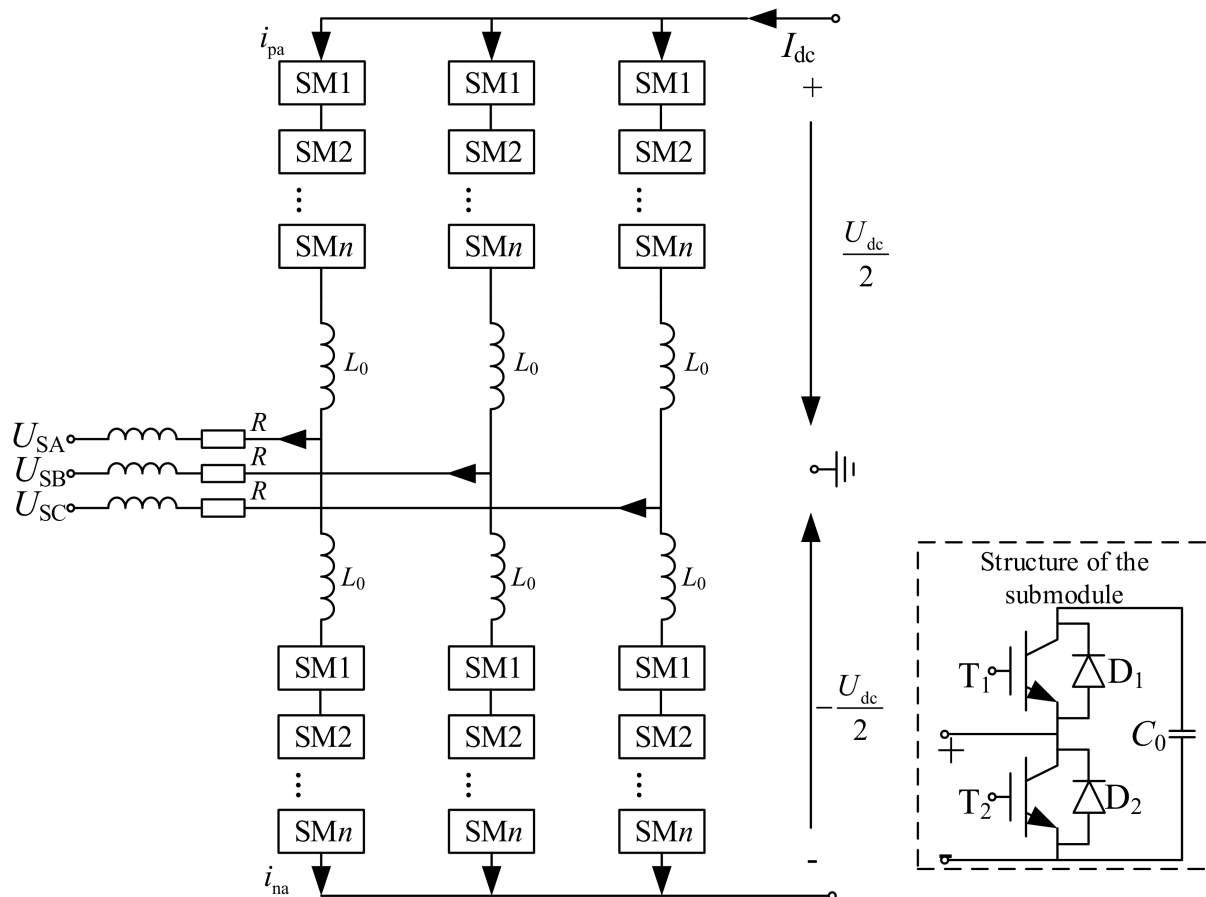


Figure 1. Topology of the MMC.

Under normal operating conditions, the converter controls submodule switching states through a modulation strategy implemented in the MMC. In this paper, NLM is adopted to make the AC terminal voltage of the MMC approximate the modulation wave. As shown in Figure 2, by combining NLM with the voltage balancing control strategy, the given modulation wave is quantized and rounded to determine the insertion states of submodules in both upper and lower arms, as expressed in (1). Then, according to the submodule insertion states, the trigger pulses are sent to the control terminals of each submodule after signal processing by the capacitor voltage balancing control strategy.

$$\begin{cases} n_{up} = \frac{1}{2}N - \text{round}(\frac{u_j^*}{U_C}) \\ n_{down} = \frac{1}{2}N + \text{round}(\frac{u_j^*}{U_C}) \end{cases} \quad (1)$$

where u_j^* denotes the phase- j modulation voltage reference, with $j = a, b, c$.

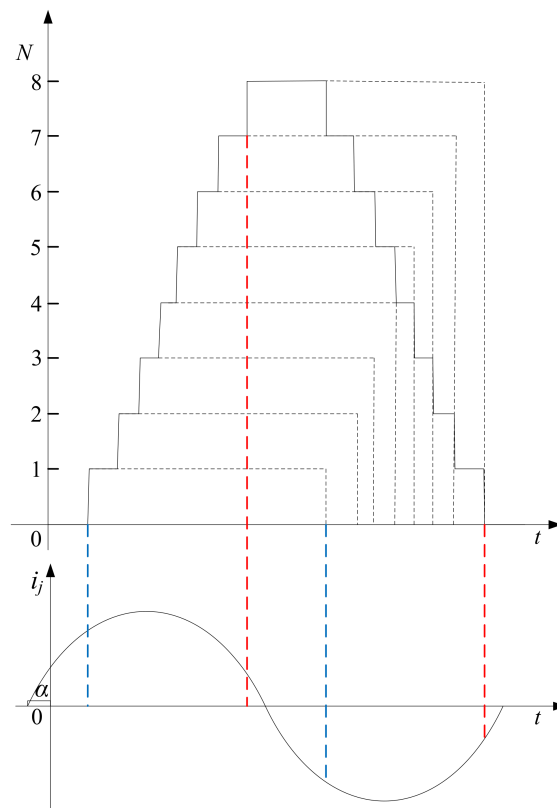


Figure 2. Relationship between the AC current and the submodule conduction intervals.

When the MMC operates under normal steady-state conditions, the DC side voltage remains constant and the AC side outputs stable sinusoidal AC voltages. In the converter station, the overall DC current I_{dc} is uniformly allocated to the three phase units, while the AC current i_j is equally shared by the upper and lower arms. Therefore, the upper- and lower-arm currents of the three phases can be written as follows:

$$\begin{cases} i_{pj} = \frac{1}{2}i_j + \frac{1}{3}I_{dc} \\ i_{nj} = -\frac{1}{2}i_j + \frac{1}{3}I_{dc} \end{cases} \quad (2)$$

where i_{pj} and i_{nj} denote the currents in the upper and lower arms of the three phases, respectively; i_j denotes the three-phase current on the converter-valve side; and I_{dc} denotes the DC current.

As the AC terminal at the converter station outputs fundamental frequency AC voltage, the modulation signal generated by the station-level converter control should also take the fundamental period as its modulation period. To analyze the energy balance of the capacitor voltage, its energy variation within a capacitor within one fundamental period T is first calculated, as shown in (3).

$$\begin{aligned} W_C &= \frac{1}{2}Cu(t) \Big|_{t_0}^{t_0+T} \\ &= \frac{1}{2}Cu(t_0 + T)^2 - \frac{1}{2}Cu(t_0)^2 \\ &= \frac{1}{2}[Cu(t_0 + T) - Cu(t_0)][Cu(t_0 + T) + Cu(t_0)] \\ &= \frac{1}{2}[q(t_0 + T) - q(t_0)][q(t_0 + T) + q(t_0)] \end{aligned} \quad (3)$$

According to (3), the energy variation of the capacitor within one fundamental period can be converted into the charge variation of the capacitor over that period. Therefore, the energy variation can be reflected by calculating the charge variation of the capacitor within

one fundamental period. Taking one fundamental period T as an example, the charge variation of a certain phase unit in the converter station within one fundamental period is calculated, as shown in (4) and (5). As the AC current i_j is sinusoidal, its integral over one fundamental period is zero, whereas the integral of the DC component is $I_{dc}T/3$. Therefore, under steady-state operating conditions, the charge variations of the upper and lower arms of each phase unit within one period are constant and equal.

$$\begin{cases} \text{upper : } q(t_0 + T) - q(t_0) = \int_{t_0}^{t_0+T} idt = \int_{t_0}^{t_0+T} \frac{1}{3} I_{dc} dt + \int_{t_0}^{t_0+T} \frac{1}{2} i_j dt \\ \text{lower : } q(t_0 + T) - q(t_0) = \int_{t_0}^{t_0+T} idt = \int_{t_0}^{t_0+T} \frac{1}{3} I_{dc} dt - \int_{t_0}^{t_0+T} \frac{1}{2} i_j dt \end{cases} \quad (4)$$

$$\begin{cases} \text{upper : } q(t_0 + T) + q(t_0) = q(t_0 + T) - q(t_0) + 2q(t_0) = \int_{t_0}^{t_0+T} idt + 2q(t_0) \\ \quad = \int_{t_0}^{t_0+T} \frac{1}{3} I_{dc} dt + \int_{t_0}^{t_0+T} \frac{1}{2} i_j dt + 2q(t_0) \\ \text{lower : } q(t_0 + T) + q(t_0) = q(t_0 + T) - q(t_0) + 2q(t_0) = \int_{t_0}^{t_0+T} idt + 2q(t_0) \\ \quad = \int_{t_0}^{t_0+T} \frac{1}{3} I_{dc} dt - \int_{t_0}^{t_0+T} \frac{1}{2} i_j dt + 2q(t_0) \end{cases} \quad (5)$$

where $q(t_0)$ denotes the charge at time t_0 , and T denotes the fundamental period.

Taking the upper arm as an example, the capacitor voltage variation of the i -th submodule within one fundamental period can be expressed by explicitly considering its own NLM-determined insertion interval $t_{on,i}$, as follows:

$$\begin{aligned} U_{SM,i}(t) &= U_{SM,i}(t_0) + \frac{1}{C} \int_{t_{on,i}}^{t_{off,i}} \left(\frac{1}{3} I_{dc} + \frac{1}{2} i_j \right) dt \\ &= \frac{q_{SM,i}(t_0)}{C} + \frac{1}{C} \int_{t_{on,i}}^{t_{off,i}} \frac{1}{3} I_{dc} dt + \frac{1}{C} \int_{t_{on,i}}^{t_{off,i}} \frac{1}{2} i_j dt \end{aligned} \quad (6)$$

where $U_{SM,i}(t)$ denotes the i -th submodule capacitor voltage, $U_{SM,i}(t_0)$ denotes the submodule capacitor voltage at the initial time t_0 within the fundamental period, and $q_{SM,i}(t_0)$ denotes the submodule charge at the initial time t_0 of the fundamental period. $t_{on,i}$ and $t_{off,i}$ denote the insertion and bypassing intervals of the i -th submodule within one fundamental period, respectively.

Based on (6), the capacitor voltage of the submodule consists of three components: the initial capacitor voltage component, the DC component, and the AC component. Among them, the initial component is determined by the submodule charge $q_{SM,i}(t_0)$ at the initial time, and this component remains constant when the capacitor voltage is stable. For the DC component, although the integral of the DC current is constant, the accumulated charge contribution to submodule SMi depends on its own insertion interval $t_{on,i}$. Under NLM, the quantization and rounding of the modulation wave result in inherently unequal insertion intervals among different submodules. Therefore, different submodules receive different DC charge components within one fundamental period. For the AC component, the difference is caused not only by the unequal total insertion durations but also by the different positions of $t_{on,i}$ within the AC-current waveform. Even if two submodules have the same total insertion duration, their insertion intervals may correspond to different AC current magnitudes and polarities, leading to different AC charge components. After one fundamental period, the total charge of each phase arm may remain bounded under steady-state operation. However, this does not imply uniform charge distribution among individual submodules. Owing to the unequal insertion intervals $t_{on,i}$ and different AC-current integration results, different submodules may accumulate different charge variations, leading to capacitor voltage deviations. Therefore, this paper analyzes the mechanism of submodule capacitor voltage variation from the viewpoint of energy balance

and, on this basis, develops a submodule capacitor voltage balancing strategy to suppress capacitor voltage fluctuation.

3. Submodule Cyclic Control Method for MMC Capacitor Voltage Balancing

For the conventional NLM-based voltage balancing strategy, the periodic energy distribution among individual submodules is not explicitly considered. As indicated by Equation (6), the capacitor voltage variation of submodule SM_i depends on both its own insertion interval $t_{on,i}$ and the arm current during this interval. Conventional sorting-based balancing mainly compensates the resulting voltage deviation according to the measured capacitor voltage and the charging/discharging state of the arm current, rather than equalizing the insertion-pattern-dependent energy accumulation over a cyclic period. As illustrated in Figure 2, the black dashed lines represent the conduction intervals of the submodules. In the calculation of the DC component according to Equation (6), as the DC current remains constant, the difference in the DC components among submodule capacitor voltages is mainly caused by the different submodule insertion durations resulting from the rounding operation applied to the sinusoidal function in the NLM strategy. In Figure 2, submodules SM_1 and SM_8 , indicated by the red and blue dashed lines, respectively, have the same insertion duration due to symmetry. The integral of the AC current over the corresponding insertion interval represents the AC component of the submodule capacitor voltage. As observed, even when the insertion durations are the same, the phase angle difference α between the modulation wave and the AC current leads to different magnitudes and polarities of the currents flowing through the two submodules during their insertion intervals, ultimately resulting in different AC components of the submodule capacitor voltages.

This conventional voltage balancing strategy mainly sorts the capacitor voltages of all submodules. When the AC current becomes positive, corresponding to the charging state, the submodule with the lowest capacitor voltage is switched in when the number of inserted submodules increases, whereas the submodule with the highest capacitor voltage is bypassed when the number of inserted submodules decreases. When the AC current becomes negative, corresponding to the discharging state, the submodule with the highest capacitor voltage is switched in when the number of inserted submodules increases, whereas the submodule with the lowest capacitor voltage is bypassed when the number of inserted submodules decreases. In this way, capacitor voltage balancing is maintained. This conventional sorting method does not consider the number of switching operations, nor does it consider the balance between the AC and DC components. Instead, it stabilizes the capacitor voltages through frequent switching according to the final capacitor voltage magnitudes and the charging or discharging state. Although this method can achieve submodule capacitor voltage balancing to a certain extent, from the perspective of energy balance, it results in complex and disordered submodule switching frequencies and switching states. Meanwhile, the computational burden caused by capacitor voltage sorting and the switching frequency remain relatively high, thereby increasing the complexity of capacitor voltage control.

To realize submodule capacitor voltage balancing control, this study investigates a capacitor voltage balancing strategy based on accurately regulating the energy in each submodule.

First, according to Equations (4) and (5) and the analysis in Section 2, under steady-state conditions, total charge variation in each arm, namely all submodules in the arm, is constant within each period. As the positive and negative pole voltages on the DC side

remain constant, the sum of the capacitor voltages of all submodules in one arm should also remain constant.

However, capacitor voltage fluctuation still exists in steady-state operation. One major reason is that the differences in submodule insertion duration, as well as the magnitude and direction of the AC current within one period, lead to unbalanced energy distribution. Therefore, capacitor voltage balancing is attainable provided that the energy of each submodule in the arm is balanced.

For submodule energy balancing, two aspects can be considered: (1) balancing the energy of submodules within one period and (2) balancing the energy of submodules beyond one period. Many studies have focused on balancing submodule energy within one period, such as exchanging submodules in the inserted and bypassed states. The main idea is to change the insertion duration or insertion sequence of each submodule. This type of method has the advantages of a short control period and high control efficiency, but it requires high control accuracy and imposes strict requirements on hardware implementation. In contrast, the proposed submodule cyclic control method balances submodule energy over multiple fundamental periods. By cyclically shifting the control signals of submodules, the unequal charge variations caused by different insertion patterns within individual fundamental periods are redistributed among all submodules over one complete cyclic control period.

After NLM is implemented in the MMC, as illustrated in Figure 3, the conduction interval of each submodule is regarded as one insertion pattern, resulting in a total of N insertion patterns. In the conventional voltage balancing method, the insertion pattern of each submodule remains unchanged in each period. As a result, under this modulation scheme, the submodules with longer conduction intervals still maintain the longest conduction intervals in every period. Due to the cumulative effect, the capacitor voltage fluctuation gradually increases. Therefore, a submodule cyclic control strategy is proposed in this paper, whereby each submodule experiences all N insertion patterns under cyclic control, so that the capacitor energy of the submodules can be balanced. The time required to complete one cyclic control process is kNT , where k is an integer. To minimize the cyclic control period within the proposed control structure, $k = 1$ is selected. Therefore, the cyclic control period is equal to N times the modulation period. After one complete cyclic control period, the accumulated insertion-pattern-dependent energy is redistributed among the submodules, thereby contributing to capacitor voltage balancing.

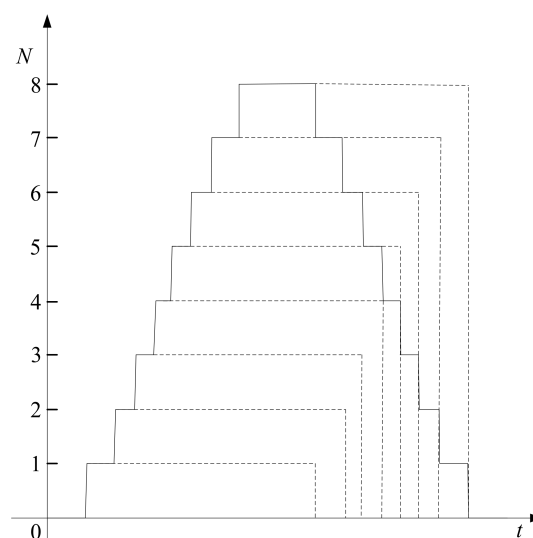


Figure 3. Submodule insertion patterns of the upper arm.

Taking the phase A upper arm of a nine-level converter as an illustrative case, after the modulation wave has been processed by NLM, the insertion patterns of the arm submodules are obtained, as shown in Figure 3. According to the principle of submodule cyclic control, one cyclic control process in this case contains eight modulation periods. In each modulation period, the control signals of the submodules are cyclically shifted, and the specific implementation process is shown in Figure 4, which presents the insertion sequence for the submodule control signals in the first two modulation periods and the last two modulation periods within one cyclic control period. The submodules indicated by arrows are in the inserted state, while those without arrows are in the bypassed state. It can be seen that the submodule cyclic control method enables each submodule SM_i to experience all N insertion patterns within one cyclic control period.

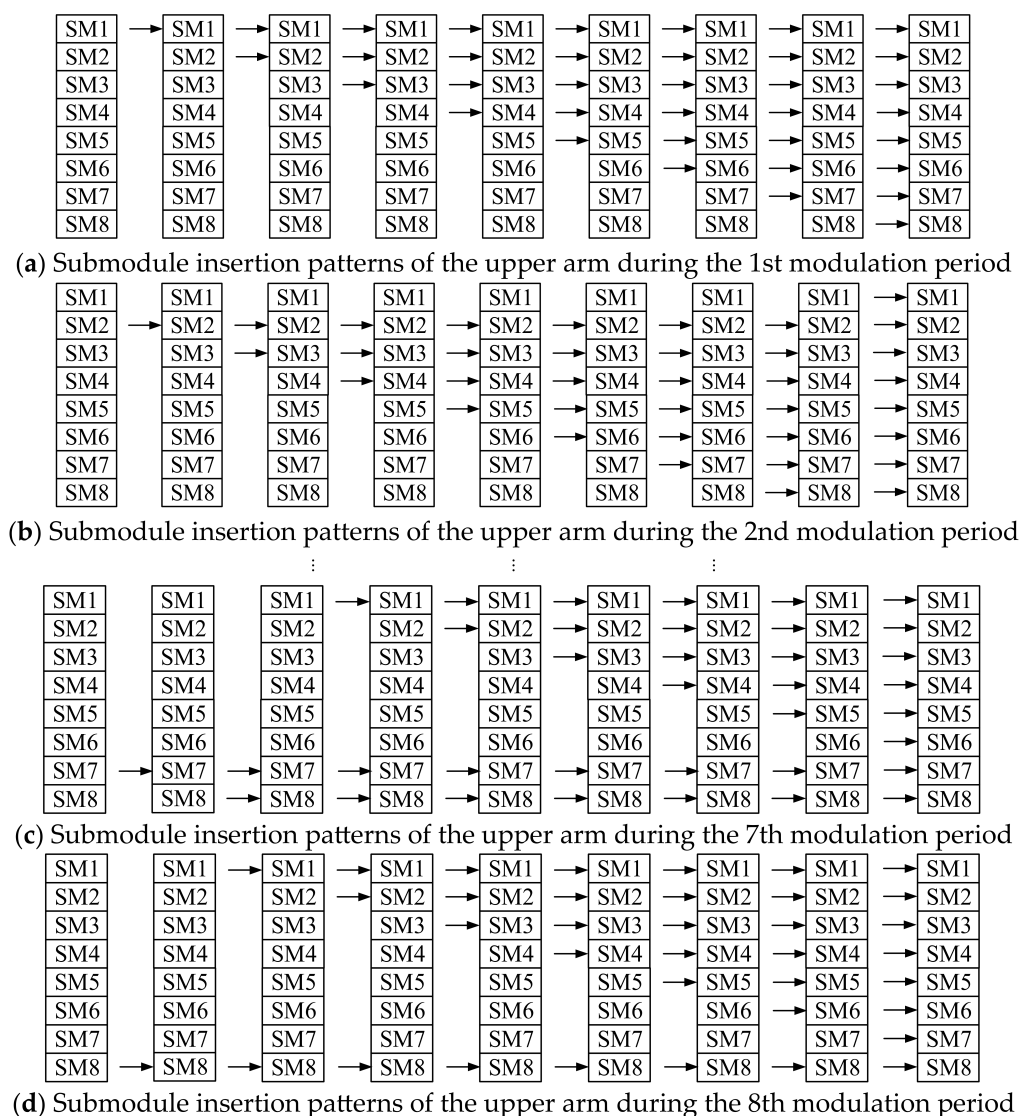


Figure 4. Schematic diagram of cyclic control.

To further clarify the energy equalization mechanism, the proposed cyclic control should not be understood as relying only on the conservation of the total arm charge. The total arm charge balance over one fundamental period only indicates that the overall arm energy is bounded under steady-state operation, but it does not directly guarantee a uniform energy distribution among individual submodules. The key mechanism of the proposed method lies in the cyclic permutation of the insertion patterns.

Let Δq_p denote the charge increment associated with the p -th insertion pattern within one fundamental period, where $p = 1, 2, \dots, N$. Under the cyclic control strategy, the insertion pattern assigned to each submodule is shifted by one position in each fundamental period. Therefore, after one complete cyclic control period, each submodule has experienced the same set of insertion patterns $\{1, 2, \dots, N\}$. The accumulated charge variation of the i -th submodule over one cyclic control period can be expressed as follows:

$$\Delta Q_i^{\text{cyc}} = \sum_{p=1}^N \Delta q_p, \quad i = 1, 2, \dots, N \quad (7)$$

As ΔQ_i^{cyc} is identical for all submodules, the accumulated energy difference caused by unequal NLM insertion intervals within a single fundamental period is compensated over the cyclic control period. Therefore, the voltage balancing effect is achieved by equalizing the accumulated insertion-pattern-dependent charge of each submodule, rather than by assuming that the conservation of the total arm charge automatically implies uniform submodule voltage distribution.

In addition, the absence of systematic periodic drift can be explained from the viewpoint of the capacitor voltage deviation at the boundaries of successive cyclic control periods. Let $e_i(k)$ denote the deviation of the i -th submodule capacitor voltage from the arm-average capacitor voltage at the beginning of the k -th cyclic control period. Under ideal periodic steady-state conditions, all submodules experience the same complete set of insertion patterns during one cyclic control period. Therefore, the accumulated pattern-dependent charge increment is identical for all submodules, and the cyclic permutation itself introduces no systematic drift term between two adjacent cyclic control periods.

When nonideal factors such as arm-current fluctuation, sampling delay, and parameter mismatch are considered, the residual voltage increment within the k -th cyclic control period can be represented by a perturbation term $\varepsilon_i(k)$. The cyclic control mechanism does not create a fixed insertion pattern bias for a particular submodule because the insertion patterns are periodically reassigned among all submodules. Therefore, any residual deviation is attributed to nonideal perturbations rather than to the systematic accumulation of unequal insertion patterns.

In addition, within one modulation period of NLM, there are multiple schemes for setting the submodule insertion patterns. For example, when the NLM-determined number of inserted upper-arm submodules is 1, submodules with indices greater than 1 may be inserted or bypassed; when the NLM-determined number of inserted upper-arm submodules is 2, submodules with indices greater than 2 may be inserted or bypassed, and so on. Compared with this scheme, the scheme adopted in this paper is shown in Figure 3. The submodule bypassing pattern indicated by the dashed lines in the figure reduces the difference in insertion duration among submodules, thereby decreasing the DC component in the submodule capacitor voltage. Therefore, the adopted bypassing pattern reduces the difference in insertion duration among submodules and consequently decreases the DC component of the capacitor voltage deviation.

4. Auxiliary Control Methods for Submodule Cyclic Control

Submodule cyclic control can achieve balanced distribution of submodule capacitor energy from the perspective of energy balance, thereby realizing capacitor voltage balancing control. However, some limitations still remain in the implementation of capacitor voltage balancing control. For example, when the number of submodules is large, the cyclic control period becomes excessively long. In addition, under transient disturbances, multiple cyclic control processes are still required to equalize the submodule capacitor voltages, resulting

in a slow system stabilization process. To address these problems, this study further develops a grouping-based auxiliary control strategy and an over-margin auxiliary control strategy based on submodule cyclic control. The grouping-based method shortens the cyclic control period, whereas the over-margin method provides event-triggered correction of out-of-margin capacitor voltage deviations.

4.1. Grouping-Based Auxiliary Control

Submodule cyclic control can solve the problem of energy imbalance among submodules in an arm and achieve capacitor voltage balancing control. However, under the NLM strategy, with the increase in the number of submodules N , the quantity of submodule insertion patterns N also increases. As the number of fundamental periods included in one submodule cyclic control period is proportional to N , the cyclic control period becomes longer. The cyclic control period is expressed in Equation (8).

$$T_{\text{cyc}} = kNT \quad (8)$$

where T_{cyc} denotes the cyclic control period; k represents the number of cycles, which is generally set to 1 to shorten the cyclic control period; N is the number of insertion patterns; and T is the period of AC current, generally corresponding to a frequency of 50 Hz.

As the number of insertion patterns N increases, the cyclic control period T_{cyc} required to complete one cyclic control process also increases accordingly. The extended cyclic control period affects the speed of capacitor voltage balancing control, and causes capacitor voltage fluctuations to accumulate within the cyclic control period due to the excessively long control duration, thereby enlarging the fluctuation range. Therefore, to improve the rapidity and control performance of submodule cyclic control, it is necessary to take measures to shorten the cyclic control period.

The period of submodule cyclic control is mainly related to the number of insertion patterns. To shorten the cyclic control period, this section starts from the submodule insertion patterns used in the control process and reduces the number of fundamental periods required for cyclic control by allowing a certain submodule voltage deviation.

Based on submodule cyclic control, an auxiliary submodule grouping method is designed to effectively shorten the cyclic control period. The main idea is as follows:

(1) For each candidate grouping number h , the steady-state capacitor voltage deviation is evaluated using Equations (9)–(13). The grouping number is then selected through the constrained discrete optimization formulated in Equation (14).

(2) During the modulation period, all h submodules are divided into one group. In the cyclic control process, the variation of submodule insertion patterns in each modulation period is cyclically shifted on a group basis.

As shown in Figure 5, taking $h = 2$ as an illustrative grouping case, every two submodules are divided into one group. During the 1st modulation period, the insertion starts from submodule 1. During the 2nd modulation period, submodule 2 is skipped, and the insertion starts from submodule 3. In this way, two adjacent submodules are grouped together. In submodule cyclic control, the cyclic control period can be reduced from NT to $NT/2$. Under the condition that the submodule capacitor voltage fluctuation remains within the allowable range, if all h submodules are grouped together, the cyclic control period can be shortened to $1/h$ of its original value, thereby accelerating this cyclic control process. In this study, the rated submodule capacitor voltage is 12.5 kV, and the basic allowable fluctuation range is set as 12–13 kV. Therefore, the allowable voltage deviation is $\Delta U_{\text{allow}} = 0.5$ kV, corresponding to $\pm 4\%$ of the rated capacitor voltage. This allowable range is used as the voltage deviation constraint for selecting the grouping number h . The grouping number h directly determines the trade-off between the cyclic control period and

the capacitor voltage balancing accuracy. When h increases, the cyclic control period is reduced from NT to $(N/h)T$. However, a larger h may enlarge the voltage deviation within each group because fewer insertion pattern exchanges are performed among individual submodules. Therefore, h is selected as the largest integer satisfying the allowable voltage deviation constraint, namely $\Delta U_{\max}(h) \leq \Delta U_{\text{allow}}$.

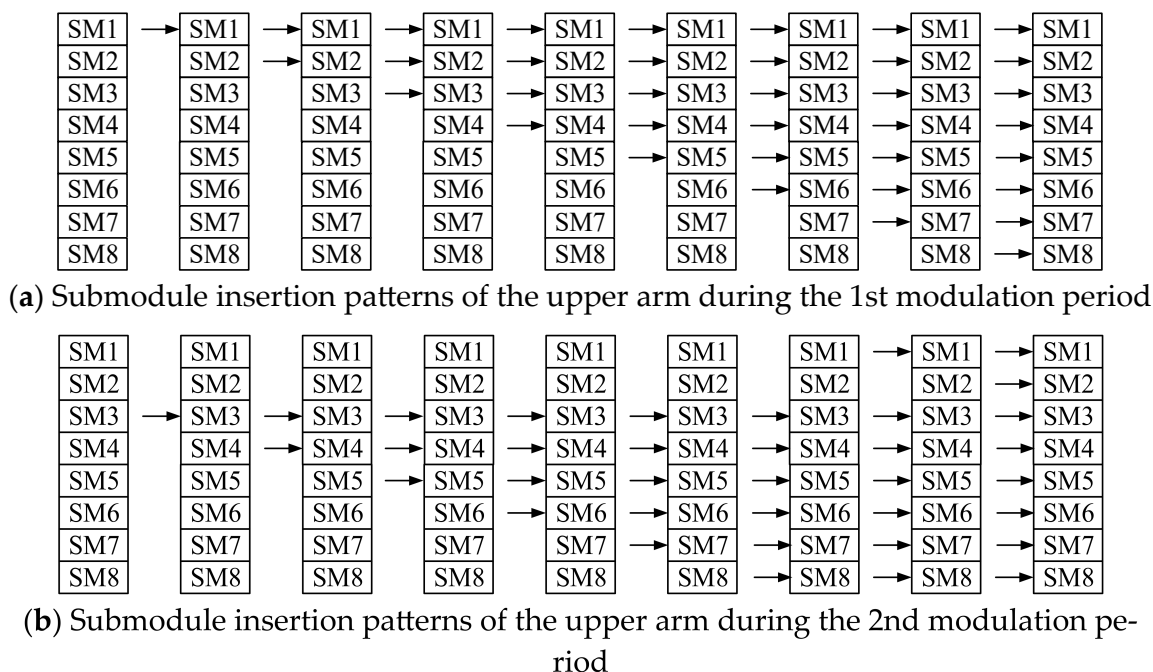


Figure 5. Schematic diagram of grouping-based cyclic control.

Submodule grouping can effectively shorten the cyclic control period. However, at the same time, voltage deviations will occur among the capacitor voltages of submodules in each group under this grouping-based submodule cyclic control. After the control process shown in Figure 5 is applied, the nine-level MMC forms two stable voltage fluctuation patterns: one with the insertion patterns cyclically shifted among SM1, SM3, SM5, and SM7, and the other with the insertion patterns cyclically shifted among SM2, SM4, SM6, and SM8. Therefore, after the grouping-based submodule cyclic control reaches steady state, the capacitor voltage fluctuation range is determined by the capacitor voltage fluctuation range within each group.

After the grouping-based submodule cyclic control reaches steady state, two stable voltage fluctuation patterns are formed. The corresponding reference voltage difference ΔU_{12} is expressed in Equation (9). As the magnitude of the reference voltage difference directly affects the capacitor voltage fluctuation range, selecting an appropriate grouping scheme has a direct influence on the performance of grouping-based cyclic control.

$$\Delta U_{12}(t) = U_{\text{SM},1}(t) - U_{\text{SM},2}(t) \quad (9)$$

Under one modulation period, the upper-arm modulation voltage u_p^* can be obtained from the modulation wave as follows:

$$u_p^*(t) = 4U_C + 4U_C \sin(\omega t) \quad (10)$$

where U_C denotes the reference submodule capacitor voltage, while ω denotes the angular frequency.

By combining the modulation waveform in Equation (10) with the NLM strategy, the submodule insertion duration can be obtained. Therefore, the submodule capacitor voltage within one modulation period can be expressed as follows:

$$U_{SM,1} = \frac{1}{C} \int_{[\arcsin(0.5/4-1)]/\omega}^{[2\pi-\arcsin(7.5/4-1)]/\omega} i_{pj}(t) dt \quad (11)$$

$$U_{SM,2} = \frac{1}{C} \int_{[\arcsin(1.5/4-1)]/\omega}^{[2\pi-\arcsin(6.5/4-1)]/\omega} i_{pj}(t) dt \quad (12)$$

By combining Equations (9), (11) and (12), the reference voltage difference between the two stable voltage waveforms can be obtained.

Based on the above analysis, when the number of levels is high, even after grouping, each group may still contain a large number of submodules. Therefore, an appropriate grouping scheme should be selected to ensure that the reference voltage difference remains within the allowable range. In this case, the deviation between any two submodule capacitor voltages within one group during one modulation period is defined as $\Delta U_i(h)$, and the maximum voltage deviation among all submodule pairs within one group is defined as $\Delta U_{\max}(h)$, as follows:

$$\Delta U_{\max}(h) = \|\Delta U(h)\|_{\infty} = \max_{1 \leq i \leq C_h^2} |\Delta U_i(h)| \quad (13)$$

where $\Delta U_i(h)$ denotes the capacitor voltage deviation of the i -th submodule pair when the grouping number is h and C_h^2 denotes the total number of submodule pairs within one group. Therefore, $\Delta U_{\max}(h)$ represents the maximum capacitor voltage deviation among all submodule pairs within the group.

In this study, the rated submodule capacitor voltage is 12.5 kV, and the basic allowable fluctuation interval is set as 12–13 kV. Accordingly, the allowable voltage deviation is $\Delta U_{\text{allow}} = 0.5$ kV, corresponding to plus or minus 4% of the rated capacitor voltage. This allowable deviation is used as the constraint for selecting the grouping number h .

For a given grouping number h , the cyclic control period is $T_{\text{cyc}}(h) = (N/h)T$. Increasing h shortens the cyclic control period but may increase $\Delta U_{\max}(h)$ because fewer insertion-pattern exchanges are performed among individual submodules. Therefore, the grouping number selection is formulated as a finite discrete optimization problem that minimizes the cyclic control period while satisfying the allowable capacitor voltage deviation constraint.

$$\begin{aligned} H &= \{h \in \mathbb{Z} | 1 \leq h \leq N, \text{mod}(N, h) = 0\} \\ T_{\text{cyc}}(h) &= \frac{N}{h}T \\ h_{\text{opt}} &= \text{argmin}_{h \in H} T_{\text{cyc}}(h) \\ \text{s.t. } \Delta U_{\max}(h) &\leq \Delta U_{\text{allow}} \end{aligned} \quad (14)$$

Equation (14) defines the candidate set, cyclic control period objective, and capacitor voltage deviation constraint for selecting h . The candidate set H contains the positive integer grouping numbers that permit equal grouping of the N submodules. For each candidate h in H , $\Delta U_{\max}(h)$ is calculated using Equation (13). Candidates that violate $\Delta U_{\max}(h) \leq \Delta U_{\text{allow}}$ are removed, and the feasible candidate yielding the minimum $T_{\text{cyc}}(h)$ is selected. As $T_{\text{cyc}}(h)$ decreases monotonically as h increases, this procedure is equivalent to selecting the largest feasible h . Therefore, the optimal grouping number is a constraint-based discrete solution rather than an empirical parameter.

4.2. Over-Margin Auxiliary Control

The grouping-based submodule cyclic control can achieve submodule capacitor voltage balancing. However, due to its inherent cyclic control period, the dynamic performance of the system is relatively limited. Therefore, to improve dynamic performance, an over-margin auxiliary control is introduced based on the grouping-based cyclic control, so that out-of-margin capacitor voltage deviations can be directly corrected during the post-fault recovery process.

Capacitor voltage fluctuation during operation is mainly caused by variations in the DC and AC components of the capacitor voltage. The fluctuation within each fundamental period is caused by the submodule conduction duration, as well as the amplitude and polarity of the AC current. As the amplitude and direction of the AC current are generally fixed, the submodule insertion duration and insertion sequence should be adjusted to suppress the submodule capacitor voltage fluctuation range.

When a system disturbance occurs, disturbance currents first appear in the converter station, causing significant fluctuations in the arm currents. Consequently, both the DC and AC components of the submodule capacitor voltages vary, leading to large capacitor voltage fluctuations. However, relying only on the grouping-based submodule cyclic control to achieve capacitor voltage balancing under disturbances requires a relatively long time. Therefore, to enhance the dynamic performance of the system, the arm current and submodule capacitor voltage are incorporated into the design of the over-margin auxiliary control.

The main idea of the over-margin auxiliary control is as follows:

- (1) A capacitor voltage fluctuation margin interval is set for the submodule capacitor voltages under grouping-based cyclic control.
- (2) According to the fluctuation state of the submodule capacitor voltages within one modulation period, two different submodules in the same group are selected as standby submodules for each other.
- (3) When an over-margin condition occurs in the submodule capacitor voltage, corrective signal exchange is performed between the standby submodules.

Considering the arm current charging and discharging states, if a certain capacitor voltage goes beyond the threshold and the control signals of the two submodules are different, their control signals are exchanged. In the grouping-based auxiliary control, this method of regulating the submodule capacitor voltage by switching the control signals between two submodules is defined as standby regulation, and the relationship between the two submodules is defined as a standby relationship.

When selecting standby submodules, taking a nine-level NLM scheme as an example, SM1 and SM8 have the same conduction duration within one modulation period, and the duration during which their control signals are identical is the shortest, providing the largest adjustable margin. Therefore, SM1 and SM8 are defined as standby submodules for each other, and the other submodules are defined in the same manner.

Assuming that the reference capacitor voltage is 12.5 kV and the fluctuation interval is 12–13 kV, the switching logic of the standby submodules is described as follows by taking the capacitor voltages of SM1 and SM8 as an example:

(1) Charging state:

If $U_{SM,1} < 12 \text{ kV}$, $U_{SM,8} > 12 \text{ kV}$, and the control signals of the two submodules are different, $U_{SM,1}$ is assigned the control signal that turns on earlier.

If $U_{SM,1} > 12 \text{ kV}$, $U_{SM,8} < 12 \text{ kV}$, and the control signals of the two submodules are different, $U_{SM,8}$ is assigned the control signal that turns on earlier.

If $U_{SM,1} < 12$ kV and $U_{SM,8} < 12$ kV, the capacitor voltages of both submodules are compared, and the submodule with the lower capacitor voltage is assigned the control signal that turns on earlier.

If $U_{SM,1} > 12$ kV and $U_{SM,8} > 12$ kV, the capacitor voltages of both submodules are higher than the lower limit; therefore, no action is required.

(2) Discharging state:

If $U_{SM,1} > 13$ kV, $U_{SM,8} < 13$ kV, and the control signals of the two submodules are different, $U_{SM,1}$ is assigned the control signal that turns on earlier.

If $U_{SM,1} < 13$ kV, $U_{SM,8} > 13$ kV, and the control signals of the two submodules are different, $U_{SM,8}$ is assigned the control signal that turns on earlier.

If $U_{SM,1} > 13$ kV and $U_{SM,8} > 13$ kV, the capacitor voltages of both submodules are compared, and the submodule with the lower capacitor voltage is assigned the control signal that turns on earlier.

If $U_{SM,1} < 13$ kV and $U_{SM,8} < 13$ kV, the capacitor voltages of both submodules are lower than the upper limit; therefore, no action is required.

The flowchart for the over-margin auxiliary control is shown in Figure 6. Under steady-state conditions, the over-margin auxiliary control only performs checking and does not affect the cyclic control of the submodules. Under nonideal operating conditions, bounded perturbations over successive cyclic control periods may cause the capacitor voltage deviation to approach or exceed the preset margin. To prevent such residual deviations from developing into continuous voltage drift, the proposed over-margin auxiliary control activates the standby-submodule signal exchange once a submodule capacitor voltage exceeds the preset margin interval. This corrective action suppresses the excessive deviation and constrains the capacitor voltage within the designed operating margin. According to the analysis in Section 4.1, after grouping, SM1, SM3, SM5, and SM7 exhibit the same fluctuation pattern, while SM2, SM4, SM6, and SM8 exhibit another common fluctuation pattern. Submodules with a standby relationship, such as SM1 and SM8, are paired to provide the signal-exchange paths required for correcting excessive capacitor voltage deviations.

The proposed cyclic, grouping-based, and over-margin controls modify only the assignment of the submodule insertion signals. Let $s_i^{\text{pre}}(t)$ and $s_i^{\text{post}}(t)$ denote the insertion states of the i -th submodule before and after the cyclic permutation or standby submodule signal exchange, respectively, where $s_i^{\text{pre}}(t), s_i^{\text{post}}(t) \in \{0, 1\}$. The total number of inserted submodules remains unchanged during the signal reassignment, i.e.,

$$\sum_{i=1}^N s_i^{\text{post}}(t) = \sum_{i=1}^N s_i^{\text{pre}}(t) = n_{\text{arm}}(t) \quad (15)$$

where $n_{\text{arm}}(t)$ is the number of inserted submodules determined by NLM at time t .

Consequently, the proposed balancing logic does not alter the NLM-determined number of inserted submodules or the converter arm-current reference. At the modulation sequence level, the nominal arm voltage level sequence is therefore preserved. As all submodules in one arm are connected in series, the conducting devices in the submodules carry the same arm current. Thus, the control signal permutation itself does not introduce an additional intentional current spike mechanism. The transient arm-current excursion remains mainly governed by the external fault, the arm inductance, and the converter current control loop. Device-level current overshoots associated with dead time, gate delay, parasitic parameters, and nonideal switching are not represented in the present system-level model.

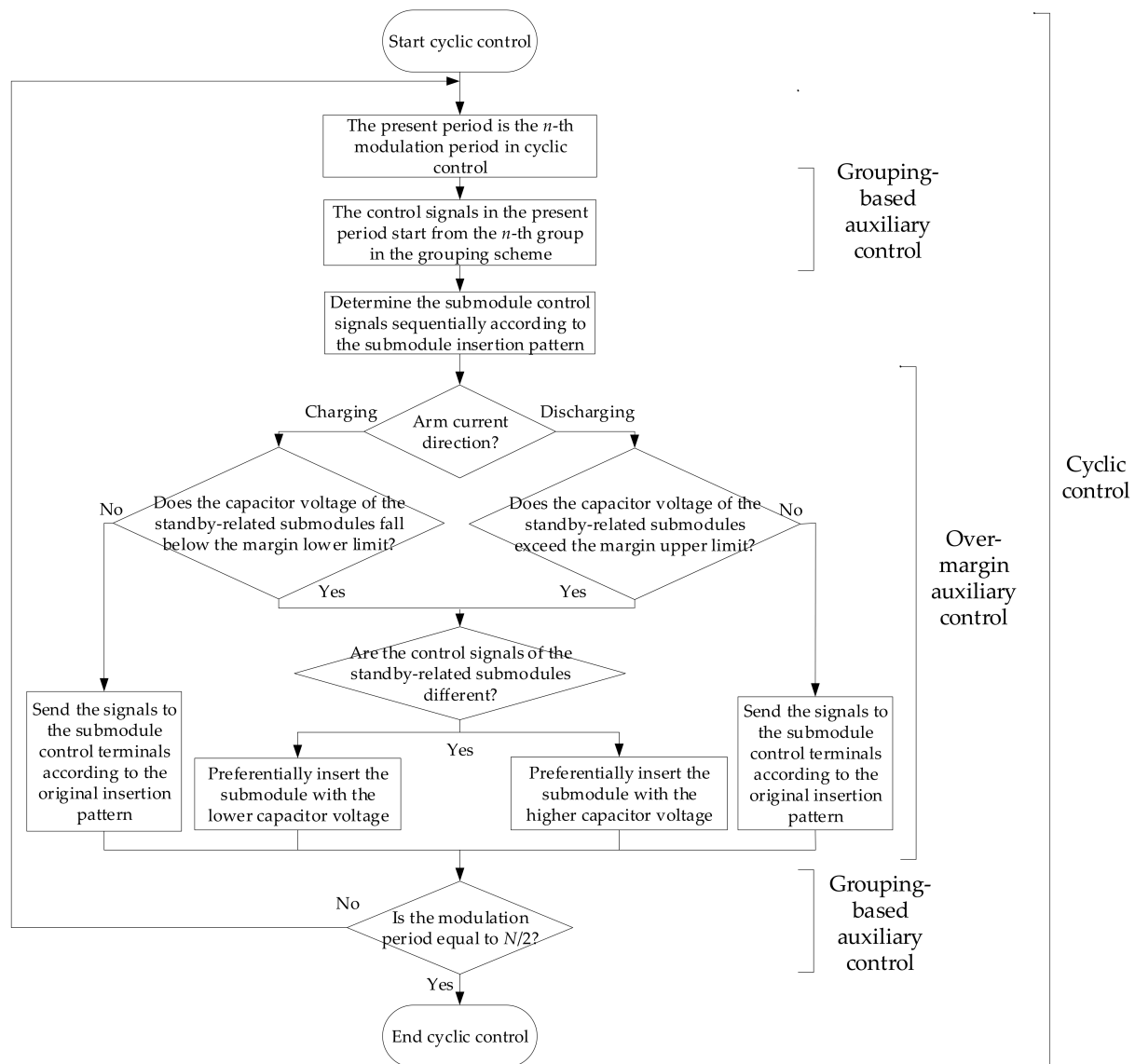


Figure 6. Flowchart of the grouping-based over-margin auxiliary control based on cyclic control.

5. Simulation Verification and Analysis

To validate the effectiveness of the proposed submodule cyclic control method for capacitor voltage balancing and its auxiliary control, a three-phase nine-level MMC simulation model is built in PSCAD/EMTDC. The system parameters are as follows: the line-to-line AC voltage of the AC system is $U_{L-L} = 10$ kV, the active power is $P = 80$ MW, while the DC-side voltage is $U_{dc} = \pm 50$ kV. The number of submodules per arm of the converter station is $N = 8$, the submodule capacitance is $C = 1$ mF, the capacitor voltage is $U_C = 12.5$ kV, and the arm inductance is $L_{arm} = 10$ mH. Simulations are carried out under both steady-state and transient operating conditions, and the corresponding simulation responses are analyzed to validate the proposed grouping-based over-margin auxiliary control method based on submodule cyclic control.

5.1. Steady-State Simulation and Analysis

The capacitor voltage waveforms of phase A upper arm on the inverter side are taken as the research object. Figures 7–9 show the simulated submodule capacitor voltage waveforms under steady-state conditions when the submodule cyclic control method, the

grouping-based auxiliary control method, and the grouping-based over-margin auxiliary control method are adopted, respectively.

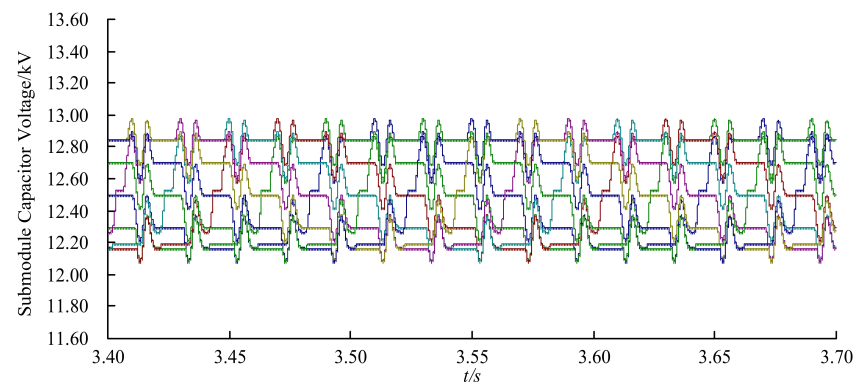


Figure 7. Capacitor voltage waveforms in steady-state operation with submodule cyclic control.

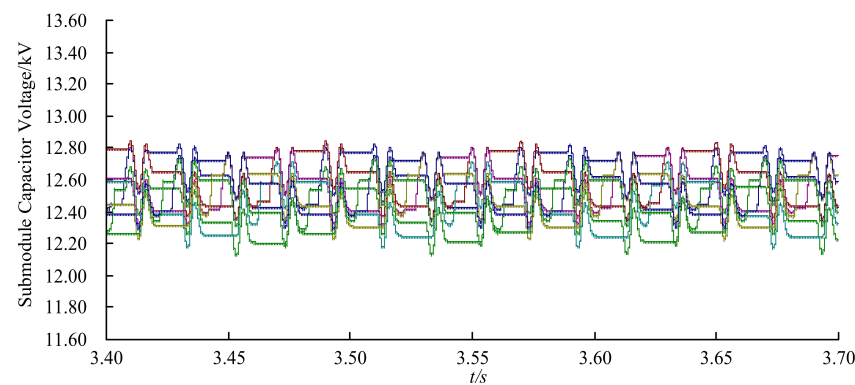


Figure 8. Capacitor voltage waveforms in steady-state operation with grouping-based auxiliary control.

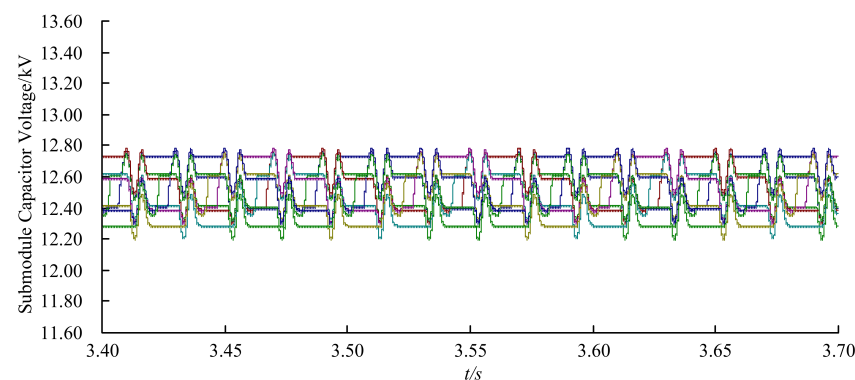


Figure 9. Capacitor voltage waveforms in steady-state operation with grouping-based and over-margin auxiliary control.

It can be seen from Figure 7 that, after adopting the submodule cyclic control-based capacitor voltage balancing strategy, the fluctuation amplitude of each submodule capacitor voltage can be stabilized within $\pm 4\%$. Moreover, the fluctuation amplitude and fluctuation period of each submodule capacitor voltage are consistent. This indicates that the submodule cyclic control method can achieve balanced energy distribution among submodules and has a good control effect on capacitor voltage balancing.

Figure 8 shows the simulation results of capacitor voltage cyclic control after adopting the grouping-based auxiliary strategy. This control primarily aims to shorten this cyclic

control period. By comparing the cyclic control periods in Figures 7 and 8, it can be seen that the cyclic control period in Figure 7 is 0.16 s, whereas that in Figure 8 is only 0.08 s, which is reduced by half. In addition, by comparing the capacitor voltage stabilization results in Figures 7 and 8, it can be concluded that the grouping-based auxiliary control based on the submodule cyclic control method can regulate the submodule capacitor voltage by shortening the cyclic control period. As shown in Figure 8, the submodule capacitor voltage fluctuation is maintained within $\pm 2.4\%$, which is lower than that in Figure 7.

Figure 9 presents the simulation results obtained using the grouping-based over-margin auxiliary control based on submodule cyclic control. The primary objective of the over-margin auxiliary control is to improve system dynamic performance. Here, its performance in steady-state operation is verified. When the submodule capacitor voltage exceeds the preset margin interval, the over-margin auxiliary control adjusts the submodule insertion patterns. In this simulation, the preset margin interval is [12.2, 12.8]. As shown in Figure 9, the cyclic control period is 0.08 s, and the submodule capacitor voltages are stabilized between 12.2 kV and 12.8 kV. This indicates that, under steady-state conditions, the over-margin control can still achieve effective capacitor voltage balancing by adjusting the capacitor voltage margin interval.

According to the steady-state simulations and analysis, the submodule cyclic control-based capacitor voltage balancing method can realize capacitor voltage balancing under steady-state conditions. On this basis, the proposed grouping-based auxiliary control can shorten the cyclic control period, while the over-margin auxiliary control enhances the stability of this proposed cyclic control strategy in steady-state operation.

5.2. Transient Simulation and Analysis

The phase A upper arm on the inverter side is selected as the study object. Figures 10–12 present the submodule capacitor voltage responses under the basic cyclic control, grouping-based cyclic control, and grouping-based over-margin control, respectively. The displayed time interval contains the complete transient process, including the pre-fault operating condition, fault inception at $t = 5.00$ s, fault clearing at $t_{\text{clr}} = 5.02$ s, the initial fault-induced capacitor voltage excursion, and the subsequent post-fault convergence. The transient responses are quantitatively evaluated using the common first-entry recovery criterion defined below.

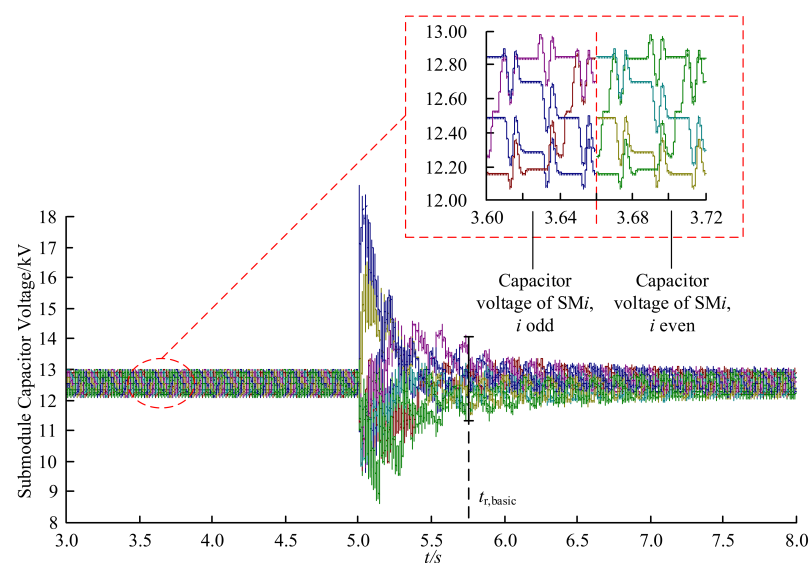


Figure 10. Complete submodule capacitor voltage transient response and post-fault convergence under basic cyclic control.

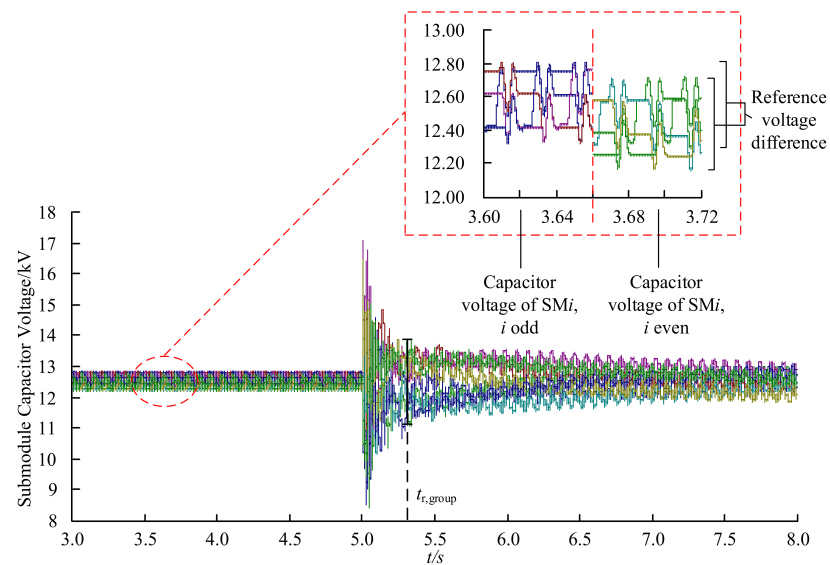


Figure 11. Complete submodule capacitor voltage transient response and post-fault convergence under grouping-based cyclic control.

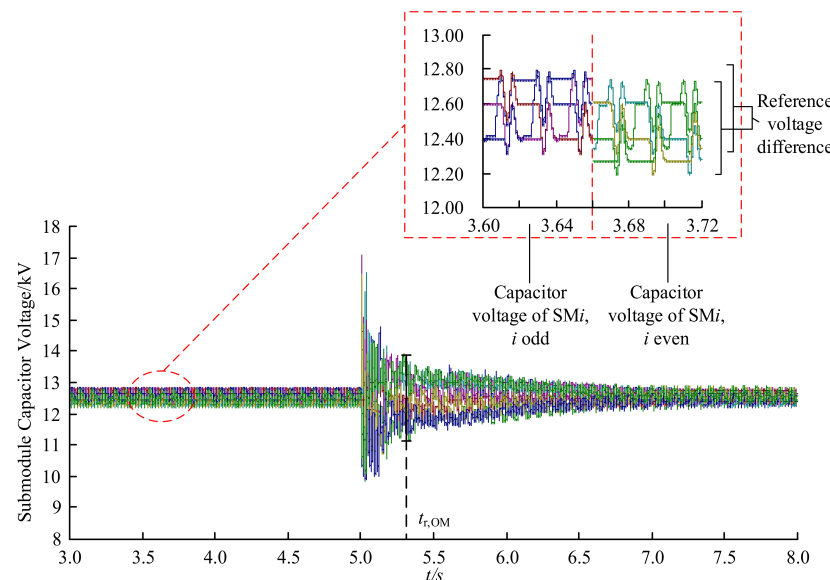


Figure 12. Complete submodule capacitor voltage transient response and post-fault convergence under grouping-based over-margin control.

To quantitatively compare the transient recovery performance of the three capacitor voltage balancing methods under a unified criterion, a common transient recovery band of [11 kV, 14 kV] is adopted. With the rated submodule capacitor voltage $U_C = 12.5$ kV, this band corresponds to a normalized voltage deviation of $\pm 12\%$. It should be emphasized that this interval is used to evaluate the speed at which the capacitor voltages first return from the fault-induced large deviation to a bounded transient range. It is different from the steady-state voltage-fluctuation margins of the three control methods. For method m , the instantaneous maximum normalized capacitor voltage deviation is defined as follows:

$$D_m(t) = \frac{\max_i |U_{SM,i}^m(t) - U_C|}{U_C} \times 100\% \quad (16)$$

where $U_{SM,i}^m(t)$ is the capacitor voltage of the i -th submodule under method m , and $U_C = 12.5$ kV is the rated submodule capacitor voltage.

The maximum deviation is defined as follows:

$$D_{\max,m} = \max_{t \in [t_f, t_{r,m}]} D_m(t) \quad (17)$$

where t_f is the fault-inception instant and $t_{r,m}$ is the first-entry recovery instant of method m , and $D_{\max,m}$ denotes the maximum normalized capacitor voltage deviation over the interval $[t_f, t_{r,m}]$. Therefore, $D_{\max,m}$ represents the maximum fault-induced voltage deviation before all submodule capacitor voltages first re-enter the common [11 kV, 14 kV] transient recovery band.

A common transient recovery criterion is adopted for all three methods. The capacitor voltages are considered to have entered the transient recovery band when all submodule capacitor voltages satisfy $U_{SM,i}^m(t) \in [11 \text{ kV}, 14 \text{ kV}]$, $i = 1, 2, \dots, N$. As the rated capacitor voltage is 12.5 kV, the above criterion is equivalently expressed as $D_m(t) \leq 12\%$.

The common $\pm 12\%$ criterion is used solely to determine the transient first-entry recovery time. After first re-entering the common transient recovery band, the capacitor voltages continue to converge toward their corresponding pre-fault periodic steady-state envelopes. These envelopes are approximately $\pm 4\%$ for the basic cyclic control and $\pm 2.4\%$ for the grouping-based and grouping-based over-margin controls. The $\pm 4\%$ and $\pm 2.4\%$ values describe the recovered steady-state voltage conditions and are not used to define an additional recovery-time metric.

After the fault is cleared at $t_{\text{clr}} = 5.02 \text{ s}$, the first-entry recovery instant $t_{r,m}$ is defined as the first time instant at which all submodule capacitor voltages under method m re-enter the common transient recovery band of [11 kV, 14 kV]. Accordingly, the first-entry recovery time is defined as follows:

$$T_{\text{rec},m} = t_{r,m} - t_{\text{clr}} \quad (18)$$

Based on this definition, the transient recovery performance of the basic cyclic control, the grouping-based cyclic control, and the grouping-based over-margin cyclic control can be quantitatively compared. This index characterizes the initial recovery speed from the large fault-induced capacitor voltage deviation to the common [11 kV, 14 kV] band. It does not represent the subsequent complete restoration to the method-specific pre-fault periodic steady-state voltage envelope.

The cyclic control period should be distinguished from the first-entry transient recovery time. For the 50 Hz system considered in this study, $T = 0.02 \text{ s}$. Therefore, the minimum period required to complete one full insertion-pattern permutation is $NT = 0.16 \text{ s}$ for the basic cyclic control and $(N/h)T = 0.08 \text{ s}$ for the grouping-based control with $h = 2$. These values represent the minimum pattern-completion intervals imposed by the control structure and should be distinguished from the first-entry recovery time $T_{\text{rec},m}$. The cyclic control period describes the time required to complete one insertion-pattern permutation, whereas $T_{\text{rec},m}$ measures the time required for all submodule capacitor voltages to first re-enter the common [11 kV, 14 kV] transient recovery band. The subsequent return to the pre-fault periodic steady-state voltage envelope is described qualitatively from the voltage waveforms and is not assigned an additional time metric in this study. As summarized in Table 1, the measured first-entry recovery times are 0.73 s, 0.33 s, and 0.33 s for the basic cyclic, grouping-based, and grouping-based over-margin controls, respectively.

Thus, under the common [11 kV, 14 kV] first-entry criterion, the grouping-based method reduces the first-entry recovery time by 54.8% relative to the basic cyclic control under the present simulation conditions. The obtained response time is not claimed to be a global mathematical optimum for all MMC parameters and operating conditions. Rather, it is the measured response achieved by the designed control structure under the specified fault condition and voltage-deviation criterion.

Table 1. Quantitative comparison of the transient first-entry recovery performance and recovered steady-state voltage conditions.

Method	Cyclic Control Period/s	Recovered Steady-State Voltage Envelope	Maximum Transient Deviation	First-Entry Recovery Time/s	Control Operation and Complexity
Basic cyclic control	0.16	[12.0, 13.0] kV (approximately $\pm 4\%$)	56%	0.73	No real-time voltage sorting; $O(1)$ cyclic-index update and $O(N)$ signal mapping
Grouping-based cyclic control	0.08	[12.2, 12.8] kV (approximately $\pm 2.4\%$)	37.6%	0.33	No real-time voltage sorting; $O(1)$ group-index update and $O(N)$ signal mapping
Grouping-based over-margin control	0.08	[12.2, 12.8] kV (approximately $\pm 2.4\%$)	37.6%	0.33	No sorting; $O(N)$ threshold and standby-pair checking, followed by $O(1)$ exchange for each activated pair

Note: The common first-entry recovery criterion for all three methods is [11 kV, 14 kV], corresponding to $\pm 12\%$ of the rated capacitor voltage. $O(1)$ denotes an index-update or signal-exchange operation whose computational cost is independent of the number of submodules, whereas $O(N)$ denotes a signal-mapping or threshold-checking operation whose computational cost increases linearly with N .

As shown in Figure 10, after fault clearing, all submodule capacitor voltages first re-enter the common [11 kV, 14 kV] transient recovery band at $t_{r,basic}$. Subsequently, the capacitor voltages continue to converge and eventually recover to the pre-fault periodic steady-state voltage envelope of approximately $\pm 4\%$.

According to the comparison of capacitor voltage stabilization responses in Figures 10 and 11, it can be concluded that the grouping-based auxiliary control based on the submodule cyclic control method can regulate the submodule capacitor voltage by shortening the cyclic control period. As illustrated in Figure 11, each submodule capacitor voltage fluctuation is maintained within $\pm 2.4\%$, which is lower than that in Figure 10. The grouping-based auxiliary control improves the initial transient recovery speed of the capacitor voltages. Under the common [11 kV, 14 kV] first-entry criterion, the first-entry recovery time of the grouping-based cyclic control is 0.33 s, which is 0.40 s shorter than the 0.73 s obtained with the basic cyclic control. After first re-entering the common transient recovery band, the capacitor voltages continue to converge and eventually recover to the pre-fault periodic steady-state envelope of approximately $\pm 2.4\%$.

To improve the dynamic performance of the grouping-based auxiliary control, an over-margin auxiliary control is proposed. When the submodule capacitor voltage exceeds the preset margin interval, the submodule insertion pattern is adjusted. In this simulation, the preset margin interval is [12.2, 12.8] kV. As shown in Figure 12, before the disturbance occurs, the submodule capacitor voltages remain within the margin interval, and the over-margin control does not participate in the control process. The submodule capacitor voltage fluctuation is maintained within $\pm 2.4\%$. After the transient disturbance, the capacitor voltage response initially exhibits a trend similar to that obtained with the grouping-based cyclic control. Under the common [11 kV, 14 kV] first-entry criterion, both methods have the same first-entry recovery time of 0.33 s. Therefore, the over-margin auxiliary control does not further reduce $T_{rec,m}$ in this case. Its effect is mainly reflected in the subsequent voltage-balancing process: standby-submodule signal exchange directly corrects out-of-margin voltage deviations, reduces the post-fault capacitor voltage spread, and facilitates the recovery of the capacitor voltages to the pre-fault periodic steady-state envelope of [12.2 kV, 12.8 kV].

The quantitative comparison based on the unified transient recovery criterion is summarized in Table 1. The first-entry recovery times of the basic cyclic control, grouping-based cyclic control, and grouping-based over-margin control are 0.73 s, 0.33 s, and 0.33 s, respectively. Compared with the basic cyclic control, the grouping-based method reduces the

first-entry recovery time by approximately 54.8%. This improvement is mainly attributed to the reduction of the cyclic control period from 0.16 s to 0.08 s, which accelerates the redistribution of submodule energy.

Under the common [11 kV, 14 kV] first-entry criterion, the grouping-based cyclic control and the grouping-based over-margin control exhibit the same first-entry recovery time of 0.33 s. Therefore, the present simulation does not demonstrate a further reduction in the first-entry recovery time after introducing the over-margin control. The main contribution of the over-margin auxiliary control is to provide direct corrective signal exchange when a submodule capacitor voltage exceeds the preset control margin, thereby improving the subsequent voltage-balancing process and facilitating the subsequent recovery of the capacitor voltages to the pre-fault periodic steady-state envelope of [12.2 kV, 12.8 kV].

From the perspective of computation, none of the three methods requires real-time capacitor voltage sorting. The basic cyclic and grouping-based controls update the insertion-pattern index and assign the corresponding signals to the submodules. The over-margin method additionally checks the capacitor voltage thresholds and performs paired signal exchange when necessary. As the number of operations increases approximately linearly with the number of submodules, the overall computational complexity of all three methods is $O(N)$. By comparison, sorting-based capacitor voltage balancing generally requires an $O(N \log N)$ voltage-sorting stage at each control update.

5.3. Comparative Analysis and Discussion of Harmonic and Loss Characteristics

As analyzed in Section 2, the submodule capacitor voltage mainly consists of three components: the initial capacitor voltage component, the DC component, and the AC component, as shown by Equation (6). Among these, the submodule insertion duration, as well as the amplitude and polarity of the AC current, are the main factors affecting the submodule capacitor voltage during steady-state operation. The improved NLM strategy proposed in [21] mainly adjusts the insertion duration of each submodule from the perspective of the modulation strategy. In contrast, the submodule cyclic control and grouping-based over-margin auxiliary control proposed in this paper not only regulate the submodule insertion duration, but also optimize the submodule insertion sequence, thereby introducing an additional degree of freedom in the insertion sequence assignment. Figures 13 and 14 further compare the switching-frequency characteristics of an individual submodule under the improved NLM strategy and the proposed cyclic control methods.

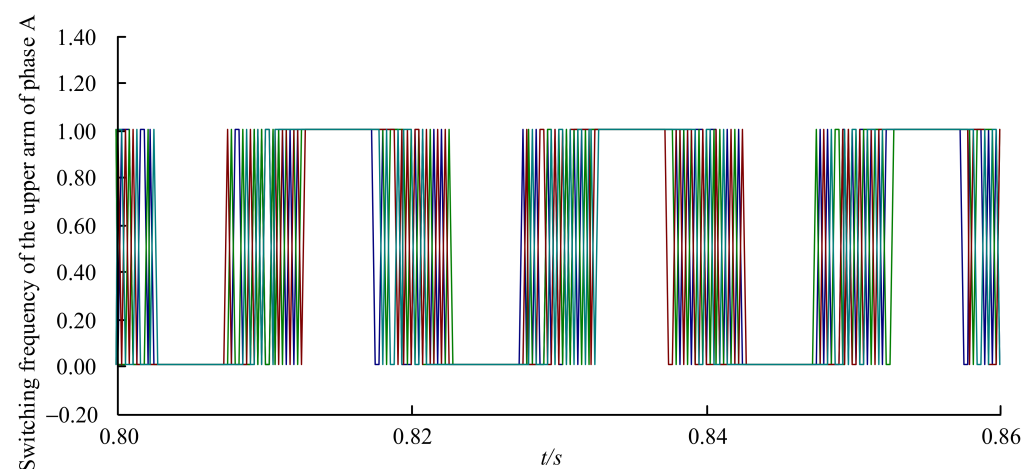


Figure 13. Switching-frequency characteristics of an individual submodule under the improved NLM strategy in steady-state operation.

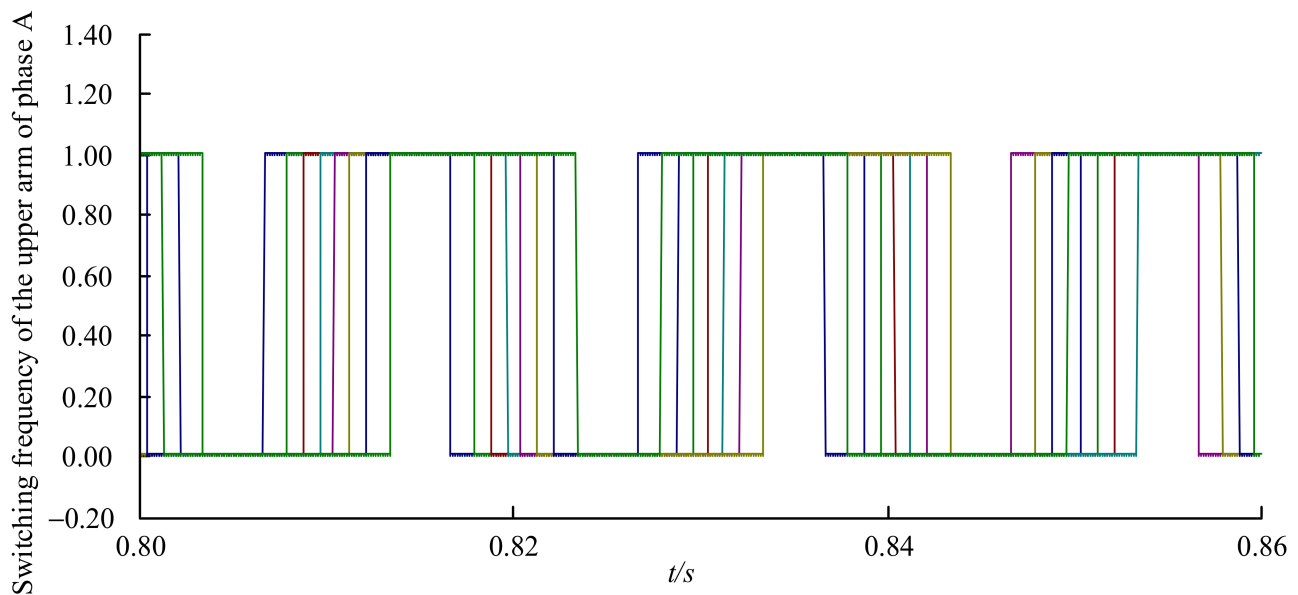


Figure 14. Switching-frequency characteristics of an individual submodule under the proposed cyclic control methods in steady-state operation.

The influence of the proposed balancing methods on the nominal output voltage harmonic characteristics can be further explained using the insertion-number invariance established by Equation (15) in Section 4.2. As the proposed signal reassignment preserves the NLM-determined inserted-submodule number $n_{\text{arm}}(t)$, the nominal voltage-level sequence remains unchanged. If the capacitor voltage of the i -th submodule is expressed as $U_{\text{SM},i}(t) = U_C + \delta U_i(t)$, the actual arm voltage after the signal reassignment can be written as follows:

$$u_{\text{arm}}(t) = \sum_{i=1}^N s_i^{\text{post}}(t) U_{\text{SM},i}(t) = n_{\text{arm}}(t) U_C + \sum_{i=1}^N s_i^{\text{post}}(t) \delta U_i(t) \quad (19)$$

The first term represents the nominal NLM staircase voltage. Because the signal reassignment preserves $n_{\text{arm}}(t)$, the proposed cyclic, grouping-based, and over-margin controls do not change the nominal voltage-level sequence generated by NLM. The second term represents the voltage perturbation caused by nonuniform submodule capacitor voltages. Therefore, under the ideal equal-capacitor voltage condition, the proposed controls do not introduce an additional harmonic mechanism at the modulation sequence level. Under practical unequal-voltage conditions, the perturbation term may still affect the output voltage THD. Accordingly, the proposed controls preserve the nominal harmonic generation mechanism of NLM, while the practical output voltage THD remains dependent on the capacitor voltage perturbation term.

The power-loss characteristics of the proposed control can be analyzed by decomposing the total semiconductor loss P_{loss} into conduction loss P_{cond} and switching loss P_{sw} :

$$P_{\text{loss}} = P_{\text{cond}} + P_{\text{sw}} \quad (20)$$

The conduction loss over an observation interval T_{obs} can be expressed in a general form as follows:

$$P_{\text{cond}} = \frac{1}{T_{\text{obs}}} \sum_{i=1}^N \int_{T_{\text{obs}}} v_{\text{on},i}(t) |i_{\text{arm}}| dt \quad (21)$$

whereas the switching loss can be expressed as follows:

$$P_{sw} = \frac{1}{T_{obs}} \sum_{i=1}^N \sum_{k=1}^{N_{sw,i}} E_{sw,i,k} \quad (22)$$

where $v_{on,i}(t)$ is the on-state voltage of the conducting semiconductor device in the i -th submodule, $i_{arm}(t)$ is the arm current, $N_{sw,i}$ is the number of switching-state transitions of the i -th submodule during T_{obs} , and $E_{sw,i,k}$ is the energy associated with its k -th switching event.

The proposed cyclic, grouping-based, and over-margin controls reassign the submodule insertion signals while preserving the NLM-determined number of inserted submodules and the converter arm-current reference. Therefore, they do not introduce an additional current-conduction branch, and the arm-level conduction-loss tendency remains comparable under the same operating condition. The principal loss difference is associated with the number and distribution of switching-state transitions.

Accordingly, the regular 50 Hz switching characteristic shown in Figure 14 indicates a lower switching-loss tendency for the proposed control under steady-state operation, whereas the nonuniform switching actions in Figure 13 lead to a more variable switching-loss distribution under the improved NLM strategy.

The capacitor voltage fluctuation range of the improved NLM strategy in [21] is $\pm 1.2\%$, whereas that of the proposed submodule cyclic control with grouping-based over-margin auxiliary control is $\pm 2.4\%$. From the perspective of capacitor voltage ripple suppression alone, the sorting-based NLM strategy provides a smaller fluctuation range. However, Figures 13 and 14 show that this smaller voltage fluctuation is accompanied by more frequent and irregular switching actions. In contrast, the proposed submodule cyclic control maintains a 50 Hz per-submodule switching frequency under steady-state operation, avoids real-time capacitor voltage sorting, and reduces the online computational operations associated with voltage balancing.

As shown in Figure 14, the switching frequency of an individual submodule under the three proposed control methods is 50 Hz in steady-state operation. The grouping-based method shortens the cyclic control period from 0.16 s to 0.08 s by changing the insertion pattern reassignment sequence, without increasing the switching frequency of an individual submodule. In addition, the over-margin auxiliary control remains inactive when all capacitor voltages are within the preset margin and therefore does not introduce additional steady-state switching actions. In contrast, the switching instants under the improved NLM strategy in Figure 13 are nonuniform and cannot be represented by a single fixed switching frequency.

To further clarify the characteristics and application boundaries of different capacitor voltage regulation approaches, Table 2 compares the proposed method with flexible NLM [17], APF-MMC [22], and the HRT-SOP with mixed-frequency modulation [23]. These methods operate at different control or topology levels. Therefore, the comparison focuses on their control mechanisms, hardware requirements, voltage balancing characteristics, harmonic and loss implications, and implementation features, rather than directly ranking numerical results obtained under different converter structures and operating conditions.

Table 2 shows that flexible NLM [17] and the proposed method both operate within the conventional MMC and NLM framework without adding a new power-conversion branch, although they adopt different switching-sequence adjustment mechanisms. In contrast, APF-MMC [22] and HRT-SOP [23] rely on additional or dedicated power-conversion structures. Therefore, these methods cannot be ranked using a single performance index. The proposed method is characterized by periodic insertion pattern reassignment without real-time capacitor voltage sorting or additional power hardware.

Table 2. Structural comparison of the proposed control with flexible NLM, APF-MMC, and HRT-SOP with mixed-frequency modulation.

Method	Framework	Extra Hardware	Voltage Balancing	Harmonic Effect	Loss and Implementation
Flexible NLM [17]	Conventional MMC with NLM	None	Trades voltage ripple against switching frequency	Retains the NLM framework; harmonics depend on switching actions	Reduces unnecessary switching; no additional hardware
APF-MMC [22]	Modified MMC topology	APF branch and capacitor	Directly suppresses SM capacitor voltage ripple	Depends on the APF branch and its control	Targets ripple and loss reduction; requires an APF branch
HRT-SOP with mixed-frequency modulation [23]	HRT-based soft open point	Dedicated SOP and transformer	Balances internal DC voltages	Mixed-frequency modulation changes internal spectra	Loss depends on the dedicated topology and mixed-frequency modulation
Proposed method	Conventional MMC with NLM	None	Approximately $\pm 4\%$ for basic cyclic control and $\pm 2.4\%$ for grouping-based control	Preserves the nominal NLM level sequence	Lower switching-loss tendency; no real-time sorting or additional power branch

6. Conclusions

This paper analyzes the mechanism of submodule capacitor voltage imbalance from a perspective of energy balance and proposes a submodule cyclic control method. By periodically circulating the submodule control signals, the capacitor energy in each converter arm is kept balanced, thereby achieving capacitor voltage balancing among submodules. Meanwhile, a grouping-based auxiliary control scheme is designed to shorten the submodule cyclic control period by selecting an appropriate grouping pattern while maintaining a low reference voltage difference. An over-margin auxiliary control scheme is also developed. By selecting standby submodules, when the voltage of a certain submodule exceeds the preset margin range, the control signals of the standby submodules are switched according to the charging or discharging state and submodule capacitor voltage condition, thereby enhancing the dynamic characteristics of the submodule cyclic control method. Finally, a PSCAD simulation model is established to evaluate the control performance of submodule cyclic control under steady-state and transient conditions. The simulation results are compared with those of the improved NLM strategy. The results demonstrate that the proposed submodule cyclic control can effectively achieve capacitor voltage balancing and reduce the switching frequency. The present study focuses on the capacitor voltage balancing mechanism, cyclic control period, transient voltage recovery, and switching-frequency characteristics. Device-level current overshoots under nonideal switching conditions are not quantitatively evaluated and will be investigated using a detailed switching-device or experimental platform in future work. Because the proposed control reassigns submodule insertion signals without changing the NLM-determined inserted-submodule number, it does not alter the nominal NLM voltage-level sequence. Nevertheless, the practical voltage THD may be influenced by capacitor voltage deviations and nonideal switching effects. Quantitative FFT-based THD verification considering dead time, gate delay, parasitic parameters, and other device-level nonidealities is not included in the present system-level study and will be addressed in future simulations and experiments.

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