

Article

A Capacitor-Less Low Dropout Regulator with Wide Input Range and High Power-Supply Rejection Ratio

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Abstract

This paper presents a capacitor-less low-dropout regulator (LDO) with a wide input-voltage range and high power-supply rejection ratio (PSRR), designed and laid out in a 0.18 μm CMOS process. The design incorporates a pre-regulation circuit to suppress power-supply noise. The proposed LDO supports an input-voltage range from 3.3 V to 40 V while maintaining an output voltage of 3.3 V. The integrated output noise from 10 Hz to 100 kHz is 4.3 nV². The proposed LDO achieves a PSRR of -109 dB at 1 kHz under a maximum load current of 100 mA, representing a 20 dB improvement compared with the same LDO without the pre-regulation circuit.

Keywords: low drop-out regulator (LDO); high PSRR; pre-regulation circuit

1. Introduction

Low dropout regulators (LDOs) are widely used in automotive electronics due to their transient response, low noise and simple architecture [1]. Automotive electronic systems require LDOs with a wide input range, ensuring stable operation even under fluctuating power-supply conditions [2]. Given the high variability in supply voltage and significant noise in automotive environments, LDOs must have a wide input range and high power-supply rejection ratio (PSRR). Since input-voltage ripple may extend over a wide frequency range from 0.1 Hz to 5 MHz, it is critical for an LDO to maintain high PSRR across this frequency range [3].

Various approaches have been proposed to improve PSRR. J. Guo et al. improved PSRR by applying feed-forward power-supply ripples to the gate of power transistor [4]. Similarly, U. Awais et al. used a replica circuit to track power-supply fluctuations by injecting reverse feed-forward current to minimize gate-source voltage errors [5]. Although these feed-forward technologies can effectively improve PSRR, they significantly increase circuit complexity. J. Zoche et al. used multi-stage power transistors in series to improve PSRR; however, their method incurs additional power consumption [6]. H. Gupta et al. proposed a high-gain amplifier with a folded cascode structure in the output stage of the amplifier, but its PSRR improvement is modest [7]. The voltage-reference circuit is also important for maintaining the output stability of an LDO. Azimi et al. proposed a two-stage subthreshold voltage reference using body-bias curvature compensation, achieving low power consumption and improved temperature stability [8]. More recently, Gagliardi et al. presented an NMOS-only self-cascode voltage reference using a decoupling pseudo-resistor



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to improve high-frequency PSR under ultra-low-voltage operation [9]. Compared with these low-voltage reference circuits, the voltage-reference structure adopted in this work requires a higher operating voltage but is more suitable for generating the stable internal 5 V supply required by the proposed high-voltage LDO.

In LDOs, PSRR is primarily determined by the error amplifier. If the PSRR of error amplifier is limited, the overall PSRR of the LDO will be constrained. Additionally, components like buffers and power stages can also introduce power noise that further degrades the PSRR of the LDO.

To address these issues, we propose a pre-regulation circuit that preprocesses the power-supply voltage, minimizing the ripples transmitted to the error amplifier, thereby enhancing PSRR. The proposed pre-regulation technology ensures a stable 5 V output in the input voltage range from 5 V to 40 V, and effectively optimizes the PSRR of the subsequent circuit stages. The design achieves a PSRR of -109 dB at 1 kHz, significantly improving the overall PSRR of the LDO.

The remainder of this paper is structured as follows: Section 2 introduces the proposed LDO architecture and transistor-level circuit. Section 3 presents the pre-layout and post-layout simulation results, and Section 4 concludes this work.

2. Circuit Design and Analysis

The employed $0.18\text{ }\mu\text{m}$ CMOS process provides high-voltage transistors rated to withstand 40 V. These high-voltage devices are used in the proposed circuit to support operation at input voltages up to 40 V.

Figure 1 illustrates the fundamental architecture of an LDO with a pre-regulation circuit. This architecture consists of a pre-regulation circuit (Pre-REG), an error amplifier (EA), a buffer, a pass element, two feedback resistors (R_{f1} , R_{f2}), and other essential modules. The pre-regulation circuit converts the high-voltage power to a low-voltage power for the error amplifier. The feedback resistors sample the output voltage and feed it back to one input of the error amplifier, while the other input is connected to the reference voltage (V_{REF}). The output of the error amplifier drives the gate of the power transistor through the buffer, generating a stable output voltage, V_{OUT} .

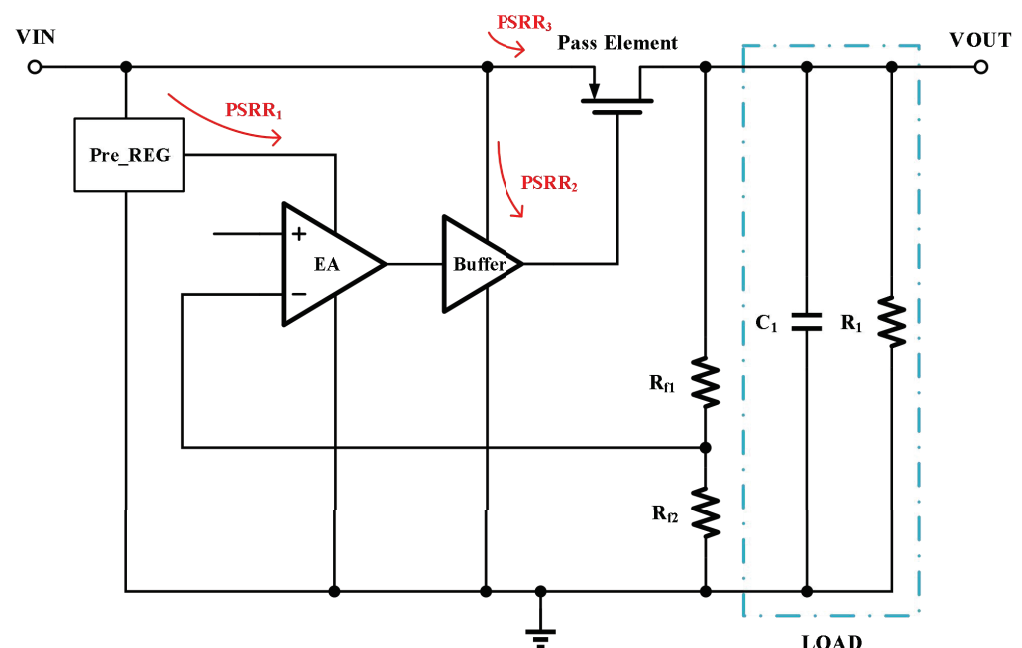


Figure 1. Fundamental architecture of LDO with a pre-regulation circuit.

2.1. Pre-REG Design

The pre-regulation circuit design is shown in Figure 2. In this design, transistors M_4 – M_{11} form a reference current source that generates a reference current I_B , independent of the supply voltage. This reference current I_B biases several diode-connected transistors and drives a source follower to produce the voltage $N3VT$, which powers the gate of LDMOS transistors M_{31} , M_{34} , M_{35} , providing high and low voltage isolation. Transistors M_{29} – M_{37} create a circuit similar to the Brokaw bandgap reference voltage source. A cascode current mirror is adopted to enhance the PSRR of the internal power supply. The linearity of the internal power supply is improved by the feedback from the current introduced in the high-voltage start-up circuit.

The pre-regulation circuit ensures a stable 5 V output, independent of temperature and input voltage, within the voltage range of 5 V to 40 V:

$$V_{DDA} = \frac{R_{11} + R_{12}}{R_{12}} \cdot \left[2 \frac{R_{10}}{R_9} V_T + V_{BE5} \right] \quad (1)$$

where V_T is thermal voltage and N is the number ratio of transistors npn_4 and npn_5 . The pre-regulation circuit effectively powers the error amplifier while mitigating power noise, significantly improving the LDO PSRR.

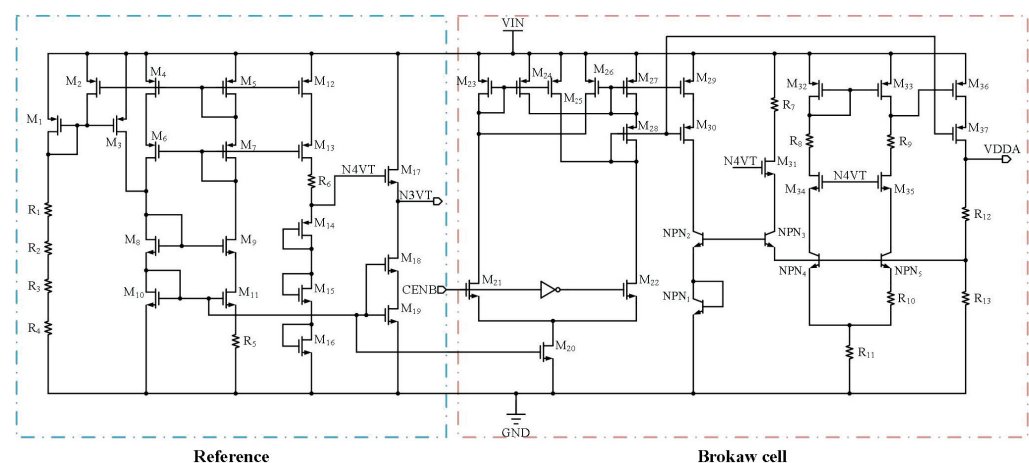


Figure 2. Pre-regulation circuit.

2.2. Proposed LDO Design

Figure 3 shows the transistor-level circuit of the LDO designed in this paper. To improve PSRR, the error amplifier uses a folded cascode two-stage operational amplifier structure, with a resistive load instead of a dynamic load at the output end of the amplifier [10]. The gain buffer stage adopts an N-type common-source amplifier (N-CS) with a current mirror load, while the power stage uses a PMOS transistor as the transmission device. The PSRR contribution path of the LDO is shown in Figure 1. The total PSRR is primarily determined by three components: the error amplifier, buffer, and power transistor. The total PSRR can be expressed as follows:

$$\text{PSRR}_{\text{LDO}} = \text{PSRR}_1 + \frac{\text{PSRR}_{\text{Buffer}}}{\beta \cdot A_{\text{EA}} \cdot A_{\text{Buffer}}} + \frac{\text{PSRR}_{\text{POW}}}{\beta \cdot A_{\text{EA}} \cdot A_{\text{Buffer}} \cdot A_{\text{POW}}} \quad (2)$$

$$\text{PSRR}_1 = \text{PSRR}_{\text{Pre-REG}} \frac{\text{PSRR}_{\text{EA}}}{\beta \cdot A_{\text{EA}}} \quad (3)$$

where A_{EA} is the amplification factor of the error amplifier, A_{Buffer} is the amplification factor of the buffer, A_{POW} is the amplification factor of the power transistor, and β is the feedback coefficient of the feedback network. The expression for β is:

$$\beta = \frac{R_{f1}}{R_{f1} + R_{f2}} \quad (4)$$

Rewriting Formula (2):

$$PSRR_{LDO} = PSRR_1 + \frac{|PSRR_{POW}| - |PSRR_{Buffer} \cdot A_{POW}|}{\beta \cdot A_{EA} \cdot A_{Buffer} \cdot A_{POW}} \quad (5)$$

From Equation (5), it can be seen that improving LDO PSRR requires maximizing PSRR of the error amplifier and designing the circuit to ensure that power-supply noise from the buffer stage and power stage cancels each other out.

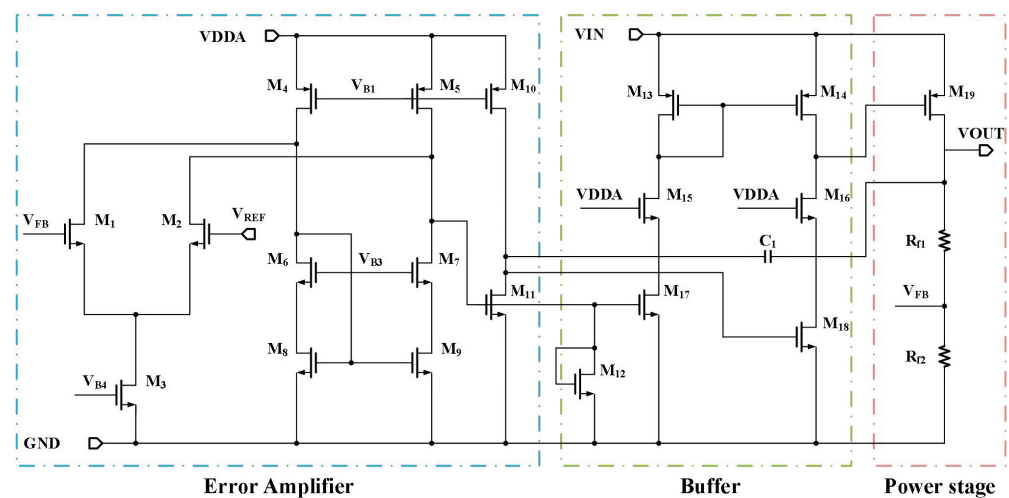


Figure 3. High PSRR capacitor-less LDO circuit.

By calculating the PSRR of PMOS power transistor and the N-CS, the expressions are:

$$PSRR_{Buffer} = \frac{A_{Buffer} \cdot g_{O,BL}}{g_{O,BIN} + A_{Buffer} \cdot g_{O,BL}} \quad (6)$$

$$\begin{aligned} PSRR_{POW} &= \frac{g_{m,POW} + g_{O,POW}}{g_{O,POW} + g_{O,L}} \\ &= -A_{POW} \cdot \left(1 + \frac{g_{O,POW}}{g_{m,POW}}\right) \end{aligned} \quad (7)$$

where $g_{O,BIN}$ is the output transconductance of the buffer stage input transistor, $g_{O,BL}$ is the output transconductance of the buffer stage load transistor, $g_{m,POW}$ is the input transconductance of the power transistor, $g_{O,POW}$ is the output transconductance of the power transistor, and $g_{O,L}$ is the load transconductance.

Substituting Equations (6) and (7) into Equation (5):

$$PSRR_{LDO} \approx PSRR_1 + \frac{\frac{g_{O,BIN}}{A_{Buffer} \cdot g_{O,BL}} + \frac{1}{A_{POW}}}{\beta \cdot A_{EA} \cdot |A_{Buffer}|} \quad (8)$$

If the intrinsic gain of the cascode structure is close to the intrinsic gain of the power transistor, Equation (8) can be simplified to:

$$\text{PSRR}_{\text{LDO}} = \text{PSRR}_1 + \frac{\frac{g_{\text{O,BIN}}}{g_{\text{O,BL}}} + 1}{\beta \cdot A_{\text{EA}} \cdot |A_{\text{Buffer}}| \cdot A_{\text{POW}}} \quad (9)$$

By comparing the symbols of the first and second terms in Equation (9), it can be found that the power-supply noise from the first stage amplifier accumulates with that from the second stage and the power stage. Thus, optimizing LDO PSRR requires simultaneously reducing both terms in Formula (9).

Furthermore, the denominator of the second term is significantly larger than that of the first term, indicating that the LDO PSRR is predominantly determined by the first term. As power noise from the buffer stage and power stage tends to cancel each other out, the noise from error amplifier becomes the primary source of LDO noise.

To enhance LDO PSRR, it is crucial to minimize the noise contribution from the error amplifier. This can be realized using a pre-regulation circuit by introducing a cascode two-stage operational amplifier for greater loop gain, with an N-type current mirror to absorb power-supply noise, thereby minimizing the effect of power-supply ripples on error amplifier.

For the capacitor-less LDO, there is no large load capacitance or bypass capacitance at the output, and the zero-pole distribution of the loop differs from that of traditional LDOs. In this design, nested Miller compensation was adopted which connects a Miller capacitor between the first stage of the error amplifier and the output. In the small-signal model, as shown in Figure 4, R_i and C_i represent the output resistance and output capacitance of stage i , C_C is the Miller compensation capacitor, C_{gd} is the parasitic capacitance of the power transistor, R_O is the load resistance of the power transistor, and C_O is the load capacitance of the power transistor.

$$V_1 \left(\frac{1}{R_1} + sC_1 + sC_C \right) - sC_C V_{\text{OUT}} = -g_{m1} V_{\text{in}} \quad (10)$$

$$V_2 \left(\frac{1}{R_2} + sC_2 \right) + g_2 V_1 = 0 \quad (11)$$

$$V_3 \left(\frac{1}{R_3} + sC_3 + sC_{gd} \right) - sC_{gd} V_{\text{OUT}} = -(g_{m4} V_1 - g_{m3} V_2) \quad (12)$$

$$V_{\text{OUT}} \left(\frac{1}{R_O} + sC_O + sC_C + sC_{gd} \right) - sC_C V_1 - sC_{gd} V_3 = -g_{mp} V_3 \quad (13)$$

$$A(s) = \frac{g_{m1}(g_{m3} + g_{m4})g_{mp}R_1R_3R_O}{1 + (g_{m3} + g_{m4})g_{mp}R_1R_3R_OC_Cs} \times \frac{1 - A_0s - A_1s^2}{1 + B_0s + B_1s^2} \quad (14)$$

$$A_0 = \frac{(g_{m3} + g_{m4})R_3R_OC_{gd} + R_OC_C}{(g_{m3} + g_{m4})g_{mp}R_3R_O} \quad (15)$$

$$A_1 = \frac{C_C (C_{gd} + C_3)}{(g_{m3} + g_{m4})g_{mp}} \quad (16)$$

$$B_0 = \frac{1}{(g_{m3} + g_{m4})g_{mp}} \left[(C_O + C_{gd}) \left(\frac{C_{gd}}{R_1 C_C} + \frac{1}{R_3} \right) + \frac{C_{gd}}{R_O} \right] \quad (17)$$

$$B_1 = \frac{C_{gd} C_O}{(g_{m3} + g_{m4})g_{mp}} \quad (18)$$

From Equation (14), the main pole of the LDO loop is located at the output of the first stage of the error amplifier:

$$p_1 = -\frac{1}{(g_{m3} + g_{m4})g_{mp}R_1R_3R_OC_C} \quad (19)$$

Setting the numerator term in Equation (14) to zero to determine the zero location.

$$1 - A_0s - A_1s^2 = 0 \quad (20)$$

$$z_{1,2} \approx \pm \sqrt{\frac{(g_{m3} + g_{m4})g_{mp}}{C_C (C_{gd} + C_3)}} \quad (21)$$

Two zeros of equal magnitude, located in the left and right half-planes, counteract the phase influence of the loop but introduce a gain change of 40 dB/dec at the zero point, which will affect the system stability. Therefore, placing these zeros at high frequency is crucial.

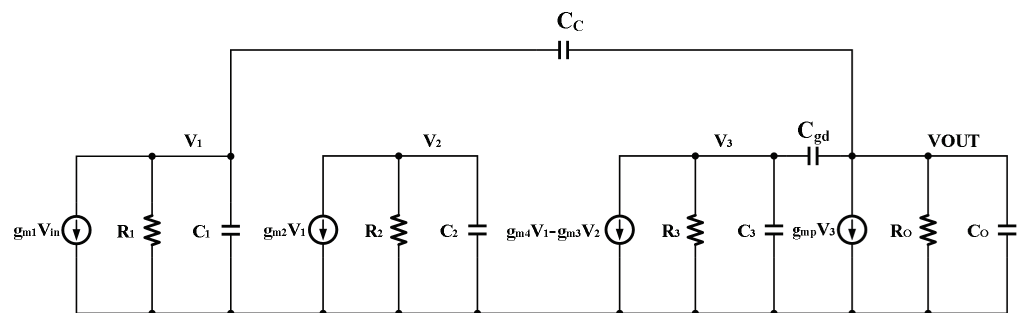


Figure 4. Small-signal model.

Setting the denominator of the second term in Formula (14) to zero and comparing it with the pole function of the second-order system to determine the additional poles:

$$1 + B_0s + B_1s^2 = 0 \quad (22)$$

$$N(s) = 1 + \frac{2\zeta}{\omega_n}s + \left(\frac{s}{\omega_n}\right)^2 \quad (23)$$

By comparing Formula (22) and (23), the expressions for ζ and ω_n are derived as follows:

$$\omega_n = \sqrt{\frac{(g_{m3} + g_{m4})g_{mp}}{C_{gd}C_O}} \quad (24)$$

$$\zeta = \frac{1}{2} \sqrt{\frac{C_O}{(g_{m3} + g_{m4})g_{mp}C_{gd}R_3^2}} \quad (25)$$

The conjugate complex poles p_2, p_3 are:

$$p_{2,3} = -\zeta\omega_n \pm \omega_n\sqrt{|\zeta^2 - 1|} \quad (26)$$

Generally, the second-order system works in an underdamped case by using $0 < \zeta < 1$, where ζ is generally selected between 0.4 and 0.8. The natural frequency ω_n should be maximized to ensure system stability.

3. Simulation Results

All circuit simulations were performed using Cadence Virtuoso 6.1.7 with the high-convergence accuracy setting.

As shown in Figure 5, under a 12 V power supply and 100 mA load, the loop gain reaches 109 dB, with a gain-bandwidth (GBW) of 1.09 MHz, and a phase margin of 66 deg. Under no-load condition with the 12 V supply, the loop gain increases to 121 dB, the GBW to 1.27 MHz and the phase margin to 69 deg, as presented in Figure 6. These alternating-current (AC) simulation results show that the capacitor-less LDO is stable across the entire load range. Figure 7 presents the simulation curves of the LDO PSRR. With a 100 mA load current and a 12 V power supply, the LDO PSRR with pre-regulation circuit reaches -109 dB at 1 kHz, improving the PSRR by 20 dB compared with the design without the pre-regulation circuit. This enhancement significantly optimizes the low-frequency LDO PSRR.

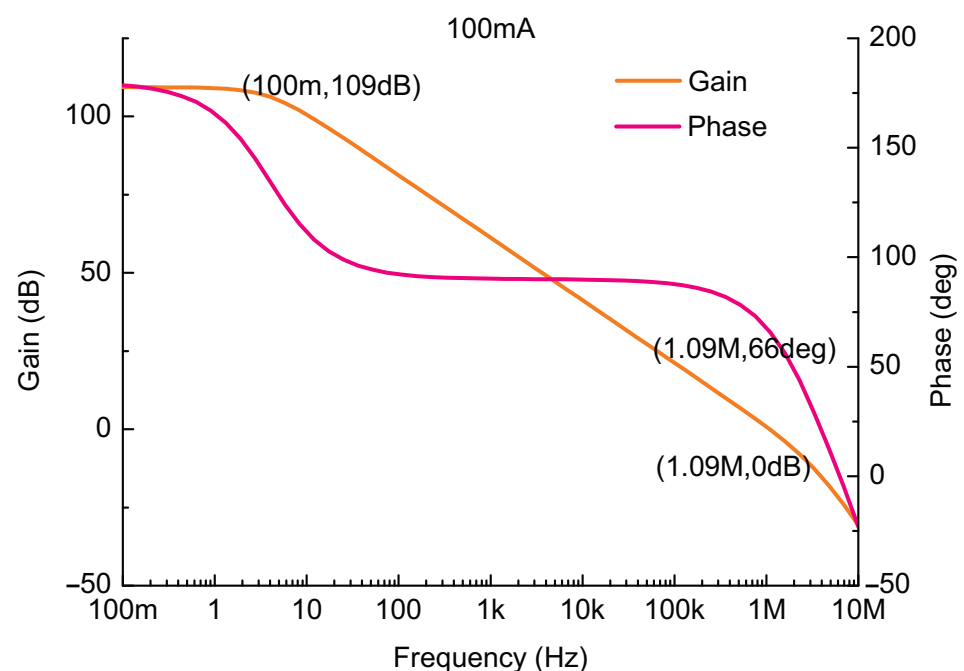


Figure 5. Simulated frequency response of the proposed LDO with 100 mA load conditions.

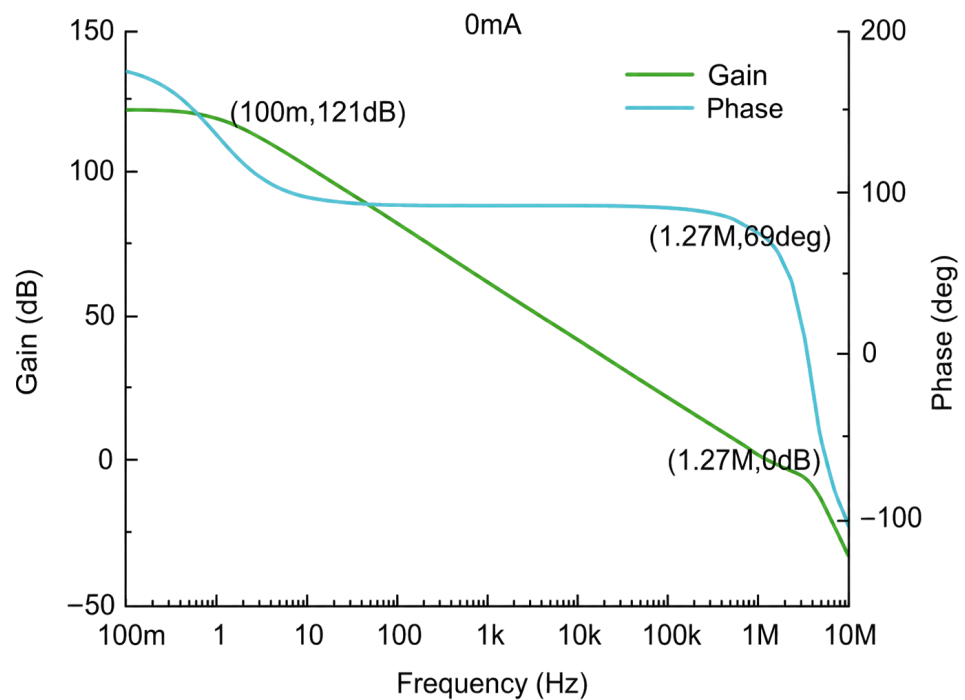


Figure 6. Simulated frequency response of the proposed LDO with no load conditions.

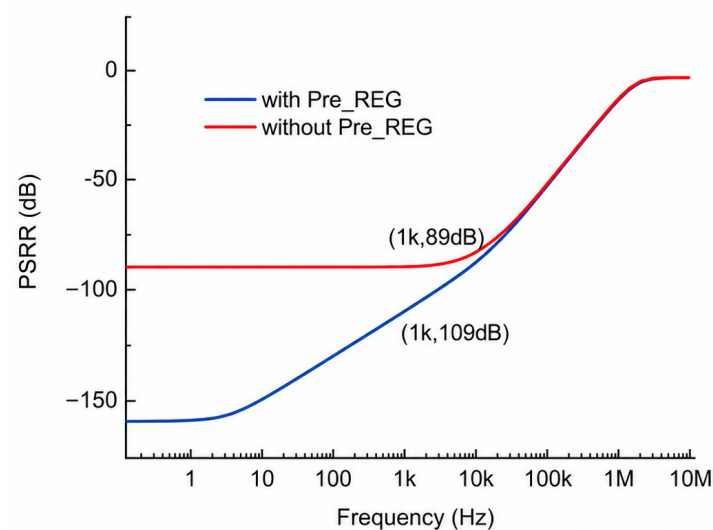


Figure 7. Simulated PSRR of the proposed LDO with $V_{IN} = 12\text{ V}$, $V_{OUT} = 3.3\text{ V}$ and $I_{LOAD} = 100\text{ mA}$.

The performance evaluation of the proposed LDO compared to existing designs reveals several key advantages and trade-offs. As outlined in Table 1, the proposed LDO demonstrates a significant PSRR enhancement, especially at lower frequencies. At 1 kHz, the proposed LDO achieves a PSRR of -109 dB , outperforming other designs, such as -71 dB in [10] and -80 dB in [11]. This significant improvement underscores the effectiveness of the novel pre-regulation circuit in mitigating power-supply noise and enhancing overall stability. The broad input voltage range of 3.3 V to 40 V offered by the proposed LDO

offers a substantial improvement over previous designs with narrower voltage ranges, making it versatile for applications such as automotive and industrial systems. The achieved dropout voltage of 170 mV is competitive compared to existing designs, such as 200 mV in [12]. A lower dropout voltage typically indicates a better performance. Our design strikes a balance between dropout voltage and other key parameters like PSRR and input voltage range.

Table 1. Performance summary and comparison.

Parameter	[10]	[12]	[11]	[13]	This Work
Technology (nm)	600	180	180	180	180
Result type	Measurement	Measurement	Measurement	Measurement	Post-layout simulation
V_{IN} (V)	2.2–5.5	1.8–2.5	NR	NR	3.3–40
V_{OUT} (V)	1.8–3.3	1.6–2.3	1	1.8	3.3
V_{DO} (mV)	105	200	200	100	170
I_{OUT} (mA)	0–150	0–200	0–50	0–1	0–100
Line regulation ($\mu V/V$)	NR	NR	NR	NR	7
Load-voltage variation (μV)	NR	NR	NR	NR	213
PSRR at 1 kHz (dB)	−71	−63	−80	−72	−109
PSRR at 10 kHz (dB)	−51	−62	−79	−55	−89
PSRR at 100 kHz (dB)	−41	−56	−62	−35	−54

NR: not reported.

The integrated output noise was calculated from the output-referred noise spectral density over the frequency range from 10 Hz to 100 kHz according to

$$\overline{V_{n,OUT}^2} = \int_{10\text{ Hz}}^{100\text{ kHz}} \overline{V_{n,EA2}^2}(f) df. \quad (27)$$

where $\overline{V_{n,EA2}^2}(f)$ represents the output-referred noise spectral density obtained through noise simulation. By numerically integrating the noise spectral density over the specified frequency range, an integrated output noise of 4.3 nV^2 was obtained.

The physical layout of the proposed LDO is shown in Figure 8. The layout dimensions are $472.315\text{ }\mu\text{m} \times 774.465\text{ }\mu\text{m}$, corresponding to an area of approximately 0.366 mm^2 . Parasitic extraction was performed based on the completed layout.

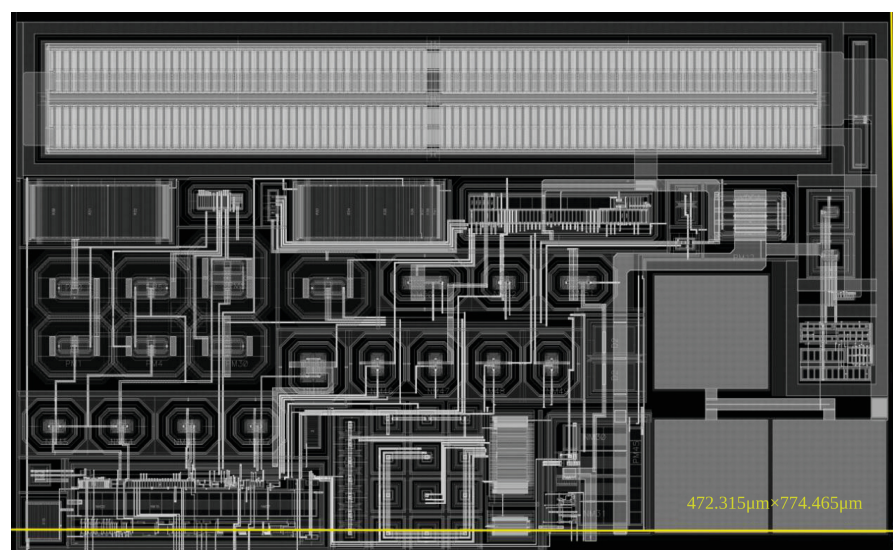


Figure 8. Physical layout of the proposed LDO designed using a $0.18\text{ }\mu\text{m}$ CMOS process. The layout dimensions are $472.315\text{ }\mu\text{m} \times 774.465\text{ }\mu\text{m}$.

The reported line regulation is $7\mu\text{V}/\text{V}$, and the output-voltage variation over the 0 mA–100 mA load-current sweep is $213\mu\text{V}$. Figure 9 presents the post-layout line-regulation and load-regulation characteristics under different process corners. The results confirm that the proposed LDO maintains stable output-voltage regulation after considering the extracted layout parasitics.

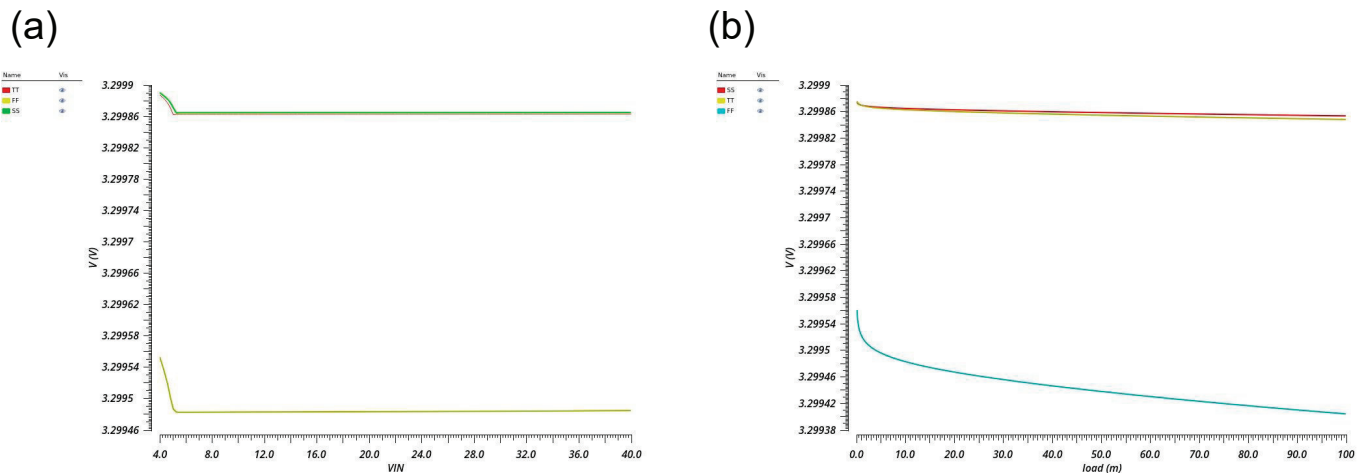


Figure 9. Post-layout regulation characteristics of the proposed LDO under different process corners: (a) V_{OUT} as a function of V_{IN} ; (b) V_{OUT} as a function of load current.

To further evaluate the robustness of the proposed LDO, additional simulations were performed across different process corners and over the temperature range from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ at a load current of 50 mA. Figure 10a presents the stability simulation results, while Figure 10b shows the corresponding PSRR simulation results. The proposed LDO maintains stable operation and effective power-supply rejection under the investigated process-corner and temperature conditions.

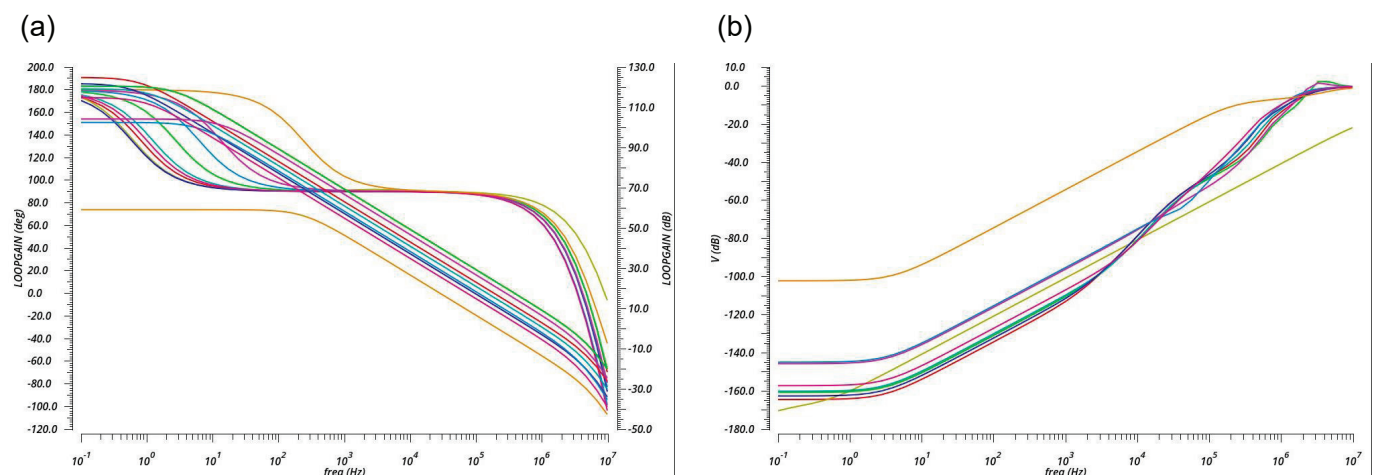


Figure 10. Simulation results of the proposed LDO across different process corners and over the temperature range from $-40\text{ }^{\circ}\text{C}$ to $125\text{ }^{\circ}\text{C}$ at $I_{LOAD} = 50\text{ mA}$: (a) stability characteristics; (b) PSRR characteristics.

It should be noted that the proposed LDO has not yet been experimentally measured. Although the results of this work are based on post-layout simulations including extracted parasitic effects, the results of the compared designs were obtained from measurements. Therefore, the comparison in Table 1 should be regarded as an indicative performance benchmark rather than a direct experimental comparison.

The proposed LDO excels in PSRR performance, particularly at lower frequencies, due to its innovative pre-regulation approach and optimized circuit design. The wide input voltage range adds significant flexibility, although there are trade-offs in dropout voltage and output current capabilities. These attributes make our LDO ideal for applications where noise rejection and voltage stability are crucial, while the output current and dropout voltage should be evaluated based on the specific application needs.

4. Conclusions

This paper presents a capacitor-less LDO with a wide input-voltage range and enhanced PSRR, designed and laid out in a 0.18 μm CMOS process. The proposed design employs an N-type common-source buffer to reduce the noise contribution of the pass transistor and a pre-regulation circuit to suppress the supply noise transmitted to the error amplifier.

Simulation results demonstrate an integrated output noise of 4.3 nV² over the frequency range from 10 Hz to 100 kHz. The achieved PSRR values are −109 dB, −89 dB, and −54 dB at 1 kHz, 10 kHz, and 100 kHz, respectively. The pre-regulation circuit improves the PSRR by 20 dB at 1 kHz compared with the same LDO without pre-regulation.

Author Contributions: Conceptualization, C.W. and W.H.; methodology, C.W. and C.Y.; software, C.Y.; validation, C.W., C.Y., Y.P. and Z.L.; formal analysis, C.W. and Z.L.; investigation, C.W.; resources, W.H.; data curation, C.W. and Y.P.; writing—original draft preparation, C.W.; writing—review and editing, Y.P., Z.L. and W.H.; visualization, C.W. and Y.P.; supervision, Z.L. and W.H.; project administration, W.H.; funding acquisition, W.H. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The data presented in this study are available on request from the corresponding author.

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Conflicts of Interest: Authors Chunlai Wang, Chen Yang and Weihua Han were employed by the company BASALT Semiconductor Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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