electronics

MDPI

Article

A CMOS Variable-Gain Low-Noise Amplifier Achieving a 33.5 dB Gain Tuning Range for Ka-Band Receiver Applications

Yo-Sheng Lin [1,*], Yu-Hao Zhuang [1] and Guann Pyng Li [2]

[1] Department of Electrical Engineering, National Chi Nan University, Puli 545301, Taiwan
[2] Department of Electrical Engineering and Computer Science, University of California, Irvine, CA 92697, USA
* Correspondence: stephenlin@ncnu.edu.tw

Abstract

We present a 14.2 mW, 17.7–25.1 GHz differential CMOS low-noise amplifier (LNA) featuring a wide gain tuning range of 33.5 dB and a low average noise figure (NF_{avg}) of 3 dB. These characteristics are enabled by the combined use of a body-to-ground floating technique, coupled transmission-line (TL) feedback, and multiple inductive-peaking techniques. The proposed LNA consists of an input transformer, a common-source (CS) input stage, current-reused CS gain and output stages, and an output transformer. The body-to-ground floating technique connects the transistor body to ground through a large body-floating resistor (R_B) of 3.2 kΩ, thereby suppressing substrate noise and leakage while enhancing the gain and reducing the NF. Moreover, coupled-TL feedback is introduced in the input stage to further improve the gain and NF, while multiple inductive-peaking techniques are adopted to extend the 3 dB gain bandwidth (f_{3dB}). In the maximum-gain mode, with the transistor switches turned off, the LNA consumes 14.2 mW and achieves a measured S_{21} of 17 ± 1.5 dB over 17.7–25.1 GHz, corresponding to an f_{3dB} of 7.4 GHz. The measured minimum NF is 2.37 dB at 17 GHz, with an NF_{avg} of 2.71 dB over 17–21 GHz. The LNA also achieves a figure of merit (FoM_1) of 12.27 GHz and a normalized figure of merit (FoM_2) of 1.55 mm^{-2}. Furthermore, a wide gain tuning range of 33.5 dB, from 16.7 to −16.8 dB, is obtained. To the best of the authors' knowledge, the proposed LNA achieves one of the lowest NF_{avg} values and the highest FoM_1 and FoM_2 among reported K- and Ka-band CMOS LNAs.

Keywords: CMOS; K-band; low noise amplifier; receiver; variable gain

1. Introduction

With the rapid expansion of K- and Ka-band transceivers for wireless and satellite communication applications, highly integrated and cost-effective CMOS radio-frequency integrated circuits (RFICs) operating in the K- and Ka-band have received increasing attention [1–5]. Figure 1 illustrates a conceptual CMOS–GaN/GaAs heterogeneously integrated transceiver front-end for K- and Ka-band wireless and satellite communication applications. This architecture offers a promising approach for developing a compact and highly integrated transceiver by leveraging the complementary advantages of different semiconductor technologies. In the K-band receiver front-end, GaAs technology is well suited for achieving low-noise performance, whereas CMOS technology provides high integration density and low power consumption. A representative receiver architecture comprises four parallel channels, each consisting of a GaAs low-noise amplifier (LNA), a CMOS variable-gain LNA, and a down-conversion mixer. The overall receiver is designed to provide a variable

Check for updates

Academic Editor: Pietro Manzoni

Received: 6 September 2026
Revised: 6 October 2026
Accepted: 14 October 2026
Published: 16 October 2026

Copyright: © 2026 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

gain of 20–60 dB, a noise figure (NF) of 1.35–4 dB, and an input third-order intercept point (IIP3) ranging from −50 to −20 dBm. On the transmitter side, the complementary characteristics of CMOS and GaN technologies can be used to realize a compact Ka-band front-end featuring high output power (P_{out}), high linearity, and high power-added efficiency (PAE). Accordingly, the proposed heterogeneously integrated architecture provides an attractive solution for realizing compact, high-performance transceivers for K- and Ka-band wireless and satellite communication applications.

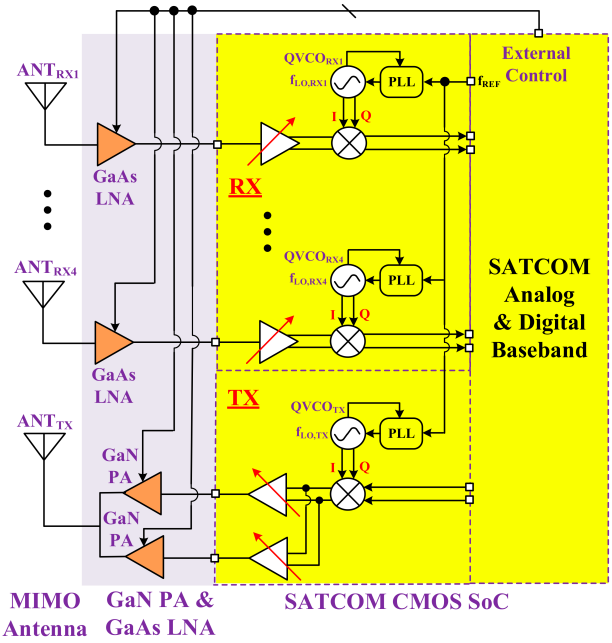


Figure 1. Illustrative diagram of a typical CMOS–GaN/GaAs heterogeneously integrated transceiver front-end for K- and Ka-band wireless and satellite communication applications.

The selection of CMOS technology for the variable-gain LNA is motivated by the different roles and performance requirements of the receiver building blocks. Compared with CMOS, GaAs generally provides superior electron mobility, higher transistor speed, and lower noise, making it attractive for the first-stage LNA, where low NF is a primary consideration. However, GaAs typically offers lower integration density and is less suitable for integrating digital, control, and signal-processing circuitry on the same chip. In contrast, CMOS benefits from mature and highly scaled fabrication technologies, enabling high integration density, compact active and passive circuits, and potentially lower implementation cost and power consumption. GaN provides high breakdown voltage, high power density, and excellent power-handling capability, making it particularly attractive for high-power transmitter applications. However, these characteristics are not essential for a low-power receiver LNA and may involve less favorable tradeoffs in terms of integration density and noise performance for the proposed application. Therefore, the use of GaAs for the first-stage LNA and CMOS for the subsequent variable-gain and frequency-conversion stages provides a practical technology partition: GaAs is employed where low-noise performance is critical, whereas CMOS is used where high integration density, low power consumption, wide gain programmability, and integration with control circuitry are more important. In particular, the CMOS variable-gain LNA must accommodate a relatively wide dynamic range after the low-noise first stage while maintaining low power consumption and stable RF performance. These requirements make CMOS an attractive technology for the proposed variable-gain receiver stage, even though GaAs may provide a lower NF for a standalone LNA.

The CMOS variable-gain LNA is a key component in the receiver front-end because it must provide a wide gain control range while simultaneously maintaining low noise and low power consumption. In addition to wide gain tunability, desirable characteristics include high gain, broad 3 dB gain bandwidth (f_{3dB}), and stable phase and power linearity over the operating range. Several K/Ka/V-band CMOS LNAs and variable-gain LNAs have recently been reported [6–16]. However, simultaneously satisfying these requirements remains a considerable design challenge. For instance, a 16.3–26.6 GHz two-stage CMOS variable-gain LNA employing a common-source (CS) first stage and a cascode second stage was reported in [11]. Cascode transconductance (g_m) boosting and shunt-series transformer feedback were utilized to enhance the gain, bandwidth, and NF, achieving a maximum S_{21} ($S_{21,max}$) of 18.1 dB and an output third-order intercept point (OIP3) of 10.1 dBm. Nevertheless, the LNA consumes 19.2 mW and exhibits an average NF (NF_{avg}) of 4.15 dB, which are relatively high, mainly due to the 16 mA bias current and the noise contribution of the input transformer. In [12], a 17–26 GHz two-stage cascode CMOS variable-gain LNA incorporating inductive source degeneration for input matching and phase stabilization was presented. The LNA achieved an $S_{21,max}$ of 18.5 dB and an OIP3 of 14.5 dBm; however, its power consumption (P_{dc}) of 67.2 mW and NF_{avg} of 4.8 dB remain relatively high. These limitations are primarily attributed to the 28 mA bias current required by each stage and the additional noise introduced by the input transformer. In [15], a 21.2–24 GHz three-stage CS CMOS LNA employing gate-source transformer feedback for simultaneous noise and impedance matching was demonstrated. Although it achieved an exceptionally low P_{dc} of 0.99 mW and an $S_{21,max}$ of 19.1 dB, the corresponding NF_{avg} of 4 dB and OIP3 of -3.8 dBm are less favorable. These performance limitations can be attributed mainly to the restricted voltage headroom resulting from the 0.3 V supply voltage.

To overcome these limitations and provide a practical CMOS variable-gain LNA solution for 17–21 GHz LEO SATCOM receivers, this work presents a 14.2 mW differential CMOS variable-gain LNA that simultaneously achieves low power consumption, low NF, high gain, wide bandwidth, and favorable phase and power-linearity performance. The proposed LNA combines a body-to-ground floating technique, coupled transmission-line (TL) feedback, and multiple inductive-peaking techniques to improve its overall performance. The proposed design achieves a measured f_{3dB} of 7.4 GHz from 17.7 to 25.1 GHz, a wide gain tuning range of 33.5 dB from 16.7 to -16.8 dB at 19 GHz, and an NF_{avg} of 3 dB over 16–25 GHz. The employed techniques enhance the gain, bandwidth, and noise performance while enabling a wide gain-control range without substantially increasing the power consumption.

The remainder of this paper is organized as follows. Section 2 presents the analysis and design methodology of the input and output transformers. Section 3 describes the design considerations and operating principles of the proposed variable-gain LNA. Section 4 presents the post-layout simulation results, including the effects of layout-extracted parasitics, of the proposed LNA based on a foundry's 90 nm CMOS technology. Section 5 discusses the measurement results and compares the performance of the proposed LNA with those of previously reported works. Finally, Section 6 concludes the paper.

2. Transformer Design

Figure 2a illustrates the simplified layout of the input transformer (TF_{in}), which converts the single-ended input signal into differential input signals. TF_{in} comprises a one-turn spiral primary coil and a three-turn spiral, symmetrical, center-tapped secondary coil. Most of the spiral structures are implemented using the top metal layer, i.e., the ninth metal layer (MT_9), with a thickness of 3.4 μm, whereas only the underlying interconnection lines are implemented using the eighth metal layer (MT_8), with a thickness of 0.85 μm. The

metal-line width and spacing are 4 μm and 3 μm, respectively. The core of TF_{in} occupies a chip area of 111 × 128.4 μm^2, corresponding to 0.014 mm^2. The normalized chip area is $5.7 \times 10^{-5}\ \lambda_0^2$.

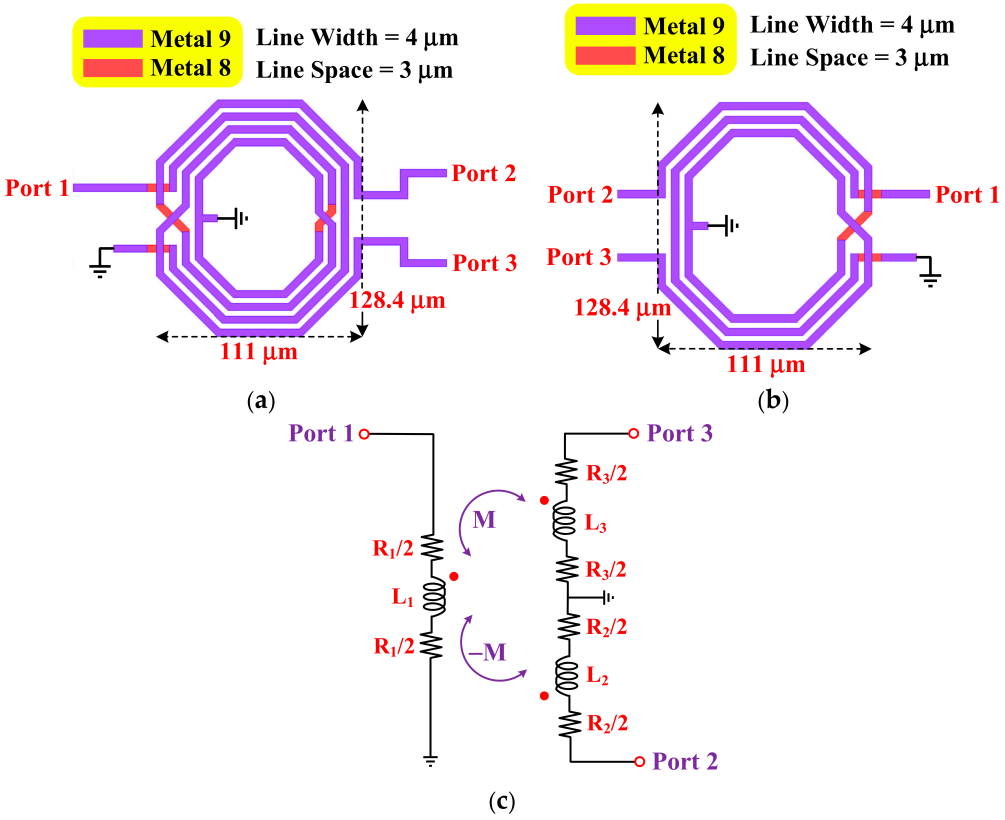


Figure 2. (**a**) Simplified layout diagrams of (**a**) the input transformer (TF_{in}) and (**b**) the output transformer (TF_{out}). (**c**) Equivalent circuit model of TF_{in} and TF_{out}.

Figure 2b presents the simplified layout of the output transformer (TF_{out}), which converts the differential output signals into a single-ended output signal. TF_{out} consists of a two-turn spiral, symmetrical, center-tapped primary coil and a one-turn spiral secondary coil. Most of the spiral structures are implemented using MT_9, with a thickness of 3.4 μm, while only the underlying interconnection lines are implemented using MT_8, with a thickness of 0.85 μm. The metal-line width and spacing are 4 μm and 3 μm, respectively. The core of TF_{out} occupies the same chip area of 111 × 128.4 μm^2, corresponding to 0.014 mm^2, with a normalized chip area of $5.7 \times 10^{-5}\ \lambda_0^2$.

Figure 2c shows the equivalent circuit model of TF_{in} and TF_{out}. L_1 and R_1 denote the equivalent series inductance and resistance, respectively, of the primary coil. L_2 and R_2 represent the equivalent series inductance and resistance, respectively, of the port-2 half of the secondary coil, while L_3 and R_3 denote the corresponding parameters of the port-3 half. Taking TF_{in} as an example, the mutual coupling -M between the clockwise primary coil and the counterclockwise port-2 half of the secondary coil is negative. In contrast, the mutual coupling M between the clockwise primary coil and the clockwise port-3 half of the secondary coil is positive. The small-signal parameters of TF_{in} and TF_{out} can be extracted from the Z-matrix. Their key derived characteristics, including the quality factor (Q) and power loss, can then be obtained from the following three-port Z-matrix:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} \\ Z_{21} & Z_{22} & Z_{23} \\ Z_{31} & Z_{32} & Z_{33} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \quad (1)$$

Figure 3a shows the simulated L_1, L_2, L_3, $L_{m2,1}$, and $L_{m3,1}$ versus frequency characteristics of TF_{in}. At 19 GHz, TF_{in} exhibits L_1 of 326.1 pH, L_2 of 537.3 pH, L_3 of 520 pH, $L_{m2,1}$ of −233.2 pH, and $L_{m3,1}$ of 217 pH. The close values of L_2 and L_3 result from the symmetrical configuration of the center-tapped secondary coil. The negative $L_{m2,1}$ and positive $L_{m3,1}$ arise from the opposite and identical winding orientations, respectively, between the primary coil and the corresponding halves of the secondary coil. Figure 3b presents the simulated R_1, R_2, R_3, $R_{m2,1}$, and $R_{m3,1}$ versus frequency characteristics of TF_{in}. At 19 GHz, TF_{in} exhibits R_1 of 2.3 Ω, R_2 of 3.5 Ω, R_3 of 3.2 Ω, $R_{m2,1}$ of −0.64 Ω, and $R_{m3,1}$ of 0.33 Ω.

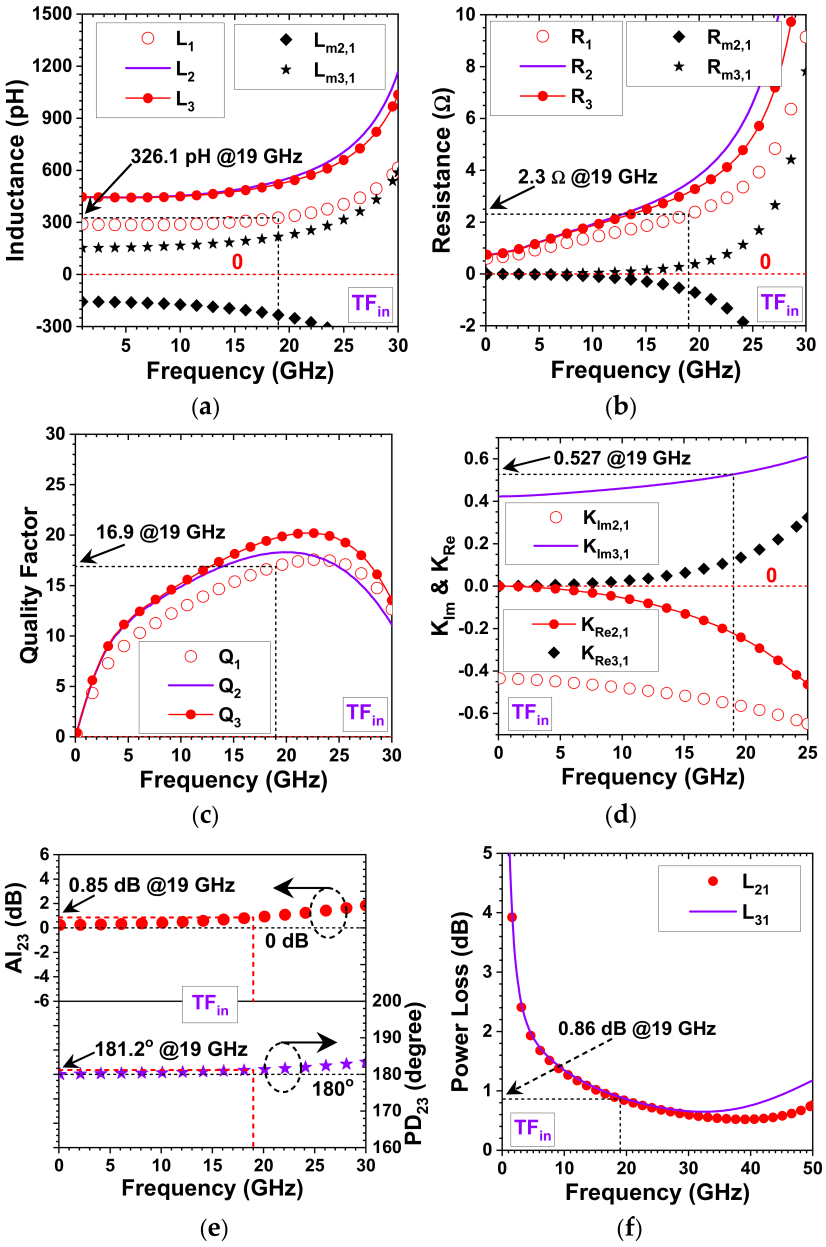


Figure 3. Simulated frequency characteristics of TF_{in}: (**a**) L_1, L_2, L_3, $L_{m2,1}$, and $L_{m3,1}$; (**b**) R_1, R_2, R_3, $R_{m2,1}$, and $R_{m3,1}$; (**c**) Q_1, Q_2, and Q_3; (**d**) $K_{Im3,1}$, $K_{Im3,2}$, $K_{Re3,1}$, and $K_{Re3,2}$; (**e**) AI_{23} and PD_{23}; and (**f**) L_{21} and L_{31}.

Figure 3c presents the simulated Q_1, Q_2, and Q_3 versus frequency characteristics of TF_{in}. At 19 GHz, TF_{in} achieves Q_1 of 16.9, Q_2 of 18.3, and Q_3 of 19.7. Figure 3d shows the simulated $K_{Im2,1}$, $K_{Im3,1}$, $K_{Re2,1}$, and $K_{Re3,1}$ versus frequency characteristics of TF_{in}.

At 19 GHz, the corresponding values are −0.557, 0.527, −0.224, and 0.122, respectively. Figure 3e illustrates the simulated AI_{23} and PD_{23} versus frequency characteristics of TF_{in}. At 19 GHz, TF_{in} achieves an AI_{23} of 0.85 dB and a PD_{23} of 181.2°. The slight deviation from the ideal PD_{23} of 180° is attributed to the symmetrical configuration of the secondary coil. Figure 3f shows the simulated L_{21} and L_{31} versus frequency characteristics of TF_{in}. At 19 GHz, TF_{in} exhibits L_{21} of 0.86 dB and L_{31} of 0.89 dB. The low power loss is attributed to the optimized spiral-transformer configuration over the 17–21 GHz frequency band of interest.

Figure 4a shows the simulated L_1, L_2, L_3, $L_{m2,1}$, and $L_{m3,1}$ versus frequency characteristics of TF_{out}. At 19 GHz, TF_{out} achieves L_1 of 279.1 pH, L_2 of 268.4 pH, L_3 of 294.2 pH, $L_{m2,1}$ of −151 pH, and $L_{m3,1}$ of 142.2 pH. The close values of L_2 and L_3 are attributed to the symmetrical structure of the center-tapped primary coil. The negative $L_{m2,1}$ and positive $L_{m3,1}$ result from the opposite and identical winding orientations, respectively, between the primary coil and the corresponding secondary-coil halves. Figure 4b shows the simulated R_1, R_2, R_3, $R_{m2,1}$, and $R_{m3,1}$ versus frequency characteristics of TF_{out}. At 19 GHz, TF_{out} exhibits R_1 of 1.9 Ω, R_2 of 1.8 Ω, R_3 of 2.1 Ω, $R_{m2,1}$ of −0.29 Ω, and $R_{m3,1}$ of 0.11 Ω.

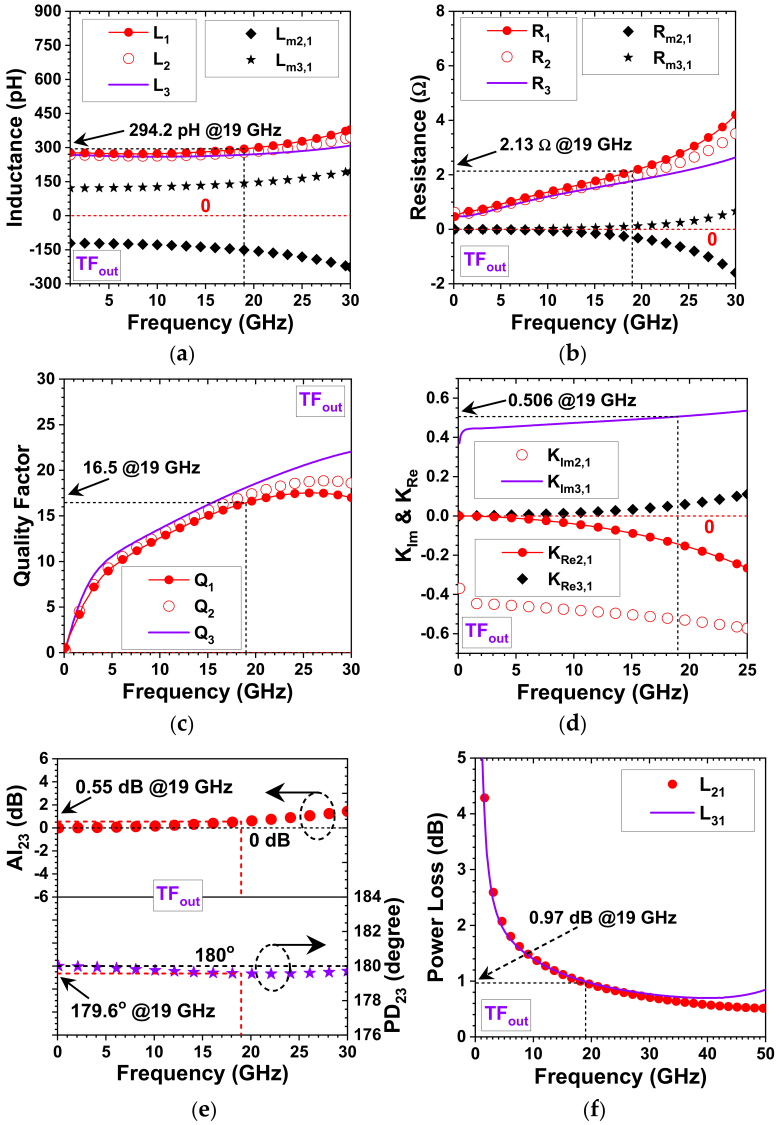
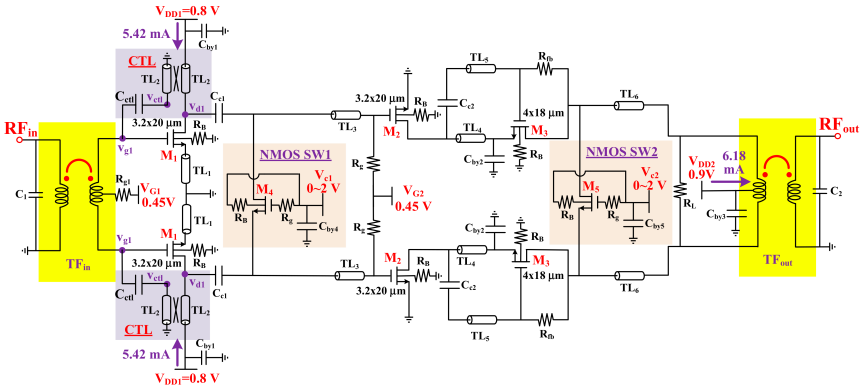


Figure 4. Simulated frequency characteristics of TF_{out}: (**a**) L_1, L_2, L_3, $L_{m2,1}$, and $L_{m3,1}$; (**b**) R_1, R_2, R_3, $R_{m2,1}$, and $R_{m3,1}$; (**c**) Q_1, Q_2, and Q_3; (**d**) $K_{Im3,1}$, $K_{Im3,2}$, $K_{Re3,1}$, and $K_{Re3,2}$; (**e**) AI_{23} and PD_{23}; and (**f**) L_{21} and L_{31}.

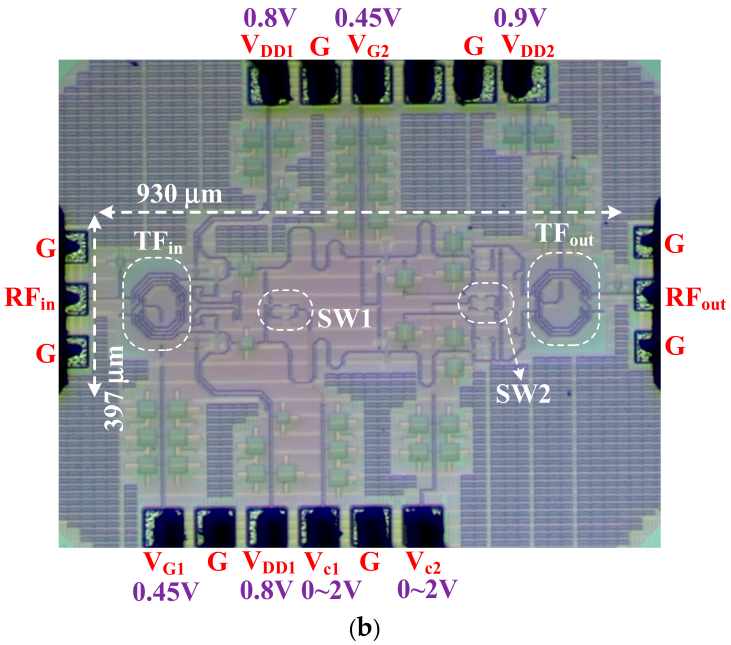
Figure 4c presents the simulated Q_1, Q_2, and Q_3 versus frequency characteristics of TF_{out}. At 19 GHz, TF_{out} achieves Q_1 of 17.2, Q_2 of 18.1, and Q_3 of 16.5. Figure 4d shows the simulated $K_{Im2,1}$, $K_{Im3,1}$, $K_{Re2,1}$, and $K_{Re3,1}$ versus frequency characteristics of TF_{out}. At 19 GHz, TF_{out} achieves $K_{Im2,1}$ of −0.527, $K_{Im3,1}$ of 0.506, $K_{Re2,1}$ of −0.143, and $K_{Re3,1}$ of 0.054. Figure 4e illustrates the simulated AI_{12} and PD_{12} versus frequency characteristics of TF_{out}. At 19 GHz, TF_{out} achieves an AI_{12} of 0.55 dB and a PD_{12} of 179.6°. The small deviation from the ideal PD_{12} of 180° is attributed to the symmetrical configuration of the primary coil. Finally, Figure 4f presents the simulated L_{31} and L_{32} versus frequency characteristics of TF_{out}. At 19 GHz, TF_{out} exhibits L_{31} of 0.97 dB and L_{32} of 0.99 dB. The low insertion loss is attributed to the optimized spiral-transformer configuration over the 17–21 GHz frequency band of interest.

3. Variable-Gain LNA Architecture

Figure 5a shows the schematic of the proposed differential CMOS variable-gain LNA.



(**a**)



(**b**)

Figure 5. (**a**) Schematic diagram, and (**b**) chip micrograph of the K-band CMOS variable-gain LNA.

The LNA comprises an input transformer, a common-source (CS) input stage, current-reused CS gain and output stages, and an output transformer. A large bypass capacitor of 8.27 pF is connected to the source node of M_3 to establish a low-impedance AC ground, exhibiting an equivalent impedance of 0.104 − j0.001 Ω at 19 GHz.

The proposed LNA simultaneously achieves wideband high gain and NF by employing a body-to-ground floating technique, coupled-TL feedback, and multiple inductive-peaking techniques. The body-to-ground floating technique is implemented in transistors M_1–M_3 by connecting each transistor body to ground through a large body-floating resistor (R_B) of 3.2 kΩ. This approach suppresses substrate noise and leakage currents, thereby improving the gain and reducing the NF. Specifically, the transistor bodies are effectively grounded under DC conditions while remaining electrically floating at AC frequencies.

Furthermore, coupled-TL feedback is incorporated into the input stage to provide additional gain enhancement and NF reduction. Multiple series- and parallel-inductive-peaking techniques are also adopted to broaden f_{3dB}. Let C_{eff1} and C_{eff2} denote the equivalent parallel capacitances at the single-ended drain nodes of the input and output stages, respectively, and let L_{eff1} and L_{eff2} represent their corresponding equivalent parallel inductances. In addition, L_{tl3} and L_{tl5} denote the equivalent inductances of TL_3 and TL_5, respectively. The parallel-peaking networks formed by L_{eff1}/C_{eff1} and L_{eff2}/C_{eff2} enhance S_{21} near the lower corner-frequency region of 13–15 GHz. In contrast, the series-peaking networks formed by L_{tl3}/C_{gs2} and $[L_{tl5} - 1/(\omega^2 C_{c2})]/C_{gs3}$ enhance S_{21} near the upper corner-frequency region of 23–25 GHz.

A 1:3 single-ended-to-differential transformer (TF_{in}), together with an input capacitance (C_1) of 189.6 fF, is employed to perform input impedance matching and single-ended-to-differential signal conversion. At the output, a 2:1 differential-to-single-ended transformer (TF_{out}), along with an output capacitance (C_2) of 173 fF, provides output impedance matching and differential-to-single-ended signal conversion. The highly symmetrical circuit topology and physical layout are expected to provide high common-mode rejection ratio (CMRR) and power-supply rejection ratio (PSRR).

An NMOS switch transistor (NMOS SW1) based on a DTMOS-with-R_B configuration is inserted between the outputs of the differential input stage. In this topology, the transistor body is connected to the gate through a large body-floating resistor (R_B) of 3.2 kΩ. The resulting configuration improves the open-circuit and short-circuit characteristics in the off- and on-states, respectively, thereby enabling a wide S_{21} tuning range [17]. A second NMOS switch transistor (NMOS SW2), employing the same DTMOS-with-R_B configuration, is placed between the outputs of the differential output stage to further expand the S_{21} tuning range.

Note that SW1 and SW2 are implemented using standard core transistors, rather than thick-oxide I/O transistors, in the adopted 90 nm CMOS technology, and are configured as DTMOS devices. Although the control voltages V_{c1} and V_{c2} range from 0 to 2 V, the actual gate-to-source and gate-to-drain voltage stresses are determined by the source/drain bias voltages of SW1 and SW2. The nominal operating-voltage range (V_{nom}) of the standard core transistors used for SW1 and SW2 is 1–1.8 V. The LNA employs low supply voltages of V_{DD1} = 0.8 V and V_{DD2} = 0.9 V primarily to reduce power consumption. For SW1, both the source and drain terminals are biased at V_{G2} = 0.45 V. Therefore, as V_{c1} varies from 0 to 2 V, V_{GS} and V_{GD} vary from −0.45 to 1.55 V. For SW2, both the source and drain terminals are biased at V_{DD2} = 0.9 V. Consequently, as V_{c2} varies from 0 to 2 V, V_{GS} and V_{GD} vary from −0.9 to 1.1 V. Thus, the maximum positive gate-to-source and gate-to-drain voltage stresses are 1.55 V for SW1 and 1.1 V for SW2, respectively, which are within the specified nominal operating-voltage range of the core devices. A dedicated accelerated gate-oxide lifetime test was not performed in this work; however, the maximum applied positive terminal voltage remains within the specified operating-voltage range of the adopted core devices. Regarding the body-to-source/drain junction currents, the 3.2 kΩ body resistor (R_B) limits the DC current between the gate-control node and the body and thereby reduces potential substrate-current injection under normal operation. At RF frequencies, R_B presents a high

impedance relative to the signal path, allowing the DTMOS configuration to provide the desired threshold-voltage modulation while minimizing its influence on the RF signal path.

Figure 5b presents the chip micrograph of the proposed variable-gain LNA. The fabricated LNA occupies a compact chip area of 0.93 × 0.397 mm^2, corresponding to 0.369 mm^2, excluding the test pads.

4. Variable-Gain LNA Design

Figure 6a shows the simulated S_{11} and S_{22} as functions of frequency for the variable-gain LNA in the maximum-gain mode, i.e., $V_{c1} = V_{c2} = 0$ V. The LNA exhibits local minimum S_{11} values of −25.8 dB at 18.6 GHz and −24.6 dB at 23.7 GHz, resulting in a wide −10 dB input-matching bandwidth (f_{10dB}) of 8 GHz from 17.2 to 25.2 GHz. Meanwhile, the minimum S_{22} of −26 dB occurs at 20.8 GHz, and S_{22} remains below −10 dB from 17.7 to 28 GHz, corresponding to an f_{10dB} of 10.3 GHz.

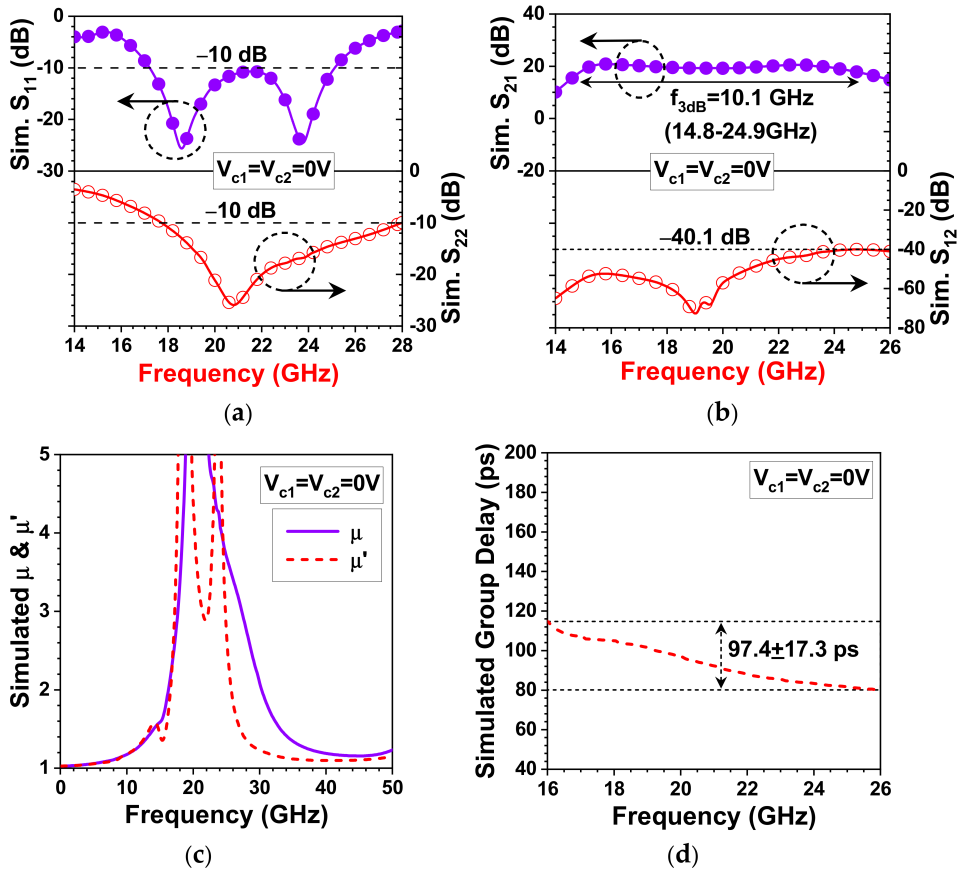


Figure 6. Simulated frequency characteristics of the variable-gain LNA with $V_{c1} = V_{c2} = 0$ V: (**a**) S_{11} and S_{22}; (**b**) S_{21} and S_{12}; (**c**) stability factors μ and μ′; and (**d**) group delay.

Figure 6b presents the simulated S_{21} and S_{12} characteristics over frequency under the same bias condition. The LNA provides a gain of 19.3 ± 1.5 dB over 14.8–24.9 GHz, corresponding to an f_{3dB} of 10.1 GHz. In addition, S_{12} remains below −40.1 dB over 14–26 GHz, indicating excellent reverse isolation.

It has been reported that μ > 1, or equivalently its dual stability parameter μ′ > 1, is a necessary and sufficient condition for unconditional stability [18]. Figure 6c shows the simulated μ and μ′ as functions of frequency. Over 0.1–50 GHz, both μ and μ′ remain greater than 1.03, confirming unconditional stability across the entire frequency range.

Furthermore, group delay (GD) is an important parameter for assessing the phase linearity and signal integrity of a wideband LNA. For a linear time-invariant (LTI) system, GD is typically derived from the phase response of S_{21} and is defined as

$$GD \equiv -\frac{d\angle S_{21}}{d\omega} \tag{2}$$

GD characterizes the frequency-dependent propagation delay experienced by the spectral components of a signal as they pass through the LTI system. Ideally, a constant GD ensures that the different frequency components of a modulated signal undergo nearly identical delays, thereby reducing phase distortion and preserving waveform integrity. Figure 6d shows the simulated GD as a function of frequency. The LNA exhibits a small GD variation of only ±17.3 ps over 16–26 GHz, demonstrating good phase linearity and limited phase distortion across the operating bandwidth.

Figure 7a shows the simulated NF and minimum available noise figure (NF_{min}) as functions of frequency for the LNA with $V_{c1} = V_{c2} = 0$ V. Over 16–26 GHz, the difference between NF and NF_{min} remains below 0.1 dB, indicating effective wideband noise matching over the frequency range of interest, particularly 17–21 GHz. The LNA achieves a minimum NF of 2.32 dB at 16.1 GHz and maintains an NF below 3 dB from 13.9 to 20.3 GHz.

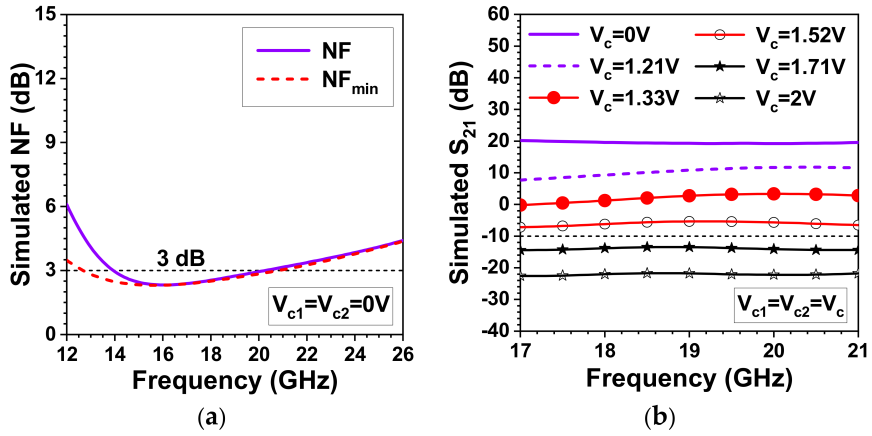


Figure 7. (**a**) Simulated NF versus frequency characteristics of the variable-gain LNA with $V_{c1} = V_{c2} = 0$ V, and (**b**) simulated S_{21} versus frequency characteristics under various $V_{c1} = V_{c2}$ values.

Figure 7b shows the simulated S_{21} characteristics versus frequency for various $V_{c1} = V_{c2}$ values. At $V_{c1} = V_{c2} = 0$ V, the LNA achieves a high and flat S_{21} of 19.3–20.2 dB over the frequency range of interest, 17–21 GHz. At 19 GHz, a wide gain tuning range of 41.1 dB is achieved, with S_{21} decreasing from 19.3 to −21.8 dB as $V_{c1} = V_{c2}$ increases from 0 to 2 V.

Figure 8a shows the simulated S_{11} characteristics versus frequency for various V_{c1} values with $V_{c2} = 0$ V. For V_{c1} ranging from 1.49 to 2 V, with NMOS switch SW1 in the on-state, S_{11} remains below −10 dB from 14.5 to 25.8 GHz, corresponding to an f_{10dB} of 11.3 GHz. The S_{11} characteristics in this control-voltage range differ from those at $V_{c1} = 0$ V, where SW1 is in the off-state, primarily because of the change in the input-stage load impedance associated with the switching state of SW1.

Figure 8b presents the simulated S_{22} versus frequency for various V_{c1} values with $V_{c2} = 0$ V. With SW1 in the on-state and V_{c1} ranging from 1.49 to 2 V, S_{22} remains below −10 dB over 17.5–28.2 GHz, corresponding to an f_{10dB} of 10.7 GHz. Compared with the $V_{c1} = 0$ V condition, where SW1 is off and an f_{10dB} of 10.3 GHz is obtained over 17.7–28 GHz, the S_{22} characteristics exhibit only a slight variation. This difference is mainly attributed to the change in the input-stage load impedance resulting from the switching state of SW1.

Figure 8c shows the simulated S_{21} characteristics versus frequency for various V_{c1} values with V_{c2} = 0 V. At V_{c1} = 0 V, the LNA achieves a high and relatively flat S_{21} of 19.3–20.2 dB over the frequency range of interest, 17–21 GHz. At 19 GHz, the LNA provides a wide gain tuning range of 19.4 dB, with S_{21} decreasing from 19.3 to −0.1 dB as V_{c1} increases from 0 to 2 V. Figure 8d presents the simulated S_{12} characteristics versus frequency for various V_{c1} values with V_{c2} = 0 V. For V_{c1} ranging from 1.49 to 2 V, with SW1 in the on-state, S_{12} remains below −45.5 dB over 12–32 GHz, demonstrating excellent reverse isolation. In comparison, with V_{c1} = 0 V and SW1 in the off-state, S_{12} remains below −40.1 dB. The difference in S_{12} characteristics between the two control-voltage ranges is mainly attributed to the change in the input-stage load impedance associated with the switching state of SW1.

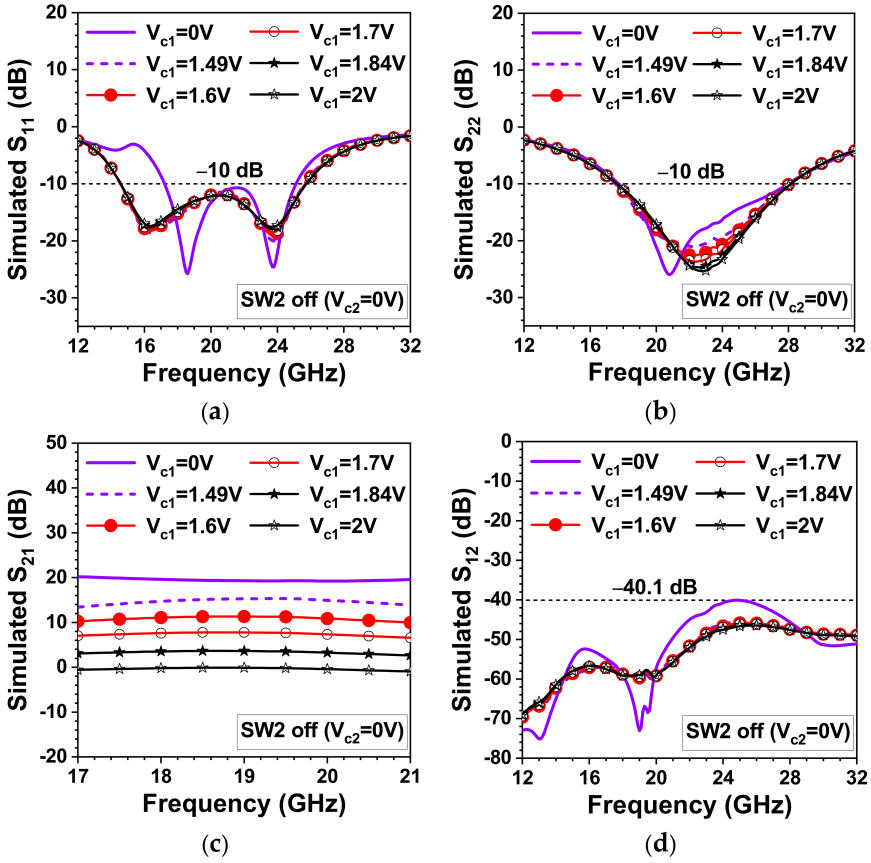


Figure 8. Simulated (**a**) S_{11}, (**b**) S_{22}, (**c**) S_{21}, and (**d**) S_{12} versus frequency characteristics of the variable-gain LNA under various V_{c1} values with V_{c2} = 0 V.

5. Measurement Results and Discussions

On-wafer S-parameter measurements from 0.1 to 50 GHz were performed using a Keysight N5247A PNA-X microwave network analyzer. With V_{G1} biased at 0.45 V, each single-ended branch of the differential input stage draws 5.42 mA from the 0.8 V supply (V_{DD1}). With V_{G2} also biased at 0.45 V, the current-reused gain and output stages draw 6.18 mA from the 0.9 V supply (V_{DD2}). Accordingly, the power consumption (P_{dc}) of the LNA is 14.2 mW. Figure 9a presents the measured S_{11} characteristics versus frequency for various V_{c1} values with V_{c2} = 0 V. For V_{c1} ranging from 0.9 to 2 V, with NMOS switch SW1 transitioning from the partially on-state to the fully on-state, S_{11} remains below −10 dB over 13.9–25.7 GHz, corresponding to an f_{10dB} of 11.8 GHz. In comparison, when V_{c1} = 0 V and SW1 is in the off-state, the LNA exhibits an f_{10dB} of 8 GHz over 17.7–25.7 GHz.

The difference in the S_{11} characteristics between these two control-voltage conditions is primarily caused by the variation in the input-stage load impedance.

Figure 9b shows the measured S_{22} characteristics versus frequency for various V_{c1} values with V_{c2} = 0 V. For V_{c1} = 0.9–2 V, with SW1 transitioning from the partially on-state to the fully on-state, S_{22} remains below −10 dB over 16.4–30.5 GHz, corresponding to an f_{10dB} of 14.1 GHz. At V_{c1} = 0 V, with SW1 in the off-state, the LNA exhibits an f_{10dB} of 13.9 GHz over 16.4–30.3 GHz. The slight difference in the S_{22} characteristics is mainly attributed to the change in the input-stage load impedance.

Figure 9c presents the measured S_{12} characteristics versus frequency for various V_{c1} values with V_{c2} = 0 V. For V_{c1} ranging from 0.9 to 2 V, S_{12} remains below −46.8 dB over 15–30 GHz, with SW1 transitioning from the partially on-state to the fully on-state. In comparison, at V_{c1} = 0 V, with SW1 in the off-state, S_{12} remains below −46 dB over the same frequency range. The slight difference in S_{12} is mainly attributed to the variation in the input-stage load impedance associated with the switching state of SW1. Figure 9d shows the measured S_{21} as a function of V_{c1} at V_{c2} = 0 V and 19 GHz. The variable-gain LNA provides a gain tuning range of 11.9 dB, with S_{21} decreasing from 16.7 to 4.8 dB as V_{c1} increases from 0 to 2 V.

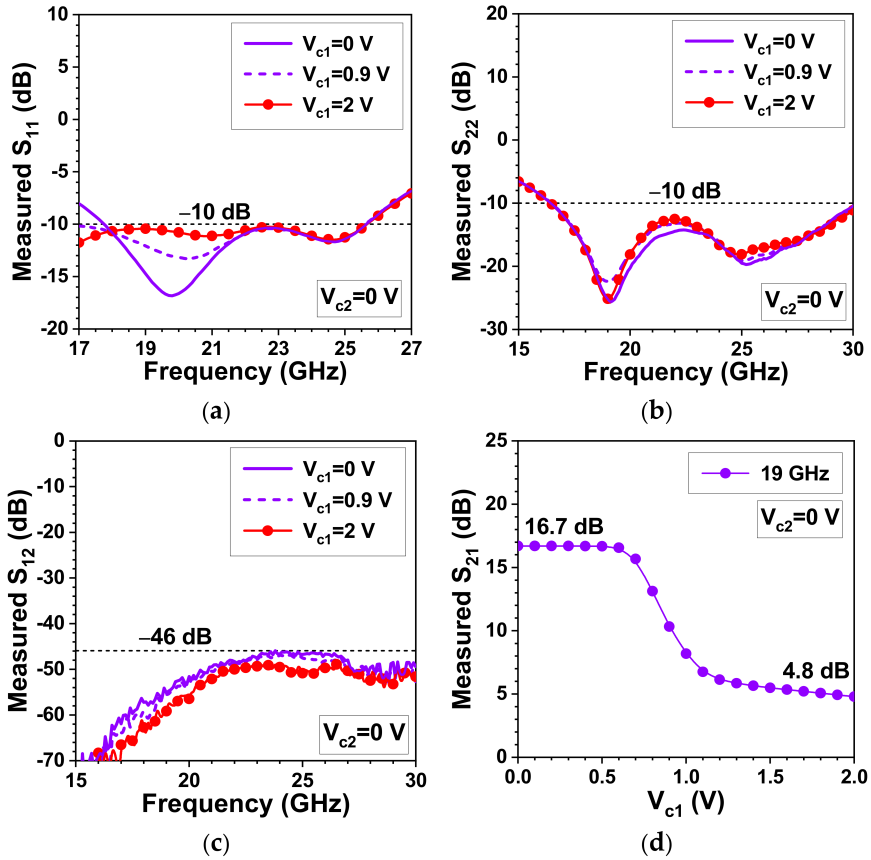


Figure 9. Measured (**a**) S_{11}, (**b**) S_{22}, and (**c**) S_{12} versus frequency characteristics of the variable-gain LNA for various V_{c1} values with V_{c2} = 0 V. (**d**) Measured S_{21} as a function of V_{c1} with V_{c2} = 0 V.

Figure 10a shows the measured S_{21} characteristics versus frequency for various V_{c2} values with V_{c1} = 0 V. At V_{c2} = 0 V, the LNA achieves a measured S_{21} of 17 ± 1.5 dB over 17.7–25.1 GHz, corresponding to an f_{3dB} of 7.4 GHz. At 17 GHz, a gain tuning range of 20.3 dB is obtained, with S_{21} decreasing from 14.8 to −5.5 dB as V_{c2} increases from 0 to 2 V. At 21 GHz, the gain tuning range increases to 21.9 dB, with S_{21} varying from 18.3 to −3.6 dB over the same control-voltage range. Figure 10b presents the measured S_{21} as a

function of V_{c2} at V_{c1} = 0 V and 19 GHz. The LNA achieves a gain tuning range of 21.6 dB, with S_{21} decreasing from 16.7 to −4.9 dB as V_{c2} increases from 0 to 2 V.

Figure 11a presents the measured S_{21} characteristics versus frequency for various $V_{c1} = V_{c2}$ values. At $V_{c1} = V_{c2}$ = 0 V, the LNA achieves a measured S_{21} of 17 ± 1.5 dB over 17.7–25.1 GHz, corresponding to an f_{3dB} of 7.4 GHz. At 17 GHz, the LNA provides a gain tuning range of 32.6 dB, with S_{21} varying from 14.8 to −17.8 dB as $V_{c1} = V_{c2}$ increases from 0 to 2 V. At 21 GHz, a gain tuning range of 33.9 dB is achieved, with S_{21} varying from 18.3 to −15.6 dB over the same control-voltage range. Figure 11b shows the measured S_{21} versus V_{c1} at 19 GHz for V_{c2} = 0 V and $V_{c2} = V_{c1}$. When $V_{c2} = V_{c1}$, the LNA achieves a gain tuning range of 33.5 dB, with S_{21} decreasing from 16.7 to −16.8 dB as $V_{c1} = V_{c2}$ increases from 0 to 2 V. In contrast, with V_{c2} = 0 V, the gain tuning range is 11.9 dB, with S_{21} decreasing from 16.7 to 4.8 dB as V_{c1} increases from 0 to 2 V.

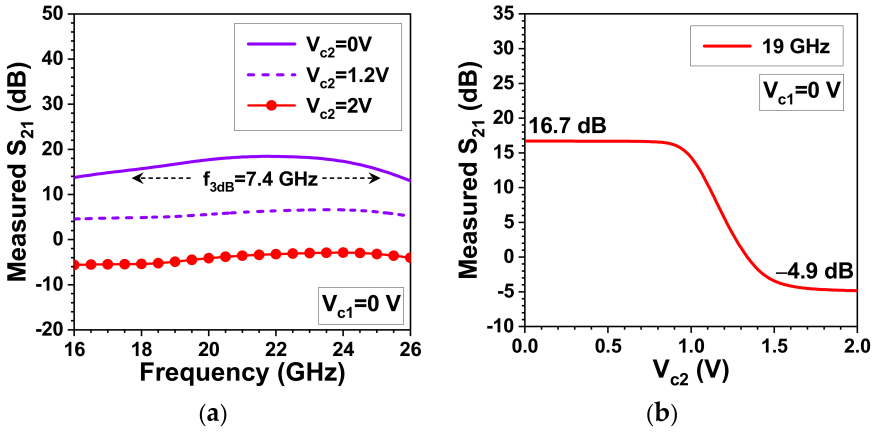


Figure 10. Measured (**a**) S_{21} versus frequency characteristics of the variable-gain LNA for various V_{c2} values with V_{c1} = 0 V, and (**b**) S_{21} as a function of V_{c2} at V_{c1} = 0 V and 19 GHz.

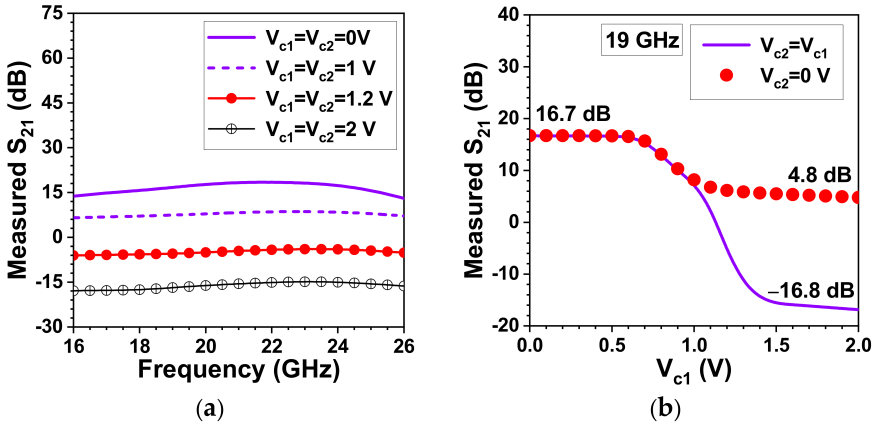


Figure 11. Measured (**a**) S_{21} versus frequency characteristics of the variable-gain LNA for various $V_{c1} = V_{c2}$ values, and (**b**) S_{21} versus V_{c1} at 19 GHz for V_{c2} = 0 V and $V_{c2} = V_{c1}$.

Figure 12 shows the measured and simulated relative S_{21} phase variation versus $V_{c1} = V_{c2}$ for the proposed variable-gain LNA at 19 GHz, with $V_{c1} = V_{c2}$ = 0 V defined as the reference state. As $V_{c1} = V_{c2}$ increases from 0 to 2 V, corresponding to a gain tuning range of 33.5 dB, the measured S_{21} phase variation remains small, ranging from −0.4° to 4.3°, which is in close agreement with the simulated variation of 0° to 4.6°. The small phase variation over the full gain-control range indicates that the proposed variable-gain LNA can maintain relatively stable phase characteristics during gain adjustment, which is desirable for phased-array receiver applications.

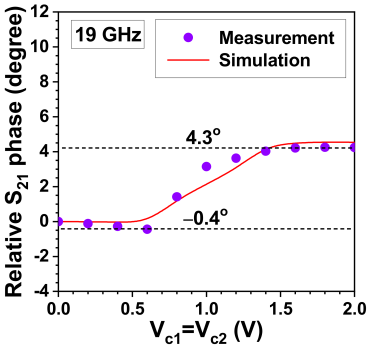


Figure 12. Measured and simulated relative S_{21} phase versus $V_{c1} = V_{c2}$ of the variable-gain LNA.

Figure 13a shows the measured stability factors μ and μ′ versus frequency for the variable-gain LNA at $V_{c1} = V_{c2} = 0$ V. Over 0.1–50 GHz, μ and μ′ remain above 1.06 and 1.07, respectively, confirming unconditional stability across the entire frequency range. Figure 13b presents the corresponding measured stability factors at $V_{c1} = V_{c2} = 2$ V. Similarly, μ and μ′ remain above 1.06 and 1.07, respectively, over 0.1–50 GHz, demonstrating that the LNA maintains unconditional stability across the entire measured frequency range.

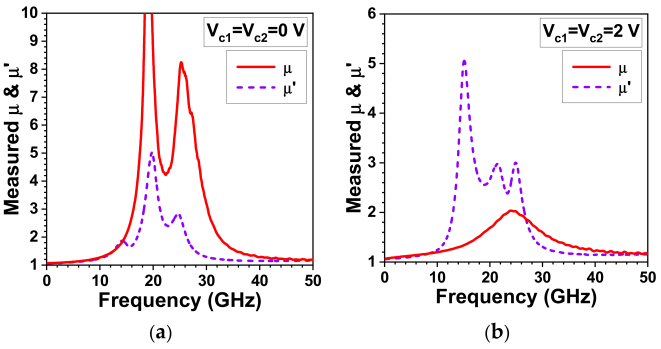


Figure 13. Measured μ and μ′ versus frequency of the LNA at (**a**) $V_{c1} = V_{c2} = 0$ V and (**b**) $V_{c1} = V_{c2} = 2$ V.

Figure 14a presents the measured and simulated NF characteristics versus frequency for the variable-gain LNA at $V_{c1} = V_{c2} = 0$ V. Over the 16–25 GHz frequency range, the measured NF reaches a minimum of 2.1 dB, with an average NF (NF_{avg}) of 3.0 dB. Within the 17–21 GHz frequency band, the measured NF reaches a minimum of 2.37 dB at 17 GHz, with an average NF of 2.71 dB over the 17–21 GHz band. These results are in close agreement with the simulation results, which predict a minimum NF of 2.38 dB at 17 GHz and an average NF of 2.74 dB over the same frequency range.

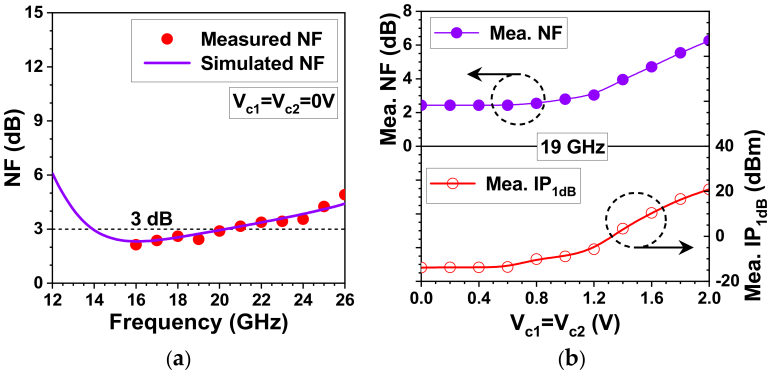


Figure 14. (**a**) Measured and simulated NF versus frequency at $V_{c1} = V_{c2} = 0$ V, and (**b**) measured NF and IP_{1dB} versus $V_{c1} = V_{c2}$ at 19 GHz of the variable-gain LNA.

On-wafer measurements of the fundamental output power (P_{out}) and third-order intermodulation output power (IM3) as functions of input power (P_{in}) were performed using a Keysight E8267D vector signal generator covering 100 kHz–44 GHz and an E4448A spectrum analyzer covering 3 Hz–50 GHz. Figure 14b shows the measured NF and input 1 dB compression point (IP_{1dB}) versus $V_{c1} = V_{c2}$ for the proposed variable-gain LNA at 19 GHz. As $V_{c1} = V_{c2}$ varies from 0 to 2 V, corresponding to a gain tuning range of 33.5 dB, the measured NF varies from 2.43 to 6.26 dB, while the measured IP_{1dB} varies from −13.9 to 20.9 dBm. As the control voltage increases and SW1 and SW2 are progressively turned on, the gain is attenuated, and the measured IP1dB improves significantly. This improvement indicates substantially enhanced linearity in the lower-gain states. Although the NF increases with gain attenuation, the measured results demonstrate a clear trade-off between noise and linearity across the entire gain-control range. These results provide experimental evidence that the proposed variable-gain LNA achieves substantially improved linearity in the gain-attenuation states while maintaining a reasonable NF, which is beneficial for variable-gain K-band receiver applications.

Figure 15a shows the measured gain versus P_{in} characteristics at 19, 20, and 21 GHz. At P_{in}= −40 dBm, the LNA exhibits small-signal gains of 16.7, 17.7, and 18.3 dB at 19, 20, and 21 GHz, respectively, with corresponding input 1 dB compression points (IP_{1dB}) of −13.9, −14.5, and −14.6 dBm.

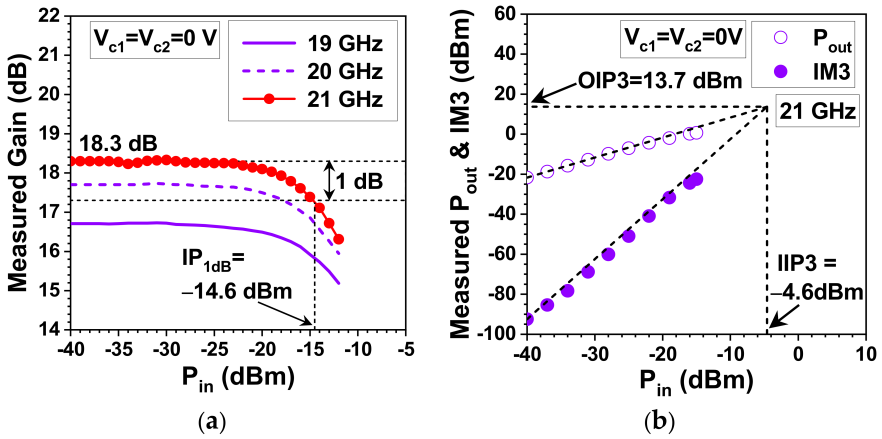


Figure 15. Measured (**a**) gain versus P_{in}, and (**b**) fundamental P_{out} and IM3 versus P_{in} of the LNA.

Figure 15b presents the measured P_{out} and IM3 versus P_{in} characteristics at 21 GHz. The LNA achieves an OIP3 of 13.7 dBm and an IIP3 of −4.6 dBm, which is 10 dB higher than the measured IP_{1dB} of −14.6 dBm shown in Figure 15a. This result is reasonably consistent with the theoretical relationship, which predicts that IIP3 is typically approximately 9.6 dB higher than IP_{1dB} [19].

A figure of merit (FoM) commonly employed to evaluate the performance of wideband LNAs is defined in [7] as

$$FoM_1\ [\text{GHz}] = \frac{BW\ [\text{GHz}] \cdot OIP3\ [\text{mW}]}{(NF-1)[1] \cdot P_{dc}\ [\text{mW}]} \tag{3}$$

where BW [GHz] denotes the 3 dB bandwidth in GHz, OIP3 [mW] represents the output third-order intercept point in mW, (NF − 1[1] is the excess noise factor corresponding to NF_{avg}, and P_{dc} [mW] denotes the DC power consumption. In addition, the following FoM is adopted to further assess the overall performance of wideband LNAs:

$$FoM_2\ [1/\text{mm}^2] = \frac{BW\ [\text{GHz}] \cdot OIP3\ [\text{mW}]}{f_0\ [\text{GHz}] \cdot (NF-1)[1] \cdot P_{dc}\ [\text{mW}] \cdot A\ [\text{mm}^2]} \tag{4}$$

where f_0 [GHz] denotes the center frequency in GHz. Accordingly, BW [GHz]/f_0 [GHz] represents the fractional bandwidth, while A [mm^2] denotes the chip area in mm^2.

Table 1 summarizes the performance of the proposed 90 nm CMOS variable-gain LNA and compares it with recently reported state-of-the-art CMOS LNAs and variable-gain LNAs implemented in 90 nm technology [6–10] and more advanced 65 nm technology [11–16]. As summarized in the table, the proposed LNA achieves a moderate chip area and low DC power consumption while providing competitive gain and 3 dB bandwidth. In addition, it offers a low noise figure and high OIP3, resulting in excellent FoM_1 and FoM_2 values. Overall, the proposed design demonstrates competitive performance and ranks among the leading reported CMOS LNA designs in terms of these key performance metrics.

Table 1. Performance summary of the CMOS variable-gain LNA and comparison with recently reported state-of-the-art CMOS LNAs and VGA operating at similar frequencies.

	S_{11} (dB)	S_{21} (dB)	f_{3dB} (GHz)	NF_{min}/NF_{avg} (dB)	OIP3 (dBm)	P_{dc} (mW)	Area (mm^2)	FoM_1 (GHz)	FoM_2 (1/mm^2)	CMOS Process
This Work	<−10	17 ± 1.5	17.7–25.1	2.1/3.0	13.7	14.2	0.369	12.27	1.55	90 nm
[6], 2022 MWCL	<−10	20.1 ± 1.5	21.3–29.2	2.74/2.99	10.2	13.7	0.348	6.1	0.69	90 nm
[7], 2022 MWCL	<−10	10.4 ± 1.5	3.1–23.7	2.53/3.97	1.5	5.85	0.364	3.33	0.68	90 nm
[8], 2021 APMC	<−10	17.8 ± 1.5	23.8–28	3.3/3.8	−3.1 *	1.8	0.6	0.82	0.05	90 nm
[9], 2021 IMS	<−10	16.1 ± 1.5	34–38.1	4.7/5.55	9.7 *	25	0.21	0.59	0.08	90 nm
[10], 2022 MWCL	<−10	15.3 ± 1.5	50–67	5.4/7	−1.1 *	5.7	0.6	0.58	0.02	90 nm
[11], 2023 IMWS-AMP	<−10	16.6 ± 1.5	16.3–26.6	3.3/4.15	10.1 *	19.2	0.19	3.43	0.84	65 nm
[12], 2021 IWS	<−10	17 ± 1.5	17–26	4.1/4.8	14.5	67.2	0.19	1.87	0.46	65 nm
[13], 2023 ICMMT	<−10	9.2 ± 1.5	16–23.4	3.2/5.6	17.5 *	25	0.2	6.33	1.61	65 nm
[14], 2019 RFIC	<−10	16.8 ± 1.5	24.9–32.5	3.25/3.73	3.9 *	20.5	0.11	0.67	0.21	65 nm
[15], 2020 MWCL	<−10	17.6 ± 1.5	21.2–24	3.6/4	−3.8 *	0.99	0.35	0.78	0.1	65 nm
[16], 2017 MWCL	<−10	8.7 ± 1.5	15.8–30.3	3.3/4.5	9.7 *	12.4	0.18	6	1.45	65 nm

* Estimation from the measured IIP3 (or IP_{1dB}) according to OIP3 = IIP3 + Gain (or IP_{1dB} + 9.6 + Gain).

6. Conclusions

A 14.2 mW, 17.7–25.1 GHz differential CMOS LNA featuring a wide 33.5 dB gain tuning range has been presented for K-band receiver applications. The proposed LNA employs body-to-ground floating, coupled-TL feedback, and multiple inductive-peaking techniques to simultaneously enhance gain, noise performance, and bandwidth. The fabricated LNA achieves a measured S_{21} of 17 ± 1.5 dB over 17.7–25.1 GHz, corresponding to a 3 dB gain bandwidth of 7.4 GHz. It also exhibits a minimum NF of 2.1 dB and an average NF of 3.0 dB over 16–25 GHz. Within the 17–21 GHz frequency band, the measured NF reaches a minimum of 2.37 dB at 17 GHz, with an average NF of 2.71 dB. In addition, a wide gain tuning range of 33.5 dB, from 16.7 to -16.8 dB, is achieved, providing substantial gain flexibility for receiver applications. The resulting FoM_1 of 12.27 GHz and normalized FoM_2 of 1.55 mm^{-2} further demonstrate the competitive performance of the proposed design compared with previously reported K- and Ka-band CMOS LNAs or variable-gain LNAs. With its low power consumption, low noise figure, wide bandwidth, and extensive gain tunability, the proposed LNA is a promising candidate for compact and energy-efficient K-band receiver applications.

Author Contributions: Conceptualization, Y.-S.L.; methodology, Y.-S.L.; software, Y.-H.Z.; validation, Y.-S.L.; formal analysis, Y.-S.L.; investigation, Y.-S.L.; resources, Y.-S.L.; data curation, Y.-S.L.; writing—original draft preparation, Y.-S.L.; writing—review and editing, Y.-S.L.; visualization, Y.-S.L.; supervision, G.P.L.; project administration, Y.-S.L.; funding acquisition, Y.-S.L. All authors have read and agreed to the published version of the manuscript.

Funding: This research was funded by the National Science and Technology Council (NSTC) of Taiwan, grant numbers NSTC114-2221-E-260-008 and NSTC115-2221-E-260-005.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Acknowledgments: The authors gratefully acknowledge the support of the Taiwan Semiconductor Research Institute (TSRI) for chip fabrication and measurements.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Satellite Industry Association (SIA). The 2025 State of the Satellite Industry Report. Available online: https://sia.org/news-resources/state-of-the-satellite-industry-report/ (accessed on 1 May 2026).
2. Wang, Y.; You, D.; Fu, X.; Nakamura, T.; Fadila, A.A.; Someya, T.; Kawaguchi, A.; Pang, J.; Yanagisawa, K.; Liu, B.; et al. A CMOS Ka-band SATCOM transceiver with ACI-cancellation enhanced dual-channel low-NF wide-dynamic-range RX and high-linearity TX. In *IEEE Radio Frequency Integrated Circuits Symposium*; IEEE: New York, NY, USA, 2020; pp. 355–358.
3. Ouvry, L.; Lachartre, D.; Bernier, C.; Lepin, F.; Dehmas, F.; Deslandes, V. An ultra-low-power 4.7mA-Rx 22.4mA-Tx transceiver circuit in 65-nm CMOS for M2M satellite communications. *IEEE Trans. Circuits Syst. II Express Briefs* **2018**, *65*, 592–596. [CrossRef]
4. LaRocca, T.R.; Thai, K.; Snyder, R.; Jai, R.; Kultran, D.; Fordham, O.; Wu, B.Y.C.; Yang, Y.; Watanabe, M.K.; Rodgers, P.; et al. Secure satellite communication digital IF CMOS Q-band transmitter and K-band receiver. *IEEE J. Solid-State Circuits* **2019**, *54*, 1329–1338. [CrossRef]
5. Fu, X.; Wang, Y.; You, D.; Wang, X.; Fadila, A.A.; Zhang, Y.; Kato, S.; Wang, C.; Li, Z.; Pang, J.; et al. A 3.4mW/element radiation-hardened Ka-band CMOS phased-array receiver utilizing magnetic-tuning phase shifter for small satellite constellation. In *IEEE International Solid-State Circuits Conference*; IEEE: New York, NY, USA, 2022; pp. 90–91.
6. Chang, J.F.; Lin, Y.S. A 13.7-mW 21–29-GHz CMOS LNA with 21.6-dB gain and 2.74-dB NF for 28-GHz 5G systems. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 137–140. [CrossRef]
7. Chang, J.F.; Lin, Y.S. 5.85 mW 3.1–23.7 GHz two-stage CMOS VGA with 2.53 dB NFmin using concurrent current steering. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 1331–1334.
8. Chang, K.C.; Wang, Y.; Wang, H. Design of a 1.8-mW K-band low noise amplifier with 19.3-dB gain and 3.3-dB noise figure in 90-nm CMOS. In *IEEE Asia-Pacific Microwave Conference (APMC)*; IEEE: New York, NY, USA, 2021; pp. 4–6.
9. Chiu, T.Y.; Wang, Y.; Wang, H. A Ka-band transformer-based switchless bidirectional PA-LNA in 90-nm CMOS process. In *IEEE/MTT-S International Microwave Symposium*; IEEE: New York, NY, USA, 2021; pp. 450–452.
10. Li, M.H.; Wang, Y.; Wang, H. A 50–67 GHz ultralow-power LNA using double-transformer-coupling technique and self-resonant matching in 90-nm CMOS. *IEEE Microw. Wirel. Compon. Lett.* **2022**, *32*, 68–71. [CrossRef]
11. Chen, X.; Ren, X.; Cheng, D.; Feng, J.; Wu, X.; Hu, Q.; Fan, X.; Li, L. A K-band low noise amplifier in 65-nm CMOS with 3.3-dB NF and 18.1-dB power gain. In *IEEE MTT-S International Microwave Workshop Series on Advanced Materials and Processes for RF and THz Applications (IMWS-AMP)*; IEEE: New York, NY, USA, 2023; pp. 1–3.
12. Cheng, D.; Li, L.; Xie, M.; Wu, X.; He, L.; Sheng, B. A K-band variable gain low-noise amplifier with low phase variation in 65-nm CMOS. In *IEEE MTT-S International Wireless Symposium (IWS)*; IEEE: New York, NY, USA, 2021; pp. 1–3.
13. Cui, G.; Zhao, C.; Liu, H.; Yu, Y.; Wu, Y.; Kang, K. Design of K-band compact wideband low noise amplifier. In *International Conference on Microwave and Millimeter Wave Technology (ICMMT)*; IEEE: New York, NY, USA, 2023; pp. 1–3.
14. Kong, S.; Lee, H.D.; Jang, S.; Park, J.; Kim, K.S.; Lee, K.C. A 28-GHz CMOS LNA with stability-enhanced Gm-boosting technique using transformers. In *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*; IEEE: New York, NY, USA, 2019; pp. 7–10.
15. Lu, B.Z.; Wang, Y.; Wu, Y.C.; Chiong, C.C.; Wang, H. A submilliwatt K-band low-noise amplifier for next generation radio astronomical receivers in 65-nm CMOS process. *IEEE Microw. Wirel. Compon. Lett.* **2020**, *30*, 669–672. [CrossRef]
16. Qin, P.; Xue, Q. Compact wideband LNA with gain and input matching bandwidth extensions by transformer. *IEEE Microw. Wirel. Compon. Lett.* **2017**, *27*, 657–659. [CrossRef]
17. Lin, Y.S.; Lan, K.S.; Chen, B.S. Wideband millimeter-wave power divider and SPDT switch using inverting spiral-coupled-line. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 1575–1579. [CrossRef]

18. Edwards, M.L.; Sinsky, J.H. A new criterion for linear 2-port stability using geometrically derived parameters. *IEEE Trans. Microw. Theory Tech.* **1992**, *40*, 2303–2311. [CrossRef]
19. Razavi, B. *RF Microelectronics*, 2nd ed.; Pearson Education, Inc.: Upper Saddle River, NJ, USA, 2011.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.