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Technical Note

A Mutual Blocking Technology Applied to Dual Power Source Switching Control

Hsin-Chuan Chen [1], Ping-Huan Kuo [2] and Chiou-Jye Huang [3,*]

[1] School of Computer Engineering, University of Electronic Science and Technology of China, Zhongshan Institute, Zhongshan 528402, China; chen_robin@foxmail.com
[2] Computer and Intelligent Robot Program for Bachelor Degree, National Pingtung University, Pingtung 90004, Taiwan; phkuo@mail.nptu.edu.tw
[3] School of Electrical Engineering and Automation, Jiangxi University of Science and Technology, Ganzhou 341000, China
* Correspondence: chioujye@163.com

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Abstract: In many industries and medical power system applications, dual power source design is often used to ensure that the equipment runs continuously, even when the main power supply is shut down. However, the voltage feedback between two independent power supplies and low loss output are critical issues for the system energy dissipation. Without using a dedicated chip, a new mutual blocking control technology is proposed in this paper to effectively solve the problem of voltage feedback existing in the conventional dual power system. In addition, without adding much hardware cost, the proposed dual power switch design can completely avoid voltage feedback and achieve a low voltage loss of about 30 mV when the load current is less than 0.5 A.

Keywords: dual power source switch; mutual blocking control technology; low loss output; voltage feedback

1. Introduction

Since it is common for equipment to work for 24 hours a day in industry applications, the equipment must therefore record the current conditions when it is shut down, and initiate the necessary processing procedures. Hence, a dual power source switch circuit is necessary to turn on the backup battery power source to ensure that the system can continue to work at the moment of the main power failure. Generally, the simplest method is to connect the main power supply and the backup power supply to the anodes of two diodes respectively, and the cathodes of the two diodes are coupled together to the load [1,2]. This method is simple and the problem of mutual feedback between the two power supplies can be avoided. However, in addition to the output voltage loss due to the diode voltage drop, when the power voltages of the dual power supplies are relatively close, both power sources will supply power to the load simultaneously. Therefore, it is not suitable for dual power switching applications. In Figure 1, we show the basic schema of the dual power source switch. At the moment of the main power failure, the equipment should not be restarted due to the power source being switched to backup power. The switch shown in Figure 1 cannot be the mechanical type like relay, which has a longer switching time. Since MOSFET switches have a faster switching speed, and their on-resistance is extremely low, the power PMOS is often used as a switching transistor [3].

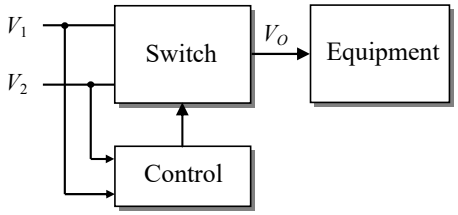


Figure 1. Schema of dual power source switching.

One reference [4] pointed out that Pavio et al. proposed dual DC source switching technology, which was an effective method for switching between the power that was supplied from the fuel cell and the secondary power source. Chen et al. [5] proposed dual AC source switching technology which was one of the key technologies to ensure power supply for important loads. During the switching process, the two power supplies usually have asynchronous characteristics, so that the zero-second switching affects the load and interferes with its normal operation and even burns down. From the previous description, it is understood that the circuit design for automatic switching between the main power supply and the backup power supply must meet the following functional requirements:

1. When the main power is present, the equipment is supported by the main power supply; when the main power supply is shut down, the automatic switch is applied to allow the backup power supply to support the equipment.
2. The two sets of power sources must be completely independent and cannot mutually give feedback to each other.
3. Voltage loss due to switching should be reduced as much as possible, regardless of whether the power supply is switched to the main or backup power source.

The major contributions of this paper include: (a) the design of an innovative dual power source switch circuit with a low loss output; (b) a mutual blocking control technology proposed to solve the voltage feedback problem existing in the conventional dual power switching design and (c) the demonstration of the proposed dual power source switch circuit implemented and analyzed.

This paper is organized as follows: Section 2 reviews the control methods of dual power switching techniques; Section 3 introduces the proposed dual power switching using mutual blocking technology; Section 4 illustrates the experimental results and analysis; and Section 5 concludes the experimental results of this paper.

2. Control Methods of Dual Power Switching

As seen in Figure 2, the switches in a dual power switching design often use two power PMOS transistors, which their source nodes are connected together. The purpose of this is to achieve faster switching and reduce conductive voltage loss. The switching control can be either a conventional control method using the main power detection, or a control method using a dedicated chip. These two methods are described in detail below.

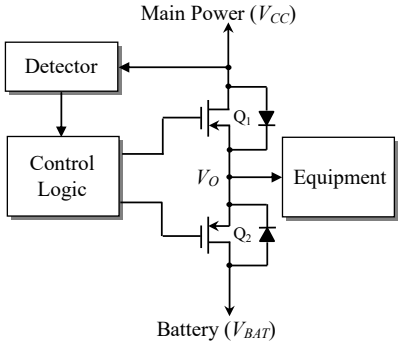


Figure 2. Switching control architecture using main power detection.

2.1. Control Method Using Main Power Detection

It is simplest to directly control the switching of dual power sources based on detecting the presence or absence of main power. In this traditional design architecture shown in Figure 2, only a common voltage detector IC such as TC54 [6] or MAX6376 [7] is needed to detect if the main power supply from the utility is shut down. In addition, two low power NMOS transistors can be used as the control logic switches [8] as seen in Figure 3. According to the state of the main power detected, the gate voltages of Q_1 and Q_2 can be controlled, where Q_1 and Q_2 are connected to main power supply (V_{CC}) and battery (V_{BAT}), respectively. Essentially, the output V_O to the equipment is given by:

$$V_O = \frac{r_{DS2}}{r_{DS1} + r_{DS2}} \times V_{CC} + \frac{r_{DS1}}{r_{DS1} + r_{DS2}} \times V_{BAT} \quad (1)$$

where, r_{DS1} and r_{DS2} are conductive resistances of two PMOS (Q_1 and Q_2), respectively.

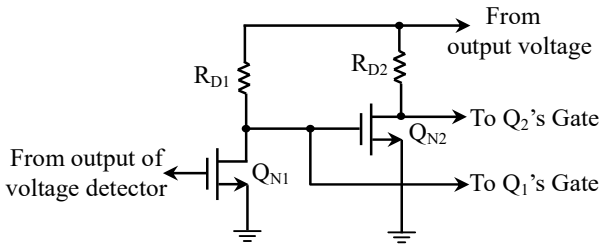


Figure 3. A control logic circuit consisting of two NMOS transistors.

When the main power source is present, the output of the voltage detector can directly turn Q_1 on by the reverse of an NMOS (Q_{N1}); and the reverse output of this NMOS can turn Q_2 off through the reverse of another NMOS (Q_{N2}). Therefore, r_{DS1} approaches 0 and r_{DS2} is almost infinite such that V_O equals V_{CC}. Conversely, when only the battery power source is present, that causes Q_1 to turn off and Q_2 to turn on (i.e., $r_{DS1} \approx \infty$ and $r_{DS2} \approx 0$), and thus the power supplied to the equipment is switched to battery power (i.e., $V_O = V_{BAT}$).

The operation principle of this circuit is as follows:

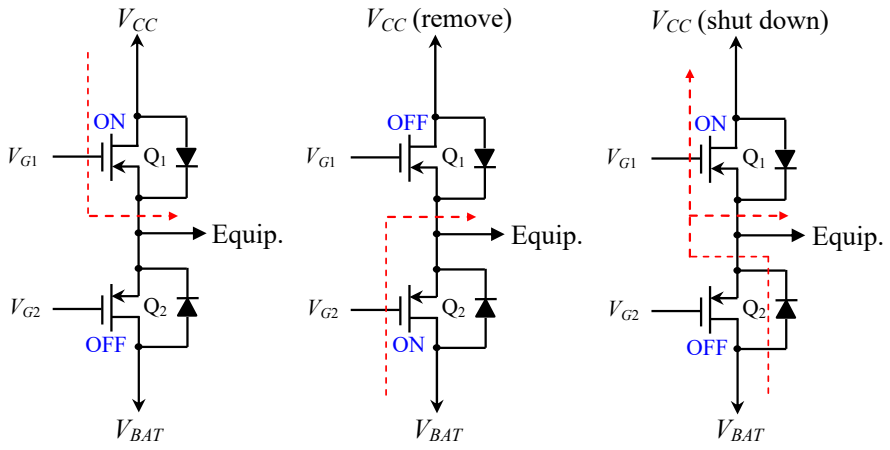
1. When the main power supply and the battery are both present, or only the main power supply is present, Q_1 is on and Q_2 is off, at this time the main power supply provides a low loss output to the equipment.
2. When only battery power supply is present, Q_2 is on and Q_1 is off, at this time, the battery power supply provides a low loss output to the equipment.
3. When the main power supply and battery power are both present but the main power supply is suddenly shut down, due to the characteristics of MOSFET delay transition [9], the battery power supply is still fed back to the main power supply terminal via the delayed Q_1. Therefore, the voltage detector still regards the main power supply as active so that the controller still keeps Q_1 on and Q_2 off. At this time, the battery power supplying the equipment will suffer an internal diode voltage drop (V_D) of Q_2, and another power discharge path through Q_1 will be formed.

According to the description of operation state (3), the output voltage should be modified as:

$$V_O = \frac{r_{DS1}}{r_{DS1} + r_{DS2}} \times V_{BAT} + \frac{r_{DS2}}{r_{DS1} + r_{DS2}} \times [V_{CC} \times F + (V_{BAT} - V_D) \times (1 - F)] \quad (2)$$

where, F denotes the presence factor of main power supply, $F = 1$ indicates presence, otherwise $F = 0$. Of course, if the sources of Q_1 and Q_2 are connected in a series with the diodes, respectively, and the cathodes of two diodes are connected to the equipment, then the power supply feedback problem can be avoided. However, in this condition, whether the main power or the battery power is present,

the output voltage to the equipment will drop by passing through another diode. Figure 4 shows the power supply paths of the three different operating conditions mentioned above.



(a) Only main power or both (b) Only battery (c) Main power shut down

Figure 4. Power supply paths under different operating conditions.

2.2. Control Method Using Dedicated Chip

In order to solve the above-mentioned problem of the battery voltage being fed back to the main power supply caused by the sudden power failure, using the operating amplifiers (OPA) with a fast response as the decision control when switching, is an often-used method [8,10]. In addition, they are integrated into the dedicated chips. Nowadays, one of dedicated control chips, such as LTC4414, has been developed by Linear Technology Semiconductor [11], and it can be applied for dual power switching control shown in Figure 5 [11,12], where V_{CC} is the main power supply and V_{BAT} is the battery power.

The circuit operation principle of Figure 5 is as follows:

1. When only V_{CC} is present and Q_1 is on, but the GATE output voltage is not high enough that Q_2 is not completely turned off and partial V_{CC} is fed back to the battery terminal.
2. When V_{CC} and V_{BAT} are both present and $V_{CC} > V_{BAT}$, and thus Q_1 is on and Q_2 is off, the main power V_{CC} has a low loss output to the equipment.
3. When only V_{BAT} is present, and thus Q_2 is on and Q_1 is off, the battery power V_{BAT} has a low loss output to the equipment.
4. When V_{CC} and V_{BAT} are both present, but V_{CC} suddenly shuts down, Q_1 turns off and Q_2 turns on, and the battery power V_{BAT} still maintains low loss output to the equipment.
5. When *Vcc* is restored, then power supply returns to state two. However, if V_{CC}-$V_{BAT} < 0.5$ V, Q_2 is still on and Q_1 is still off, the output V_O cannot be switched back to V_{CC} from V_{BAT}.

According to the above operation principles, if the main power supply is suddenly shut down, the LTC4414 indeed can reduce output loss, when switching to battery power and not incur feedback to the main power terminal. If the main power supply is restored and the output is switched back to the main power again, the limiting condition is that the main power supply voltage must be more than 0.5 V higher than the battery voltage. In addition, if the battery voltage is much lower than the main power voltage, some of the voltage of the main power supply will feed back to the battery power terminal, and the equipment will not be able to obtain full supply voltage of the main power.

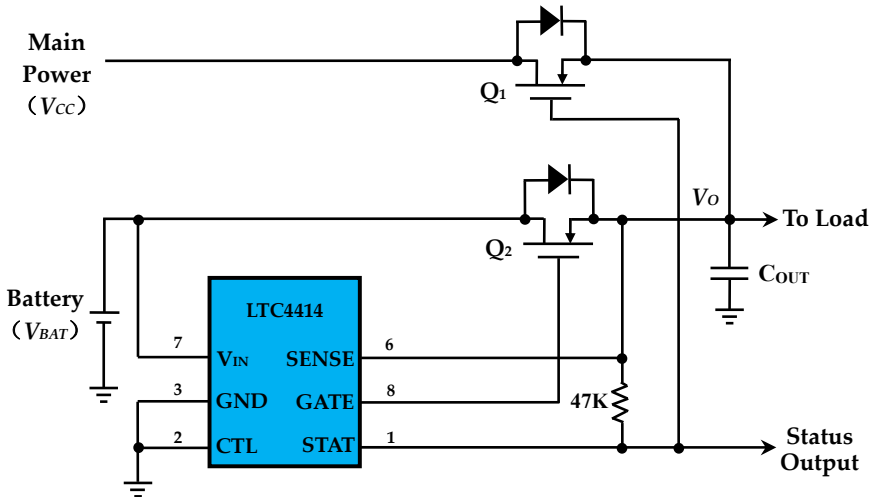


Figure 5. Typical application circuit of LTC4414. Source: Linear Technology Corporation.

3. Dual Power Switching Using Mutual Blocking Technology

The conventional dual power switching design has the problem of voltage feedback, which is when the main power is shut down and the battery power not only provides the equipment with power, but also feeds voltage back to the main power supply terminal. Therefore, a battery discharge path forms, but this also shortens the battery supply hours. In this paper, we propose an innovative design architecture shown in Figure 6. We still apply the voltage detector IC to determine the presence of a main power source, and separately control PMOS (Q_1) connected to the main power supply and PMOS (Q_2) connected to the battery by the NMOS control logic. However, unlike traditional designs, Q_1 and Q_2 are connected to the respective power inputs with their sources instead of their drains [2]. In addition, two PMOS (Q_3 and Q_4) with the gate cross control and source docking are added to form a mutual blocking control circuit as shown in Figure 9 to avoid voltage feedback. The circuit operation principle designed in this paper is as follows:

1. Considering that the main power supply and the battery power supply are both present, by detecting the presence of the main power supply, Q_1 and Q_3 will be on and Q_2 and Q_4 will be off.
2. When the main power supply is shut down (i.e., its supply current $I_{CC} = 0$), the control logic prepares to turn on Q_2 and turn off Q_1, although Q_1 has not changed its operating state immediately, the voltage V_{G4} from the drain of Q_1 is quickly lowered to zero, which will cause Q_4 to turn on.
3. At this time, the voltage V_{G3} from the drain of Q_2 rises to the battery voltage, which causes Q_3's gate voltage to rise and turn off Q_3. By the diode inside Q_3, the battery voltage would not be fed back to the main power supply terminal, and thus the battery power supply can provide a low loss output for the equipment. This situation is shown in Figure 8.
4. When the main power is restored, the control logic switches Q_1 on and Q_2 off, and V_{G3} is lowered due to the battery supply current $I_{BAT} = 0$, thus causing Q_3 to turn on.
5. At this time, V_{G4} is raised to the main power supply voltage to turn off Q_4. As shown in Figure 7, the internal diode of Q_4 prevents the main power from being fed back to the battery terminal, and the main power supply provides the equipment an output with low loss again.
6. In addition, if only the main power supply is present, or if the battery voltage is much lower than that of the main power supply, the design will not allow the main power supply voltage to give feedback to the battery terminal.

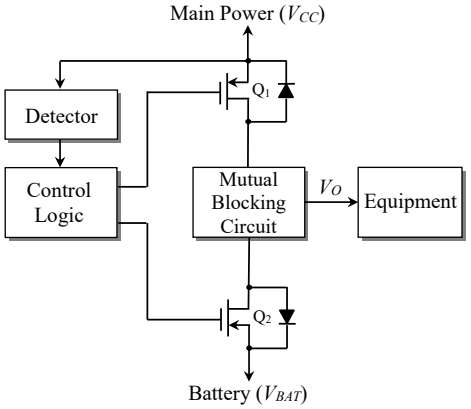


Figure 6. Proposed switching architecture using mutual blocking.

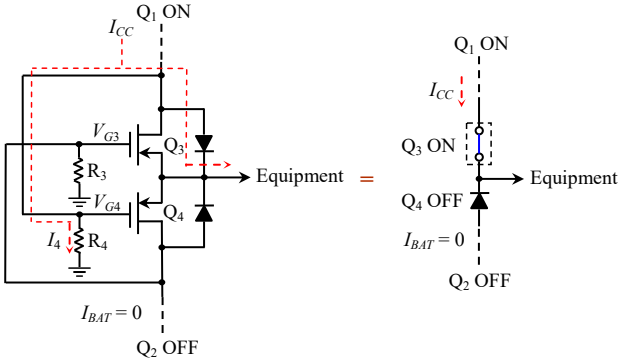


Figure 7. Mutual blocking when the main power supply is restored.

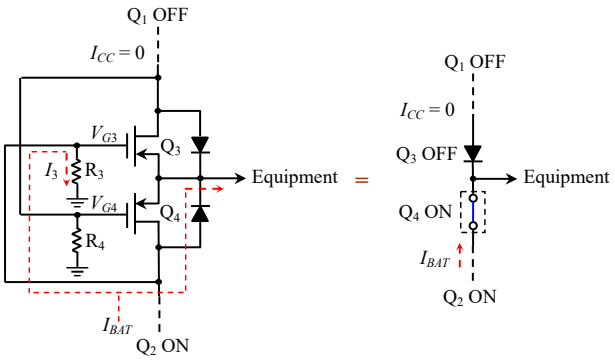


Figure 8. Mutual blocking when the main power supply is shut off.

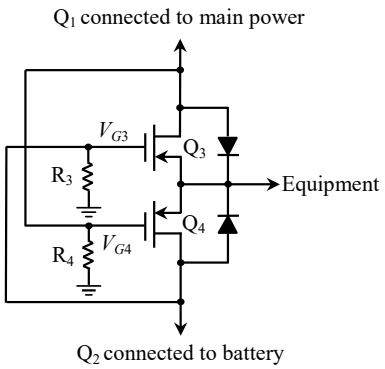


Figure 9. Mutual blocking circuit.

Therefore, from the equivalent circuit on the right side of Figures 7 and 8, the roles of Q_3 and Q_4 are hereby equivalent to two approximately ideal dynamic diode switches. When they are turned on, there is only a very low voltage drop, and when they are turned off, their internal diodes can block the voltage feedback. Assume that the conductive resistances r_{DS} of Q_3 and Q_4 are zero in the ideal case, the output voltage to the equipment can be given by:

$$V_O = \left(\frac{r_{DS2}}{r_{DS1} + r_{DS2}}\right)(V_{CC} - V_D \times S_1(t)) + \left(\frac{r_{DS1}}{r_{DS1} + r_{DS2}}\right)(V_{BAT} - V_D \times S_2(t)) \quad (3)$$

where, $S_1(t)$ is the control function of Q_3 to determine whether Q_3 is on or off, depending on I_3 from the battery supply current I_{BAT}. Similarly, $S_2(t)$ is used as the control function for Q_4 and is controlled by I_4 from the main power supply current I_{CC}. Equations (4) and (5) represent the control functions: $S_1(t)$ and $S_2(t)$, respectively, where V_{th} is the threshold voltage of PMOS. Here, R_3 and R_4 should be ~MΩ to minimize these extra incurred current as possible.

$$S_1(t) = \begin{cases} 0 & if v_{GS3} = I_3 \times R_3 - V_O < V_{th} \\ 1 & if v_{GS3} = I_3 \times R_3 - V_O \geq V_{th} \end{cases} \quad (4)$$

$$S_2(t) = \begin{cases} 0 & if v_{GS4} = I_4 \times R_4 - V_O < V_{th} \\ 1 & if v_{GS4} = I_4 \times R_4 - V_O \geq V_{th} \end{cases} \quad (5)$$

Although this mutual blocking design adds two more PMOS, and the voltage loss of the power supply to the equipment slightly increases by one PMOS voltage drop, the voltage loss has been effectively reduced, compared with the general diode voltage drop. Particularly for equipment with a large load, the improvement in voltage and power loss is more obvious when the power PMOS with ultra low on-resistance is chosen. Meanwhile, it can effectively solve the problem of voltage feedback in the conventional design of dual power switching.

4. Experimental Results and Analysis

Basically, no matter which MOSFET-based dual power switching design is used, when power supply is switched, it will not cause the equipment to reset at the moment of switching. In order to verify the operation of different types of dual power switching design and compare the performances among them, under the same PMOS specifications, we have implemented three different types of dual power switching circuits including the conventional control type using the main power detection, the control type using dedicated chip, and the proposed mutual blocking control type. Figure 10 shows the circuit prototype of the proposed dual power source switch, where two other low power NMOS transistors are used as the control logic to turn on or turn off the two PMOS switches (Q_1 and Q_2), and the control logic circuit is the same as the circuit shown in Figure 3. Here the main power voltage (V_{CC} = 12.2 V) comes from the utility power adapter, while the other power source is supplied by a lithium battery pack (V_{BAT} = 11.8 V). According to the various switching conditions, the performance of the three types of switching circuits are measured and compared. The maximum supply current to the equipment depends on the power PMOS used as a switch. In our experiments, all power PMOS transistors are the same component of IRF9540, and the maximum continuous drain current of IRF9540 [13] is about 19 A.

4.1. Measured Waveforms

In the practical measurement, we try to observe the waveforms shown in Figure 11 during switching, where CH1 represents the main power voltage, CH2 represents the battery voltage, and CH3 indicates the output voltage. For clearer observation, the battery voltage is adjusted to 11 V temporarily. When the main power voltage starts to drop, the output to the equipment is not switched to the battery supply immediately; that is because the main power voltage does not drop to the desired threshold

voltage of the voltage detector IC. This threshold voltage depends on the voltage that ensures the equipment works correctly, where the threshold voltage is set to 9.27 V in the proposed design. When the main power is restored, the output to the equipment can be quickly switched back to the main power supply. The switching time of the proposed design is very short, only about a few μs, and it depends on the used PMOS.

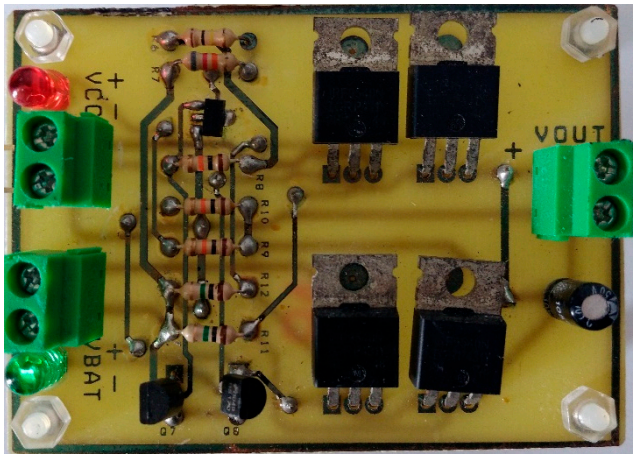


Figure 10. Circuit implementation of the proposed dual power source switch.

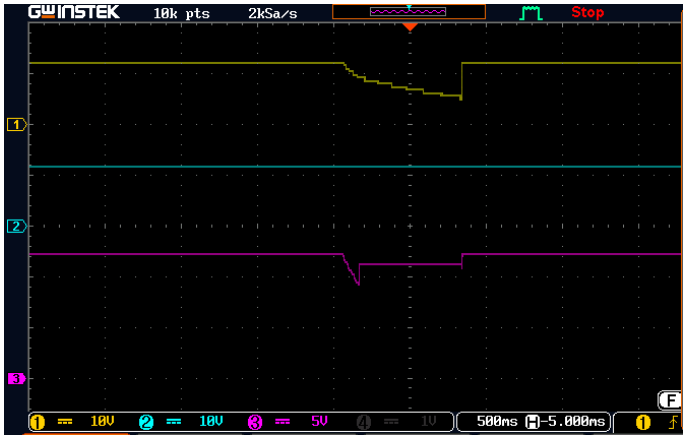


Figure 11. Waveforms of switching operation.

4.2. Output Voltage and Power Loss

Using PMOS as a switching power transistor, the output voltage loss is extremely low in a fully conductive state. It can be seen from Table 1 that only the switching circuit using the main power detection causes the battery output voltage to lose about 0.6 V when the main power supply is momentarily shut down. Whether the other switching circuits switch to the main power or the battery, the output to the equipment is almost equal to the original supply voltage. However, since the main power supply voltage is not greater than the battery voltage by more than 0.5 V in our experiment, if the dedicated chip control is applied to the switching circuit, the output cannot be switched back to the main power supply from the battery when the main power supply is restored. Whatever the main power supply is greater than the battery or not, the switching circuit using a mutual blocking control does not appear in the above situation.

Considering the different current levels of the load, Table 2 shows the power loss during the turn-on caused by the power PMOS or the diode for different switching control methods. For the switching circuit using the main power detection control, the load current from the backup power supply will pass through an internal diode of PMOS when the main power supply is shut down.

Thus, there exists a power loss caused by this internal diode. Although the power loss of the mutual blocking control is twice as large as that of the dedicated chip control due to the adding of one power PMOS on the load current path, the power loss caused by the power PMOS is still reduced compared with the power loss of the diode. If the power PMOS with ultra low on-resistance is further chosen, like PMN50XP [14], the improvement in power loss will be more obvious even for large loads.

Table 1. Output voltage to equipment.

Condition	Main Power Detection Control	Dedicated Chip Control	Mutual Blocking Control
Only main power is present	12.2 V (V_{CC})	12.2 V (V_{CC})	12.2 V (V_{CC})
Only battery	11.8 V (V_{BAT})	11.8 V (V_{BAT})	11.8 V (V_{BAT})
Main power and battery are present	12.2 V (V_{CC})	12.2 V (V_{CC})	12.2 V (V_{CC})
Main power shut down	11.2 V (V_{BAT})	11.8 V (V_{BAT})	11.8 V (V_{BAT})
Main power restored	12.2 V (V_{CC})	11.8 V (V_{BAT})	12.2 V (V_{CC})

Table 2. Power loss of power PMOS or diode under different load current.

Load Current	Main Power Detection Control	Dedicated Chip Control	Mutual Blocking Control
0.1 A	0.06 W	0.002 W	0.003 W
0.5 A	0.37 W	0.043 W	0.085 W
1 A	0.72 W	0.17 W	0.34 W
1.5 A	1.22 W	0.42 W	0.83 W
2 A	1.82 W	0.71 W	1.42 W

4.3. Output Voltage Feedback

A good design for dual power switching should consider that the two power supplies must be completely independent and does not mutually give feedback to each other. After the practical measurement shown in Table 3, we find that the switching circuit using the main power detection control will feed battery voltage back to the main power supply terminal when the main power supply is momentarily shut down. When only the main power supply is present, or if the battery voltage is lower than that of the main power supply, the voltage feedback from the main power to the battery terminal also occurs in the switching circuit using a dedicated chip. However, if the mutual blocking control is adopted in the switching circuit, the two power supplies can be independent from each other under any condition, and they do not mutually give feedback to each other.

Table 3. Power voltage feedback situation.

Condition	Main Power Detection Control	Dedicated Chip Control	Mutual Blocking Control
Only main power is present	No	Feedback to V_{BAT}	No
Only battery is present	No	No	No
Main power and battery are present	No	No	No
Main power shut down	Feedback to V_{CC}	No	No
Main power restored	No	No	No

5. Conclusions

In addition to reducing circuit complexity, the use of commercial chips (such as the LTC4414) also effectively solves the voltage feedback problem of the conventional dual power switching design; and its output voltage retains the advantage of low loss in PMOS conduction. However, if the main power supply voltage varies to be only slightly higher than that of the backup power, or even lower than the backup power voltage, when the main power supply is shut down and restored again,

the output voltage cannot be switched back to the main power supply from the backup power supply. Therefore, the use of commercial chips is not the best choice for practical applications that are intended to meet various power supply conditions. In this paper, a mutual blocking control technology is proposed to be applied to the dual power switching design, which can switch correctly and achieve a low loss output voltage. According to the experimental results, the voltage loss is about less than 0.3 V under a load current of 1 A, and if the power PMOS with ultra low on-resistance is further chosen, the voltage loss still keeps low even for a large load current. Moreover, the proposed dual power switching design can also completely avoid the voltage feedback problem under any condition, and it will satisfy the requirement of the equipment running continually and have a better performance.

Author Contributions: H.-C.C. planned this study, completed the circuit design, and presented the analysis of experiment results. P.-H.K. completed this circuit implementation and test. C.-J.H. handled this circuit measurement and the partial article writing. H.-C.C., P.-H.K. and C.-J.H. contributed in drafted and revised the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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